19-2722; Rev 0; 04/03

MAXIM

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface



## General Description

The MAX1266/MAX1268 low-power, 12-bit analog-to-digital converters (ADCs) feature a successive-approximation ADC, automatic power-down, fast wake-up (2µs), an on-chip clock, +2.5V internal reference, and a high-speed 12-bit parallel interface. They operate with a single +5V analog supply.

Power consumption is only 10mW at the maximum sampling rate of 420ksps. Two software-selectable power-down modes enable the MAX1266/MAX1268 to be shut down between conversions; accessing the parallel interface returns them to normal operation. Powering down between conversions can reduce supply below 10µA at lower sampling rates.

Both devices offer software-configurable analog inputs for unipolar/bipolar and single-ended/pseudo-differential operation. In single-ended mode, the MAX1266 has six input channels and the MAX1268 has two (three input channels and one input channel, respectively, when in pseudo-differential mode).

Excellent dynamic performance and low power, combined with ease of use and small package size, make these converters ideal for battery-powered and data-acquisition applications or for other circuits with demanding power-consumption and space requirements. The MAX1266 is offered in a 28-pin QSOP package, while the MAX1268 is available in a 24-pin QSOP. For pin-compatible +3V, 12-bit versions, see the MAX1265/MAX1267.

## Applications

| | |
|---|---|
| Industrial Control Systems | Data Logging |
| Energy Management | Patient Monitoring |
| Data-Acquisition Systems | Touch Screens |

## Ordering Information

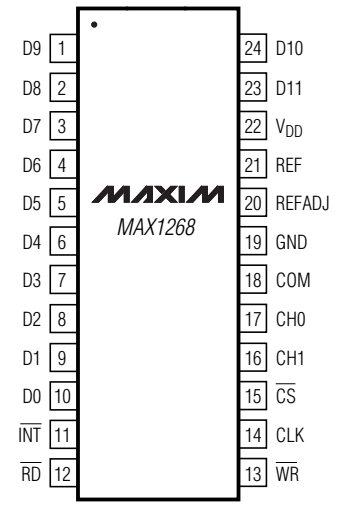
| PART | TEMP RANGE | PIN-PACKAGE | INL (LSB) |
|---|---|---|---|
| **MAX1266**ACEI | 0°C to +70°C | 28 QSOP | ±0.5 |
| MAX1266BCEI | 0°C to +70°C | 28 QSOP | ±1 |
| MAX1266AEEI | -40°C to +85°C | 28 QSOP | ±0.5 |
| MAX1266BEEI | -40°C to +85°C | 28 QSOP | ±1 |
| **MAX1268**ACEG | 0°C to +70°C | 24 QSOP | ±0.5 |
| MAX1268BCEG | 0°C to +70°C | 24 QSOP | ±1 |
| MAX1268AEEG | -40°C to +85°C | 24 QSOP | ±0.5 |
| MAX1268BEEG | -40°C to +85°C | 24 QSOP | ±1 |

## Features

- **12-Bit Resolution, ±0.5 LSB Linearity**
- **Single +5V Operation**
- **Internal +2.5V Reference**
- **Software-Configurable Analog Input Multiplexer**
  - **6-Channel Single Ended/**
  - **3-Channel Pseudo-Differential (MAX1266)**
  - **2-Channel Single Ended/**
  - **1-Channel Pseudo-Differential (MAX1268)**
- **Software-Configurable Unipolar/Bipolar Analog Inputs**
- **Low Current**
  - **2.8mA (420ksps)**
  - **1.0mA (100ksps)**
  - **400µA (10ksps)**
  - **2µA (Shutdown)**
- **Internal 6MHz Full-Power Bandwidth Track/Hold**
- **Parallel 12-Bit Interface**
- **Small Footprint**
  - **28-Pin QSOP (MAX1266)**
  - **24-Pin QSOP (MAX1268)**

## Pin Configurations

TOP VIEW




QSOP

*Pin Configurations continued at end of data sheet.*

***Typical Operating Circuits appear at end of data sheet.***



***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....-0.3V to +6V
CH0–CH5, COM to GND .....-0.3V to ($V_{DD}$ + 0.3V)
REF, REFADJ to GND.....-0.3V to ($V_{DD}$ + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
Digital Outputs (D0–D11, $\overline{INT}$) to GND.....-0.3V to ($V_{DD}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
28-Pin QSOP (derate 8.0mW/°C above +70°C).....667mW

Operating Temperature Ranges
MAX1266_C_ _/MAX1268_C_ _ .....0°C to +70°C
MAX1266_E_ _/MAX1268_E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +5V ±10%, COM = GND, REFADJ = $V_{DD}$, $V_{REF}$ = +2.5V, 4.7µF capacitor at REF pin, $f_{CLK}$ = 7.6MHz (50% duty cycle), $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY** (Note 1) | | | | | | |
| Resolution | RES | | 12 | | | Bits |
| Relative Accuracy (Note 2) | INL | MAX126_A | | | ±0.5 | LSB |
| | | MAX126_B | | | ±1 | |
| Differential Nonlinearity | DNL | No missing codes overtemperature | | | ±1 | LSB |
| Offset Error | | | | | ±4 | LSB |
| Gain Error | | (Note 3) | | | ±4 | LSB |
| Gain Temperature Coefficient | | | | ±2.0 | | ppm/°C |
| Channel-to-Channel Offset Matching | | | | ±0.2 | | LSB |
| **DYNAMIC SPECIFICATIONS** ($f_{IN(sine\ wave)}$ = 50kHz, $V_{IN}$ = 2.5$V_{P-P}$, 420ksps, external $f_{CLK}$ = 7.6MHz, bipolar input mode) | | | | | | |
| Signal-to-Noise Plus Distortion | SINAD | | 67 | 70 | | dB |
| Total Harmonic Distortion (Including 5th-Order Harmonic) | THD | | | | -80 | dB |
| Spurious-Free Dynamic Range | SFDR | | -80 | | | dB |
| Intermodulation Distortion | IMD | $f_{IN1}$ = 49kHz, $f_{IN2}$ = 52kHz | | 76 | | dB |
| Channel-to-Channel Crosstalk | | $f_{IN}$ = 175kHz (Note 4) | | -78 | | dB |
| Full-Linear Bandwidth | | SINAD > 68dB | | 350 | | kHz |
| Full-Power Bandwidth | | -3dB rolloff | | 6 | | MHz |
| **CONVERSION RATE** | | | | | | |
| Conversion Time (Note 5) | $t_{CONV}$ | External clock mode | 2.1 | | | µs |
| | | External acquisition/internal clock mode | 2.5 | 3.0 | 3.5 | |
| | | Internal acquisition/internal clock mode | 3.2 | 3.6 | 4 | |
| T/H Acquisition Time | $t_{ACQ}$ | | | | 400 | ns |
| Aperture Delay | | External acquisition or external clock mode | | 25 | | ns |
| Aperture Jitter | | External acquisition or external clock mode | | <50 | | ps |
| | | Internal acquisition/internal clock mode | | <200 | | |
| External Clock Frequency | $f_{CLK}$ | | 0.1 | | 7.6 | MHz |
| Duty Cycle | | | 30 | | 70 | % |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +5V ±10%, COM = GND, REFADJ = $V_{DD}$, $V_{REF}$ = +2.5V, 4.7µF capacitor at REF pin, $f_{CLK}$ = 7.6MHz (50% duty cycle), $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | | | |
| Analog Input Voltage Range Single Ended and Differential (Note 6) | $V_{IN}$ | Unipolar, $V_{COM}$ = 0 | | 0 | | $V_{REF}$ | V |
| | | Bipolar, $V_{COM}$ = $V_{REF}$ / 2 | | -$V_{REF}$/2 | | +$V_{REF}$/2 | |
| Multiplexer Leakage Current | | On-/off-leakage current, $V_{IN}$ = 0 or $V_{DD}$ | | | ±0.01 | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 12 | | pF |
| **INTERNAL REFERENCE** | | | | | | | |
| REF Output Voltage | | | | 2.49 | 2.5 | 2.51 | V |
| REF Short-Circuit Current | | | | | 15 | | mA |
| REF Temperature Coefficient | $TC_{REF}$ | | | | ±20 | | ppm/°C |
| REFADJ Input Range | | For small adjustments | | | ±100 | | mV |
| REFADJ High Threshold | | To power down the internal reference | | $V_{DD}$ - 1 | | | V |
| Load Regulation | | 0 to 0.5mA output load (Note 7) | | | 0.2 | | mV/mA |
| Capacitive Bypass at REFADJ | | | | | 0.01 | 1 | µF |
| Capacitive Bypass at REF | | | | 4.7 | | 10 | µF |
| **EXTERNAL REFERENCE AT REF** | | | | | | | |
| REF Input Voltage Range | $V_{REF}$ | | | 1.0 | | $V_{DD}$ + 50mV | V |
| REF Input Current | $I_{REF}$ | $V_{REF}$ = 2.5V, $f_{SAMPLE}$ = 420ksps | | | 200 | 300 | µA |
| | | Shutdown mode | | | | 2 | |
| **DIGITAL INPUTS AND OUTPUTS** | | | | | | | |
| Input Voltage High | $V_{IH}$ | | | 4.0 | | | V |
| Input Voltage Low | $V_{IL}$ | | | | | 0.8 | V |
| Input Hysteresis | $V_{HYS}$ | | | | 200 | | mV |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0 or $V_{DD}$ | | | ±0.1 | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 15 | | pF |
| Output Voltage Low | $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | | 0.4 | V |
| Output Voltage High | $V_{OH}$ | $I_{SOURCE}$ = 1mA | | $V_{DD}$ - 0.5 | | | V |
| Tri-State Leakage Current | $I_{LEAKAGE}$ | $\overline{CS}$ = $V_{DD}$ | | | ±0.1 | ±1 | µA |
| Tri-State Output Capacitance | $C_{OUT}$ | $\overline{CS}$ = $V_{DD}$ | | | 15 | | pF |
| **POWER REQUIREMENTS** | | | | | | | |
| Analog Supply Voltage | $V_{DD}$ | | | 4.5 | | 5.5 | V |
| Positive Supply Current | $I_{DD}$ | Operating mode, $f_{SAMPLE}$ = 420ksps | Internal reference | | 3.3 | 3.6 | mA |
| | | | External reference | | 2.8 | 3.1 | |
| | | Standby mode | Internal reference | | 1.0 | 1.2 | |
| | | | External reference | | 0.5 | 0.8 | |
| | | Shutdown mode | | | 2 | 10 | µA |
| Power-Supply Rejection | PSR | $V_{DD}$ = 5V ±10%, full-scale input | | | ±0.3 | ±0.9 | mV |

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## TIMING CHARACTERISTICS

($V_{DD}$ = +5V ±10%, COM = GND, REFADJ = $V_{DD}$, $V_{REF}$ = +2.5V, 4.7µF capacitor at REF pin, $f_{CLK}$ = 7.6MHz (50% duty cycle), $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| CLK Period | $t_{CP}$ | | 132 | | | ns |
| CLK Pulse Width High | $t_{CH}$ | | 40 | | | ns |
| CLK Pulse Width Low | $t_{CL}$ | | 40 | | | ns |
| Data Valid to $\overline{WR}$ Rise Time | $t_{DS}$ | | 40 | | | ns |
| $\overline{WR}$ Rise to Data Valid Hold Time | $t_{DH}$ | | 0 | | | ns |
| $\overline{WR}$ to CLK Fall Setup Time | $t_{CWS}$ | | 60 | | | ns |
| CLK Fall to $\overline{WR}$ Hold Time | $t_{CWH}$ | | 40 | | | ns |
| $\overline{CS}$ to CLK or $\overline{WR}$ Setup Time | $t_{CSWS}$ | | 40 | | | ns |
| CLK or $\overline{WR}$ to $\overline{CS}$ Hold Time | $t_{CSWH}$ | | 0 | | | ns |
| $\overline{CS}$ Pulse Width | $t_{CS}$ | | 100 | | | ns |
| $\overline{WR}$ Pulse Width | $t_{WR}$ | (Note 8) | 60 | | | ns |
| $\overline{CS}$ Rise to Output Disable | $t_{TC}$ | $C_{LOAD}$ = 20pF, Figure 1 | 10 | | 60 | ns |
| $\overline{RD}$ Rise to Output Disable | $t_{TR}$ | $C_{LOAD}$ = 20pF, Figure 1 | 10 | | 40 | ns |
| $\overline{RD}$ Fall to Output Data Valid | $t_{DO}$ | $C_{LOAD}$ = 20pF, Figure 1 | 10 | | 50 | ns |
| $\overline{RD}$ Fall to $\overline{INT}$ High Delay | $t_{INT1}$ | $C_{LOAD}$ = 20pF, Figure 1 | | | 50 | ns |
| $\overline{CS}$ Fall to Output Data Valid | $t_{DO2}$ | $C_{LOAD}$ = 20pF, Figure 1 | | | 100 | ns |

**Note 1:** Tested at $V_{DD}$ = +5V, COM = GND, unipolar single-ended input mode.
**Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.
**Note 3:** Offset nulled.
**Note 4:** On channel is grounded; sine wave applied to off channels.
**Note 5:** Conversion time is defined as the number of clock cycles times the clock period; clock has a 50% duty cycle.
**Note 6:** Input voltage range referenced to negative input. The absolute range for the analog inputs is from GND to $V_{DD}$.
**Note 7:** External load should not change during conversion for specified accuracy.
**Note 8:** When bit 5 is set low for internal acquisition, $\overline{WR}$ must not return low until after the first falling clock edge of the conversion.

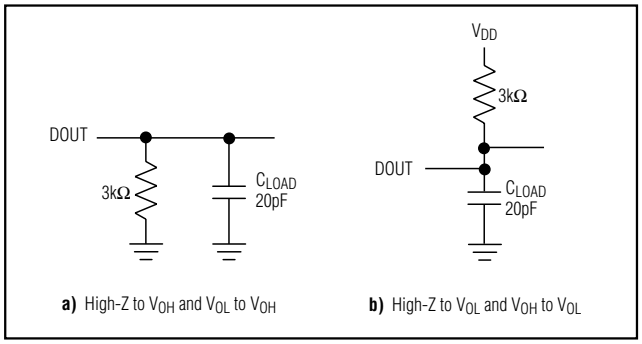


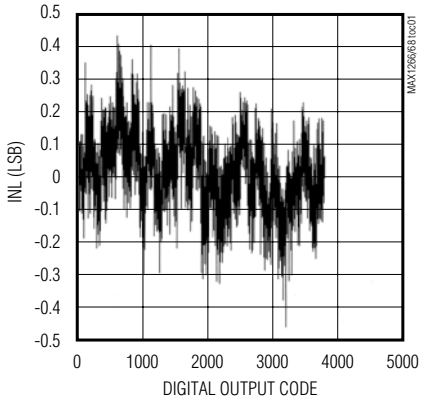

*Figure 1. Load Circuits for Enable/Disable Times*

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

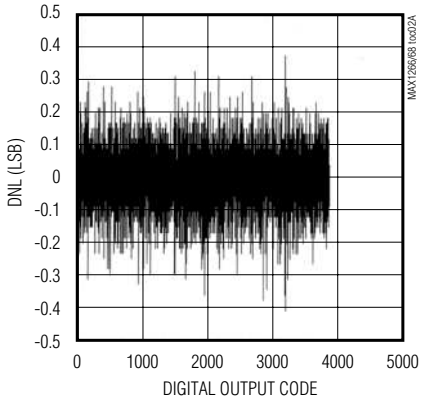
## Typical Operating Characteristics

($V_{DD}$ = +5V, $V_{REF}$ = +2.500V, $f_{CLK}$ = 7.6MHz, $C_L$ = 20pF, $T_A$ = +25°C, unless otherwise noted.)

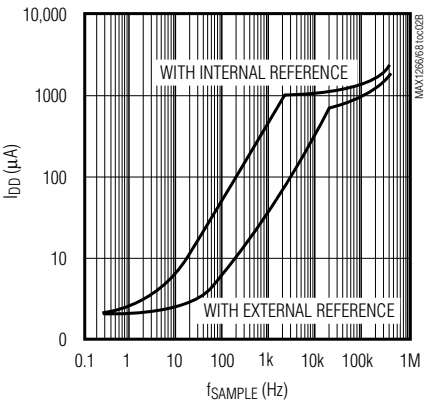
**INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE**



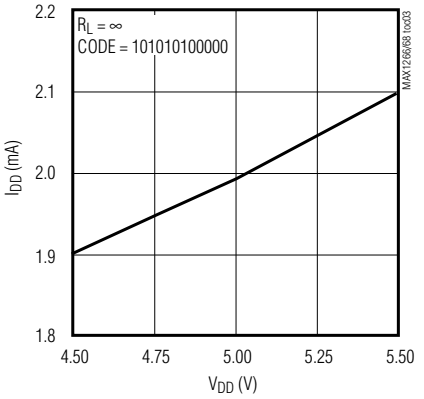

**DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE**



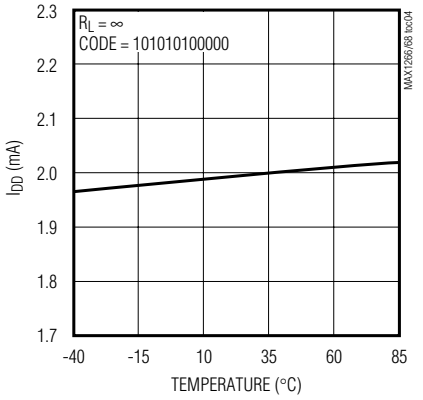

**SUPPLY CURRENT vs. SAMPLE FREQUENCY**



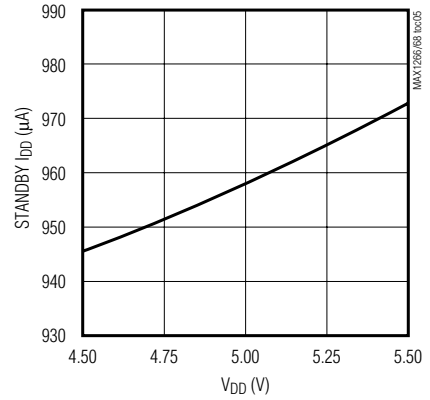

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



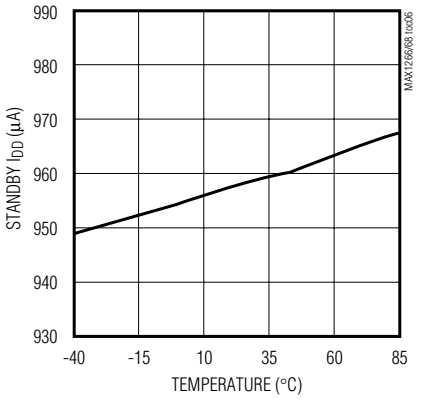

**SUPPLY CURRENT vs. TEMPERATURE**



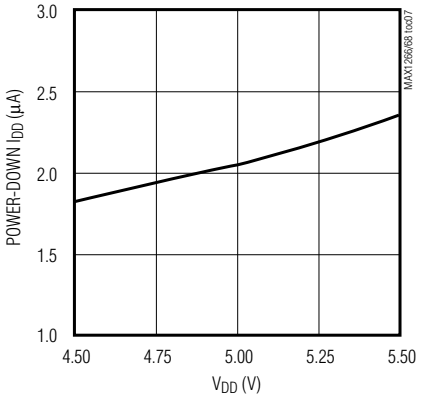

**STANDBY CURRENT vs. SUPPLY VOLTAGE**



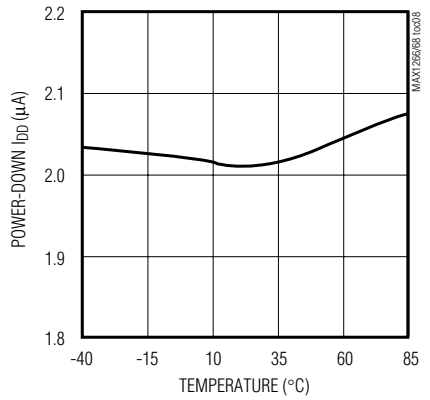

**STANDBY CURRENT vs. TEMPERATURE**




**POWER-DOWN CURRENT vs. SUPPLY VOLTAGE**




**POWER-DOWN CURRENT vs. TEMPERATURE**

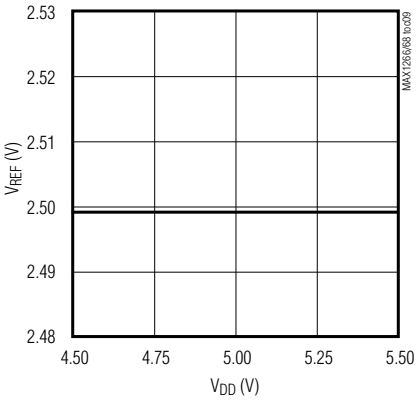


# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

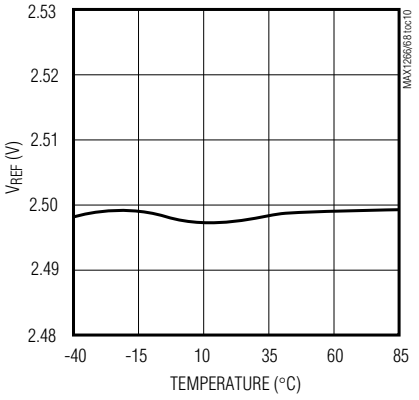
## Typical Operating Characteristics (continued)

($V_{DD}$ = +5V, $V_{REF}$ = +2.500V, $f_{CLK}$ = 7.6MHz, $C_L$ = 20pF, $T_A$ = +25°C, unless otherwise noted.)

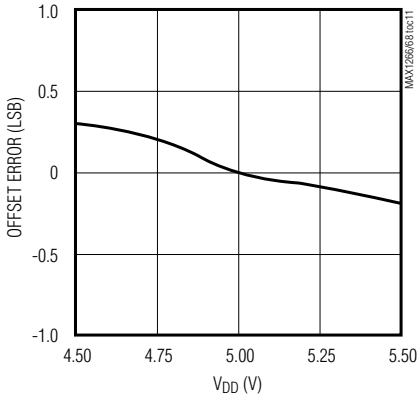
**INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE**



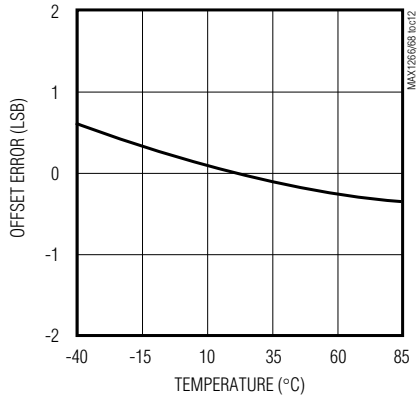

**REFERENCE VOLTAGE vs. TEMPERATURE**



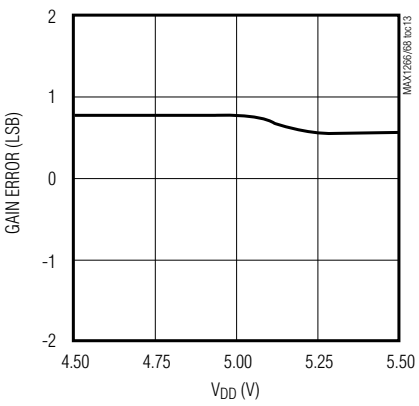

**OFFSET ERROR vs. SUPPLY VOLTAGE**



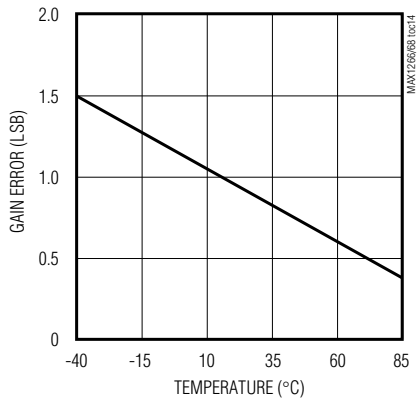

**OFFSET ERROR vs. TEMPERATURE**



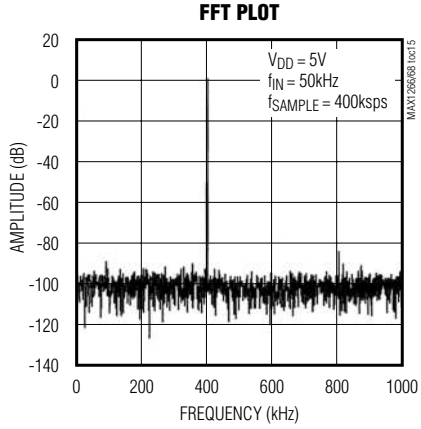

**GAIN ERROR vs. SUPPLY VOLTAGE**




**GAIN ERROR vs. TEMPERATURE**




**FFT PLOT**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1266 | MAX1268 | | |
| 1 | 1 | D9 | Tri-State Digital Output (D9) |
| 2 | 2 | D8 | Tri-State Digital Output (D8) |
| 3 | 3 | D7 | Tri-State Digital I/O Line (D7) |
| 4 | 4 | D6 | Tri-State Digital I/O Line (D6) |
| 5 | 5 | D5 | Tri-State Digital I/O Line (D5) |
| 6 | 6 | D4 | Tri-State Digital I/O Line (D4) |
| 7 | 7 | D3 | Tri-State Digital I/O Line (D3) |
| 8 | 8 | D2 | Tri-State Digital I/O Line (D2) |
| 9 | 9 | D1 | Tri-State Digital I/O Line (D1) |
| 10 | 10 | D0 | Tri-State Digital I/O Line (D0) |
| 11 | 11 | $\overline{INT}$ | $\overline{INT}$ goes low when the conversion is complete and output data is ready. |
| 12 | 12 | $\overline{RD}$ | Active-Low Read Select. If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ enables the read operation on the data bus. |
| 13 | 13 | $\overline{WR}$ | Active-Low Write Select. When $\overline{CS}$ is low in the internal acquisition mode, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{CS}$ is low in external acquisition mode, the first rising edge on $\overline{WR}$ ends acquisition and starts a conversion. |
| 14 | 14 | CLK | Clock Input. In external clock mode, drive CLK with a TTL-/CMOS-compatible clock. In internal clock mode, connect this pin to either $V_{DD}$ or GND. |
| 15 | 15 | $\overline{CS}$ | Active-Low Chip Select. When $\overline{CS}$ is high, digital outputs (D11–D0) are high impedance. |
| 16 | — | CH5 | Analog Input Channel 5 |
| 17 | — | CH4 | Analog Input Channel 4 |
| 18 | — | CH3 | Analog Input Channel 3 |
| 19 | — | CH2 | Analog Input Channel 2 |
| 20 | 16 | CH1 | Analog Input Channel 1 |
| 21 | 17 | CH0 | Analog Input Channel 0 |
| 22 | 18 | COM | Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode and must be stable to ±0.5 LSB during conversion. |
| 23 | 19 | GND | Analog and Digital Ground |
| 24 | 20 | REFADJ | Bandgap Reference Output/Bandgap Reference Buffer Input. Bypass to GND with a 0.01µF capacitor. When using an external reference, connect REFADJ to $V_{DD}$ to disable the internal bandgap reference. |

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1266 | MAX1268 | | |
| 25 | 21 | REF | Bandgap Reference Buffer Output/External Reference Input. Add a 4.7µF capacitor to GND when using the internal reference. |
| 26 | 22 | $V_{DD}$ | Analog +5V Power Supply. Bypass with a 0.1µF capacitor to GND. |
| 27 | 23 | D11 | Tri-State Digital Output (D11) |
| 28 | 24 | D10 | Tri-State Digital Output (D10) |

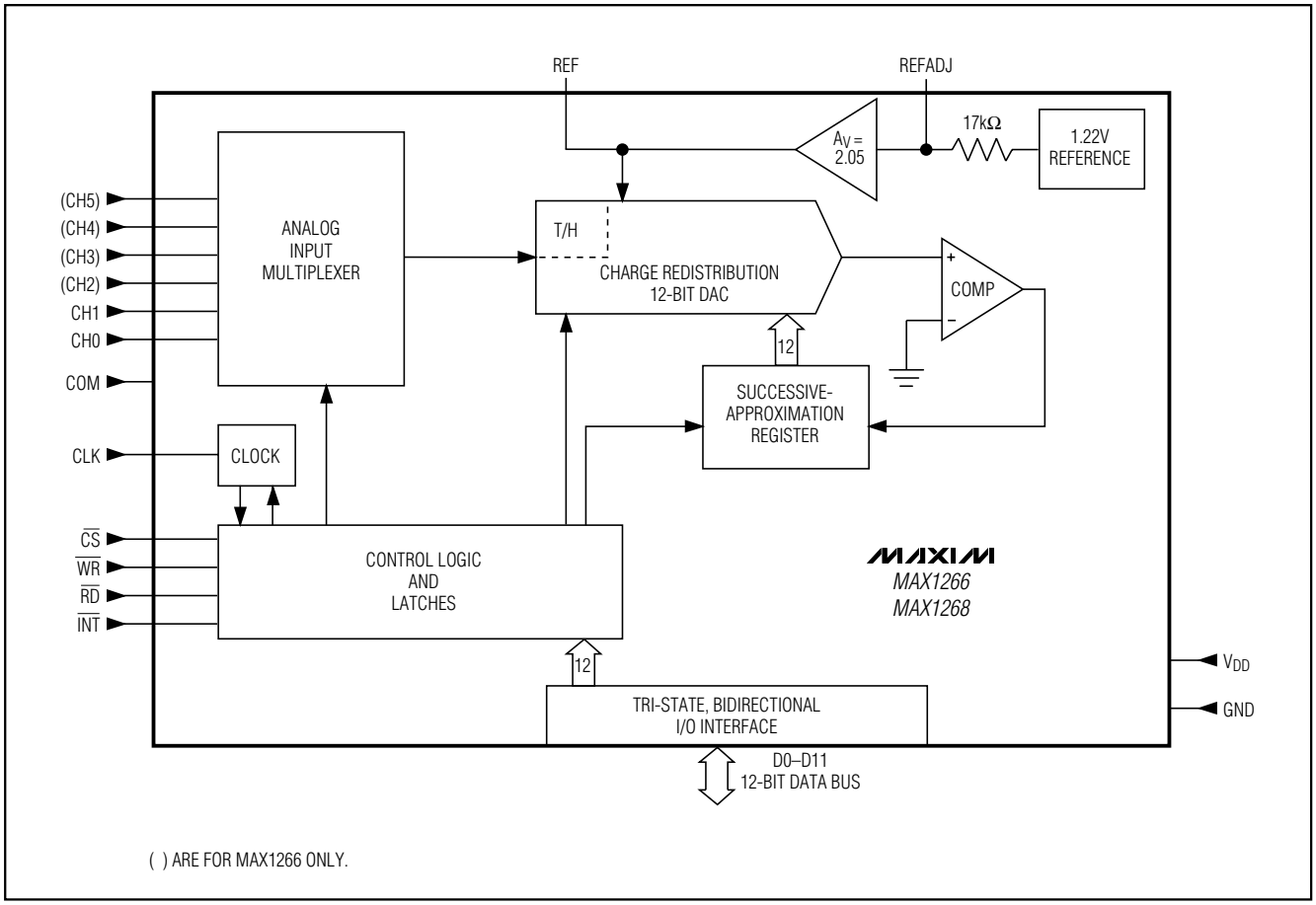



*Figure 2. Simplified Functional Diagram*

## Detailed Description

### Converter Operation

The MAX1266/MAX1268 ADCs use a successive-approximation (SAR) conversion technique and an input track/hold (T/H) stage to convert an analog input signal to a 12-bit digital output. This output format provides easy interface to standard microprocessors (µPs). Figure 2 shows the simplified internal architecture of the MAX1266/MAX1268.

### Single-Ended and Pseudo-Differential Operation

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuits of Figure 3. In single-ended mode, IN+ is internally switched to channels CH0–CH5 for the MAX1266 (Figure 3a) and to CH0–CH1 for the MAX1268 (Figure 3b), while IN- is switched to COM (Table 2). In differential mode, IN+ and IN- are selected from analog input pairs (Table 3) and are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5 LSB (±0.1 LSB for best performance) with respect to GND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected input) to GND.

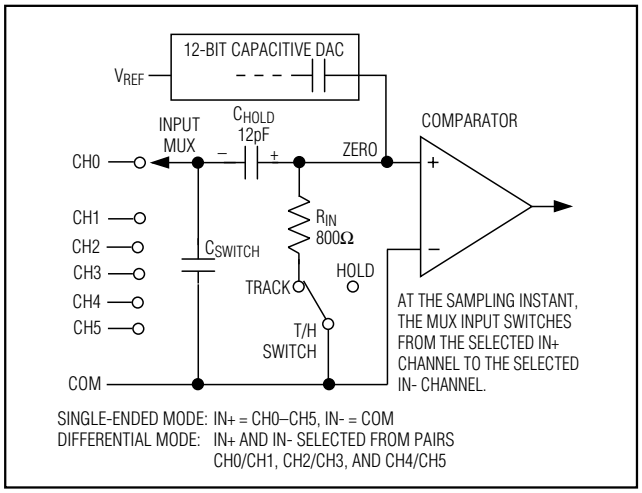



*Figure 3a. MAX1266 Simplified Input Structure*

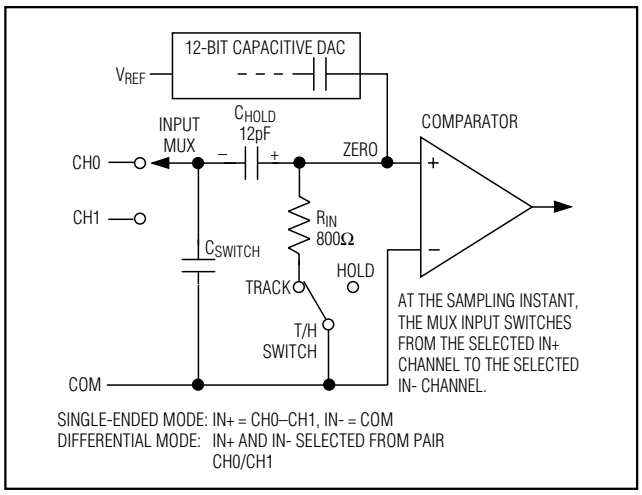



*Figure 3b. MAX1268 Simplified Input Structure*

## Table 1. Control-Byte Functional Description

| BIT | NAME | FUNCTIONAL DESCRIPTION | | |
|---|---|---|---|---|
| D7, D6 | PD1, PD0 | **PD1** and **PD0** select the various clock and power-down modes. | | |
| | | **0** | **0** | Full power-down mode. Clock mode is unaffected. |
| | | **0** | **1** | Standby power-down mode. Clock mode is unaffected. |
| | | **1** | **0** | Normal operation mode. Internal clock mode selected. |
| | | **1** | **1** | Normal operation mode. External clock mode selected. |
| D5 | ACQMOD | ACQMOD = 0: Internal acquisition mode<br>ACQMOD = 1: External acquisition mode | | |
| D4 | SGL/$\overline{DIF}$ | SGL/$\overline{DIF}$ = 0: Pseudo-differential analog input mode<br>SGL/$\overline{DIF}$ = 1: Single-ended analog input mode<br>In single-ended mode, input signals are referred to COM. In pseudo-differential mode, the voltage difference between two channels is measured (Tables 2 and 4). | | |
| D3 | UNI/$\overline{BIP}$ | UNI/$\overline{BIP}$ = 0: Bipolar mode<br>UNI/$\overline{BIP}$ = 1: Unipolar mode<br>In unipolar mode, an analog input signal from 0V to $V_{REF}$ can be converted; in bipolar mode, the signal can range from $-V_{REF}/2$ to $+V_{REF}/2$. | | |
| D2, D1, D0 | A2, A1, A0 | Address bits A2, A1, A0 select which of the 6/2 (MAX1266/MAX1268) channels is to be converted (Tables 2 and 3). | | |

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

**Table 2. Channel Selection for Single-Ended Operation (SGL/$\overline{DIF}$ = 1)**

| A2 | A1 | A0 | CH0 | CH1 | CH2* | CH3* | CH4* | CH5* | COM |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | + | | | | | | - |
| 0 | 0 | 1 | | + | | | | | - |
| 0 | 1 | 0 | | | + | | | | - |
| 0 | 1 | 1 | | | | + | | | - |
| 1 | 0 | 0 | | | | | + | | - |
| 1 | 0 | 1 | | | | | | + | - |

**Channels CH2–CH5 apply to MAX1266 only.*

**Table 3. Channel Selection for Pseudo-Differential Operation (SGL/$\overline{DIF}$ = 0)**

| A2 | A1 | A0 | CH0 | CH1 | CH2* | CH3* | CH4* | CH5* |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | + | | | | | |
| 0 | 0 | 1 | | + | | | | |
| 0 | 1 | 0 | | | + | - | | |
| 0 | 1 | 1 | | | | + | | |
| 1 | 0 | 0 | | | | | + | - |
| 1 | 0 | 1 | | | | | - | + |

**Channels CH2–CH5 apply to MAX1266 only.*

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor $C_{HOLD}$. At the end of the acquisition interval, the T/H switch opens, retaining charge on $C_{HOLD}$ as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching $C_{HOLD}$ from the positive input (IN+) to the negative input (IN-). This unbalances node zero at the comparator's positive input. The capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node 0 to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a 12pF [($V_{IN+}$ - $V_{IN-}$)] charge from $C_{HOLD}$ to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

### Analog Input Protection

Internal protection diodes, which clamp the analog input to $V_{DD}$ and GND, allow each input channel to swing within (GND - 300mV) to ($V_{DD}$ + 300mV) without damage. However, for accurate conversions near full scale, both inputs must not exceed ($V_{DD}$ + 50mV) or be less than (GND - 50mV).

If an analog input voltage exceeds the supplies by more than 50mV, limit the forward-bias input current to 4mA.

### Track/Hold

The MAX1266/MAX1268 T/H stage enters its tracking mode on the rising edge of $\overline{WR}$. In external acquisition mode, the part enters its hold mode on the next on rising edge of WR. In internal acquisition mode, the part enters its hold mode on the fourth falling edge of clock after writing the control byte. Note that, in internal clock mode, this is approximately 1µs after writing the control byte.

In single-ended operation, IN- is connected to COM and the converter samples the positive (+) input. In pseudo-differential operation, IN- connects to the negative (-) input, and the difference of |(IN+) - (IN-)| is sampled. At the beginning of the next conversion, the positive input connects back to IN+ and $C_{HOLD}$ charges to the input signal.

The time required for the T/H stage to acquire an input signal depends on how quickly its input capacitance is charged. If the input signal's source impedance is high,

the acquisition time lengthens and more time must be allowed between conversions. The acquisition time, $t_{ACQ}$, is the maximum time the device takes to acquire the signal, and is also the minimum time required for the signal to be acquired. Calculate this with the following equation:

$$t_{ACQ} = 9(R_S + R_{IN})C_{IN}$$

where $R_S$ is the source impedance of the input signal, $R_{IN}$ (800Ω) is the input resistance, and $C_{IN}$ (12pF) is the ADC's input capacitance. Source impedances below 3kΩ have no significant impact on the MAX1266/MAX1268s' AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Together with the input impedance, this capacitor forms an RC filter, limiting the ADC's signal bandwidth.

### Input Bandwidth

The MAX1266/MAX1268 T/H stage offers a 350kHz full-linear and a 6MHz full-power bandwidth. This makes it possible to digitize high-speed transients and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

### Starting a Conversion

Initiate a conversion by writing a control byte, which selects the multiplexer channel and configures the MAX1266/MAX1268 for either unipolar or bipolar operation. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD (acquisition mode) bit in the input control byte (Table 1) offers two options for acquiring the signal: an internal and an external acquisition. The conversion period lasts for 13 clock cycles in either the internal or external clock or acquisition mode. Writing a new control byte during a conversion cycle aborts the conversion and starts a new acquisition interval.

#### Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this acquisition interval (three external clock cycles or approximately 1µs in internal clock mode) ends (Figure 4). Note that, when the internal acquisition is combined with the internal clock, the aperture jitter can be as high as 200ps. Internal clock users wishing to achieve the 50ps jitter specification should always use external acquisition mode.

#### External Acquisition

Use external acquisition mode for precise control of the sampling aperture and/or dependent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0 (all other bits in control byte unchanged), terminates acquisition and starts conversion on $\overline{WR}$ rising edge (Figure 5).

The address bits for the input multiplexer must have the same values on the first and second write pulse. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Modes* section). Changing other bits in the control byte corrupts the conversion.

### Reading a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the MAX1266/MAX1268 to flag the µP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when the conversion is complete and the output data is ready (Figures 4 and 5). It returns high on the first read cycle or if a new control byte is written.

### Selecting Clock Mode

The MAX1266/MAX1268 operate with either an internal or an external clock. Control bits D6 and D7 select either internal or external clock mode. The part retains the last-requested clock mode if a power-down mode is selected in the current input word. For both internal and external clock mode, internal or external acquisition can be used. At power-up, the MAX1266/MAX1268 enter the default external clock mode.

#### Internal Clock Mode

Select internal clock mode to release the µP from the burden of running the SAR conversion clock. Bit D7 of the control byte must be set to 1 and bit D6 must be set to zero. The internal clock frequency is then selected, resulting in a conversion time of 3.6µs. When using the internal clock mode, tie the CLK pin either high or low to prevent the pin from floating.

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

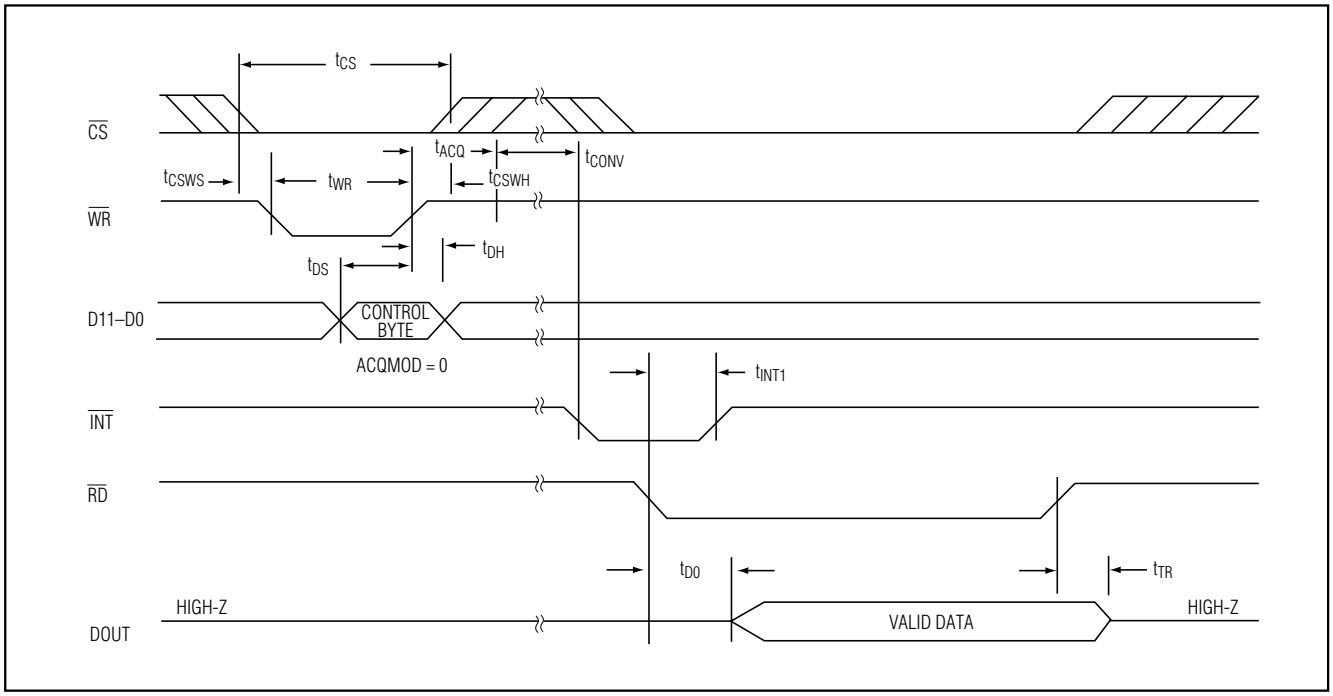



*Figure 4. Conversion Timing Using Internal Acquisition Mode*

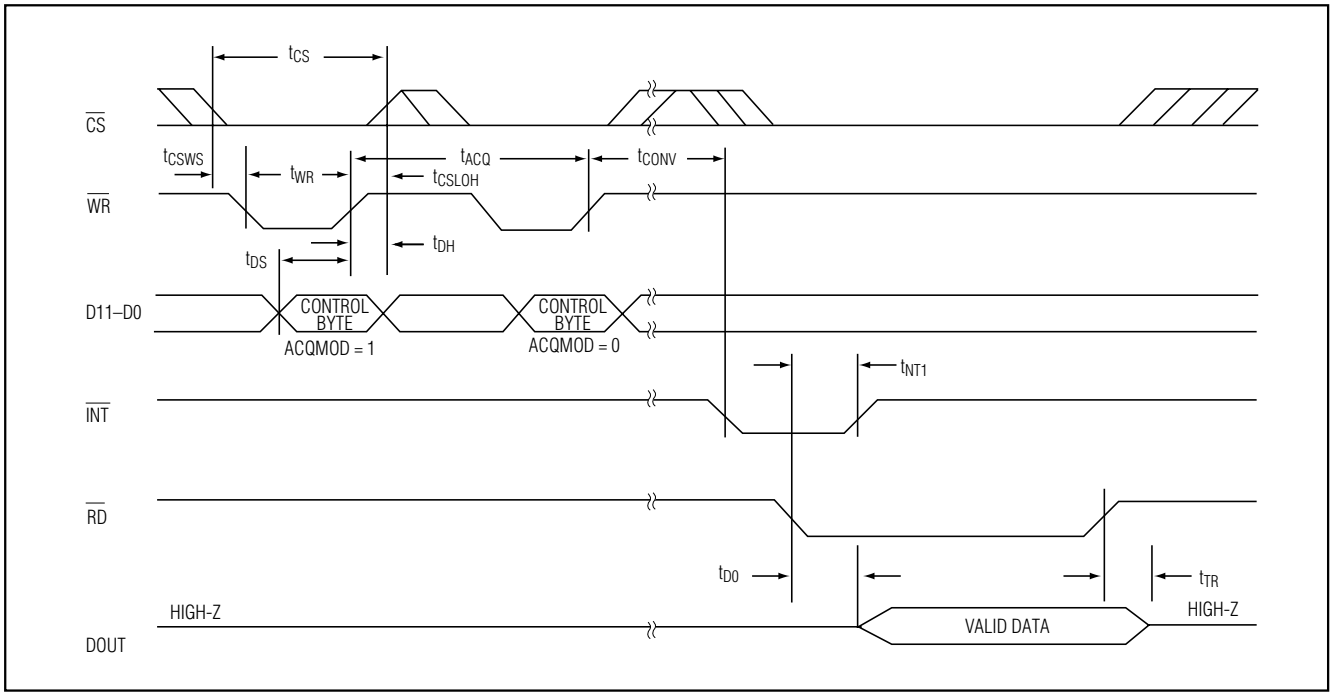



*Figure 5. Conversion Timing Using External Acquisition Mode*

### External Clock Mode

To select external clock mode, bits D6 and D7 of the control byte must be set to 1. Figure 6 shows the clock and $\overline{WR}$ timing relationship for internal (Figure 6a) and external (Figure 6b) acquisition modes with an external clock. For proper operation, a 100kHz to 7.6MHz clock frequency with 30% to 70% duty cycle is recommended. Operating the MAX1266/MAX1268 with clock frequencies lower than 100kHz is not recommended, because the resulting voltage droop across the hold capacitor in the T/H stage degrades performance.

### Digital Interface

The input and output data are multiplexed on a tri-state parallel interface (I/O) that can easily be interfaced with standard µPs. The signals $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ represents the chip-select signal, which enables a µP to address the MAX1266/MAX1268 as an I/O port. When high, $\overline{CS}$ disables the CLK, $\overline{WR}$, and $\overline{RD}$ inputs and forces the interface into a high-impedance (high-Z) state.

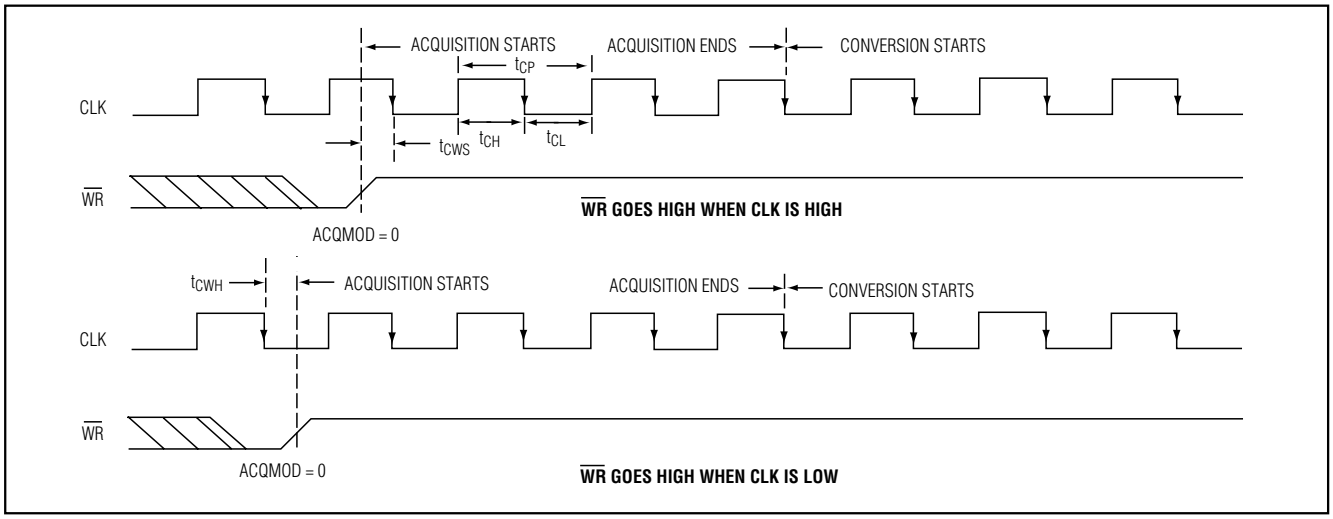



*Figure 6a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)*

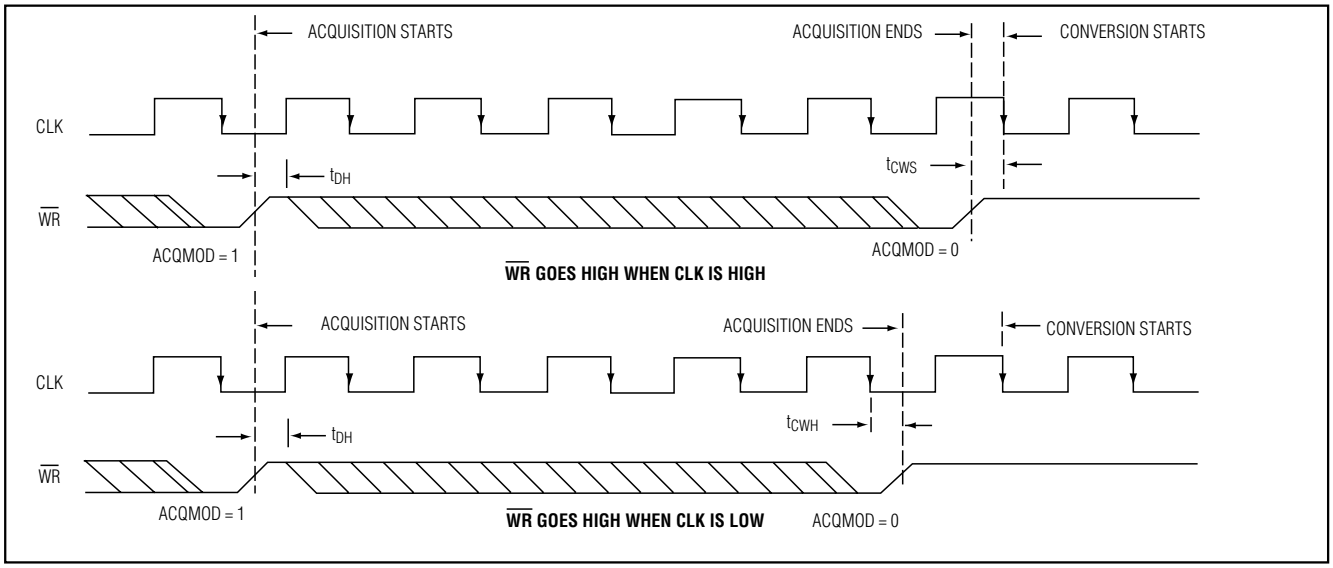



*Figure 6b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)*

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## Table 4. Control-Byte Format

| D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) |
|---|---|---|---|---|---|---|---|
| PD1 | PD0 | ACQMOD | SGL/$\overline{DIF}$ | UNI/$\overline{BIP}$ | A2 | A1 | A0 |

### *Input Format*

The control bit sequence is latched into the device on pins D7–D0 during a write command. Table 4 shows the control-byte format.

### *Output Data Format*

The 12-bit-wide output format for both the MAX1266/MAX1268 is binary in unipolar mode and two's complement in bipolar mode. $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{INT}$, and the 12 bits of output data can interface directly to a 16-bit data bus. When reading the output data, $\overline{CS}$ and $\overline{RD}$ must be low.

## Applications Information

### Power-On Reset

When power is first applied, internal power-on reset circuitry activates the MAX1266/MAX1268 in external clock mode and sets $\overline{INT}$ high. After the power supplies stabilize, the internal reset time is 10µs; no conversions should be attempted during this phase. When using the internal reference, 500µs are required for $V_{REF}$ to stabilize.

### Internal and External Reference

The MAX1266/MAX1268 can be used with an internal or external reference voltage. An external reference can be connected directly to REF or REFADJ.

An internal buffer is designed to provide +2.5V at REF for both devices. The internally trimmed +1.22V reference is buffered with a +2.05V/V gain.

### *Internal Reference*

The full-scale range with the internal reference is +2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference buffer allows for small adjustments (±100mV) in the reference voltage (Figure 7).

**Note:** The reference buffer must be compensated with an external capacitor (4.7µF min) connected between REF and GND to reduce reference noise and switching spikes from the ADC. To further minimize reference noise, connect a 0.01µF capacitor between REFADJ and GND.

### *External Reference*

With the MAX1266/MAX1268, an external reference can be placed at either the input (REFADJ) or the output (REF) of the internal-reference buffer amplifier.

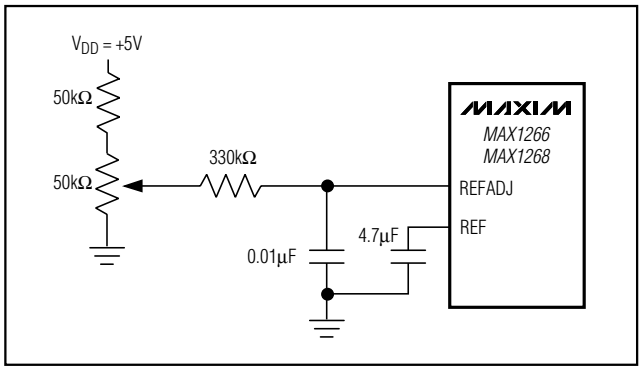



*Figure 7. Reference Adjustment with External Potentiometer*

Using the REFADJ input makes buffering the external reference unnecessary. The REFADJ input impedance is typically 17kΩ.

When applying an external reference to REF, disable the internal reference buffer by connecting REFADJ to $V_{DD}$. The DC input resistance at REF is 25kΩ. Therefore, an external reference at REF must deliver up to 200µA DC load current during a conversion and have an output impedance less than 10Ω. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

### Power-Down Modes

To save power, place the converter in a low-current shutdown state between conversions. Select standby mode or shutdown mode using bits D6 and D7 of the control byte (Tables 1 and 4). In both software power-down modes, the parallel interface remains active, but the ADC does not convert.

### *Standby Mode*

While in standby mode, the supply current is typically 1mA. The part powers up on the next rising edge of $\overline{WR}$ and is ready to perform conversions. This quick turn-on time allows the user to realize significantly reduced power consumption for conversion rates below 420ksps.

**Table 5. Full Scale and Zero Scale for Unipolar and Bipolar Operation**

| UNIPOLAR MODE | | BIPOLAR MODE | |
|---|---|---|---|
| Full scale | $V_{REF}$ + COM | Positive full scale | $V_{REF}/2$ + COM |
| Zero scale | COM | Zero scale | COM |
| — | — | Negative full scale | $-V_{REF}/2$ + COM |

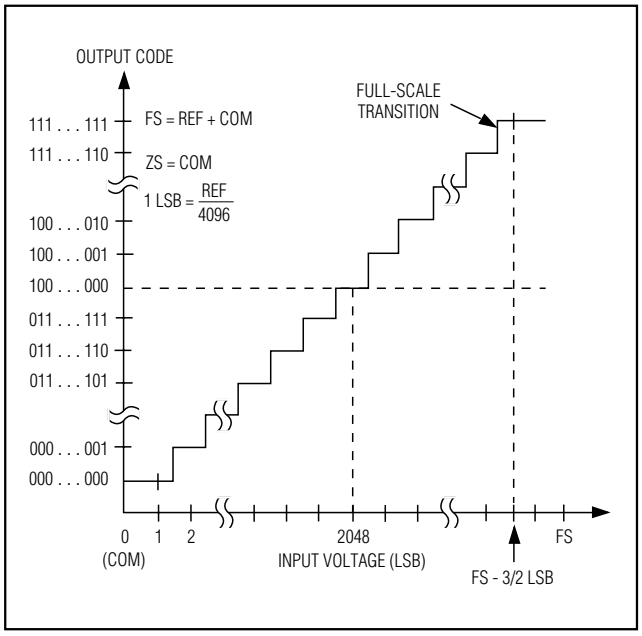



*Figure 8. Unipolar Transfer Functions*

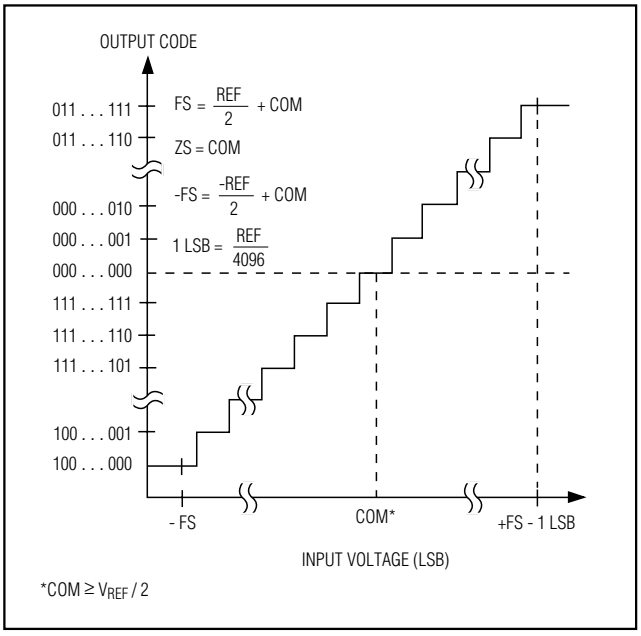



*Figure 9. Bipolar Transfer Functions*

### *Shutdown Mode*

Shutdown mode turns off all chip functions that draw quiescent current, reducing the typical supply current to 2µA immediately after the current conversion is completed. A rising edge on $\overline{WR}$ causes the MAX1266/MAX1268 to exit shutdown mode and return to normal operation. To achieve full 12-bit accuracy with a 4.7µF reference bypass capacitor, 500µs is required after power-up. Waiting 500µs in standby mode, instead of in full-power mode, can reduce power consumption by a factor of 3 or more. When using an external reference, only 50µs is required after power-up. Enter standby mode by performing a dummy conversion with the control byte specifying standby mode.

**Note:** Bypass capacitors larger than 4.7µF between REF and GND result in longer power-up delays.

### *Transfer Function*

Table 5 shows the full-scale voltage ranges for unipolar and bipolar modes. Figures 8 depicts the nominal unipolar input/output (I/O) transfer function, and Figure 9 shows the bipolar I/O transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = ($V_{REF}$ / 4096).

### *Maximum Sampling Rate/ Achieving 475ksps*

When running at the maximum clock frequency of 7.6MHz, the specified throughput of 420ksps is achieved by completing a conversion every 18 clock cycles: 1 write cycle, 3 acquisition cycles, 13 conversion cycles, and 1 read cycle. This assumes that the results of the last conversion are read before the next control byte is written. It is possible to achieve higher throughputs, up to 475ksps, by first writing a control byte to begin the acquisition cycle of the next conversion, then reading the results of the previous conversion from the bus. This technique (Figure 10) allows a conversion to be completed every 16 clock cycles. Note that the switching of the data bus during acquisi-

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

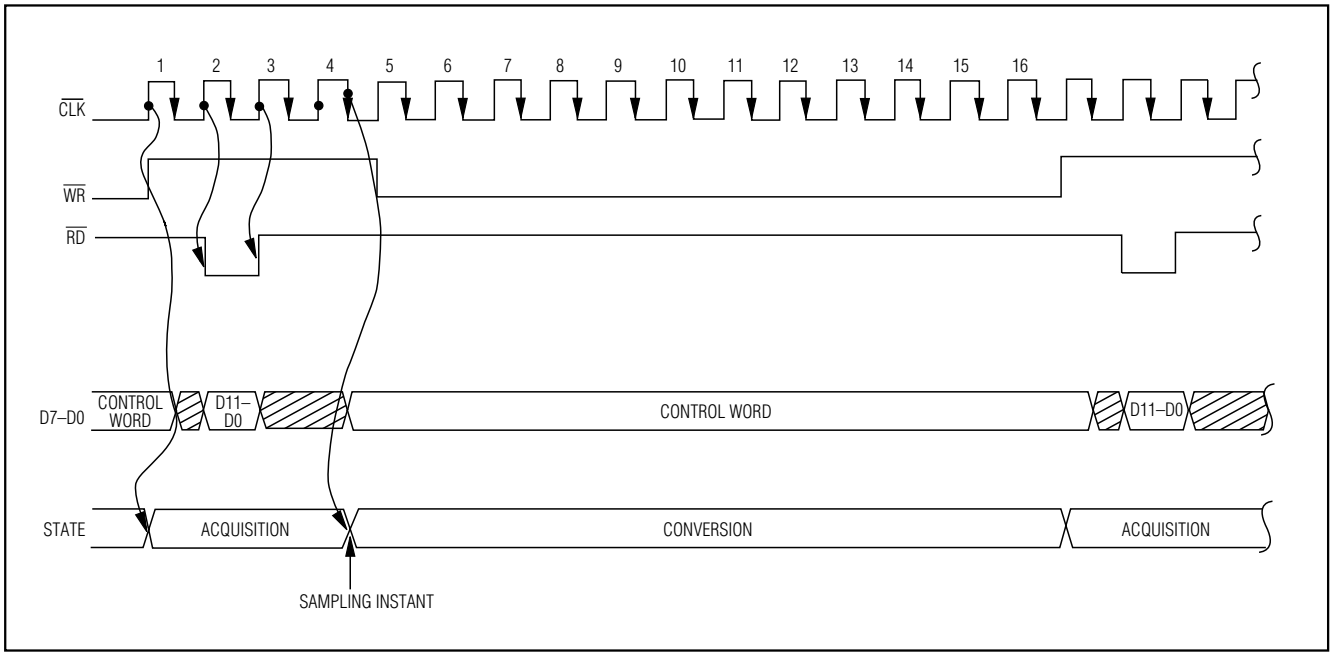



*Figure 10. Timing Diagram for Fastest Conversion*

tion or conversion can cause additional supply noise, which can make it difficult to achieve true 12-bit performance.

### Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap configurations are not recommended, since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital PC board ground sections with only one star point (Figure 11) connecting the two ground systems (analog and digital). For lowest noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply, $V_{DD}$, could impair operation of the ADC's fast comparator. Bypass $V_{DD}$ to the star ground with a network of two parallel capacitors, 0.1µF and 4.7µF, located as close to the MAX1266/MAX1268s' power-supply pin as possible. Minimize capacitor lead length for best supply-noise rejection and add an attenuation resistor (5Ω) if the power supply is extremely noisy.

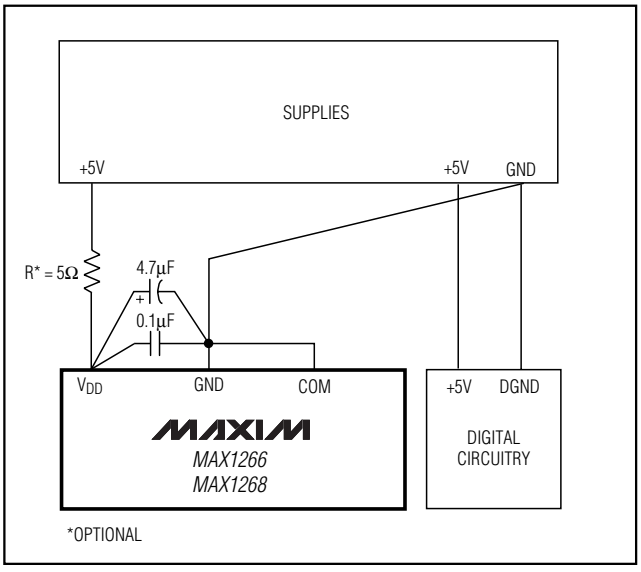



*Figure 11. Power-Supply and Grounding Connections*

## Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1266/MAX1268 is measured using the end-point method.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

### Aperture Jitter

Aperture jitter ($t_{AJ}$) is the sample-to-sample variation in the time between the samples.

### Aperture Delay

Aperture delay ($t_{AD}$) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

### Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N-bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

### Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD\ (dB) = 20 \times \log\ (Signal_{RMS} / Noise_{RMS})$$

### Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)} / V_1\right)$$

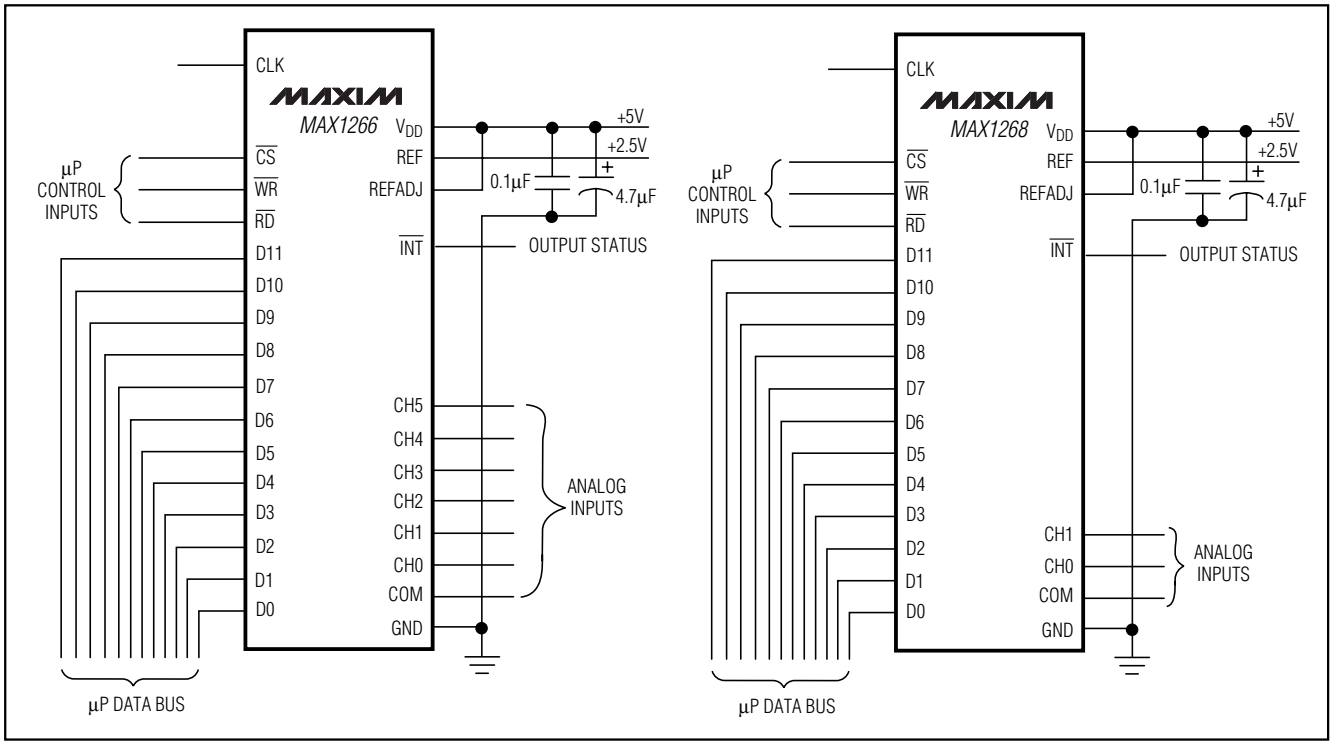
where V1 is the fundamental amplitude, and V2 through V5 are the amplitudes of the 2nd- through 5th-order harmonics.

### Spurious-Free Dynamic Range

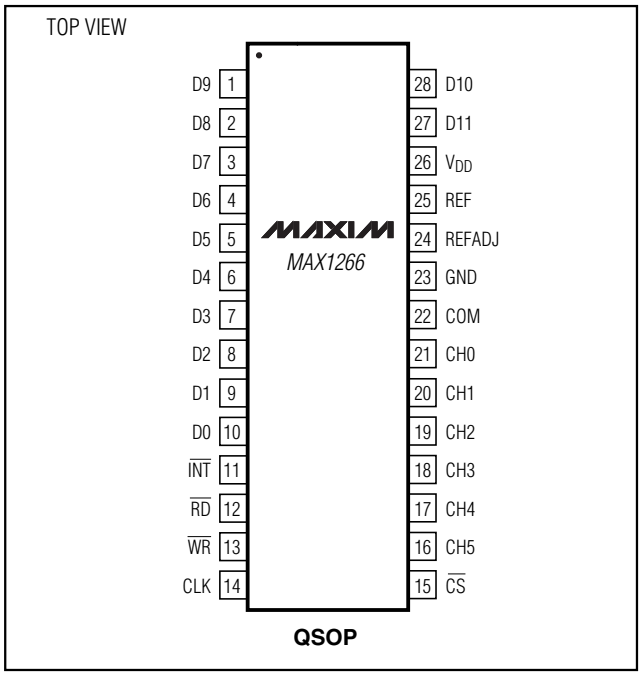
Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## Typical Operating Circuits




## Pin Configurations (continued)




## Chip Information

TRANSISTOR COUNT: 5781

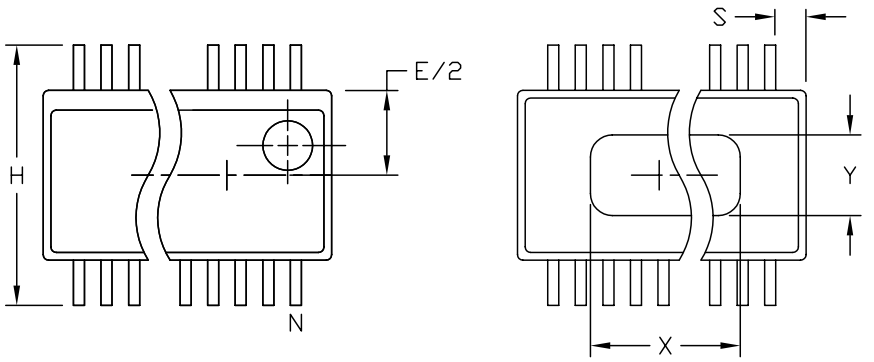
SUBSTRATE CONNECTED TO GND

# 420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS




| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | .061 | .068 | 1.55 | 1.73 |
| A1 | .004 | .0098 | 0.102 | 0.249 |
| A2 | .055 | .061 | 1.40 | 1.55 |
| B | .008 | .012 | 0.20 | 0.31 |
| C | .0075 | .0098 | 0.191 | 0.249 |
| D | SEE VARIATIONS | | | |
| E | .150 | .157 | 3.81 | 3.99 |
| e | .025 BSC | | 0.635 BSC | |
| H | .230 | .244 | 5.84 | 6.20 |
| h | .010 | .016 | 0.25 | 0.41 |
| L | .016 | .035 | 0.41 | 0.89 |
| N | SEE VARIATIONS | | | |
| X | SEE VARIATIONS | | | |
| Y | .071 | .087 | 1.803 | 2.209 |
| α | 0° | 8° | 0° | 8° |

VARIATIONS:

| | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | N | |
|---|---|---|---|---|---|---|
| D | .189 | .196 | 4.80 | 4.98 | 16 | AA |
| S | .0020 | .0070 | 0.05 | 0.18 | | |
| X | .107 | .123 | 2.72 | 3.12 | | |
| D | .337 | .344 | 8.56 | 8.74 | 20 | AB |
| S | .0500 | .0550 | 1.270 | 1.397 | | |
| D | .337 | .344 | 8.56 | 8.74 | 24 | AC |
| S | .0250 | .0300 | 0.635 | 0.762 | | |
| D | .386 | .393 | 9.80 | 9.98 | 28 | AD |
| S | .0250 | .0300 | 0.635 | 0.762 | | |
| X | .271 | .287 | 6.88 | 7.29 | | |

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV | |
|---|---|---|---|
| | 21-0055 | C | 1/1 |

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