MAX1300/MAX1301

8- and 4-Channel, ±3 x V_{REF} Multirange Inputs, Serial 16-Bit ADCs

General Description

The MAX1300/MAX1301 multirange, low-power, 16-bit, successive-approximation, analog-to-digital converters (ADCs) operate from a single +5V supply and achieve throughput rates up to 115ksps. A separate digital supply allows digital interfacing with 2.7V to 5.25V systems using the SPI-/QSPI™-/MICROWIRE®-compatible serial interface. Partial power-down mode reduces the supply current to 1.3mA (typ). Full power-down mode reduces the power-supply current to 1µA (typ).

The MAX1300 provides eight (single-ended) or four (true differential) analog input channels. The MAX1301 provides four (single-ended) or two (true differential) analog input channels. Each analog input channel is independently software programmable for seven single-ended input ranges [0 to (3 x V_{REF})/2, (-3 x V_{REF})/2 to 0, 0 to 3 x V_{REF}, -3 x V_{REF} to 0, (±3 x V_{REF})/4, (±3 x V_{REF})/2, ±3 x V_{REF}] and three differential input ranges [(±3 x V_{REF})/2, ±3 x V_{REF}, ±6 x V_{REF}].

An on-chip +4.096V reference offers a small convenient ADC solution. The MAX1300/MAX1301 also accept an external reference voltage between 3.800V and 4.136V.

The MAX1300 is available in a 24-pin TSSOP package and the MAX1301 is available in a 20-pin TSSOP package. Each device is specified for operation from -40°C to +85°C.

Applications

- Industrial Control Systems
- Data-Acquisition Systems
- Avionics
- Robotics

QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

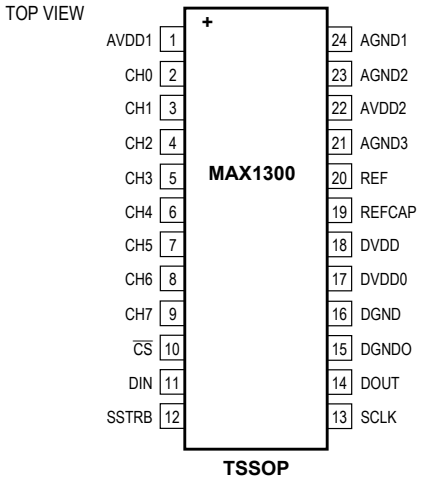
- Software-Programmable Input Range for Each Channel
- Single-Ended Input Ranges (V_{REF} = 4.096V)
  0 to (3 x V_{REF})/2, (-3 x V_{REF})/2 to 0, 0 to 3 x V_{REF}, -3 x V_{REF} to 0, (±3 x V_{REF})/4, (±3 x V_{REF})/2, ±3 x V_{REF}
- Differential Input Ranges
  (±3 x V_{REF})/2, ±3 x V_{REF}, ±6 x V_{REF}
- Eight Single-Ended or Four Differential Analog Inputs (MAX1300)
- Four Single-Ended or Two Differential Analog Inputs (MAX1301)
- ±16.5V Overvoltage Tolerant Inputs
- Internal or External Reference
- 115ksps Maximum Sample Rate
- Single +5V Power Supply
- 20-/24-Pin TSSOP Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	CHANNELS
MAX1300AEUG+	-40°C to +85°C	24 TSSOP	8
MAX1300BEUG+	-40°C to +85°C	24 TSSOP	8
MAX1301AEUP+	-40°C to +85°C	20 TSSOP	4
MAX1301BEUP+	-40°C to +85°C	20 TSSOP	4

+Denotes lead(Pb)-free/RoHS-compliant package.

Pin Configurations



TSSOP

Pin Configurations continued at end of data sheet.

maxim integrated™

Absolute Maximum Ratings

AVDD1 to AGND1 .....-0.3V to +6V
AVDD2 to AGND2 .....-0.3V to +6V
DVDD to DGND.....-0.3V to +6V
DVDDO to DGNDO.....-0.3V to +6V
DVDD to DVDDO .....-0.3V to +6V
DVDD, DVDDO to AVDD1.....-0.3V to +6V
AVDD1, DVDD, DVDDO to AVDD2.....-0.3V to +6V
DGND, DGNDO, AGND3, AGND2 to AGND1 .....-0.3V to +0.3V
$\overline{CS}$, SCLK, DIN, DOUT, SSTRB to DGNDO ..... -0.3V to (V_{DVDDO} + 0.3V)
CH0–CH7 to AGND1.....-16.5V to +16.5V
REF, REFCAP to AGND1..... -0.3V to (V_{AVDD1} + 0.3V)
Continuous Current (any pin).....±50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 11mW/°C above +70°C).....879mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C).....976mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range (±3 x V_{REF}), C_{DOUT} = 50pF, C_{SSTRB} = 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Notes 1, 2)							
Resolution				16			Bits
Integral Nonlinearity	INL	MAX130_A			±1.0	±2	LSB
		MAX130_B			±1.0	±4	
Differential Nonlinearity	DNL	No missing codes		-1		+2	LSB
Transition Noise		External or internal reference			1		LSB_{RMS}
Offset Error		Single-ended inputs	Unipolar		0	±20	mV
			Bipolar		-1.0	±12	
		Differential inputs (Note 3)	Bipolar		-2.0	±20	
Channel-to-Channel Gain Matching		Unipolar or bipolar			0.025		%FSR
Channel-to-Channel Offset Error Matching		Unipolar or bipolar			1.0		mV
Offset Temperature Coefficient		Unipolar			3		µV/°C
		Bipolar			1		
		Fully differential			2		
Gain Error		Unipolar				±0.5	%FSR
		Bipolar				±0.8	
		Fully differential				±1	
Gain Temperature Coefficient		Unipolar			2		ppm/°C
		Bipolar			1		
		Fully differential			2		
DYNAMIC SPECIFICATIONS $f_{IN(SINE-WAVE)}$ = 5kHz, V_{IN} = FSR - 0.05dB (Notes 1, 2)							
Signal-to-Noise Plus Distortion	SINAD	Differential inputs, FSR = ±6 x V_{REF}			91		dB
		Single-ended inputs, FSR = ±3 x V_{REF}			89		
		Single-ended inputs, FSR = (±3 x V_{REF})/2			86		
		Single-ended inputs, FSR = (±3 x V_{REF})/4		80	83		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range (±3 x V_{REF}), C_{DOUT} = 50pF, C_{SSTRB} = 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	Differential inputs, FSR = ±6 x V_{REF}		91		dB
		Single-ended inputs, FSR = ±3 x V_{REF}		89		
		Single-ended inputs, FSR = (±3 x V_{REF})/2		86		
		Single-ended inputs, FSR = (±3 x V_{REF})/4		83		
Total Harmonic Distortion (Up to the 5th Harmonic)	THD			-97		dB
Spurious-Free Dynamic Range	SFDR		92	99		dB
Aperture Delay	t_{AD}	Figure 21		15		ns
Aperture Jitter	t_{AJ}	Figure 21		100		ps
Channel-to-Channel Isolation				105		dB
CONVERSION RATE						
Byte-Wide Throughput Rate	f_{SAMPLE}	External clock mode, Figure 2			114	ksps
		External acquisition mode, Figure 3			84	
		Internal clock mode, Figure 4			106	
ANALOG INPUTS (CH0–CH3 MAX1301, CH0–CH7 MAX1300, AGND1)						
Small-Signal Bandwidth		All input ranges, V_{IN} = 100mV_{P-P} (Note 2)		2		MHz
Full-Power Bandwidth		All input ranges, V_{IN} = 4V_{P-P} (Note 2)		700		kHz
Input Voltage Range (Table 6)	$V_{CH_}$	R[2:1] = 001	(-3 x V_{REF})/4		(+3 x V_{REF})/4	V
		R[2:1] = 010	(-3 x V_{REF})/2		0	
		R[2:1] = 011	0		(+3 x V_{REF})/2	
		R[2:1] = 100	(-3 x V_{REF})/2		(+3 x V_{REF})/2	
		R[2:1] = 101	-3 x V_{REF}		0	
		R[2:1] = 110	0		+3 x V_{REF}	
		R[2:1] = 111	-3 x V_{REF}		+3 x V_{REF}	
True-Differential Analog Common-Mode Voltage Range	V_{CMDR}	DIF/$\overline{SGL}$ = 1 (Note 4)	-14		+9	V
Common-Mode Rejection Ratio	CMRR	DIF/$\overline{SGL}$ = 1, input voltage range = (±3 x V_{REF})/4		75		dB
Input Current	$I_{CH_}$	-3 x V_{REF} < $V_{CH_}$ < +3 x V_{REF}	-1250		+900	µA
Input Capacitance	$C_{CH_}$			5		pF
Input Resistance	$R_{CH_}$			17		kΩ

Electrical Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range (±3 x V_{REF}), C_{DOUT} = 50pF, C_{SSTRB} = 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE (Bypass REFCAP with 0.1µF to AGND1 and REF with 1.0µF to AGND1)						
Reference Output Voltage	V_{REF}		4.056	4.096	4.136	V
Reference Temperature Coefficient	TC_{REF}			±30		ppm/°C
Reference Short-Circuit Current	I_{REFSC}	REF shorted to AGND1		10		mA
		REF shorted to AVDD		-1		
Reference Load Regulation		I_{REF} = 0 to 0.5mA		0.1	10	mV
EXTERNAL REFERENCE (REFCAP = AVDD)						
Reference Input Voltage Range	V_{REF}		3.800		4.136	V
REFCAP Buffer Disable Threshold	V_{RCTH}	(Note 5)	V_{AVDD1} - 0.4		V_{AVDD1} - 0.1	V
Reference Input Current	I_{REF}	V_{REF} = +4.096V, external clock mode, external acquisition mode, internal clock mode, or partial power-down mode		90	200	µA
		V_{REF} = +4.096V, full power-down mode		±0.1	±10	
Reference Input Resistance	R_{REF}	External clock mode, external acquisition mode, internal clock mode, or partial power-down mode	20	45		kΩ
		Full power-down mode		40		MΩ
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)						
Input High Voltage	V_{IH}		0.7 x V_{DVDDO}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDDO}	V
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage Current	I_{IN}	V_{IN} = 0 to V_{DVDDO}	-10		+10	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Low Voltage	V_{OL}	V_{DVDDO} = 4.75V, I_{SINK} = 10mA			0.4	V
		V_{DVDDO} = 2.7V, I_{SINK} = 5mA			0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DVDDO} - 0.4			V
DOUT Tri-State Leakage Current	I_{DDO}	$\overline{CS}$ = V_{DVDDO}	-10		+10	µA
POWER REQUIREMENTS (AVDD1 and AGND1, AVDD2 and AGND2, DVDD and DGND, DVDDO and DGNDO)						
Analog Supply Voltage	AVDD1		4.75		5.25	V
Digital Supply Voltage	DVDD		4.75		5.25	V

Electrical Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range (±3 x V_{REF}), C_{DOUT} = 50pF, C_{SSTRB} = 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Preamplifier Supply Voltage	AVDD2			4.75		5.25	V
Digital I/O Supply Voltage	DVDDO			2.70		5.25	V
AV_{DD1} Supply Current	I_{AVDD1}	External clock mode, external acquisition mode, or internal clock mode	Internal reference		3	3.5	mA
			External reference		2.3	3	
DV_{DD} Supply Current	I_{DVDD}	External clock mode, external acquisition mode, or internal clock mode			0.8	2	mA
AV_{DD2} Supply Current	I_{AVDD2}	External clock mode, external acquisition mode, or internal clock mode			13.5	20	mA
DV_{DDO} Supply Current	I_{DVDDO}	External clock mode, external acquisition mode, or internal clock mode			0.01	1	mA
Total Supply Current		Partial power-down mode			1.3		mA
		Full power-down mode			0.5		µA
Power-Supply Rejection Ratio	PSRR	All analog input ranges			±0.5		LSB
TIMING CHARACTERISTICS (Figures 15 and 16)							
SCLK Period	t_{CP}	External clock mode		0.272		62	µs
		External acquisition mode		0.228		62	
		Internal clock mode		0.1			
SCLK High Pulse Width (Note 6)	t_{CH}	External clock mode		109			ns
		External acquisition mode		92			
		Internal clock mode		40			
SCLK Low Pulse Width (Note 6)	t_{CL}	External clock mode		109			ns
		External acquisition mode		92			
		Internal clock mode		40			
DIN to SCLK Setup	t_{DS}			40			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to DOUT Valid	t_{DO}					40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}					40	ns

Electrical Characteristics (continued)

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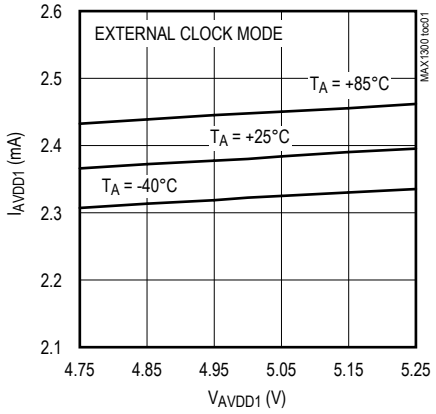
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise to DOUT Disable	t_{TR}				40	ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		40			ns
$\overline{CS}$ High Minimum Pulse Width	t_{CSPW}		40			ns
SCLK Fall to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SSTRB Rise to $\overline{CS}$ Fall Setup		(Note 4)	40			ns
DOUT Rise/Fall Time		C_L = 50pF		10		ns
SSTRB Rise/Fall Time		C_L = 50pF		10		ns

Note 1: Parameter tested at V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V.
Note 2: See definitions in the *Parameter Definitions* section at the end of the data sheet.
Note 3: Guaranteed by correlation with single-ended measurements.
Note 4: Not production tested. Guaranteed by design.
Note 5: To ensure external reference operation, V_{REFCAP} must exceed (V_{AVDD1} - 0.1V). To ensure internal reference operation, V_{REFCAP} must be below (V_{AVDD1} - 0.4V). Bypassing REFCAP with a 0.1µF or larger capacitor to AGND1 sets V_{REFCAP} ≈ 4.096V. The transition point between internal reference mode and external reference mode lies between the REFCAP buffer disable threshold minimum and maximum values (Figures 17 and 18).
Note 6: The SCLK duty cycle can vary between 40% and 60%, as long as the t_{CL} and t_{CH} timing requirements are met.

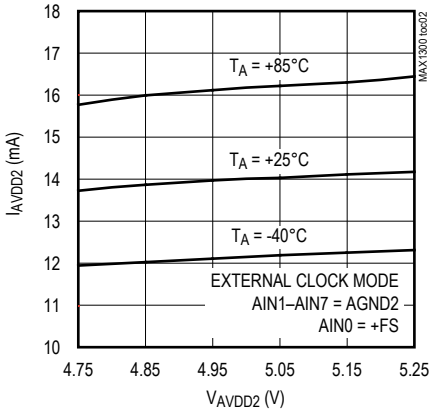
Typical Operating Characteristics

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range, C_{DOUT} = 50pF, C_{SSTRB} = 50pF; unless otherwise noted.)

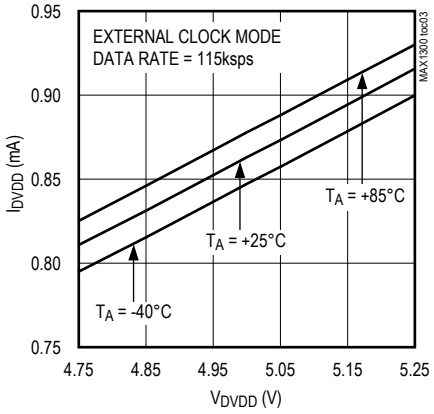
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



PREAMPLIFIER SUPPLY CURRENT vs. PREAMPLIFIER SUPPLY VOLTAGE



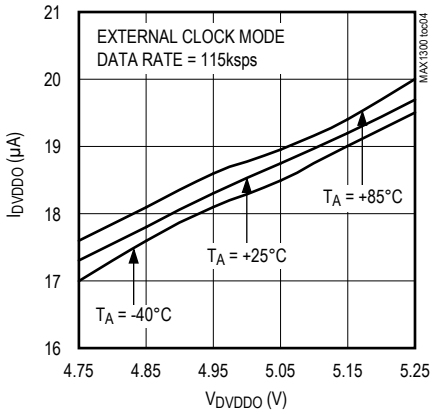
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



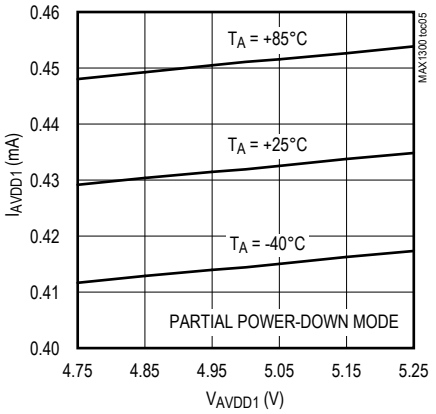
Typical Operating Characteristics (continued)

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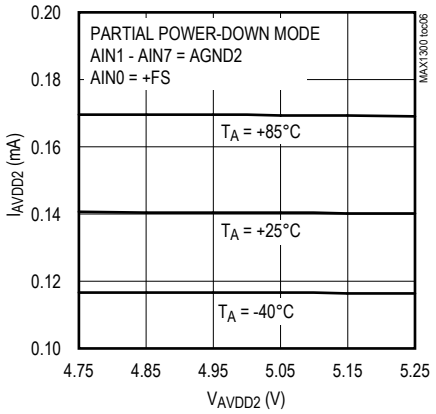
DIGITAL I/O SUPPLY CURRENT vs. DIGITAL I/O SUPPLY VOLTAGE



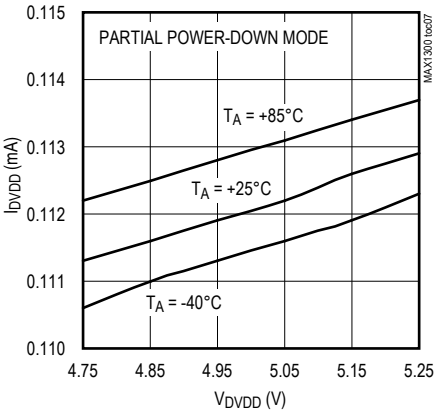
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



PREAMPLIFIER SUPPLY CURRENT vs. PREAMPLIFIER SUPPLY VOLTAGE



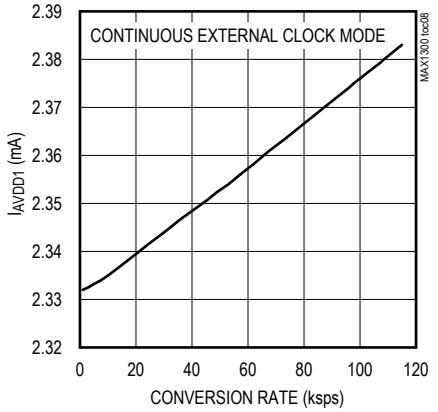
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



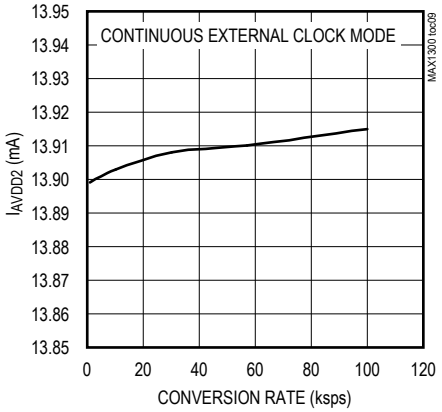
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range, C_{DOUT} = 50pF, C_{SSTRB} = 50pF; unless otherwise noted.)

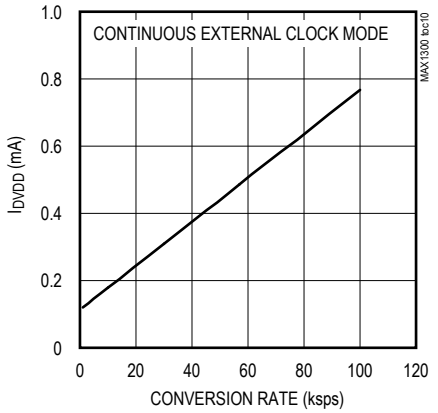
ANALOG SUPPLY CURRENT vs. CONVERSION RATE



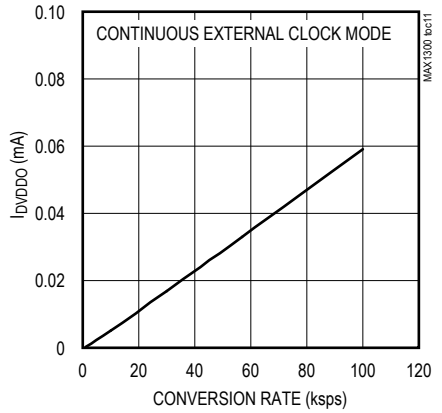
ANALOG SUPPLY CURRENT vs. CONVERSION RATE



DIGITAL SUPPLY CURRENT vs. CONVERSION RATE



DIGITAL I/O SUPPLY CURRENT vs. CONVERSION RATE

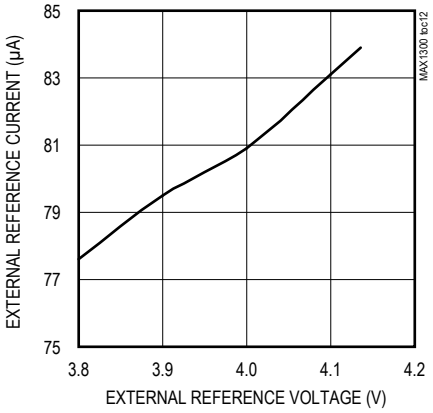


Note 7: For partial power-down and full power-down modes, external clock mode was used for a burst of continuous samples. Partial power-down or full power-down modes were entered thereafter. By using this method, the conversion rate was found by averaging the number of conversions over the time starting from the first conversion to the end of the partial power-down or full power-down modes.

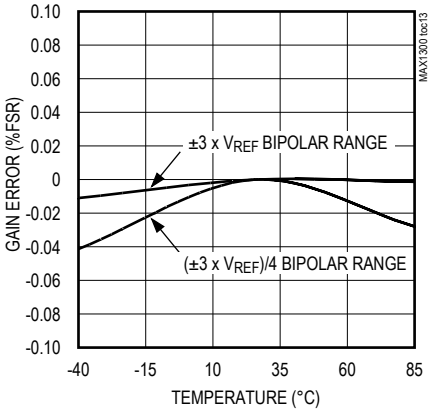
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range, C_{DOUT} = 50pF, C_{SSTRB} = 50pF; unless otherwise noted.)

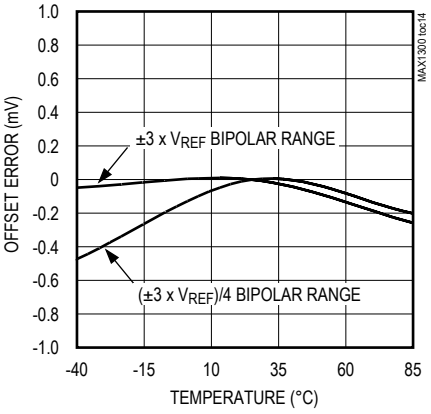
EXTERNAL REFERENCE INPUT CURRENT vs. EXTERNAL REFERENCE INPUT VOLTAGE



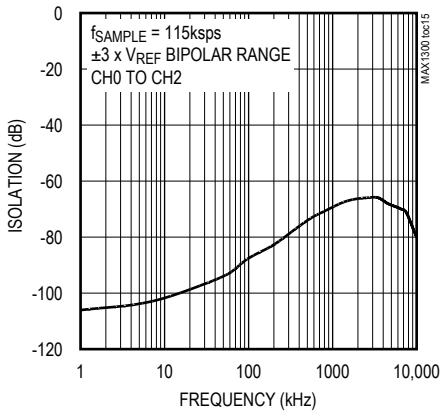
GAIN DRIFT vs. TEMPERATURE



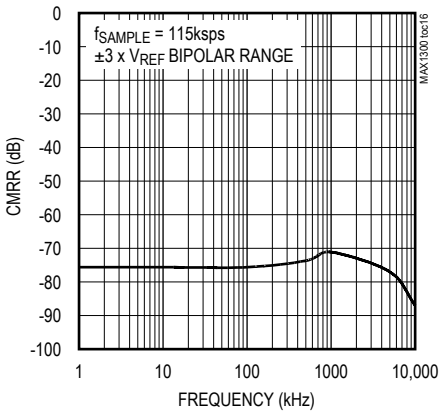
OFFSET DRIFT vs. TEMPERATURE



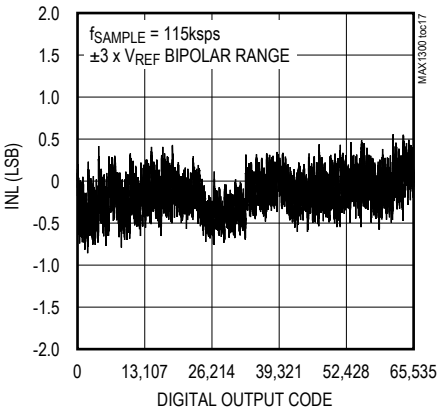
CHANNEL-TO-CHANNEL ISOLATION vs. INPUT FREQUENCY



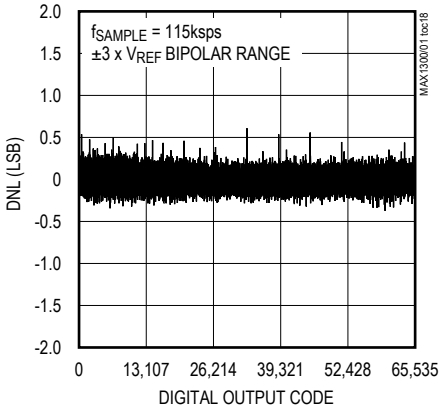
COMMON-MODE REJECTION RATIO vs. FREQUENCY



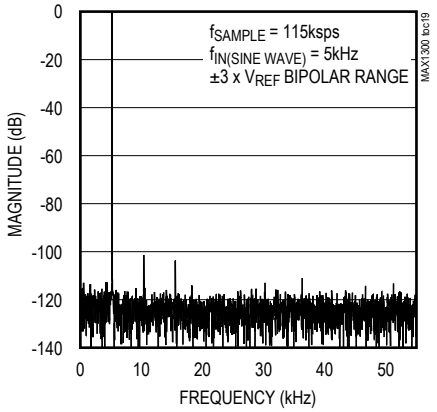
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



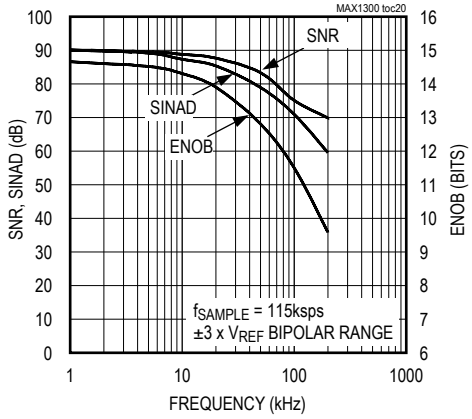
FFT AT 5kHz



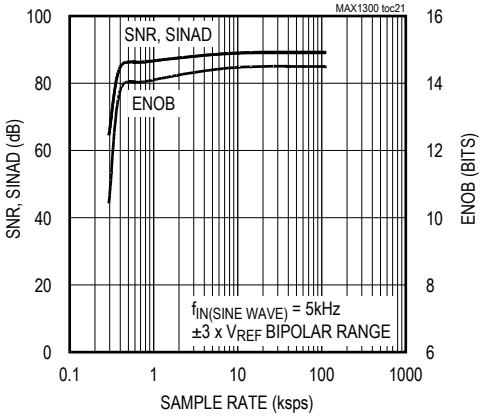
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range, C_{DOUT} = 50pF, C_{SSTRB} = 50pF; unless otherwise noted.)

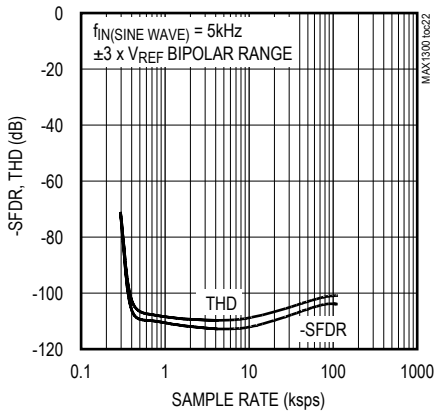
SNR, SINAD, ENOB vs. ANALOG INPUT FREQUENCY



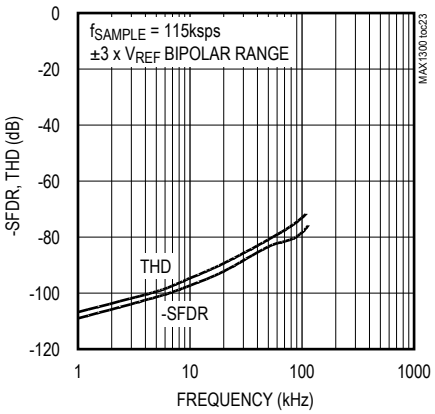
SNR, SINAD, ENOB vs. SAMPLE RATE



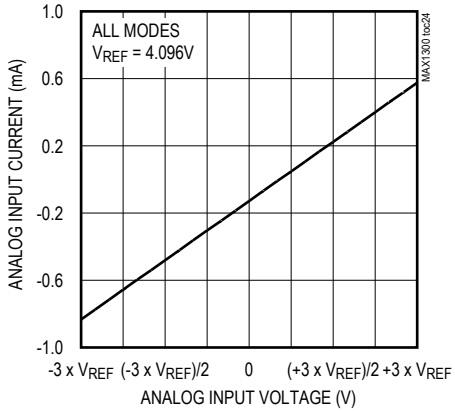
-SFDR, THD vs. SAMPLE RATE



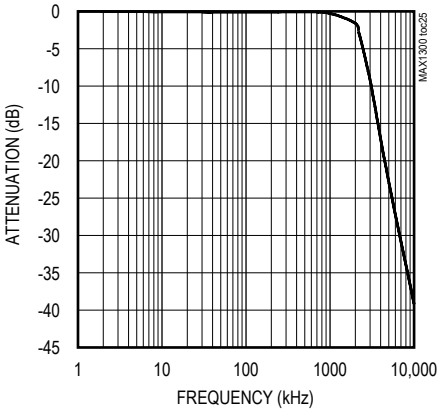
-SFDR, THD vs. ANALOG INPUT FREQUENCY



ANALOG INPUT CURRENT vs. ANALOG INPUT VOLTAGE



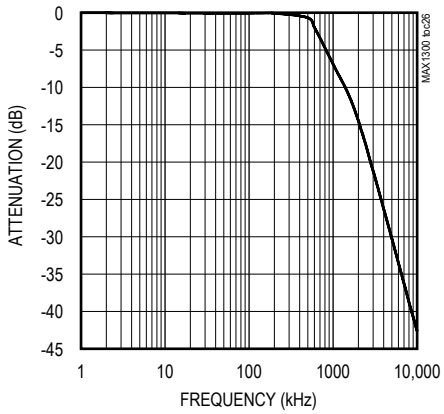
SMALL-SIGNAL BANDWIDTH



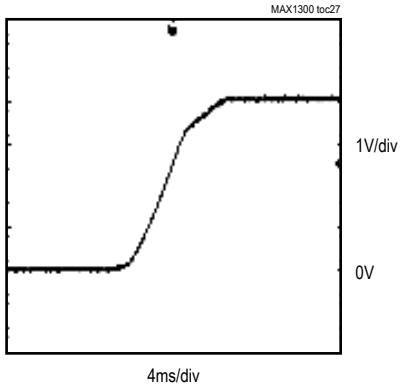
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{AVDD2} = V_{DVDD} = V_{DVDDO} = 5V, V_{AGND1} = V_{DGND} = V_{DGNDO} = V_{AGND2} = V_{AGND3} = 0V, f_{CLK} = 3.5MHz (50% duty cycle), external clock mode, V_{REF} = 4.096V (external reference operation), REFCAP = AVDD1, maximum single-ended bipolar input range, C_{DOUT} = 50pF, C_{SSTRB} = 50pF; unless otherwise noted.)

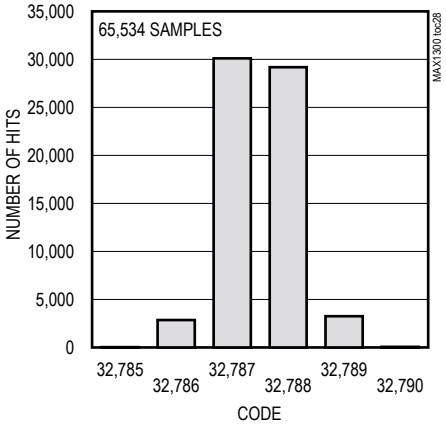
FULL-POWER BANDWIDTH



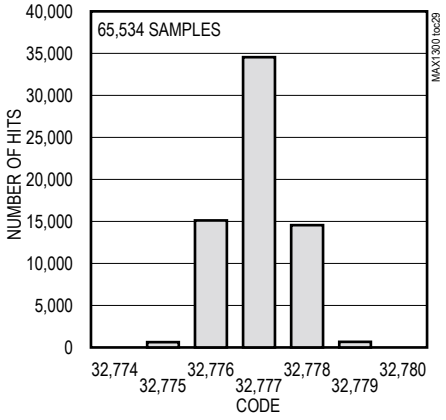
REFERENCE VOLTAGE vs. TIME



NOISE HISTOGRAM (CODE EDGE)



NOISE HISTOGRAM (CODE CENTER)



Pin Description

PIN		NAME	FUNCTION
MAX1300	MAX1301		
1	2	AVDD1	Analog Supply Voltage 1. Connect AVDD1 to a +4.75V to +5.25V power-supply voltage. Bypass AVDD1 to AGND1 with a 0.1µF capacitor.
2	3	CH0	Analog Input Channel 0
3	4	CH1	Analog Input Channel 1
4	5	CH2	Analog Input Channel 2
5	6	CH3	Analog Input Channel 3
6	—	CH4	Analog Input Channel 4
7	—	CH5	Analog Input Channel 5
8	—	CH6	Analog Input Channel 6
9	—	CH7	Analog Input Channel 7
10	7	$\overline{CS}$	Active-Low Chip-Select Input. When $\overline{CS}$ is low, data is clocked into the device from DIN on the rising edge of SCLK. With $\overline{CS}$ low, data is clocked out of DOUT on the falling edge of SCLK. When $\overline{CS}$ is high, activity on SCLK and DIN is ignored and DOUT is high impedance.
11	8	DIN	Serial Data Input. When $\overline{CS}$ is low, data is clocked in on the rising edge of SCLK. When $\overline{CS}$ is high, transitions on DIN are ignored.
12	9	SSTRB	Serial-Strobe Output. When using the internal clock, SSTRB rising edge transitions indicate that data is ready to be read from the device. When operating in external clock mode, SSTRB is always low. SSTRB does not tri-state, regardless of the state of $\overline{CS}$, and therefore requires a dedicated I/O line.
13	10	SCLK	Serial Clock Input. When $\overline{CS}$ is low, transitions on SCLK clock data into DIN and out of DOUT. When $\overline{CS}$ is high, transitions on SCLK are ignored.
14	11	DOUT	Serial Data Output. When $\overline{CS}$ is low, data is clocked out of DOUT with each falling SCLK transition. When $\overline{CS}$ is high, DOUT is high impedance.
15	12	DGNDO	Digital I/O Ground. DGND, DGNDO, AGND3, AGND2, and AGND1 must be connected together.
16	13	DGND	Digital Ground. DGND, DGNDO, AGND3, AGND2, and AGND1 must be connected together.
17	14	DVDDO	Digital I/O Supply Voltage Input. Connect DVDDO to a +2.7V to +5.25V power-supply voltage. Bypass DVDDO to DGNDO with a 0.1µF capacitor.
18	15	DVDD	Digital-Supply Voltage Input. Connect DVDD to a +4.75V to +5.25V power-supply voltage. Bypass DVDD to DGND with a 0.1µF capacitor.
19	16	REFCAP	Bandgap-Voltage Bypass Node. For external reference operation, connect REFCAP to AVDD. For internal reference operation, bypass REFCAP with a 0.01µF capacitor to AGND1 (V_{REFCAP} ≈ 4.096V).
20	17	REF	Reference-Buffer Output/ADC Reference Input. For external reference operation, apply an external reference voltage from 3.800V to 4.136V to REF. For internal reference operation, bypassing REF with a 1µF capacitor to AGND1 sets V_{REF} = 4.096V ±1%.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1300	MAX1301		
21	18	AGND3	Analog Signal Ground 3. AGND3 is the ADC negative reference potential. Connect AGND3 to AGND1. DGND, DGNDO, AGND3, AGND2, and AGND1 must be connected together.
22	19	AVDD2	Analog Supply Voltage 2. Connect AVDD2 to a +4.75V to +5.25V power-supply voltage. Bypass AVDD2 to AGND2 with a 0.1µF capacitor.
23	20	AGND2	Analog Ground 2. This ground carries approximately five times more current than AGND1. DGND, DGNDO, AGND3, AGND2, and AGND1 must be connected together.
24	1	AGND1	Analog Ground 1. DGND, DGNDO, AGND3, AGND2, and AGND1 must be connected together.

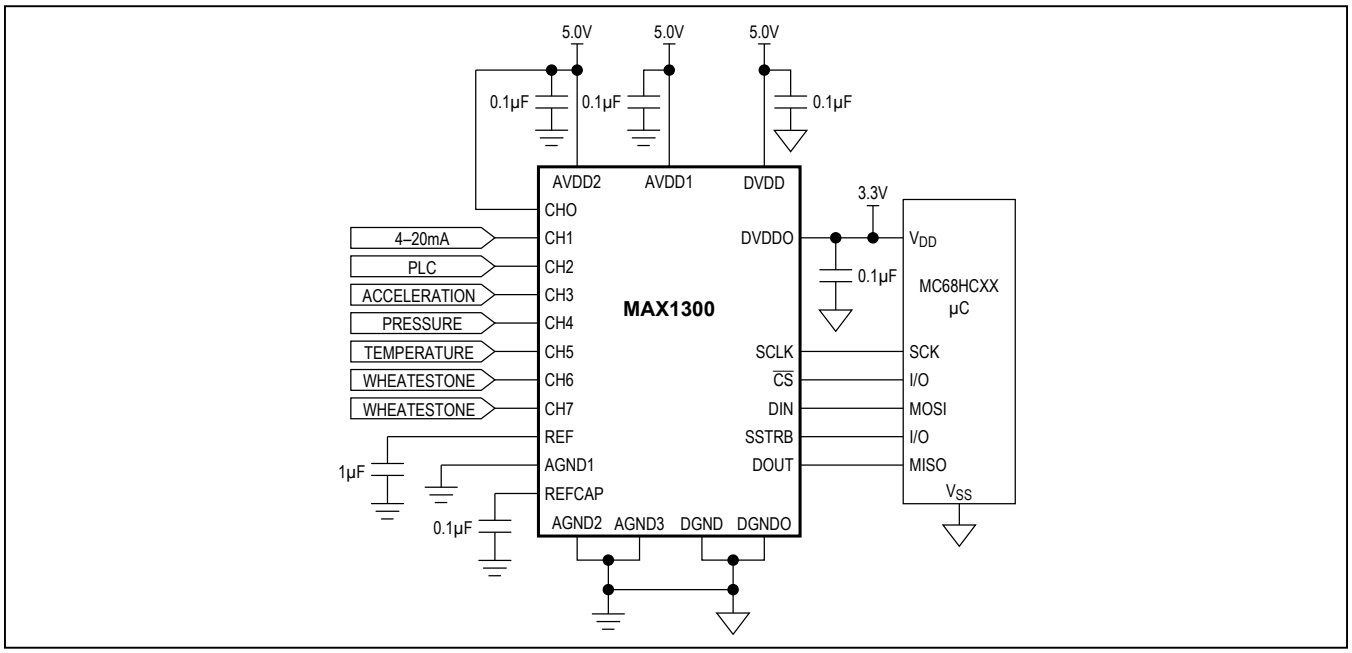


Figure 1. Typical Application Circuit

Detailed Description

The MAX1300/MAX1301 multirange, low-power, 16-bit successive-approximation ADCs operate from a single +5V supply and have a separate digital supply allowing digital interface with 2.7V to 5.25V systems. These 16-bit ADCs have internal track-and-hold (T/H) circuitry that supports single-ended and fully differential inputs. For single-ended conversions, the valid analog input voltage range spans from -3 x V_{REF} below ground to +3 x V_{REF} above ground. The maximum allowable differential input voltage spans from -6 x V_{REF} to +6 x V_{REF}. Data can be converted in a variety of software-programmable channel and data-acquisition configurations. Microprocessor (µP) control is made easy through an SPI-/QSPI-/ MICROWIRE-compatible serial interface.

The MAX1300 has eight single-ended analog input channels or four differential channels (see the *Block Diagram* at the end of the data sheet). The MAX1301 has four single-ended analog input channels or two differential channels. Each analog input channel is independently software programmable for seven single-ended input ranges [0 to (+3 x V_{REF})/2, (-3 x V_{REF})/2 to 0, 0 to +3 x V_{REF}, -3 x V_{REF} to 0, (±3 x V_{REF})/4, (±3 x V_{REF})/2, ±3 x V_{REF}] and three differential input ranges [(±3 x V_{REF})/2, ±3 x V_{REF}, ±6 x V_{REF}]. Additionally, all analog input channels are fault tolerant to ±16.5V. A fault condition on an idle channel does not affect the conversion result of other channels.

Power Supplies

To maintain a low-noise environment, the MAX1300 and MAX1301 provide separate power supplies for each section of circuitry. Table 1 shows the four separate power supplies. Achieve optimal performance using separate AVDD1, AVDD2, DVDD, and DVDDO supplies. Alternatively, connect AVDD1, AVDD2, and DVDD together as close to the device as possible for a convenient power connection. Connect AGND1, AGND2, AGND3, DGND, and DGNDO together as close to the device as possible. Bypass each supply to the corresponding ground using a 0.1µF capacitor (Table 1). If significant low-frequency noise is present, add a 10µF capacitor in parallel with the 0.1µF bypass capacitor.

Converter Operation

The MAX1300/MAX1301 ADCs feature a fully differential, successive-approximation register (SAR) conversion technique and an on-chip T/H block to convert voltage signals into a 16-bit digital result. Both single-ended and differential configurations are supported with programmable unipolar and bipolar signal ranges.

Track-and-Hold Circuitry

The MAX1300/MAX1301 feature a switched-capacitor T/H architecture that allows the analog input signal to be stored as charge on sampling capacitors. See Figures 2, 3, and 4 for T/H timing and the sampling instants for each operating mode. The MAX1300/MAX1301 analog input circuitry buffers the input signal from the sampling capacitors, resulting in a constant input impedance with varying input voltage (Figure 5).

Analog Input Circuitry

Select differential or single-ended conversions using the associated analog input configuration byte (Table 2). The analog input signal source must be capable of driving the ADC's 17kΩ input resistance (Figure 6).

Figure 6 shows the simplified analog input circuit. The analog inputs are ±16.5V fault tolerant and are protected by back-to-back diodes. The summing junction voltage, V_{SJ}, is a function of the channel's input common-mode voltage:

$$V_{SJ} = \left(\frac{R1}{R1+R2}\right) \times 2.375V + \left(1+\left(\frac{R1}{R1+R2}\right)\right) \times V_{CM}$$

As a result, the analog input impedance is relatively constant over input voltage as shown in Figure 5.

Table 1. MAX1300/MAX1301 Power Supplies and Bypassing

POWER SUPPLY/GROUND	SUPPLY VOLTAGE RANGE (V)	TYPICAL SUPPLY CURRENT (mA)	CIRCUIT SECTION	BYPASSING
DVDDO/DGNDO	2.7 to 5.25	0.03	Digital I/O	0.1µF to DGNDO
AVDD2/AGND2	4.75 to 5.25	135	Analog Circuitry	0.1µF to AGND2
AVDD1/AGND1	4.75 to 5.25	3.0	Analog Circuitry	0.1µF to AGND1
DVDD/DGND	4.75 to 5.25	0.8	Digital Control Logic and Memory	0.1µF to DGND

Table 2. Analog Input Configuration Byte

BIT NUMBER	NAME	DESCRIPTION
7	START	Start Bit. The first logic 1 after $\overline{CS}$ goes low defines the beginning of the analog input configuration byte.
6	C2	Channel-Select Bits. SEL[2:0] select the analog input channel to be configured (Tables 4 and 5).
5	C1	
4	C0	
3	DIF/$\overline{SGL}$	Differential or Single-Ended Configuration Bit. DIF/$\overline{SGL}$ = 0 configures the selected analog input channel for single-ended operation. DIF/$\overline{SGL}$ = 1 configures the channel for differential operation. In single-ended mode, input voltages are measured between the selected input channel and AGND1, as shown in Table 4. In differential mode, the input voltages are measured between two input channels, as shown in Table 5. Be aware that changing DIF/$\overline{SGL}$ adjusts the FSR, as shown in Table 6.
2	R2	Input-Range-Select Bits. R[2:0] select the input voltage range, as shown in Table 6 and Figure 7.
1	R1	
0	R0	

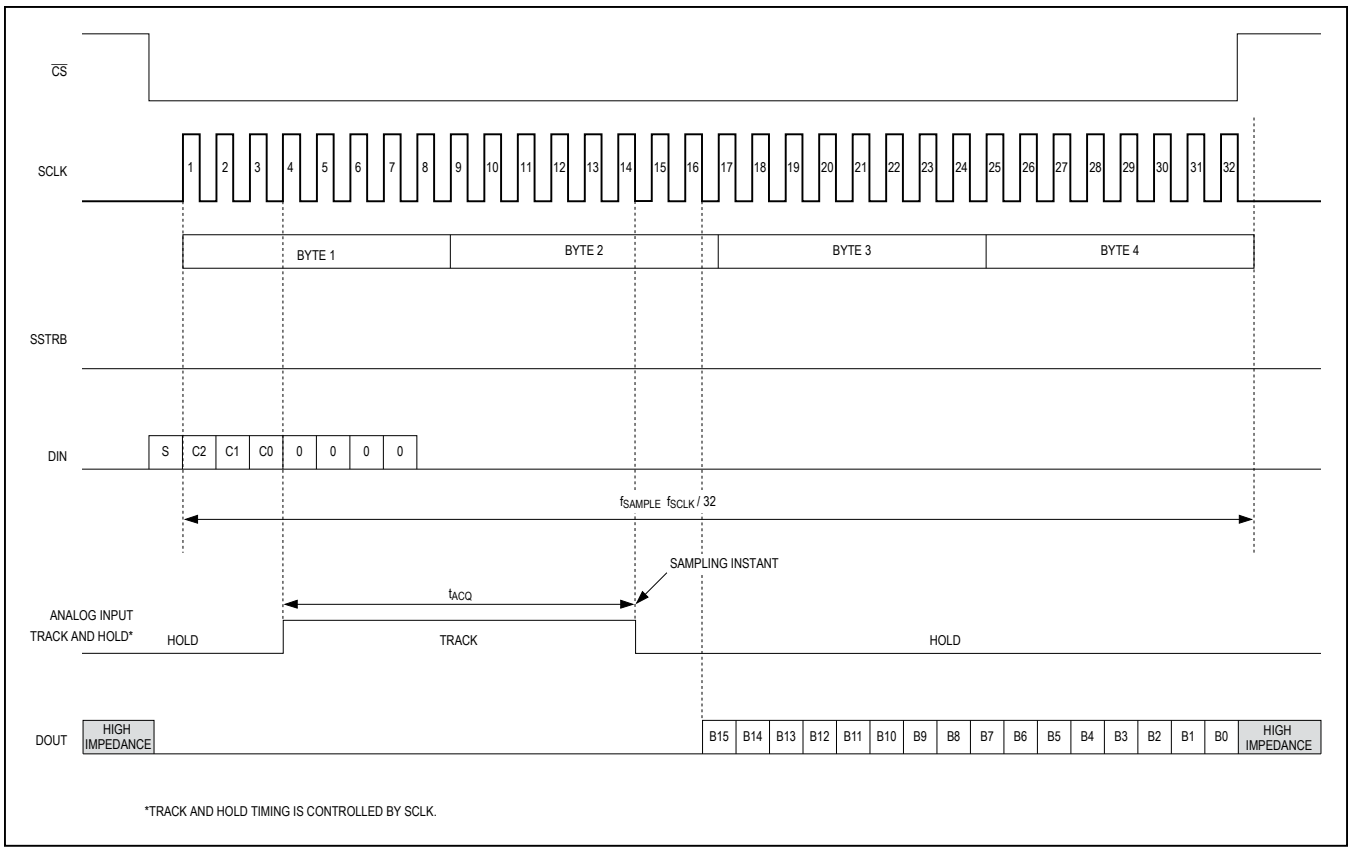


Figure 2. External Clock-Mode Conversion (Mode 0)

Single-ended conversions are internally referenced to AGND1 (Tables 3 and 4). In differential mode, IN+ and IN- are selected according to Tables 3 and 5. When configuring differential channels, the differential pair follows the analog configuration byte for the positive channel. For example, to configure CH2 and CH3 for a ±3 x V_{REF} differential conversion, set the CH2 analog configuration byte for a differential conversion with the ±3 x V_{REF} range (1010 1100). To initiate a conversion for the CH2 and CH3 differential pair, issue the command 1010 0000.

Analog Input Bandwidth

The MAX1300/MAX1301 input-tracking circuitry has a 2MHz small-signal bandwidth. The 2MHz input bandwidth makes it possible to digitize high-speed transient events. Harmonic distortion increases when digitizing signal frequencies above 15kHz as shown in the THD and -SFDR vs. Input Frequency plot in the *Typical Operating Characteristics*.

Analog Input Range and Fault Tolerance

Figure 7 illustrates the software-selectable single-ended analog input voltage range that produces a valid digital output. Each analog input channel can be independently programmed to one of seven single-ended input ranges by setting the R[2:0] control bits with DIF/$\overline{SGL}$ = 0.

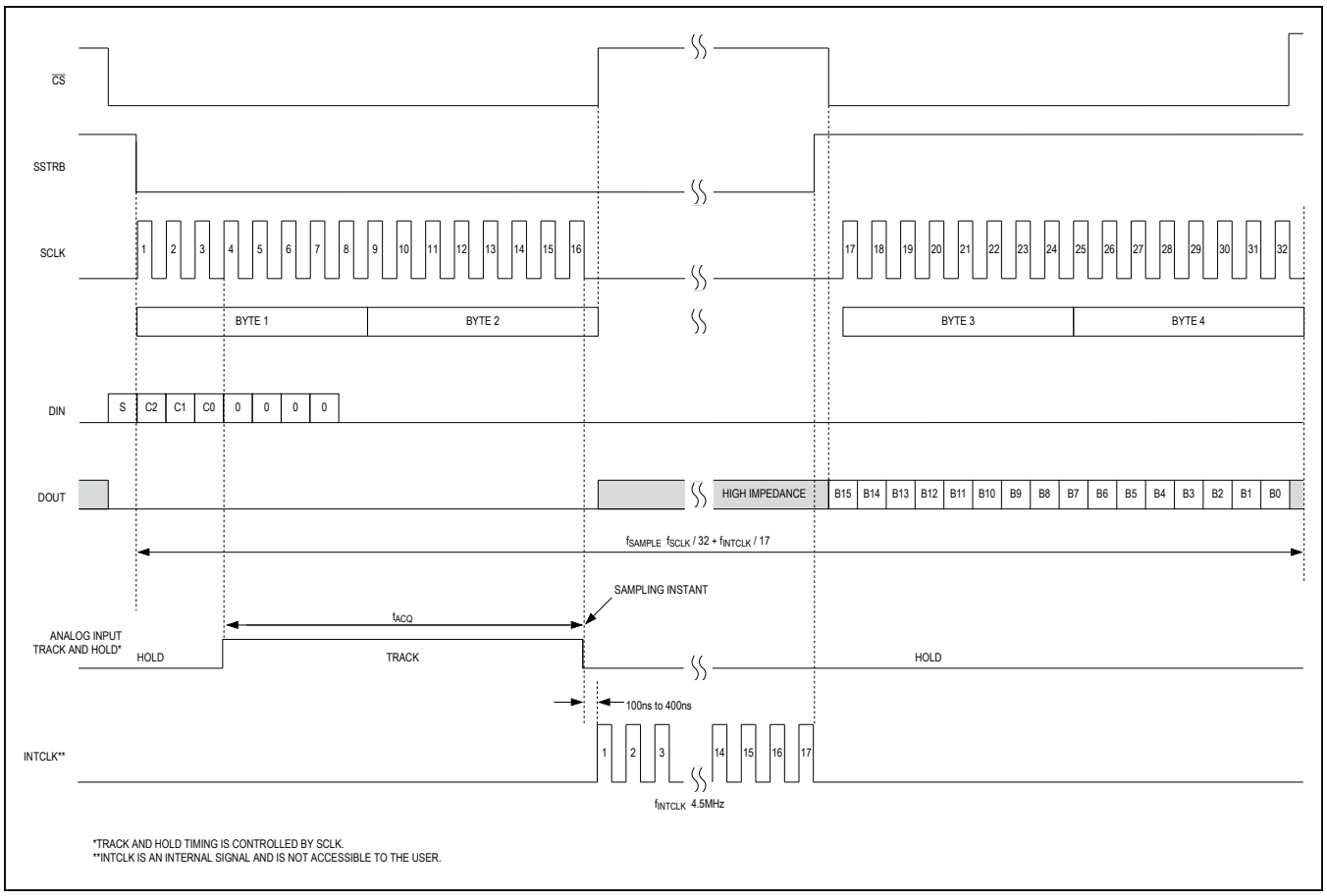


Figure 3. External Acquisition-Mode Conversion (Mode 1)

Figure 8 illustrates the software-selectable differential analog input voltage range that produces a valid digital output. Each analog input differential pair can be independently programmed to one of three differential input ranges by setting the R[2:0] control bits with DIF/$\overline{SGL}$ = 1.

Regardless of the specified input voltage range and whether the channel is selected, each analog input is ±16.5V fault tolerant. The analog input fault protection is active whether the device is unpowered or powered. Any voltage beyond FSR, but within the ±16.5V fault tolerant range, applied to an analog input results in a full-scale output voltage for that channel.

Clamping diodes with breakdown thresholds in excess of 16.5V protect the MAX1300/MAX1301 analog inputs during ESD and other transient events (Figure 6). The clamping diodes do not conduct during normal device operation, nor do they limit the current during such transients. When operating in an environment with the potential for high-energy voltage and/or current transients, protect the MAX1300/MAX1301 externally.

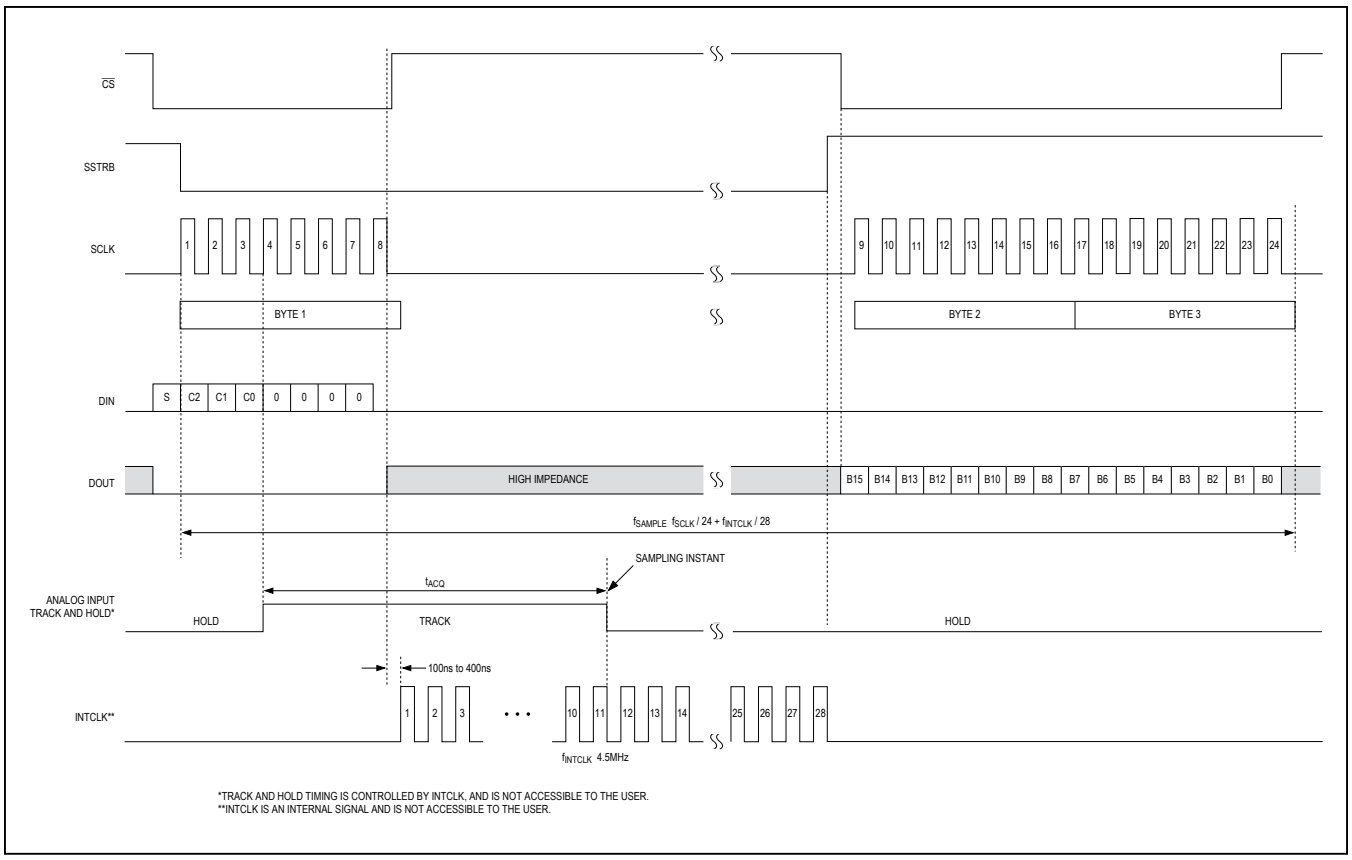


Figure 4. Internal Clock-Mode Conversion (Mode 2)

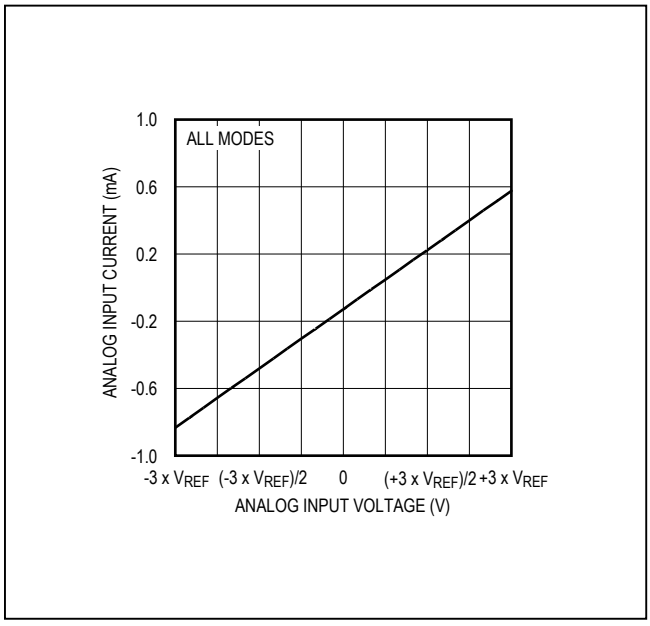


Figure 5. Analog Input Current vs. Input Voltage

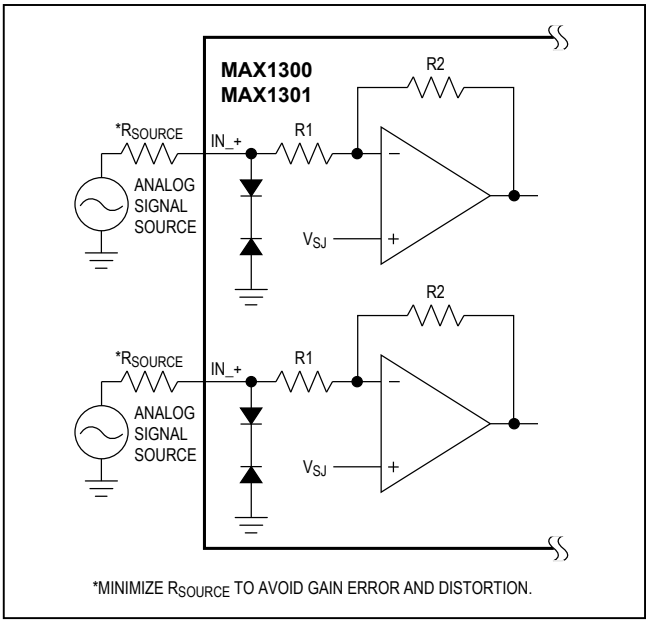


Figure 6. Simplified Analog Input Circuit

Table 3. Input Data Word Formats

OPERATION	DATA BIT							
	D7 (START)	D6	D5	D4	D3	D2	D1	D0
Conversion-Start Byte (Tables 4 and 5)	1	C2	C1	C0	0	0	0	0
Analog-Input Configuration Byte (Table 2)	1	C2	C1	C0	DIF/$\overline{SGL}$	R2	R1	R0
Mode-Control Byte (Table 7)	1	M2	M1	M0	1	0	0	0

Table 4. Channel Selection in Single-Ended Mode (DIF/$\overline{SGL}$ = 0)

CHANNEL-SELECT BIT			CHANNEL								
C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND1
0	0	0	+								-
0	0	1		+							-
0	1	0			+						-
0	1	1				+					-
1	0	0					+				-
1	0	1						+			-
1	1	0							+		-
1	1	1								+	-

Table 5. Channel Selection in True-Differential Mode (DIF/$\overline{SGL}$ = 1)

CHANNEL-SELECT BIT			CHANNEL								
C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND1
0	0	0	+	-							
0	0	1	RESERVED								
0	1	0			+	-					
0	1	1	RESERVED								
1	0	0					+	-			
1	0	1	RESERVED								
1	1	0							+	-	
1	1	1	RESERVED								

Differential Common-Mode Range

The MAX1300/MAX1301 differential common-mode range (V_{CMDR}) must remain within -14V to +10V to obtain valid conversion results. The differential common-mode range is defined as:

$$V_{CMDR} = \frac{(CH_+) + (CH_-)}{2}$$

In addition to the common-mode input voltage limitations, each individual analog input must be limited to ±16.5V with respect to AGND1.

The range-select bits R[2:0] in the analog input configuration bytes determine the full-scale range for the corresponding channel (Tables 2 and 6). Figures 9, 10, and 11 show the valid analog input voltage ranges for the MAX1300/MAX1301 when operating with FSR = (±3 x V_{REF})/2, FSR = ±3 x V_{REF}, and FSR = ±6 x V_{REF}, respectively. The shaded area contains the valid common-mode voltage ranges that support the entire FSR.

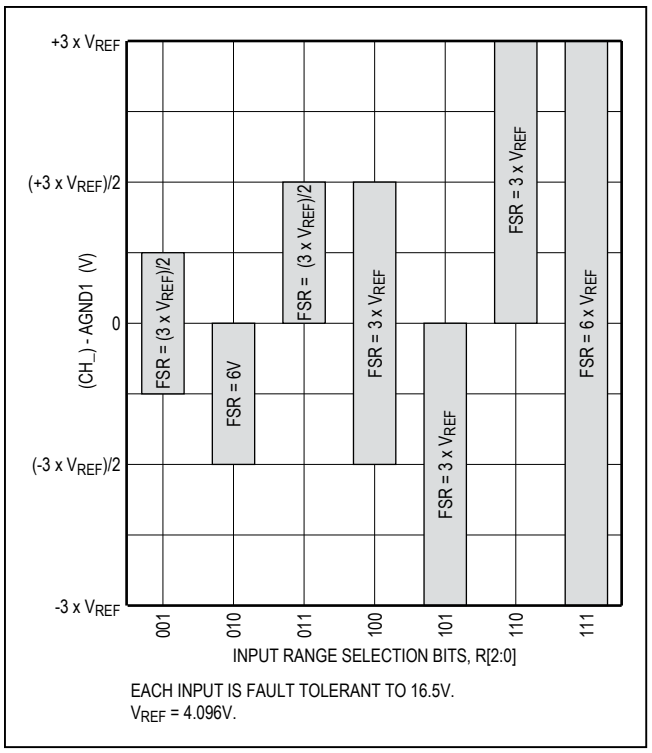


Figure 7. Single-Ended Input Voltage Ranges

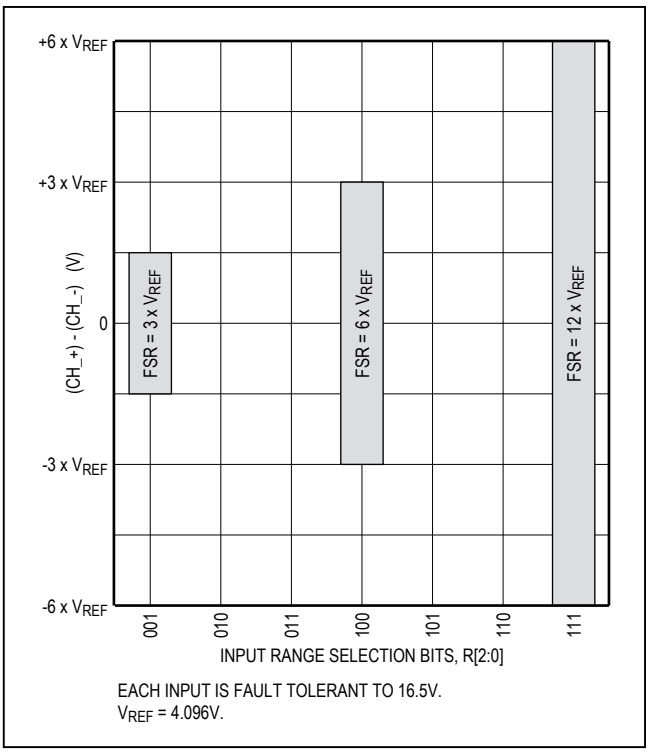


Figure 8. Differential Input Voltage Ranges

Digital Interface

The MAX1300/MAX1301 feature a serial interface that is compatible with SPI/QSPI and MICROWIRE devices. DIN, DOUT, SCLK, $\overline{CS}$, and SSTRB facilitate bidirectional communication between the MAX1300/MAX1301 and the master at SCLK rates up to 10MHz (internal clock mode, mode 2), 3.67MHz (external clock mode, mode 0), or 4.39MHz (external acquisition mode, mode 1). The master, typically a microcontroller, should use the CPOL = 0, CPHA = 0, SPI transfer format, as shown in the timing diagrams of Figures 2, 3, and 4.

The digital interface is used to:

- Select single-ended or true-differential input channel configurations
- Select the unipolar or bipolar input range
- Select the mode of operation:
  External clock (mode 0)
  External acquisition (mode 1)
  Internal clock (mode 2)
  Reset (mode 4)
  Partial power-down (mode 6)
  Full power-down (mode 7)
- Initiate conversions and read results

Chip Select ($\overline{CS}$)

$\overline{CS}$ enables communication with the MAX1300/MAX1301. When $\overline{CS}$ is low, data is clocked into the device from DIN on the rising edge of SCLK and data is clocked out of DOUT on the falling edge of SCLK. When $\overline{CS}$ is high, activity on SCLK and DIN is ignored and DOUT is high impedance allowing DOUT to be shared with other peripherals. SSTRB is never high impedance and therefore cannot be shared with other peripherals.

Serial Strobe Output (SSTRB)

As shown in Figures 3 and 4, the SSTRB transitions high to indicate that the ADC has completed a conversion and results are ready to be read by the master. SSTRB remains low in the external clock mode (Figure 2) and consequently may be left unconnected. SSTRB is driven high or low regardless of the state of $\overline{CS}$, therefore SSTRB cannot be shared with other peripherals.

Table 6. Range-Select Bits

DIF/$\overline{SGL}$	R2	R1	R0	MODE	TRANSFER FUNCTION
0	0	0	0	No Range Change*	—
0	0	0	1	Single-Ended Bipolar (-3 x V_{REF})/4 to (+3 x V_{REF})/4 Full-Scale Range (FSR) = (3 x V_{REF})/2	Figure 12
0	0	1	0	Single-Ended Unipolar (-3 x V_{REF})/2 to 0 FSR = (3 x V_{REF})/2	Figure 13
0	0	1	1	Single-Ended Unipolar 0 to (+3 x V_{REF})/2 FSR = (+3 x V_{REF})/2	Figure 14
0	1	0	0	Single-Ended Bipolar (-3 x V_{REF})/2 to (+3 x V_{REF})/2 FSR = 3 x V_{REF}	Figure 12
0	1	0	1	Single-Ended Unipolar -3 x V_{REF} to 0 FSR = 3 x V_{REF}	Figure 13
0	1	1	0	Single-Ended Unipolar 0 to +3 x V_{REF} FSR = 3 x V_{REF}	Figure 14
0	1	1	1	**DEFAULT SETTING** Single-Ended Bipolar -3 x V_{REF} to +3 x V_{REF} FSR = 6 x V_{REF}	Figure 12
1	0	0	0	No Range Change**	—
1	0	0	1	Differential Bipolar (-3 x V_{REF})/2 to (+3 x V_{REF})/2 FSR = 3 x V_{REF}	Figure 12
1	0	1	0	Reserved	—
1	0	1	1	Reserved	—
1	1	0	0	Differential Bipolar -3 x V_{REF} to +3 x V_{REF} FSR = 6 x V_{REF}	Figure 12
1	1	0	1	Reserved	—
1	1	1	0	Reserved	—
1	1	1	1	Differential Bipolar -6 x V_{REF} to +6 x V_{REF} FSR = 12 x V_{REF}	Figure 12

**Conversion-Start Byte (see Table 3).*

***Mode-Control Byte (see Table 3).*

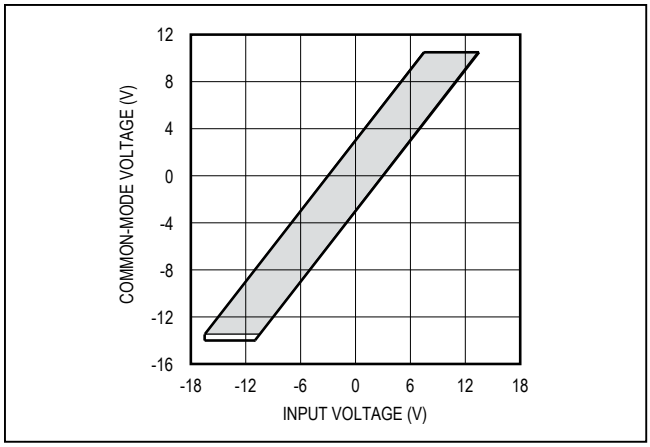


Figure 9. Common-Mode Voltage vs. Input Voltage (FSR = 3 x V_{REF})

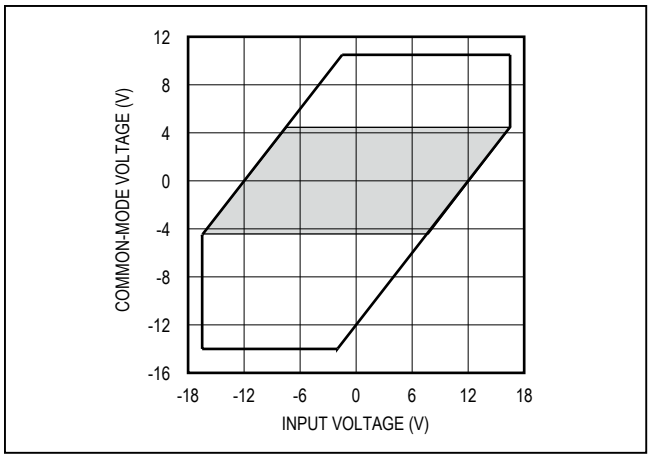


Figure 11. Common-Mode Voltage vs. Input Voltage (FSR = 12 x V_{REF})

Start Bit

Communication with the MAX1300/MAX1301 is accomplished using the three input data word formats shown in Table 3. Each input data word begins with a start bit. The start bit is defined as the first high bit clocked into DIN with $\overline{CS}$ low when any of the following are true:

- Data conversion is not in process and all data from the previous conversion has clocked out of DOUT.
- The device is configured for operation in external clock mode (mode 0) and previous conversion-result bits B15–B3 have clocked out of DOUT.
- The device is configured for operation in external acquisition mode (mode 1) and previous conversion-result bits B15–B7 have clocked out of DOUT.
- The device is configured for operation in internal clock mode, (mode 2) and previous conversion result bits B15–B4 have clocked out of DOUT.

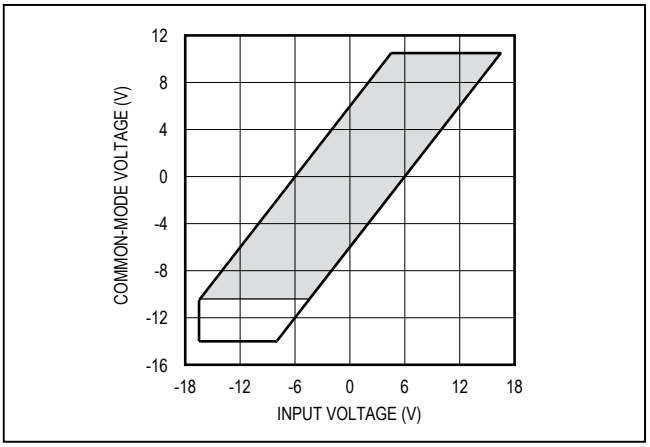


Figure 10. Common-Mode Voltage vs. Input Voltage (FSR = 6 x V_{REF})

Output Data Format

Output data is clocked out of DOUT in offset binary format on the falling edge of SCLK, MSB first (B15). For output binary codes, see the *Transfer Function* section and Figures 12, 13, and 14.

Configuring Analog Inputs

Each analog input has two configurable parameters:

- Single-ended or true-differential input
- Input voltage range

These parameters are configured using the analog input configuration byte as shown in Table 2. Each analog input has a dedicated register to store its input configuration information. The timing diagram of Figure 15 shows how to write to the analog input configuration registers. Figure 16 shows DOUT and SSTRB timing.

Transfer Function

An ADC's transfer function defines the relationship between the analog input voltage and the digital output code. Figures 12, 13, and 14 show the MAX1300/MAX1301 transfer functions. The transfer function is determined by the following characteristics:

- Analog input voltage range
- Single-ended or differential configuration
- Reference voltage

The axes of an ADC transfer function are typically in least significant bits (LSBs). For the MAX1300/MAX1301, an LSB is calculated using the following equation:

$$1LSB = \frac{FSR \times V_{REF}}{2^N \times 4.096V}$$

where N is the number of bits (N = 16) and FSR is the full-scale range (see Figures 7 and 8).

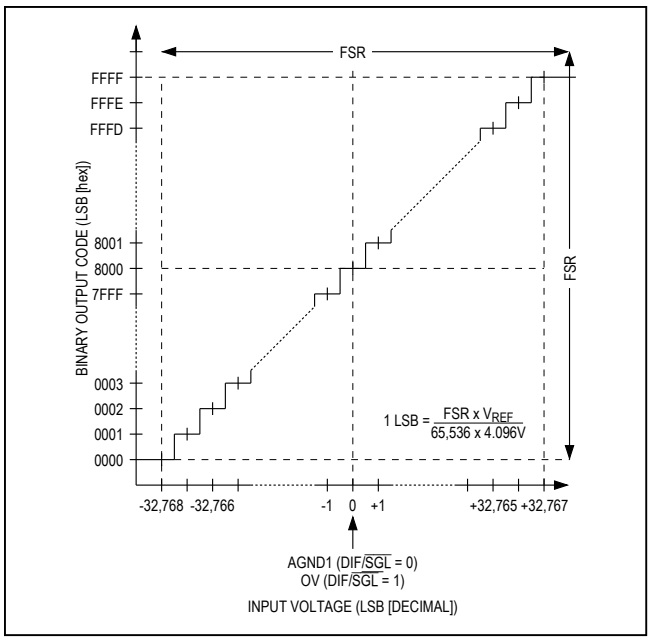


Figure 12. Ideal Bipolar Transfer Function, Single-Ended or Differential Input

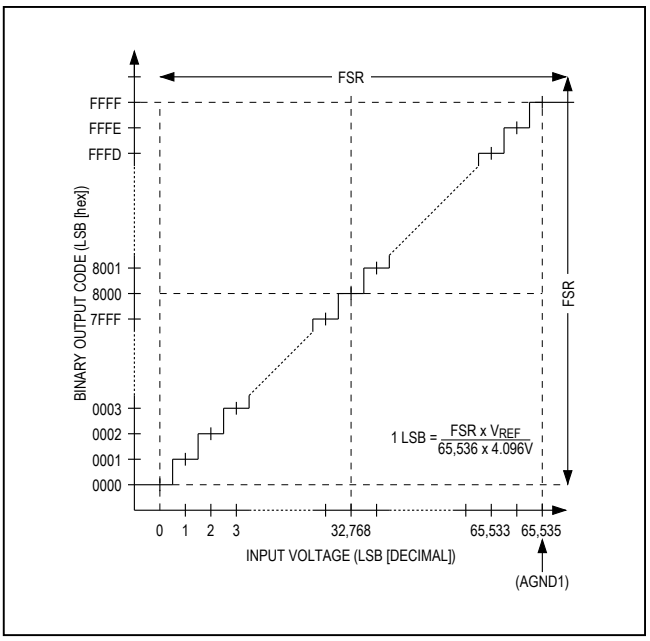


Figure 13. Ideal Unipolar Transfer Function, Single-Ended Input, -FSR to 0

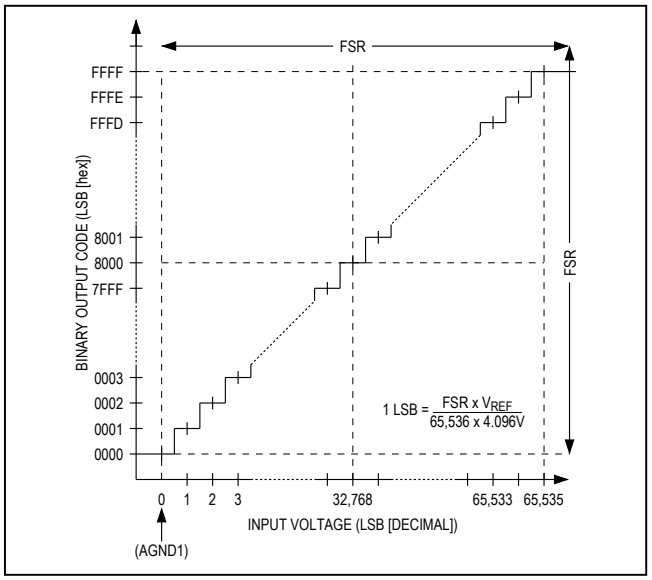


Figure 14. Ideal Unipolar Transfer Function, Single-Ended Input, 0 to +FSR

Mode Control

The MAX1300/MAX1301 contain one byte-wide mode-control register. The timing diagram of Figure 15 shows how to use the mode-control byte, and the mode-control byte format is shown in Table 7. The mode-control byte is used to select the conversion method and to control the power modes of the MAX1300/MAX1301.

Selecting the Conversion Method

The conversion method is selected using the mode-control byte (see the *Mode Control* section), and the conversion is initiated using a conversion-start command (Table 3, and Figures 2, 3, and 4).The MAX1300/MAX1301 convert analog signals to digital data using one of three methods:

- External Clock Mode, Mode 0 (Figure 2)
  - Highest maximum throughput (see the *Electrical Characteristics* table)
  - User controls the sample instant
  - $\overline{CS}$ remains low during the conversion
  - User supplies SCLK throughout the ADC conversion and reads data at DOUT
- External Acquisition Mode, Mode 1 (Figure 3)
  - Lowest maximum throughput (see the *Electrical Characteristics* table)
  - User controls the sample instant
  - User supplies two bytes of SCLK, then drives $\overline{CS}$ high to relieve processor load while the ADC converts
  - After SSTRB transitions high, the user supplies two bytes of SCLK and reads data at DOUT
- Internal Clock Mode, Mode 2 (Figure 4)
  - High maximum throughput (see the *Electrical Characteristics* table)

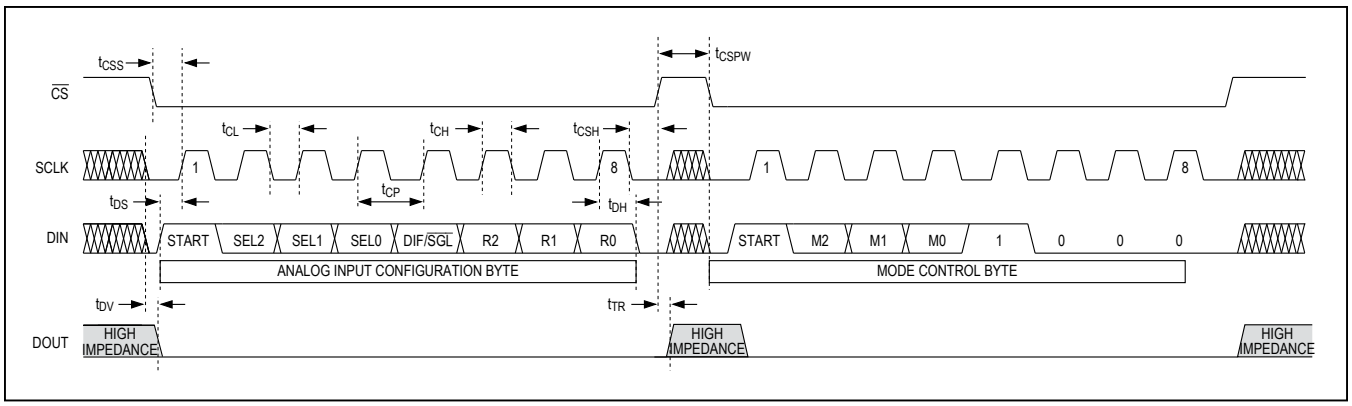
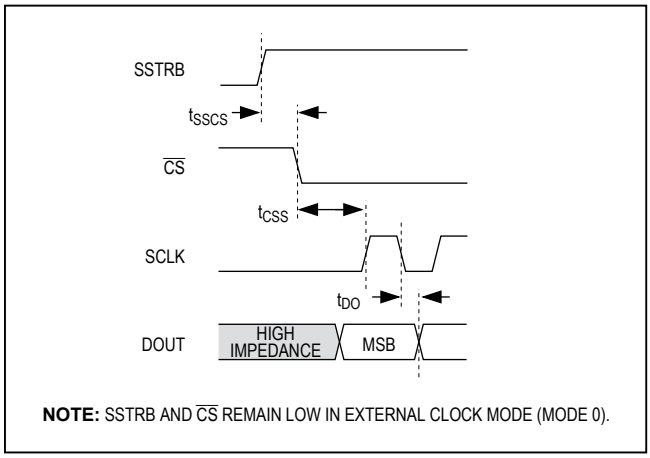


Figure 15. Analog Input Configuration Byte and Mode-Control Byte Timing



NOTE: SSTRB AND $\overline{CS}$ REMAIN LOW IN EXTERNAL CLOCK MODE (MODE 0).

Figure 16. DOUT and SSTRB Timing

- The internal clock controls the sampling instant
- User supplies one byte of SCLK, then drives $\overline{CS}$ high to relieve processor load while the ADC converts
- After SSTRB transitions high, the user supplies two bytes of SCLK and reads data at DOUT

External Clock Mode (Mode 0)

The MAX1300/MAX1301's fastest maximum throughput rate is achieved operating in external clock mode. SCLK controls both the acquisition and conversion of the analog signal, facilitating precise control over when the analog signal is captured. The analog input sampling instant is at the falling edge of the 14th SCLK (Figure 2).

Since SCLK drives the conversion in external clock mode, the SCLK frequency should remain constant while the conversion is clocked. The minimum SCLK frequency prevents droop in the internal sampling capacitor voltages during conversion.

SSTRB remains low in the external clock mode, and as a result may be left unconnected if the MAX1300/ MAX1301 will always be used in the external clock mode.

Table 7. Mode-Control Byte

BIT NUMBER	BIT NAME	DESCRIPTION
7	START	Start Bit. The first logic 1 after $\overline{CS}$ goes low defines the beginning of the mode-control byte.
6	M2	Mode-Control Bits. M[2:0] select the mode of operation as shown in Table 8.
5	M1	
4	M0	
3	1	Bit 3 must be a logic 1 for the mode-control byte.
2	0	Bit 2 must be a logic 0 for the mode-control byte.
1	0	Bit 1 must be a logic 0 for the mode-control byte.
0	0	Bit 0 must be a logic 0 for the mode-control byte.

Table 8. Mode-Control Bits M[2:0]

M2	M1	M0	MODE
0	0	0	External Clock **(DEFAULT)**
0	0	1	External Acquisition
0	1	0	Internal Clock
0	1	1	Reserved
1	0	0	Reset
1	0	1	Reserved
1	1	0	Partial Power-Down
1	1	1	Full Power-Down

External Acquisition Mode (Mode 1)

The slowest maximum throughput rate is achieved with the external acquisition method. SCLK controls the acquisition of the analog signal in external acquisition mode, facilitating precise control over when the analog signal is captured. The internal clock controls the conversion of the analog input voltage. The analog input sampling instant is at the falling edge of the 16th SCLK (Figure 3).

For the external acquisition mode, $\overline{CS}$ must remain low for the first 15 clock cycles and the rise on or after the falling edge of the 16th SCLK cycle as shown in Figure 3. For optimal performance, idle DIN and SCLK during the conversion. With careful board layout, transitions at DIN and SCLK during the conversion have a minimal impact on the conversion result.

After the conversion is complete, SSTRB asserts high and $\overline{CS}$ can be brought low to read the conversion result. SSTRB returns low on the rising SCLK edge of the subsequent start bit.

Internal Clock Mode (Mode 2)

In internal clock mode, the internal clock controls both acquisition and conversion of the analog signal. The internal clock starts approximately 100ns to 400ns after the falling edge of the eighth SCLK and has a rate of about 4.5MHz. The analog input sampling instant occurs at the falling edge of the 11th internal clock signal (Figure 4).

For the internal clock mode, $\overline{CS}$ must remain low for the first seven SCLK cycles and then rise on or after the falling edge of the eighth SCLK cycle. After the conversion is complete, SSTRB asserts high and $\overline{CS}$ can be brought low to read the conversion result. SSTRB returns low on the rising SCLK edge of the subsequent start bit.

Reset (Mode 4)

As shown in Table 8, set M[2:0] = 100 to reset the MAX1300/MAX1301 to its default conditions. The default conditions are full power operation with each channel configured for ±3 x V_{REF}, bipolar, single-ended conversions using external clock mode (mode 0).

Partial Power-Down Mode (Mode 6)

As shown in Table 8, when M[2:0] = 110, the device enters partial power-down mode. In partial power-down, all analog portions of the device are powered down except for the reference voltage generator and bias supplies.

To exit partial power-down, change the mode by issuing one of the following mode-control bytes (see the *Mode Control* section):

- External-Clock-Mode Control Byte
- External-Acquisition-Mode Control Byte
- Internal-Clock-Mode Control Byte
- Reset Byte
- Full Power-Down-Mode Control Byte

This prevents the MAX1300/MAX1301 from inadvertently exiting partial power-down mode because of a $\overline{CS}$ glitch in a noisy digital environment.

Full Power-Down Mode (Mode 7)

When M[2:0] = 111, the device enters full power-down mode and the total supply current falls to 1µA (typ). In full power-down, all analog portions of the device are powered down. When using the internal reference, upon exiting full power-down mode, allow 10ms for the internal reference voltage to stabilize prior to initiating a conversion.

To exit full power-down, change the mode by issuing one of the following mode-control bytes (see the *Mode Control section*):

- External-Clock-Mode Control Byte

- External-Acquisition-Mode Control Byte
- Internal-Clock-Mode Control Byte
- Reset Byte
- Partial Power-Down-Mode Control Byte

This prevents the MAX1300/MAX1301 from inadvertently exiting full power-down mode because of a $\overline{CS}$ glitch in a noisy digital environment.

Power-On Reset

The MAX1300/MAX1301 power up in normal operation configured for external clock mode with all circuitry active (Tables 7 and 8). Each analog input channel (CH0–CH7) is set for single-ended conversions with a ±3 x V_{REF} bipolar input range (Table 6).

Allow the power supplies to stabilize after power-up. Do not initiate any conversions until the power supplies have stabilized. Additionally, allow 10ms for the internal reference to stabilize when C_{REF} = 1.0µF and C_{REFCAP} = 0.1µF. Larger reference capacitors require longer stabilization times.

Internal or External Reference

The MAX1300/MAX1301 operate with either an internal or external reference. The reference voltage impacts the ADC's FSR (Figures 12, 13, and 14). An external reference is recommended if more accuracy is required than the internal reference provides, and/or multiple converters require the same reference voltage.

Internal Reference

The MAX1300/MAX1301 contain an internal 4.096V bandgap reference. This bandgap reference is connected to REFCAP through a nominal 5kΩ resistor (Figure 17). The voltage at REFCAP is buffered creating 4.096V at REF. When using the internal reference, bypass REFCAP with a 0.1µF or greater capacitor to AGND1 and bypass REF with a 1.0µF or greater capacitor to AGND1.

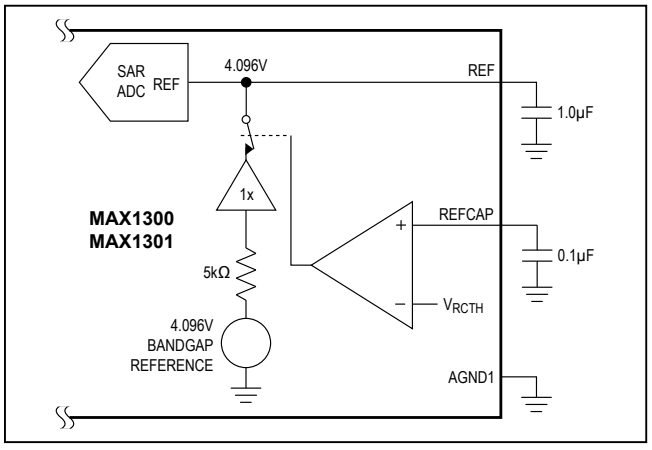


Figure 17. Internal Reference Operation

External Reference

For external reference operation, disable the internal reference and reference buffer by connecting REFCAP to AVDD1. With AVDD1 connected to REFCAP, REF becomes a high-impedance input and accepts an external reference voltage. The MAX1300/MAX1301 can accept an external reference voltage of 4.096V or less. However, to meet all of the electrical characteristic specifications, V_{REF} must be > 38V. The MAX1300/ MAX1301 external reference current varies depending on the applied reference voltage and the operating mode (see the External Reference Input Current vs. External Reference Input Voltage graph in the *Typical Operating Characteristics*).

Applications Information

Noise Reduction

Additional samples can be taken and averaged (oversampling) to remove the effect of transition noise on conversion results. The square root of the number of samples determines the improvement in performance. For example, with 2/3LSB_{RMS} (4LSB_{P-P}) transition noise, 16 (4^2 = 16) samples must be taken to reduce the noise to 1LSB_{P-P}.

Interface with 0 to 10V Signals

In industrial control applications, 0 to 10V signaling is common. For 0 to 10V applications, configure the selected MAX1300/MAX1301 input channel for the single-ended 0 to 3 x V_{REF} input range (R[2:0] = 110, Table 6). The 0 to 3 x V_{REF} range accommodates 0 to 10V where the signals saturate at approximately 3 x V_{REF} if out of range.

Interface with 4–20mA Signals

Figure 19 illustrates a simple interface between the MAX1300/MAX1301 and a 4–20mA signal. 4–20mA signaling can be used as a binary switch (4mA represents a logic-low signal, 20mA represents a logic-high signal), or for precision communication where currents between 4mA and 20mA represent intermediate analog data. For binary switch applications, connect the 4–20mA signal to the MAX1300/MAX1301 with a resistor to ground. For example, a 250Ω resistor converts the 4–20mA signal to a 1V to 5V signal. Adjust the resistor value so the parallel combination of the resistor and the MAX1300/MAX1301 source impedance is 250Ω. In this application, select the single-ended 0 to (3 x V_{REF})/2 range (R[2:0] = 011, Table 6). For applications that require precision measurements of continuous analog currents between 4mA and 20mA, use a buffer to prevent the MAX1300/MAX1301 input from diverting current from the 4–20mA signal.

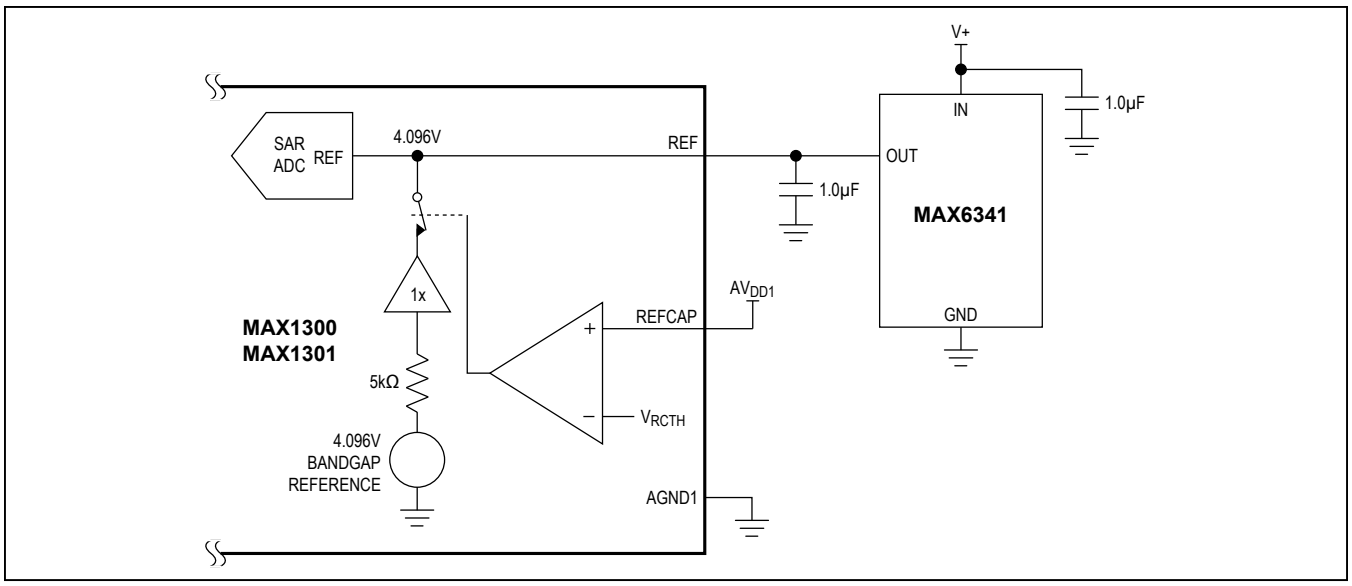


Figure 18. External Reference Operation

Bridge Application

The MAX1300/MAX1301 convert 1kHz signals more accurately than a similar sigma-delta converter that might be considered in bridge applications. The input impedance of the MAX1300, in combination with the current-limiting resistors, can affect the gain of the MAX1300. In many applications this error is acceptable, but for applications that cannot tolerate this error, the MAX1300 inputs can be buffered (Figure 20). Connect the bridge to a low-offset differential amplifier and then the true-differential inputs of the MAX1300/MAX1301. Larger excitation voltages take advantage of more of the (±3 x V_{REF})/4 differential input voltage range. Select an input voltage range that matches the amplifier output. Be aware of the amplifier offset and offset-drift errors when selecting an appropriate amplifier.

Dynamically Adjusting the Input Range

Software control of each channel's analog input range and the unipolar endpoint overlap specification make it possible for the user to change the input range for a channel dynamically and improve performance in some applications. Changing the input range results in a small LSB step-size over a wider output voltage range. For example, by switching between a (-3 x V_{REF})/2 to 0V range and a 0 to (+3 x V_{REF})/2 range, an LSB is

$$\frac{(+3 \times V_{REF}) / 2 \times V_{REF}}{65{,}536 \times 4.096}$$

but the input voltage range effectively spans from (-3 x V_{REF})/2 to (+3 x V_{REF})/2 (FSR = 3 x V_{REF}).

Layout, Grounding, and Bypassing

Careful PCB layout is essential for best system performance. Boards should have separate analog and digital ground planes and ensure that digital and analog signals are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the device package.

Figure 1 shows the recommended system ground connections. Establish an analog ground point at AGND1 and a digital ground point at DGND. Connect all analog grounds to the star analog ground. Connect the digital grounds to the star digital ground. Connect the digital ground plane to the analog ground plane at one point. For lowest noise operation, make the ground return to the star ground's power-supply low impedance and as short as possible.

High-frequency noise in the AVDD1 power supply degrades the ADC's high-speed comparator performance. Bypass AVDD1 to AGND1 with a 0.1µF ceramic surface-mount capacitor. Make bypass capacitor connections as short as possible.

Parameter Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best straight-line fit or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. The MAX1300/MAX1301 INL is measured using the endpoint method.

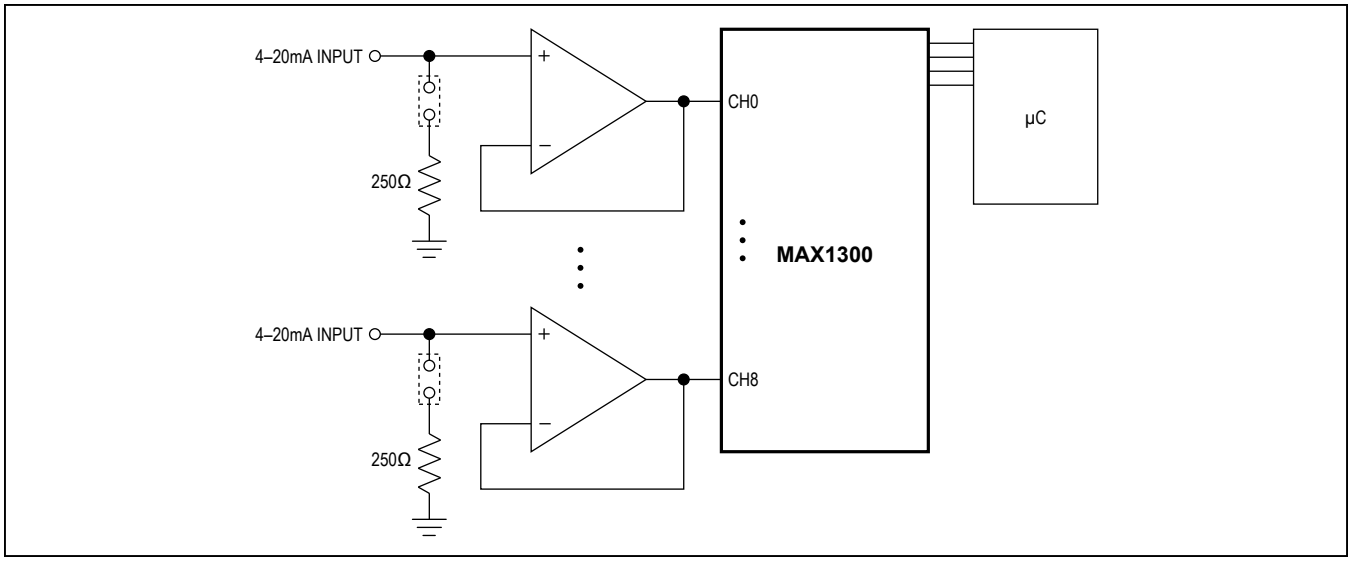


Figure 19. 4–20mA Application

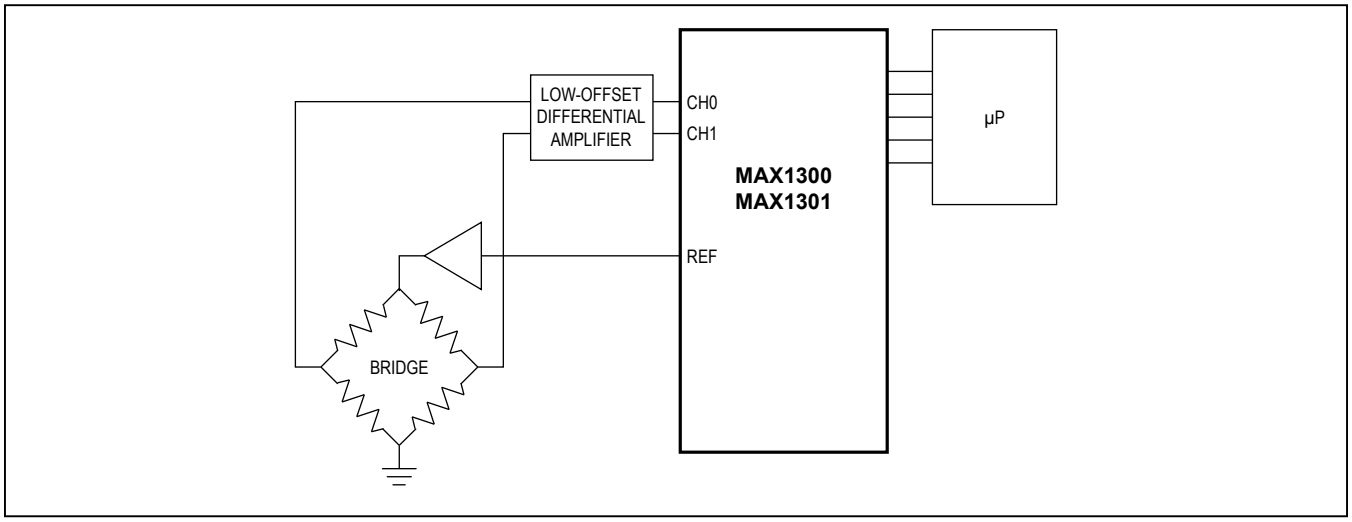


Figure 20. Bridge Application

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function.

Transition Noise

Transition noise is the amount of noise that appears at a code transition on the ADC transfer function. Conversions performed with the analog input right at the code transition can result in code flickering in the LSBs.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the others. The channel-to-channel isolation for these devices is measured by applying a near full-scale magnitude 5kHz sine wave to the selected analog input channel while applying an equal magnitude sine wave of a different frequency to all unselected channels. An FFT of the selected channel output is used to determine the ratio of the magnitudes of the signal applied to the unselected channels and the 5kHz signal applied to the selected analog input channel. This ratio is reported, in dB, as channel-to-channel isolation.

Unipolar Offset Error

-FSR to 0V

When a zero-scale analog input voltage is applied to the converter inputs, the digital output is all ones (0xFFFF). Ideally, the transition from 0xFFFF to 0xFFFE occurs at AGND1 - 0.5 LSB. Unipolar offset error is the amount of deviation between the measured zero-scale transition point and the ideal zero-scale transition point, with all untested channels grounded.

0V to +FSR

When a zero-scale analog input voltage is applied to the converter inputs, the digital output is all zeros (0x0000). Ideally, the transition from 0x0000 to 0x0001 occurs at AGND1 + 0.5 LSB. Unipolar offset error is the amount of deviation between the measured zero-scale transition point and the ideal zero-scale transition point, with all untested channels grounded.

Bipolar Offset Error

When a zero-scale analog input voltage is applied to the converter inputs, the digital output is a one followed by all zeros (0x8000). Ideally, the transition from 0x7FFF to 0x8000 occurs at (2^{N-1} - 0.5)LSB. Bipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point, with untested channels grounded.

Gain Error

When a positive full-scale voltage is applied to the converter inputs, the digital output is all ones (0xFFFF). The transition from 0xFFFE to 0xFFFF occurs at 1.5 LSB below full scale. Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point with the offset error removed and all untested channels grounded.

Unipolar Endpoint Overlap

Unipolar endpoint overlap is the change in offset when switching between complementary input voltage ranges. For example, the difference between the voltage that results in a 0xFFFF output in the -3 x V_{REF}/2 to 0V input voltage range and the voltage that results in a 0x0000 output in the 0 to +3 x V_{REF}/2 input voltage range is the unipolar endpoint overlap. The unipolar endpoint overlap is positive for the MAX1300/MAX1301, preventing loss of signal or a dead zone when switching between adjacent analog input voltage ranges.

Small-Signal Bandwidth

A 100mV_{P-P} sine wave is applied to the ADC, and the input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Full-Power Bandwidth

A 95% of full-scale sine wave is applied to the ADC, and the input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ability of a device to reject a signal that is “common” to or applied to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is expressed in decibels. Common-mode rejection ratio is the ratio of the differential signal gain to the common-mode signal gain. CMRR applies only to differential operation.

Power-Supply Rejection Ratio (PSRR)

PSRR is the ratio of the output-voltage shift to the power-supply-voltage shift for a fixed input voltage. For the MAX1300/MAX1301, AV_{DD1} can vary from 4.75V to 5.25V. PSRR is expressed in decibels and is calculated using the following equation:

$$PSRR[dB] = 20 \times \log\left(\frac{5.25V - 4.75V}{V_{OUT}(5.25V) - V_{OUT}(4.75V)}\right)$$

For the MAX1300/MAX1301, PSRR is tested in bipolar operation with the analog inputs grounded.

Aperture Jitter

Aperture jitter, t_{AJ}, is the statistical distribution of the variation in the sampling instant (Figure 21).

Aperture Delay

Aperture delay, t_{AD}, is the time from the falling edge of SCLK to the sampling instant (Figure 21).

Signal-to-Noise Ratio (SNR)

SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

$$SINAD(dB) = 20 \times \log\left(\frac{Signal_{RMS}}{Noise_{RMS}}\right)$$

Effective Number of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02} \right)$$

Total Harmonic Distortion (THD)

For the MAX1300/MAX1301, THD is the ratio of the RMS sum of the input signal's first four harmonic components to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonic components.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spectral component.

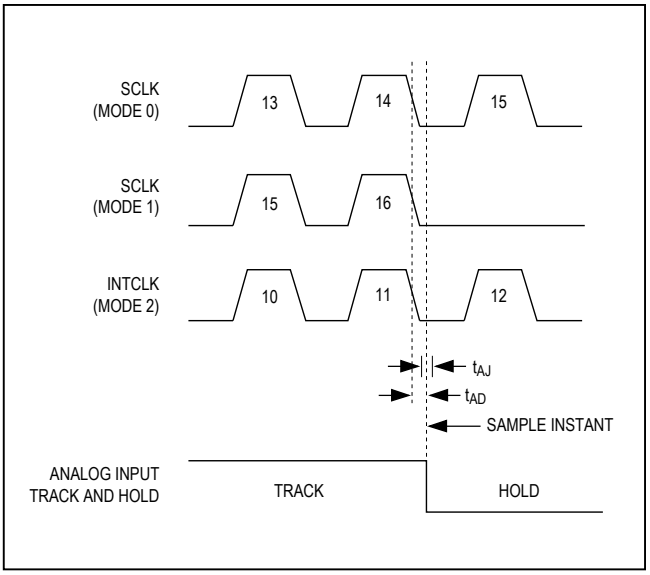
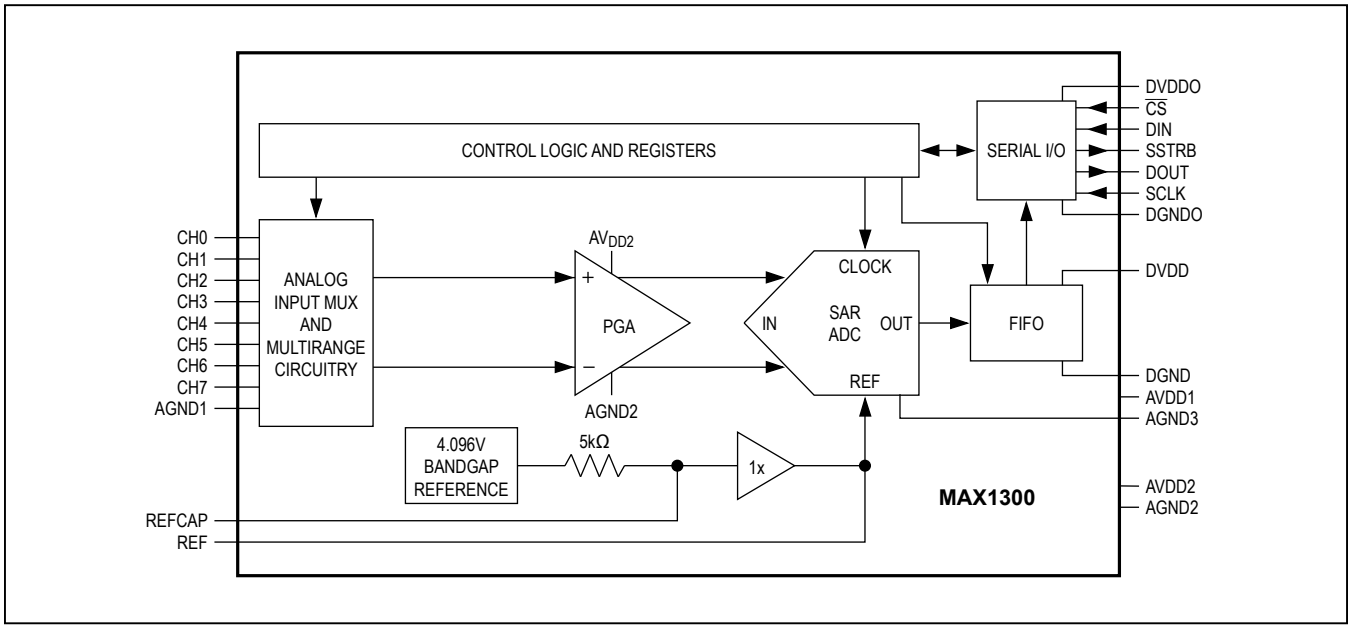
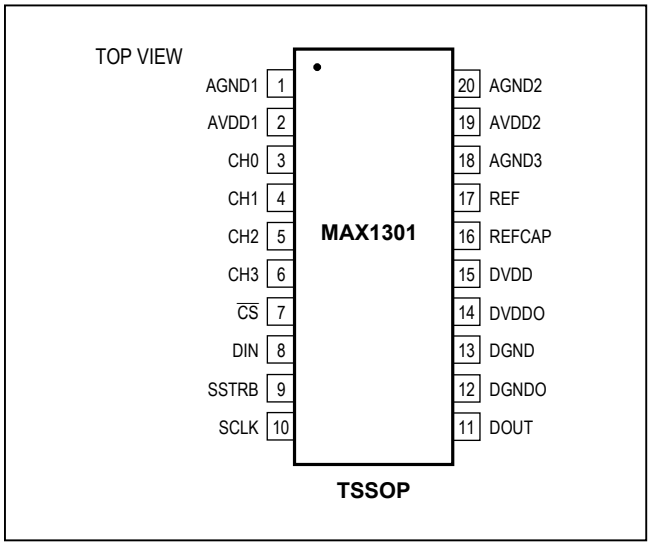


Figure 21. Aperture Diagram

Block Diagram



Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP	U20+2	21-0066	90-0116
24 TSSOP	U24+1		90-0118

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/06	Initial release	1
2	6/10	Updated *Electrical Characteristics* tables, TOCs to optimize yield.	1–10, 13, 14, 15, 17–21, 24, 25, 26, 28, 31
3	12/11	Released MAX1300 and updated the *Electrical Characteristics* table.	1, 2

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