19-3266; Rev 2; 12/04

MAXIM

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

General Description

The MAX13013/MAX13014/MAX3023 single-/dual-/quad-level translators provide the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX13013 single-, the MAX13014 dual-, and the MAX3023 (UCSP™ package) quad-level translators feature an enable (EN) input. The MAX3023 (TSSOP package) quad-level translator features EN and $\overline{EN}$ inputs. When disabled, each device places all inputs/outputs on both sides in tri-state and reduces the V_{CC} supply current to 0.03µA, and the V_L supply current to 0.1µA. These devices operate at a guaranteed 100Mbps data rate for V_L > 1.8V.

The MAX13013/MAX13014/MAX3023 accept a +1.65V to +3.6V V_{CC} voltage and a +1.2V to (V_{CC} - 0.4V) V_L voltage, making them ideal for data transfer between low-voltage ASICs/programmable logic devices (PLDs) and higher voltage systems. The MAX13013 is available in 3 x 2 UCSP and 6-pin SC70 packages. The MAX13014 is available in 3 x 3 UCSP and 8-pin SOT23 packages. The MAX3023 is available in 4 x 3 UCSP and 14-pin TSSOP packages. All devices operate over the extended -40°C to +85°C temperature range.

Applications

CMOS Logic-Level Translation

Low-Voltage ASIC Level Translation

Cell Phones

SPI™, MICROWIRE™ Level Translation

Portable POS Systems

Portable Communication Devices

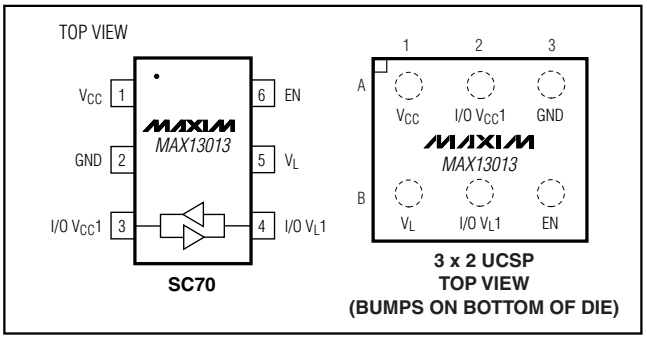
GPS

Telecommunications Equipment

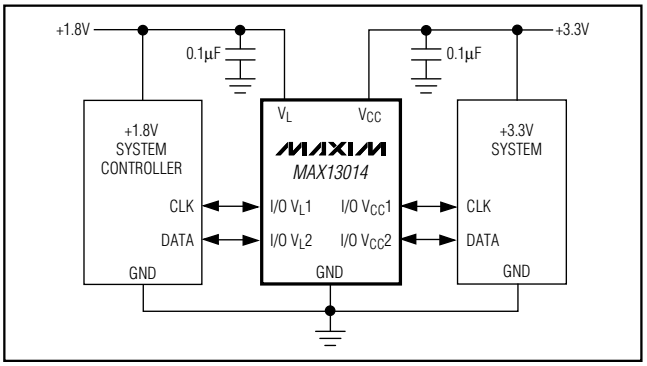
Features

- **100Mbps Guaranteed Data Rate**
- **Bidirectional Level Translation**
  - **MAX13013 (Single)**
  - **MAX13014 (Dual)**
  - **MAX3023 (Quad)**
- **V_L Operation Down to +1.2V**
- **Ultra-Low 0.1µA Supply Current When Disabled**
- **Low-Quiescent Current (0.1µA)**
- **UCSP, SC70, SOT23, and TSSOP Packages**

Pin Configurations



Typical Operating Circuit



Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE	TOP MARK	NUMBER OF $V_L \rightarrow V_{CC}$ TRANSLATORS	Number of $V_{CC} \rightarrow V_L$ TRANSLATORS	EN	$\overline{EN}$
MAX13013EXT	-40°C to +85°C	6 SC70	—	ACD	1	1	✓	—

MICROWIRE is a trademark of National Semiconductor Corp.
SPI is a trademark of Motorola, Inc.
UCSP is a trademark of Maxim Integrated Products, Inc.

Pin Configurations continued at end of data sheet.
Ordering Information/Selector Guide continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to GND.
V_{CC} .....-0.3V to +4V
V_L.....-0.3V to +4V
I/O $V_{CC_}$.....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L_}$.....-0.3V to (V_L + 0.3V)
EN, $\overline{EN}$.....-0.3V to (V_L + 0.3V)
Short-Circuit Duration I/O $V_{L_}$,
I/O $V_{CC_}$ to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C).....245mW
6-Bump UCSP (derate 3.9mW/°C above +70°C).....308mW
8-Bump UCSP (derate 4.7mW/°C above +70°C).....379mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
12-Bump UCSP (derate 6.5mW/°C above +70°C) ...518.8mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V), EN = V_L, $\overline{EN}$ = open (MAX3023 TSSOP package only), C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_L Supply Range	V_L		1.2		V_{CC} - 0.4	V
V_{CC} Supply Range	V_{CC}		1.65		3.60	V
Supply Current from V_{CC}	IQV_{CC}	I/O $V_{CC_}$ = 0, I/O $V_{L_}$ = 0 or I/O $V_{CC_}$ = V_{CC}, I/O $V_{L_}$ = V_L		0.1	1	µA
Supply Current from V_L	IQV_L	I/O $V_{CC_}$ = 0, I/O $V_{L_}$ = 0 or I/O $V_{CC_}$ = V_{CC}, I/O $V_{L_}$ = V_L		0.2	2	µA
		I/O $V_{CC_}$ = 0, I/O $V_{L_}$ = 0 or I/O $V_{CC_}$ = V_{CC}, I/O $V_{L_}$ = V_L, V_L < V_{CC} - 0.2V		10	100	
V_{CC} Tri-state Output-Mode Supply Current	I_{TS-VCC}	T_A = +25°C, EN = 0		0.03	1	µA
V_L Tri-state Output-Mode Supply Current (MAX13013/MAX13014)	I_{TS-VL}	T_A = +25°C, EN = 0		0.1	0.2	µA
		T_A = +25°C, EN = 0, V_L = V_{CC} - 0.2V		1	2	
V_L Tri-state Output-Mode Supply Current (MAX3023 TSSOP Package Only)	I_{TS-VL}	T_A = +25°C, EN = 0		50	70	µA
		T_A = +25°C, EN = 0, V_L = V_{CC} - 0.2V		55	74	
I/O Tri-state Output-Mode Leakage Current		T_A = +25°C, EN = 0			0.15	µA
		T_A = +25°C, EN = 0, V_L = V_{CC} - 0.2V			20	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V), EN = V_L, $\overline{EN}$ = open (MAX3023 TSSOP package only), $C_{IOVL} \le 15pF$, $C_{IOVCC} \le 40pF$, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC-LEVEL THRESHOLDS						
I/O $V_{L_}$ Input-Voltage High	V_{IHL}		2/3 x V_L			V
I/O $V_{L_}$ Input-Voltage Low	V_{ILL}				1/3 x V_L	V
Pullup Resistance on I/O $V_{L_}$			120			Ω
Pulldown Resistance on I/O $V_{L_}$			75			Ω
I/O $V_{CC_}$ Input-Voltage High	V_{IHC}		2/3 x V_{CC}			V
I/O $V_{CC_}$ Input-Voltage Low	V_{ILC}				1/3 x V_{CC}	V
Pullup Resistance on I/O $V_{CC_}$			2.5			kΩ
Pulldown Resistance on I/O $V_{CC_}$			2.5			kΩ
EN, $\overline{EN}$ Input-Voltage High	V_{IH}		2/3 x V_L			V
EN, $\overline{EN}$ Input-Voltage Low	V_{IL}				1/3 x V_L	V
EN Input Current		MAX13013/MAX13014	-5		+5	µA
Pullup Resistance on EN		MAX3023	46	62	81	kΩ
Pulldown Resistance on $\overline{EN}$		MAX3023, TSSOP package only	46	62	81	kΩ
I/O $V_{L_}$ Output-Voltage High	V_{OHL}	I/O V_L source current = 20µA	2/3 x V_L			V
I/O $V_{L_}$ Output-Voltage Low	V_{OLL}	I/O V_L sink current = 20µA			1/3 x V_L	V
I/O $V_{CC_}$ Output-Voltage High	V_{OHC}	I/O V_{CC} source current = 20µA	2/3 x V_{CC}			V
I/O $V_{CC_}$ Output-Voltage Low	V_{OLC}	I/O V_{CC} sink current = 20µA			1/3 x V_{CC}	V

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V), EN = V_L, $\overline{EN}$ = open (MAX3023 TSSOP package only), $C_{IOVL} \le 15pF$, $C_{IOVCC} \le 40pF$, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC_}$ Rise Time	t_{RVCC}	C_{IOVCC} = 15pF, Figure 1			2.5	ns
		C_{IOVCC} = 20pF, Figure 1			3	
		C_{IOVCC} = 40pF, Figure 1			4	
I/O $V_{CC_}$ Fall Time	t_{FVCC}	C_{IOVCC} = 15pF, Figure 1			2.5	ns
		C_{IOVCC} = 20pF, Figure 1			3	
		C_{IOVCC} = 40pF, Figure 1			4	
I/O $V_{CC_}$ One-Shot Output Impedance					18.5	Ω
I/O $V_{L_}$ Rise Time	t_{RVL}	C_{IOVL} = 15pF, Figure 2			2.5	ns
I/O $V_{L_}$ Fall Time	t_{FVL}	C_{IOVL} = 15pF, Figure 2			2.5	ns
I/O $V_{L_}$ One-Shot Output Impedance					12.5	Ω
Propagation Delay, Driving I/O $V_{L_}$	I/O_{VL-VCC}	C_{IOVCC} = 15pF, Figure 1			6.5	ns
Propagation Delay, Driving I/O $V_{CC_}$	I/O_{VCC-VL}	C_{IOVL} = 15pF, Figure 2			6	ns
Part-to-Part Skew (Note 3)	t_{PPSKEW}	C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_{CC} = 2.5V, V_L = 1.8V			4	ns
Propagation Delay from I/O $V_{L_}$ to I/O $V_{CC_}$ after Enable	t_{EN-VCC}	C_{IOVCC} = 15pF, Figure 3			1000	ns
Propagation Delay from I/O $V_{CC_}$ to I/O $V_{L_}$ after Enable	t_{EN-VL}	C_{IOVL} = 15pF, Figure 4			1000	ns
Maximum Data Rate		C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.8V	100			Mbps
		C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.2V	80			

Note 1: V_L must be less than or equal to V_{CC} - 0.4V during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

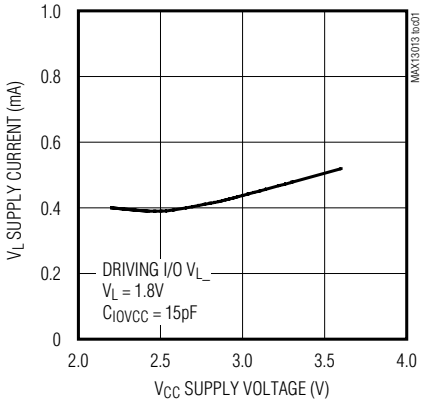
Note 3: Not production tested. Guaranteed by design.

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

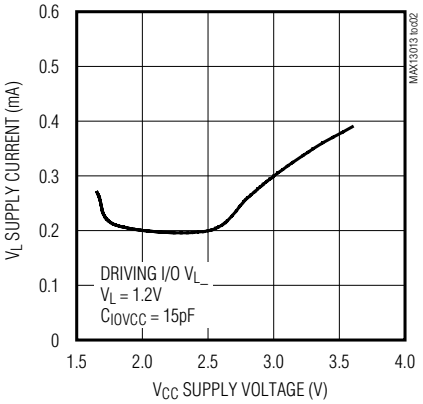
Typical Operating Characteristics

(Data rate = 100Mbps, V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C, unless otherwise noted.)

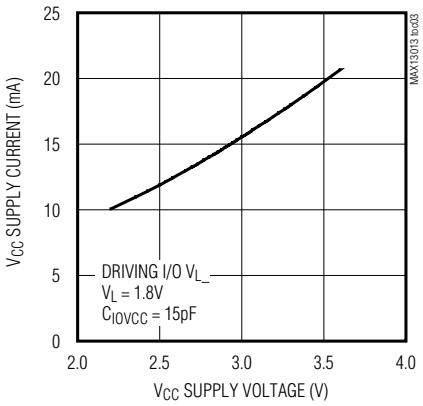
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



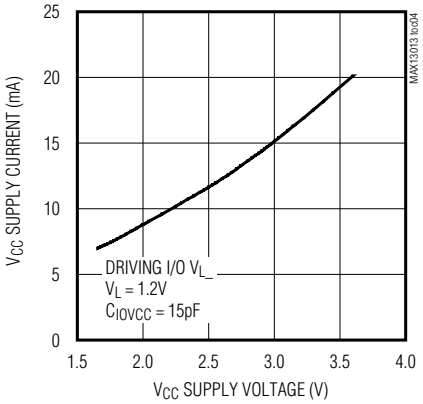
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



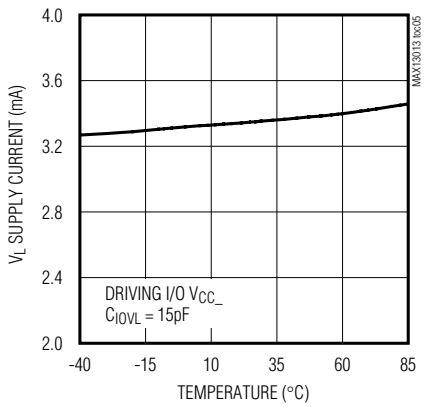
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



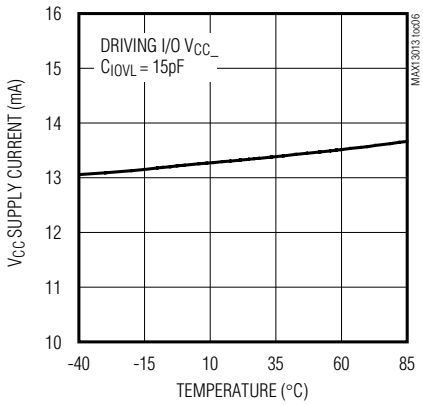
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



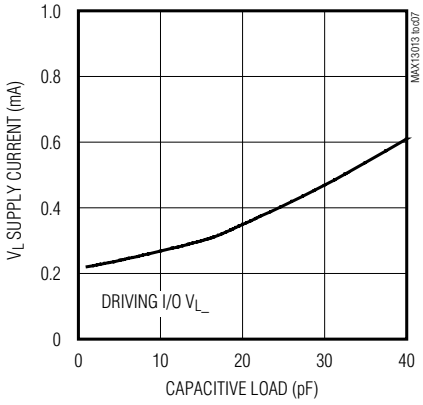
V_L SUPPLY CURRENT vs. TEMPERATURE



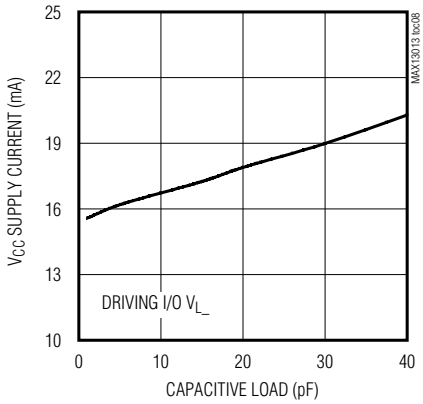
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



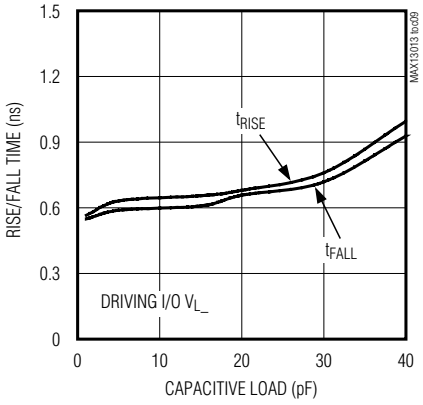
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{CC_}$



V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{CC_}$



RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{CC_}$

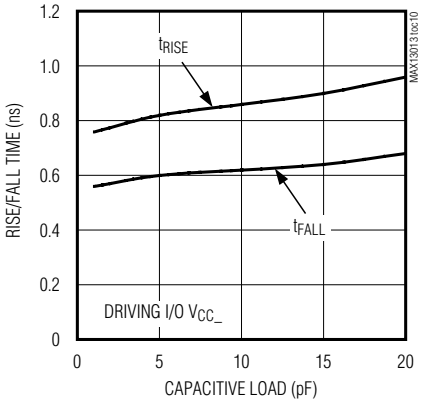


+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

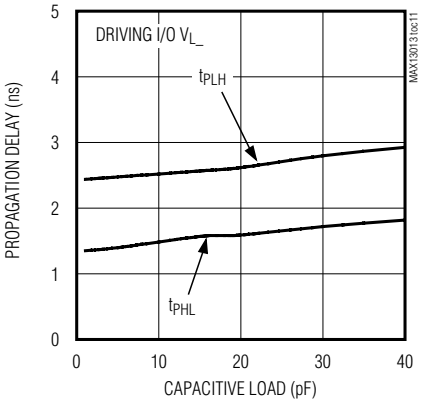
Typical Operating Characteristics (continued)

(Data rate = 100Mbps, V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C, unless otherwise noted.)

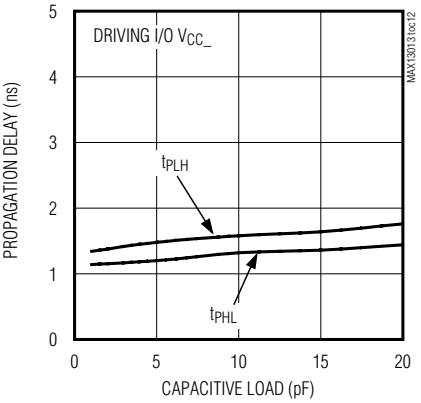
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L_



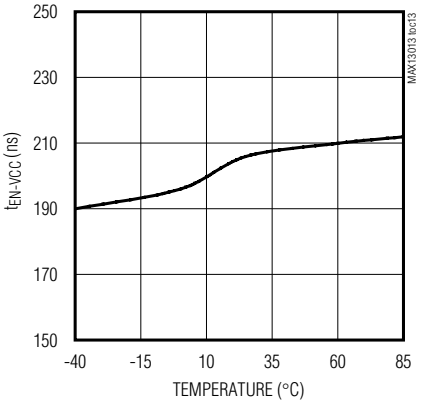
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC}_



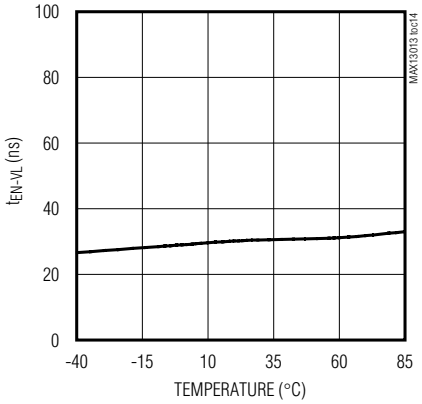
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L_



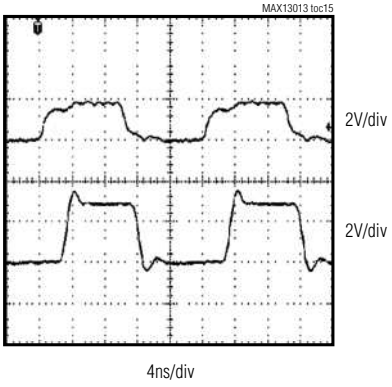
t_{EN-VCC} vs. TEMPERATURE (C_{IOVCC} = 15pF)



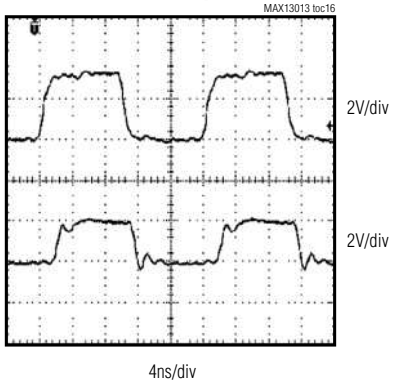
t_{EN-VL} vs. TEMPERATURE (C_{IOVL} = 15pF)



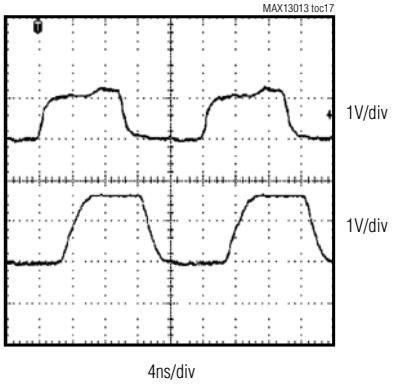
TYPICAL I/O V_L_ DRIVING (C_{IOVCC} = 40pF)



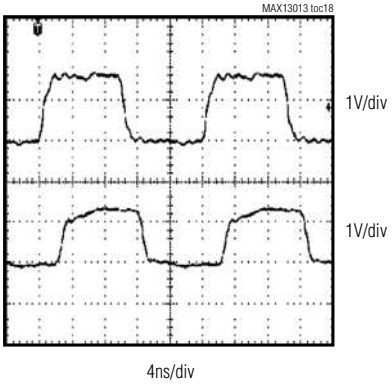
TYPICAL I/O V_{CC}_ DRIVING (C_{IOVL} = 15pF)



TYPICAL I/O V_L_ DRIVING (V_{CC} = 1.65V, V_L = 1.2V, C_{IOVCC} = 40pF)



TYPICAL I/O V_{CC}_ DRIVING (V_{CC} = 1.65V, V_L = 1.2V, C_{IOVL} = 15pF)



Pin Description—MAX13013/MAX13014/MAX3023 (Bidirectional Devices)

PIN						NAME	FUNCTION
MAX3023		MAX13013		MAX13014			
TSSOP	4 x 3 UCSP	SC70	3 x 2 UCSP	SOT23	3 x 3 UCSP		
1	A1	4	B2	7	A2	I/O V_L1	Input/Output 1, Referenced to V_L
2	B2	—	—	6	A3	I/O V_L2	Input/Output 2, Referenced to V_L
3	A2	5	B1	8	A1	V_L	V_L Input Voltage, +1.2V ≤ V_L ≤ V_{CC} - 0.4V. Bypass V_L to GND with a 0.1µF capacitor.
4	—	—	—	—	—	N.C.	No Connection
5	B3	—	—	—	—	I/O V_L3	Input/Output 3, Referenced to V_L
6	A3	—	—	—	—	I/O V_L4	Input/Output 4, Referenced to V_L
7	A4	6	B3	5	B1	EN	Active-High Enable Input. If EN is pulled low, all inputs/outputs are in tristate. Drive EN high (V_L) for normal operation.
8	—	—	—	—	—	$\overline{EN}$	Active-Low Enable Input. If $\overline{EN}$ is pulled high (V_L), all inputs/outputs are in tri-state. Drive $\overline{EN}$ low for normal operation (MAX3023 TSSOP package only).
9	B4	—	—	—	—	I/O V_{CC}4	Input/Output 4, Referenced to V_{CC}
10	C4	—	—	—	—	I/O V_{CC}3	Input/Output 3, Referenced to V_{CC}
11	C3	2	A3	4	B3	GND	Ground
12	C2	1	A1	1	C1	V_{CC}	V_{CC} Input Voltage, +1.65V ≤ V_{CC} ≤ +3.6V. Bypass V_{CC} to GND with a 0.1µF capacitor.
13	C1	—	—	3	C3	I/O V_{CC}2	Input/Output 2, Referenced to V_{CC}
14	B1	3	A2	2	C2	I/O V_{CC}1	Input/Output 1, Referenced to V_{CC}

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Test Circuits/Timing Diagrams

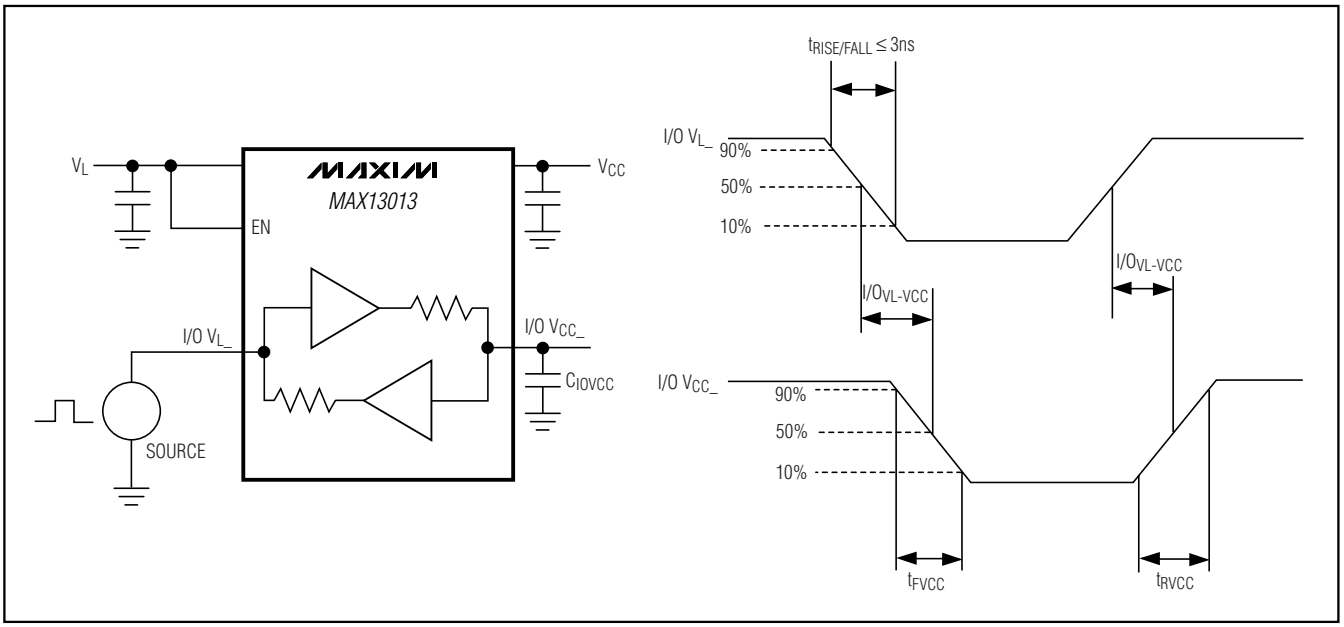


Figure 1. Driving I/O $V_{L_}$ Test Circuit and Timing

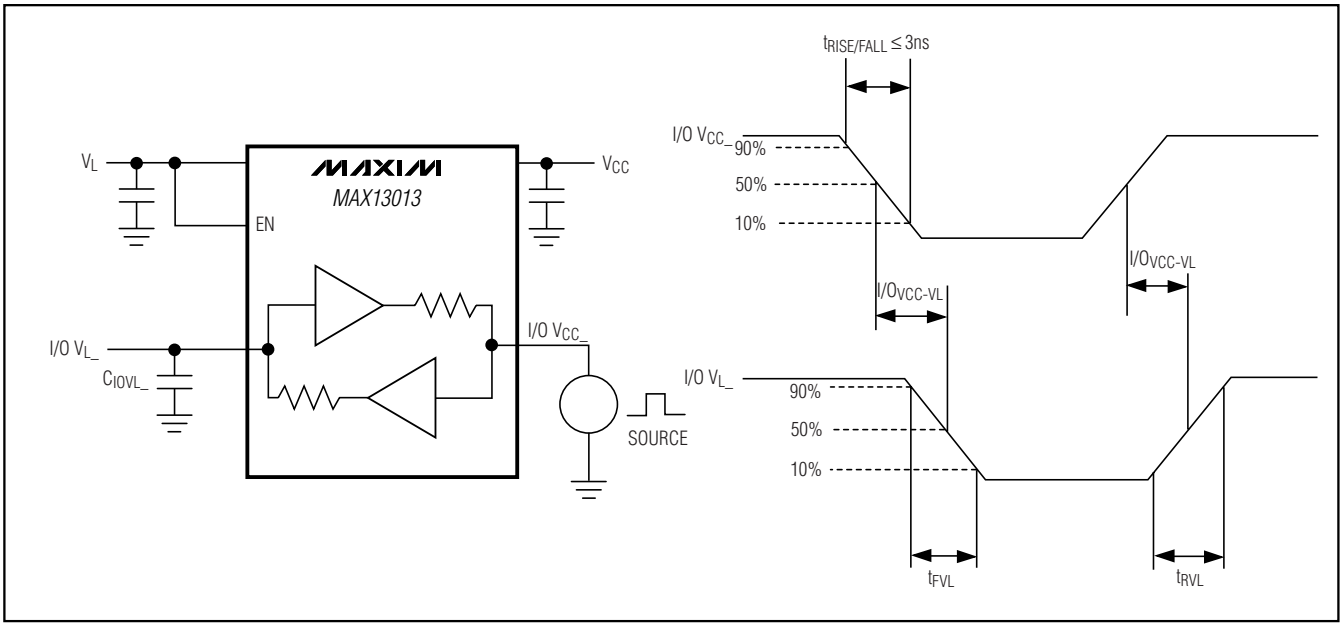


Figure 2. Driving I/O $V_{CC_}$ Test Circuit and Timing

Test Circuits/Timing Diagrams (continued)

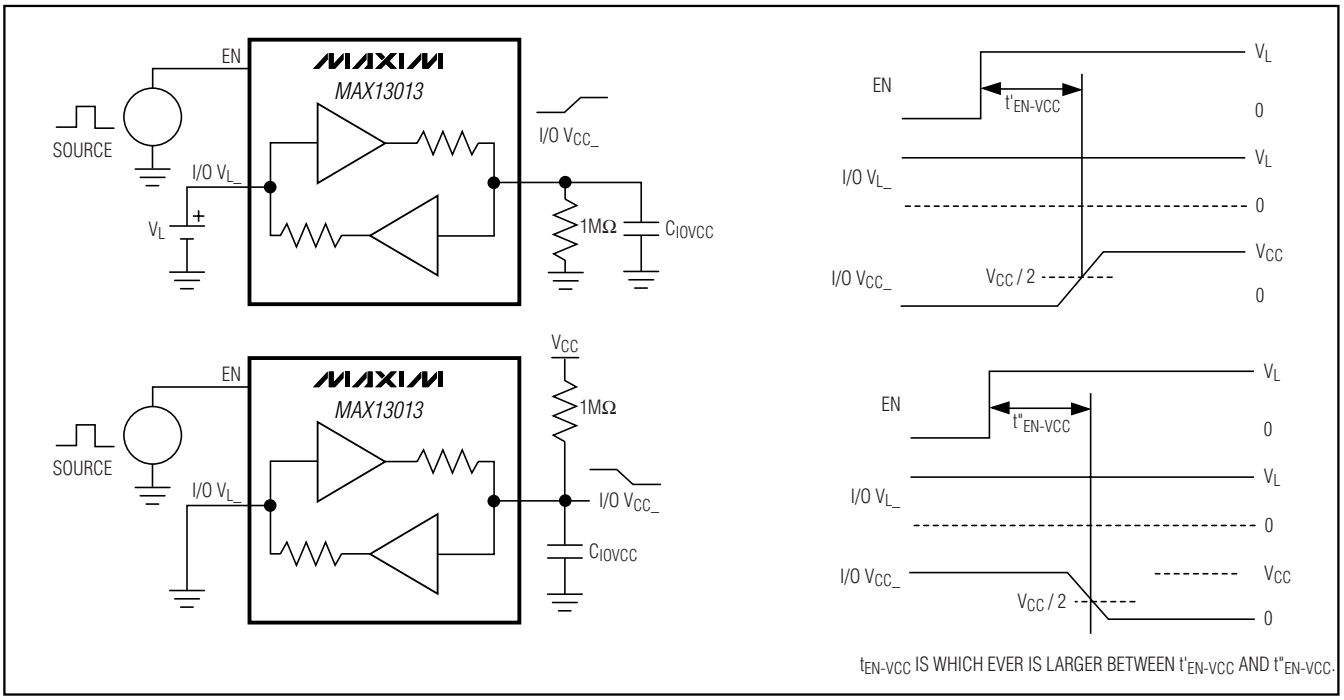


Figure 3. Propagation Delay from I/O $V_{L_}$ to I/O $V_{CC_}$ After EN

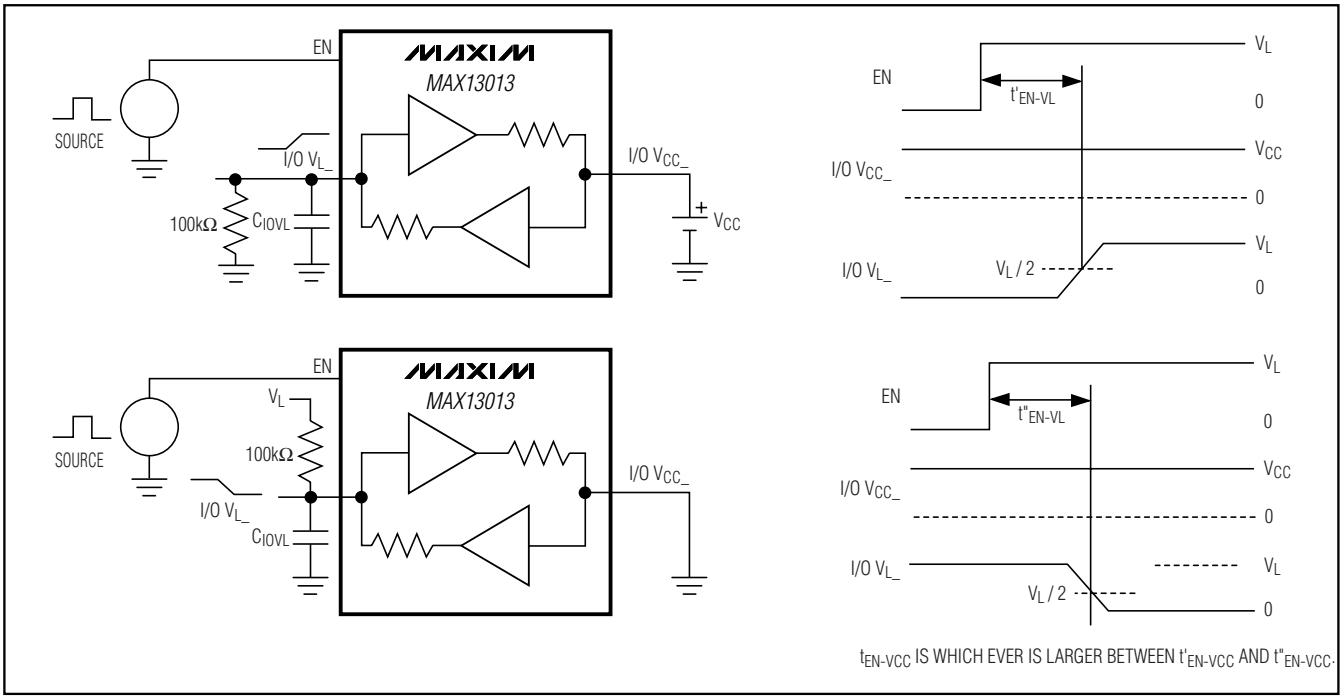


Figure 4. Propagation Delay from I/O $V_{CC_}$ to I/O $V_{L_}$ After EN

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Detailed Description

The MAX13013/MAX13014/MAX3023 logic-level translators provide the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher-voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX13013/MAX13014/MAX3023 bidirectional level translators allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX13013/MAX13014/MAX3023 accept V_L from +1.2V to (V_{CC} - 0.4V) and operate with V_{CC} from +1.65V to +3.6V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

When in tri-state mode, the MAX13013/MAX13014/MAX3023 reduce the V_{CC} supply current to 0.03µA, and the V_L supply current to 0.1µA. These devices operate at a guaranteed data rate of 100Mbps for V_L > 1.8V.

Level Translation

For proper operation, ensure that $+1.65V \le V_{CC} \le +3.6V$, and $+1.2V \le V_L \le V_{CC} - 0.4V$. During power-up sequencing, $V_L \ge V_{CC}$ does not damage the device. During power-supply sequencing, when V_{CC} is floating and V_L is powering up, up to 40mA current can be sourced to each load on the V_L side, without the device latching up. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics* Rise/Fall Time graph), output impedance of the driver, and the operating voltage range (Table 1).

Input Driver Requirements

The MAX13013/MAX13014/MAX3023 architecture is based on a one-shot accelerator output stage (see Figure 5). Accelerator output stages are in tri-state mode except when there is a transition on any of the translators on the input side, either I/O V_L_ or I/O V_{CC}_. A short pulse is then generated during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to the architecture, both sides become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior simply helps to speed up the transition on the driven side.

For proper operation, the driver has to meet the following conditions: less than 25Ω output impedance and greater than 20mA peak output current capability.

Table 1. Data Rate

V_L (V)	GUARANTEED DATA RATE (Mbps)
V_L < 1.8	80
$V_L \ge 1.8$	100

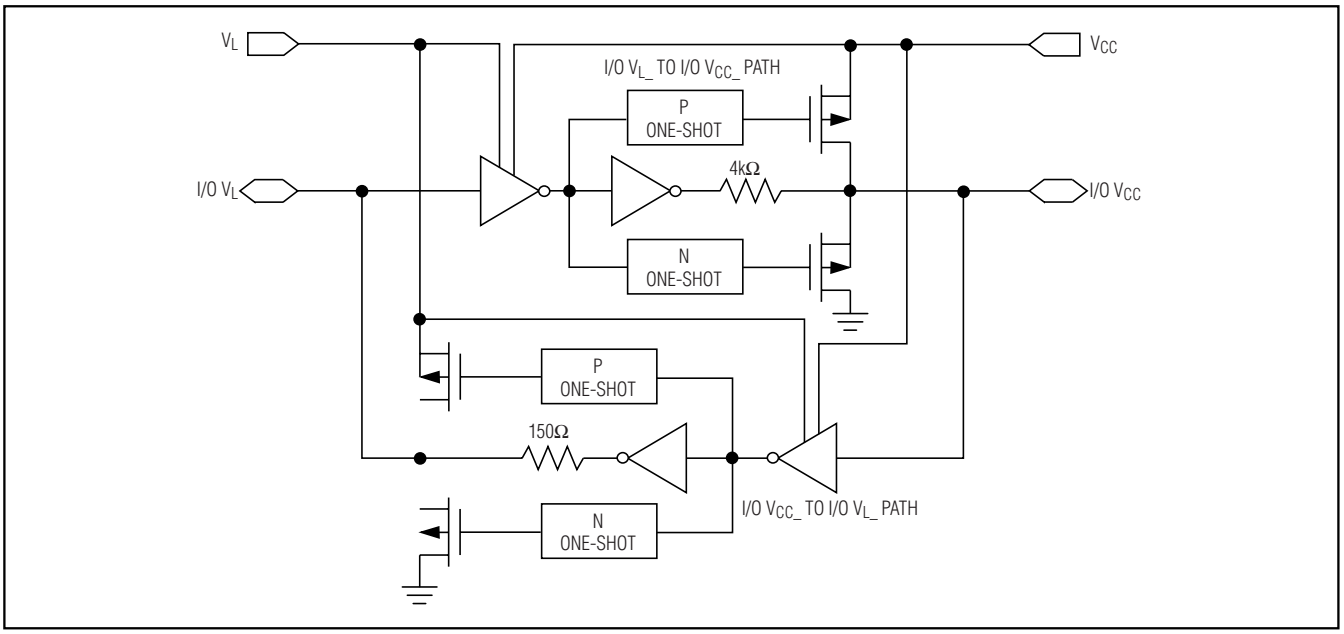


Figure 5. Simplified Functional Diagram (One I/O Line)

Figure 6 shows a graph of typical input current versus input voltage.

Output Load Requirements

The MAX13013/MAX13014/MAX3023 I/O are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ. Also, do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/MAX3001E logic-level-translators data sheet.

For I²C level translation, refer to the MAX3372E-MAX3379E/MAX3390E–MAX3393E data sheet.

Enable Inputs

The MAX13013 single-, the MAX13014 dual- and the MAX3023 (UCSP package) quad-level translators feature an EN input. The MAX3023 (TSSOP package) quad-level translator features both EN and $\overline{EN}$ inputs (see Table 2 for operating mode). Note that the MAX3023 (TSSOP package) has internal pullup and pulldown circuitry on EN and $\overline{EN}$, respectively. If left unconnected, EN is pulled up to V_L and $\overline{EN}$ is pulled down to GND.

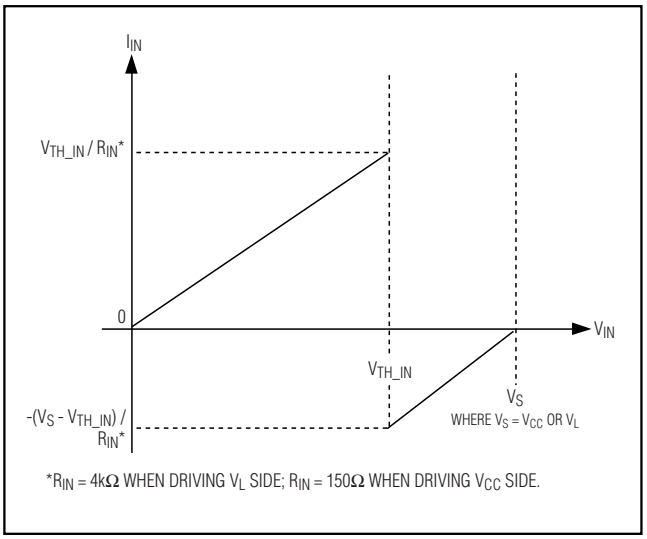


Figure 6. Typical I_{IN} vs. V_{IN}

Table 2. MAX3023 (TSSOP Package) Operating Mode

EN	$\overline{EN}$	OPERATING MODE
0	0	Both I/O V_L_ and I/O V_{CC}_ are in tri-state.
V_L	0	Normal operation.
0	V_L	Both I/O V_L_ and I/O V_{CC}_ are in tri-state.
V_L	V_L	Both I/O V_L_ and I/O V_{CC}_ are in tri-state.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with a 0.1µF ceramic capacitor. Place all capacitors as close to the power-supply inputs as possible.

Unidirectional vs. Bidirectional Level Translator

The MAX13013/MAX13014/MAX3023 bidirectional translators can operate as a unidirectional device to translate signals without inversion. These devices provide the smallest solution (UCSP package) for unidirectional level translation without inversion.

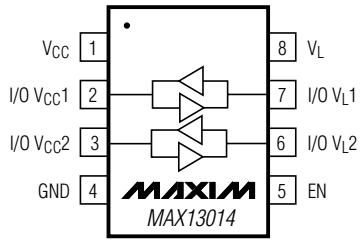
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's web site at www.maxim-ic.com/ucsp to find the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

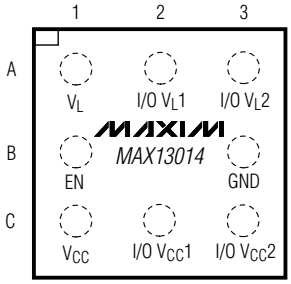
+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Pin Configurations (continued)

TOP VIEW

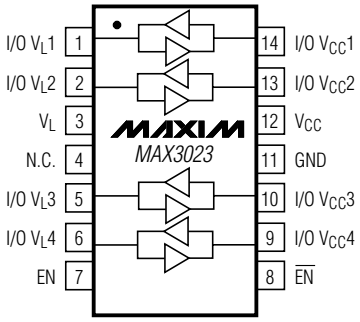


SOT23

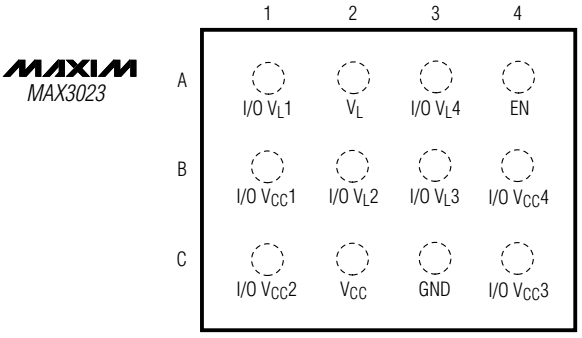


UCSP
(BUMPS ON BOTTOM OF DIE)

TOP VIEW



TSSOP



UCSP
(BUMPS ON BOTTOM OF DIE)

Ordering Information/Selector Guide (continued)

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE	TOP MARK	NUMBER OF $V_L \rightarrow V_{CC}$ TRANSLATORS	Number of $V_{CC} \rightarrow V_L$ TRANSLATORS	EN	$\overline{EN}$
MAX13013EBT-T	-40°C to +85°C	3 x 2 UCSP-6	B6-1	ADF	1	1	✓	—
MAX13014EKA	-40°C to +85°C	8 SOT23	—	AEKB	2	2	✓	—
MAX13014EBL-T	-40°C to +85°C	3 x 3 UCSP-9	B9-2	AEN	2	2	✓	—
MAX3023EUD	-40°C to +85°C	14 TSSOP	—	—	4	4	✓	✓
MAX3023EBC-T	-40°C to +85°C	4 x 3 UCSP-12	B12-1	ABW	4	4	✓	—

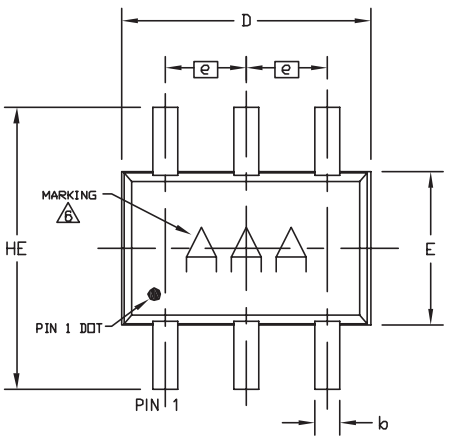
Chip Information

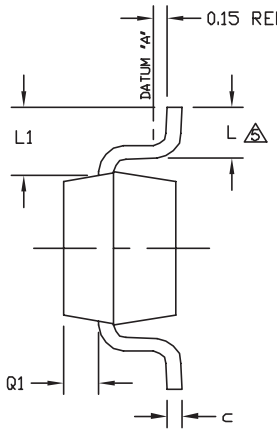
TRANSISTOR COUNT:
MAX13013: 261
MAX13014: 444
MAX3023: 791
PROCESS: BiCMOS

Package Information

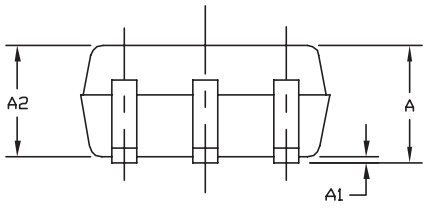
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 6L.EPS





COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.30
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.41
L1	0.425 TYP.	
Q1	0.10	0.40



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0077	C	1/1

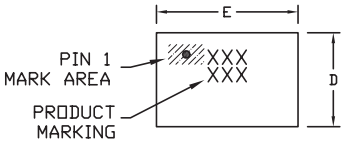
-DRAWING NOT TO SCALE-

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6L, UCSP.EPS

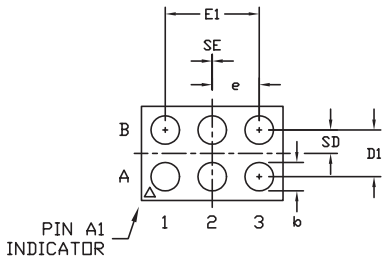


TOP VIEW

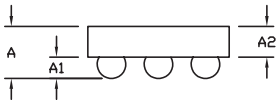
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

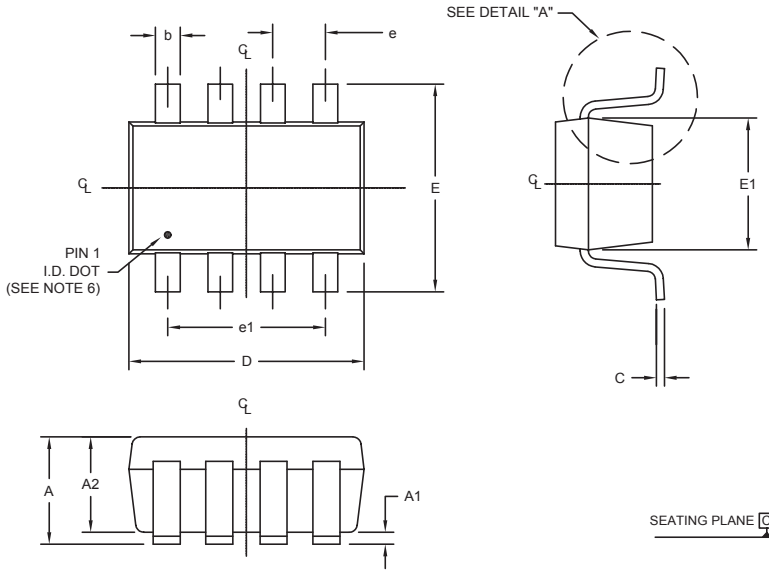
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APPROVAL	DOCUMENT CONTROL NO.	REV.	
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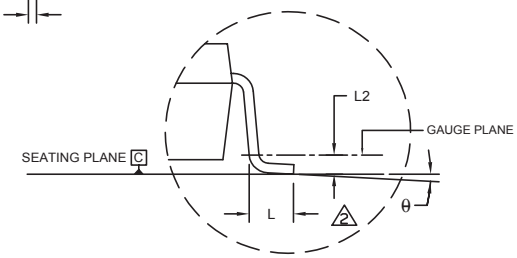
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0∞	8∞



DETAIL "A"

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ÿ MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

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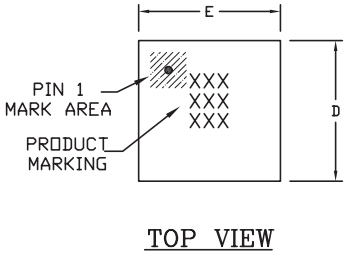
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+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

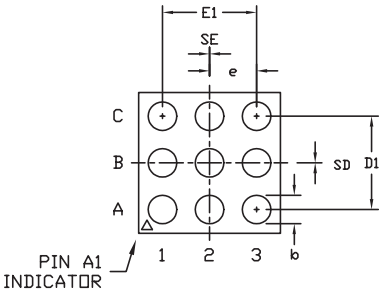


TOP VIEW

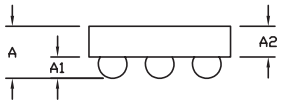
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

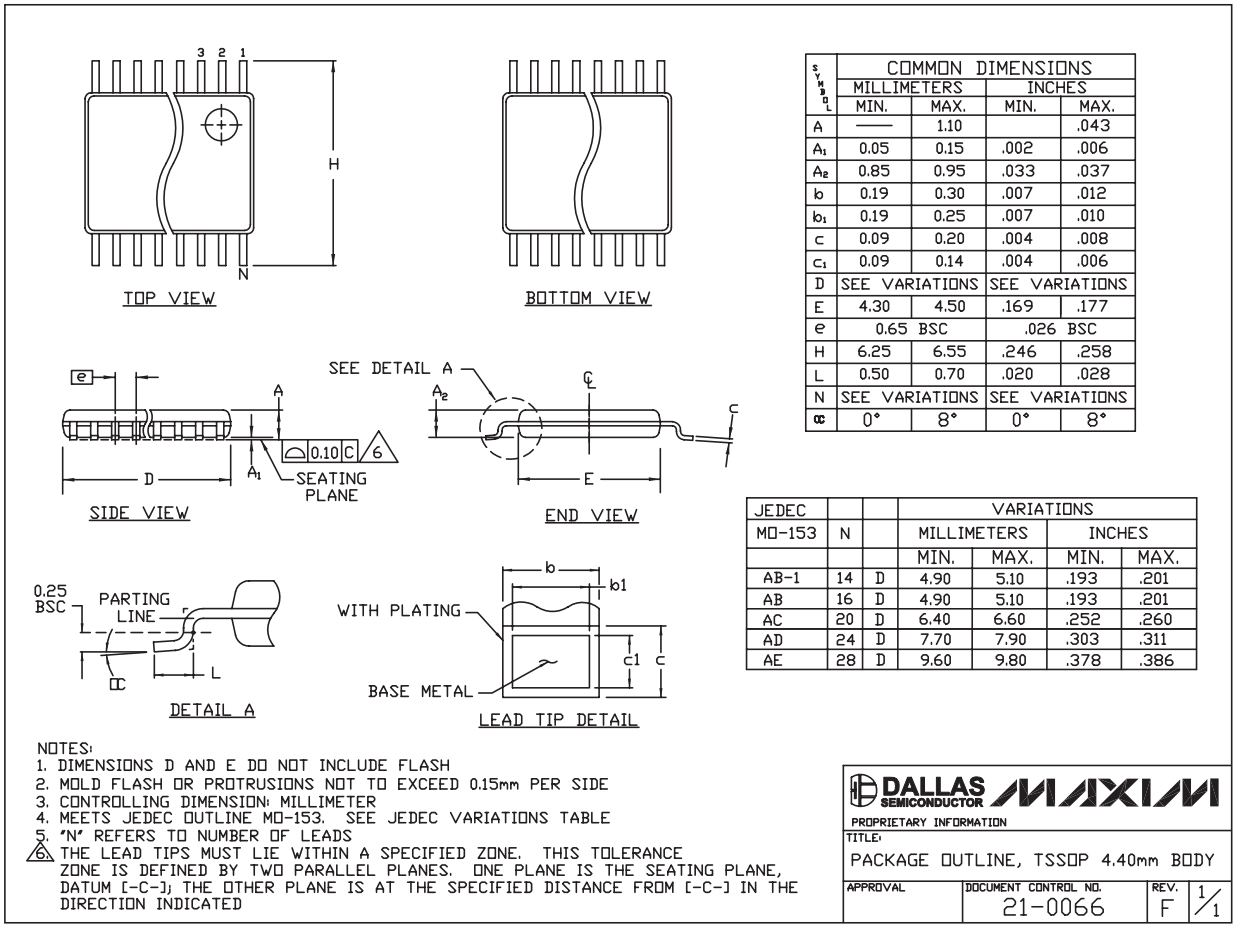
TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

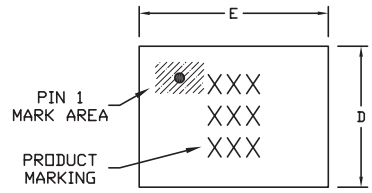
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

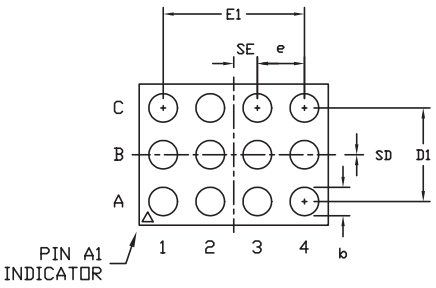
12L, UCSP 4x3.EPS



TOP VIEW

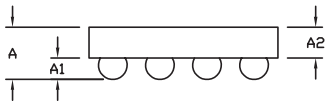
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

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