19-3054; Rev 1a; 2/04

MAXIM

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

General Description

The MAX1497/MAX1499 low-power, 3.5- and 4.5-digit, analog-to-digital converters (ADCs) with integrated light-emitting diode (LED) drivers operate from a single 2.7V to 5.25V power supply. They include an internal reference, a high-accuracy on-chip oscillator, and a multiplexed LED display driver. An internal charge pump generates the negative supply needed to power the integrated input buffers for single-supply operation. The ADC is configurable for either a ±2V or ±200mV input range and it outputs its conversion results to an LED and/or to a microcontroller (µC). Microcontroller communication is possible through an SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. The MAX1497 is a 3.5-digit (±1999 count) device and the MAX1499 is a 4.5-digit (±19,999 count) device.

The MAX1497/MAX1499 do not require external precision integrating capacitors, autozero capacitors, crystal oscillators, charge pumps, or other circuitry required with dual-slope ADCs (commonly used in panel meter circuits).

These devices also feature on-chip buffers for the differential signal and reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset-calibration and offer >100dB rejection of 50Hz and 60Hz line noise. Other features include data hold and peak detection, overrange and underrange detection, and a user-programmable low-battery monitor.

The MAX1499 is available in a 32-pin, 7mm × 7mm TQFP package and the MAX1497 is available in 28-pin SSOP and 28-pin PDIP packages. All devices in this family operate over the -40°C to +85°C extended temperature range.

Applications

Digital Panel Meters

Hand-Held Meters

Digital Voltmeters

Digital Multimeters

Features

- **High Resolution**
  MAX1499: 4.5 Digits (±19,999 Count)
  MAX1497: 3.5 Digits (±1999 Count)
- **Sigma-Delta ADC Architecture**
  No Integrating Capacitors Required
  No Autozeroing Capacitors Required
  >100dB of Simultaneous 50Hz and 60Hz Rejection
- **Operate from a Single 2.7V or 5.25V Supply**
- **Selectable Input Range of ±200mV or ±2V**
- **Selectable Voltage Reference: Internal 2.048V or External**
- **Internal High-Accuracy Oscillator Needs No External Components**
- **Automatic Offset Calibration**
- **Low Power (Exclude LED Driver Current)**
  Maximum 664µA Operating Current
  Maximum 268µA Shutdown Current
- **Small 32-Pin, 7mm x 7mm TQFP Package (4.5 Digits), 28-Pin SSOP Package (3.5 Digits)**
- **Also Available in a PDIP Package (3.5 Digits)**
- **Multiplexed LED Drivers**
  Resistor-Programmable Segment Current
- **SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- **Extended Temperature Range (-40°C to +85°C)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESOLUTION (DIGITS)
MAX1497EAI*	-40°C to +85°C	28 SSOP	3.5
MAX1497EPI	-40°C to +85°C	28 PDIP	3.5
MAX1499ECJ	-40°C to +85°C	32 TQFP	4.5

**Future product—contact factory for availability.*

Pin Configurations appear at end of data sheet.

SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND (MAX1499).....-0.3V to +6V
DV_{DD} to GND (MAX1499) .....-0.3V to +6V
AIN+, AIN- to GND (MAX1499) .....VNEG to (AV_{DD} to +0.3V)
REF+, REF- to GND (MAX1499)..... VNEG to (AV_{DD} to +0.3V)
LOWBATT to GND (MAX1499) .....-0.3V to (AV_{DD} + 0.3V)
CLK, $\overline{EOC}$, $\overline{CS}$, DIN, SCLK,
DOUT to GND (MAX1499).....-0.3V to (DV_{DD} + 0.3V)
VNEG to GND (MAX1499) .....-2.6V to (AV_{DD} + 0.3V)
LED_EN to GND (MAX1499).....-0.3V to (DV_{DD} + 0.3V)
ISET to GND (MAX1499).....-0.3V to (AV_{DD} + 0.3V)
V_{DD} to GND (MAX1497).....-0.3V to +6V
AIN+, AIN- to GND (MAX1497).....VNEG to (V_{DD} to +0.3V)
REF+, REF- to GND (MAX1497) ..... VNEG to (V_{DD} to +0.3V)
CLK, $\overline{EOC}$, $\overline{CS}$, DIN, SCLK,
DOUT to GND (MAX1497).....-0.3V to (V_{DD} + 0.3V)
VNEG to GND (MAX1497).....-2.6V to (V_{DD} + 0.3V)
ISET to GND (MAX1497) .....-0.3V to (V_{DD} + 0.3V)
VLED to GLED .....-0.3V to +6V
GLED to GND .....-0.3V to +0.3V
SEG_ to GLED.....-0.3V to (VLED + 0.3V)
DIG_ to GLED .....-0.3V to (VLED + 0.3V)
DIG_ Sink Current 300mA
DIG_ Source Current.....50mA
SEG_ Sink Current 50mA
SEG_ Source Current.....50mA
Maximum Current Input into Any Other Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 20.7mW/°C above +70°C).....1652.9mW
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
28-Pin PDIP (derate 14.3mW/°C above +70°C).....1142.9mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, GLED = 0, V_{LED} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference) C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Noise-Free Resolution		MAX1499	-19,999		+19,999	Count
		MAX1497	-1999		+1999	
Integral Nonlinearity (Note 1)	INL	2.000V range		±1		Count
		200mV range		±1		
Range Change Ratio		(V_{AIN+} - V_{AIN-} = 0.100V) on 200mV range (V_{AIN+} - V_{AIN-} = 0.100V) on 2.0V range		10:1		Ratio
Rollover Error		V_{AIN+} - V_{AIN-} = full scale V_{AIN-} - V_{AIN+} = full scale		±1		Count
Output Noise				10		μV_{P-P}
Offset Error (Zero Input Reading)	Offset	V_{IN} = 0 (Note 2)	-0		0	Reading
Gain Error		(Note 3)	-0.5		+0.5	%FSR
Offset Drift (Zero Reading Drift)		V_{IN} = 0 (Note 4)		0.1		µV/°C
Gain Drift				±1		ppm/°C
INPUT CONVERSION RATE						
External-Clock Frequency				4.9152		MHz
External-Clock Duty Cycle			40		60	%
Conversion Rate		Internal clock		5		Hz
		External clock, f_{CLK} = 4.9152MHz		5		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, GLED = 0, V_{LED} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference) C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS (AIN+, AIN-) (bypass to GND with 0.1µF or greater capacitors)						
AIN Input Voltage Range (Note 5)		RANGE bit = 0	-2.0		+2.0	V
		RANGE bit = 1	-0.2		+0.2	
AIN Absolute Input Voltage Range to GND			-2.2		+2.2	
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.9152MHz		120		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
LOW-BATTERY VOLTAGE MONITOR (LOWBATT) (MAX1499 only)						
LOWBATT TripThreshold				2.048		V
LOWBATT Leakage Current				10		pA
Hysteresis				20		mV
INTERNAL REFERENCE (REF- = GND, INTREF bit = 1) (bypass REF+ to GND with a 4.7µF capacitor)						
REF Output Voltage	V_{REF}	AV_{DD} = V_{DD} = 5V	2.007	2.048	2.089	V
REF Output Short-Circuit Current				1		mA
REF Output Temperature Coefficient	TC_{VREF}	AV_{DD} = V_{DD} = 5V		40		ppm/°C
Load Regulation		I_{SOURCE} = 0 to 300µA, I_{SINK} = 0 to 30µA		6		mV/µA
Line Regulation				50		µV/V
Noise Voltage		0.1Hz to 10Hz		25		$µV_{P-P}$
		10Hz to 10kHz		400		
EXTERNAL REFERENCE (INTREF bit = 0) (bypass REF+ and REF- to GND with 0.1µF or greater capacitors)						
REF Input Voltage		Differential (V_{REF+} - V_{REF-})		2.048		V
Absolute REF+, REF- Input Voltage to GND			-2.2		+2.2	
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.9152MHz		120		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, GLED = 0, V_{LED} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference) C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
CHARGE PUMP						
Output Voltage	VNEG	C_{VNEG} = 0.1µF	-2.60	-2.42	-2.30	V
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, CLK)						
Input Current	I_{IN}	V_{IN} = 0 or DV_{DD} = V_{DD}	-10		+10	µA
Input Low Voltage	V_{INL}	MAX1499			0.3 x DV_{DD}	V
		MAX1497			0.3 x V_{DD}	
Input High Voltage	V_{INH}	MAX1499	0.7 x DV_{DD}			V
		MAX1497	0.7 x V_{DD}			
Input Hysteresis	V_{HYS}	DV_{DD} = V_{DD} = 3.0V		200		mV
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA, MAX1499	0.8 x DV_{DD}			V
		I_{SOURCE} = 200µA, MAX1497	0.8 x V_{DD}			
Tri-State Leakage Current	I_L	DOUT only	-1		+1	µA
Tri-State Output Capacitance	C_{OUT}	DOUT only		15		pF
POWER SUPPLY (Note 10)						
V_{DD} Voltage	V_{DD}	MAX1497	2.70		5.25	V
AV_{DD} Voltage	AV_{DD}	MAX1499	2.70		5.25	V
DV_{DD} Voltage	DV_{DD}	MAX1499	2.70		5.25	V
Power-Supply Rejection V_{DD}	PSRR	(Note 7)		80		dB
Power-Supply Rejection AV_{DD}	$PSRR_A$	(Note 7)		80		dB
Power-Supply Rejection DV_{DD}	$PSRR_D$	(Note 7)		100		dB
V_{DD} Current (Notes 8, 9)	I_{VDD}	V_{DD} = 5.25V		664	744	µA
		V_{DD} = 3.3V		618	663	
		Standby mode		268	325	
AV_{DD} Current (Notes 8, 9)	I_{AVDD}	AV_{DD} = 5.25V			640	µA
		AV_{DD} = 3.3V			600	
		Standby mode			305	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, GLED = 0, V_{LED} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference) C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DV_{DD} Current (Notes 8, 9)	I_{DVDD}	DV_{DD} = 5V			320	µA
		DV_{DD} = 3.3V			180	
		Standby mode			20	
LED Drivers Bias Current		From AV_{DD} or V_{DD}		120		µA
LED DRIVERS (Table 6)						
LED Supply Voltage	V_{LED}		2.70		5.25	V
LED Shutdown Supply Current	I_{SHDN}	LED driver shutdown mode			10	µA
LED Supply Current	I_{LED}	Seven segments and decimal point on, R_{ISET} = 25kΩ		176		mA
Display Scan Rate	f_{OSC}	MAX1499		512		Hz
		MAX1497		640		
Segment Current Slew Rate	$\Delta I_{SEG}/\Delta t$			25		mA/µs
DIG_ Voltage Low	V_{DIG}	$I_{DIG_}$ = 176mA		0.178	0.300	V
Segment Drive Source Current Matching	ΔI_{SEG}			±3	±10	%
Segment Drive Source Current	I_{SEG}	V_{LED} - V_{SEG} = 0.6V, R_{ISET} = 25kΩ	16	20	25.5	mA
Interdigit Blanking Time				4		µs

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

TIMING CHARACTERISTICS (Notes 11, 12, Figure 8)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, GLED = 0, V_{LED} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference) C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Operating Frequency	f_{SCLK}		0		4.2	MHz
SCLK Pulse-Width High	t_{CH}		100			ns
SCLK Pulse-Width Low	t_{CL}		100			ns
DIN to SCLK Setup	t_{DS}		50			ns
DIN to SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		50			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 50pF, Figures 13, 14			120	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 50pF, Figures 13, 14			120	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 50pF, Figures 13, 14			120	ns

Note 1: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after nulling the gain error and offset error.

Note 2: Offset calibrated. See $\overline{OFFSET_CAL1}$ and OFFSET_CAL2 (MAX1499 only) in the *On-Chip Registers* section.

Note 3: Offset nulled.

Note 4: Offset drift error is eliminated by recalibration at the new temperature.

Note 5: The input voltage range for the analog inputs is given with respect to the voltage on the negative input of the differential pair.

Note 6: V_{AIN+} or V_{AIN-} = -2.2V to +2.2V. V_{REF+} or V_{REF-} = -2.2V to +2.2V. All input structures are identical. Production tested on AIN+ and REF+ only.

Note 7: Measured at DC by changing the power-supply voltage from 2.7V to 5.25V and measuring the effect on the conversion error with external reference. PSRR at 50Hz and 60Hz exceeds 120dB with filter notches at 50Hz and 60Hz (Figure 2).

Note 8: CLK and SCLK are disabled.

Note 9: LED drivers are disabled.

Note 10: Power-supply currents are measured with all digital inputs at either GND, DV_{DD}, or V_{DD} and with the device in internal-clock mode.

Note 11: All input signals are specified with t_{RISE} = t_{FALL} = 5ns (10% to 90% of DV_{DD}) and are timed from a voltage level of 50% of DV_{DD}, unless otherwise noted.

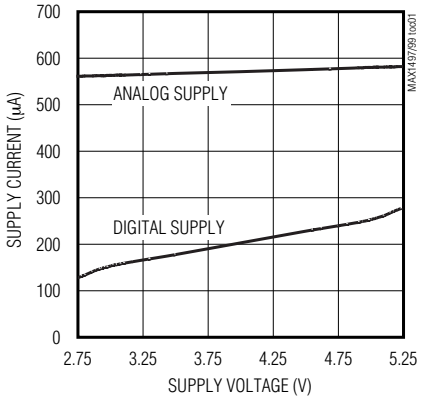
Note 12: See the serial-interface timing diagrams.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

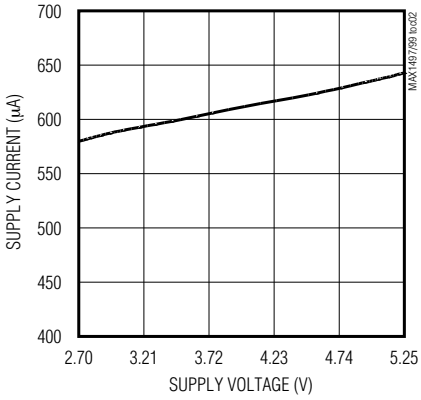
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, V_{LED} = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, C_{REF+} = C_{REF-} = 0.1µF, RANGE bit = 1, internal clock mode, C_{VNEG} = 0.1µF. T_A = +25°C, unless otherwise noted.)

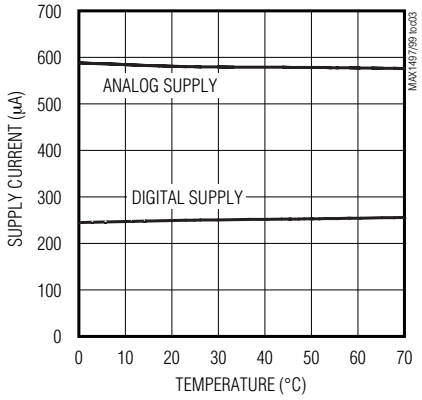
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1499)



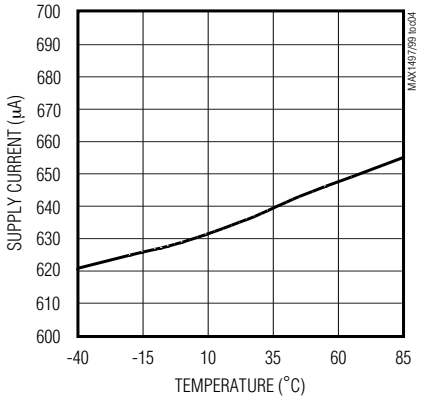
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1497)



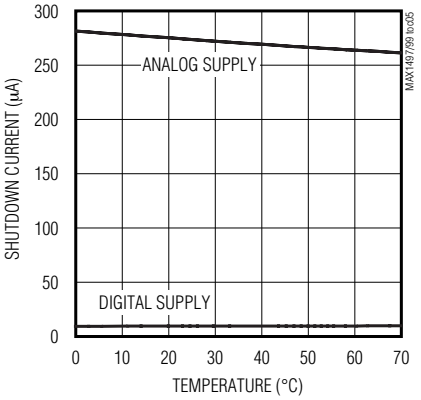
SUPPLY CURRENT vs. TEMPERATURE (MAX1499)



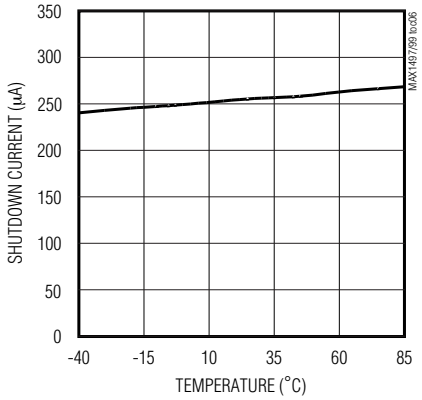
SUPPLY CURRENT vs. TEMPERATURE (MAX1497)



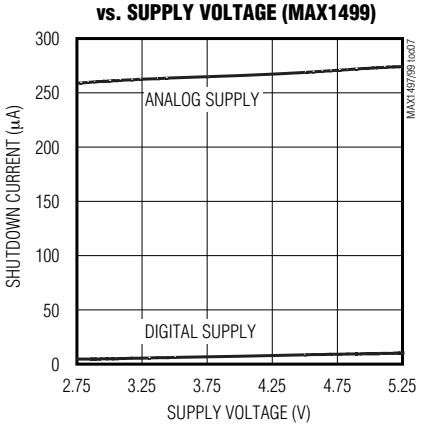
SHUTDOWN CURRENT vs. TEMPERATURE (MAX1499)



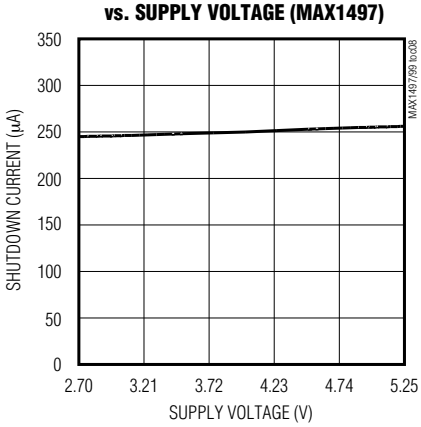
SHUTDOWN CURRENT vs. TEMPERATURE (MAX1497)



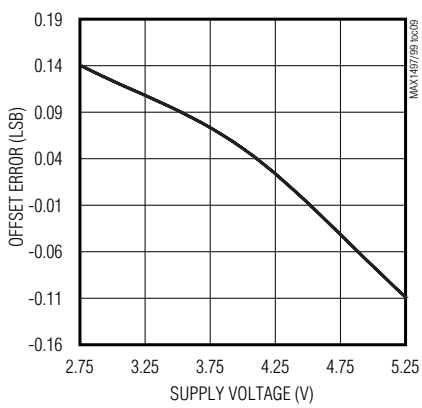
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE (MAX1499)



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE (MAX1497)



MAX1499 OFFSET ERROR vs. SUPPLY VOLTAGE

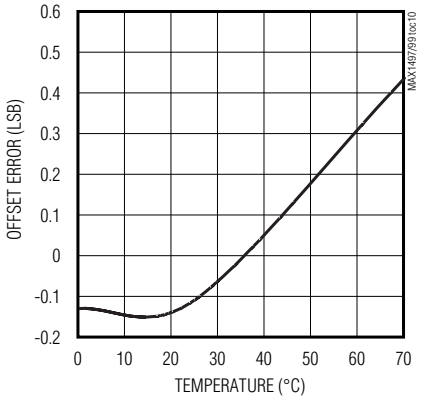


3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

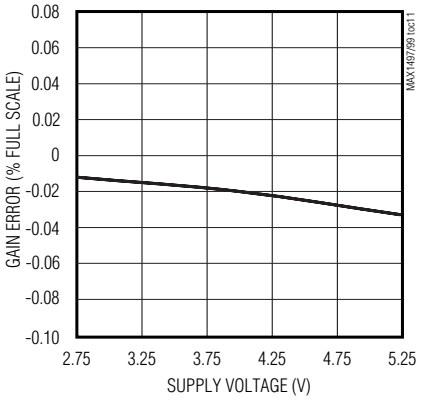
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, V_{LED} = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, C_{REF+} = C_{REF-} = 0.1µF, RANGE bit = 1, internal clock mode, C_{VNEG} = 0.1µF. T_A = +25°C, unless otherwise noted.)

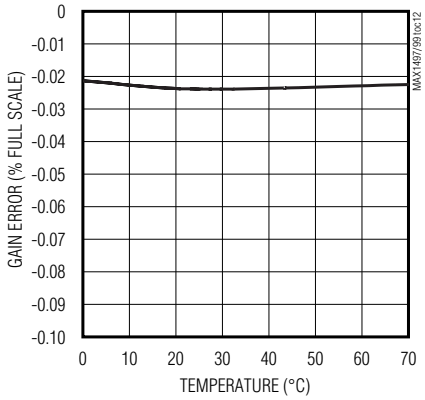
MAX1499
OFFSET ERROR vs. TEMPERATURE



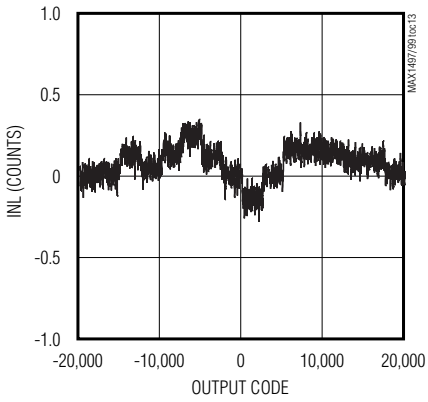
MAX1499
GAIN ERROR vs. SUPPLY VOLTAGE



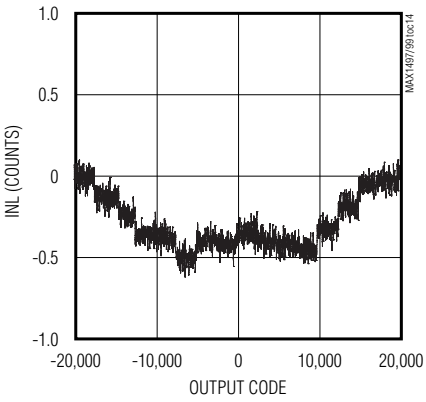
MAX1499
GAIN ERROR vs. TEMPERATURE



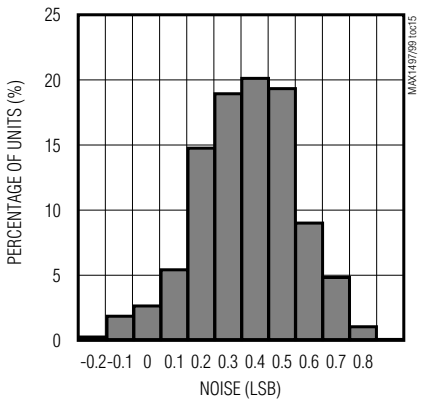
MAX1499
(±200mV INPUT RANGE) INL vs. OUTPUT CODE



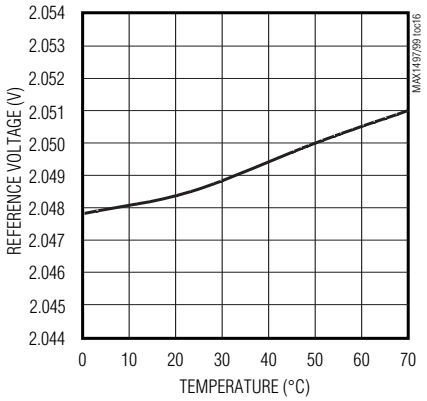
MAX1499
(±2V INPUT RANGE) INL vs. OUTPUT CODE



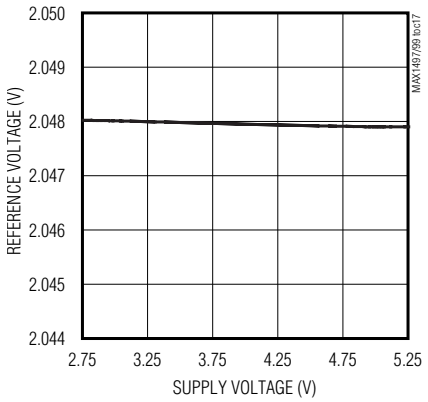
NOISE DISTRIBUTION



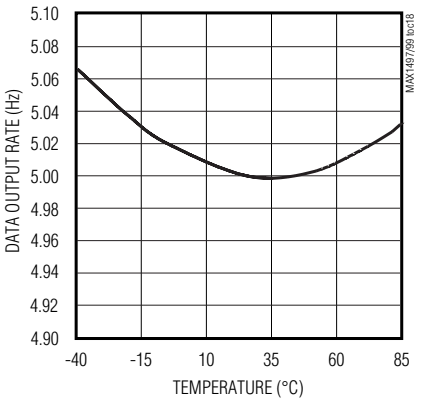
INTERNAL REFERENCE VOLTAGE
vs. TEMPERATURE



INTERNAL REFERENCE VOLTAGE
vs. ANALOG SUPPLY VOLTAGE



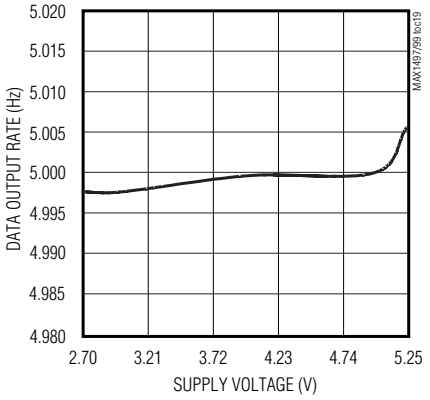
DATA OUTPUT RATE
vs. TEMPERATURE



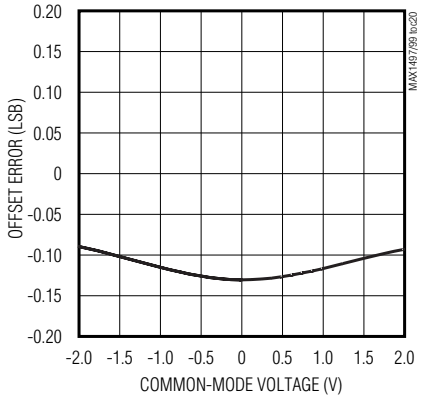
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, V_{LED} = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, C_{REF+} = C_{REF-} = 0.1µF, RANGE bit = 1, internal clock mode, C_{VNEG} = 0.1µF. T_A = +25°C, unless otherwise noted.)

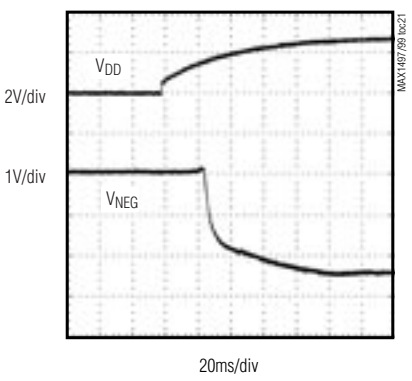
DATA OUTPUT RATE vs. SUPPLY VOLTAGE



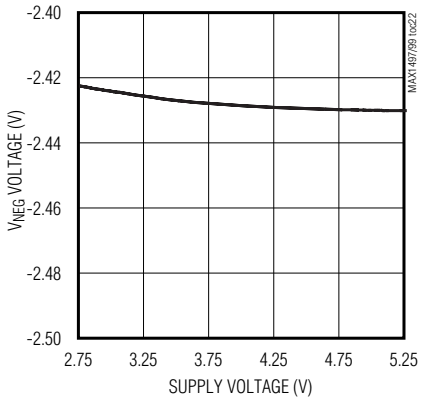
OFFSET ERROR vs. COMMON-MODE VOLTAGE



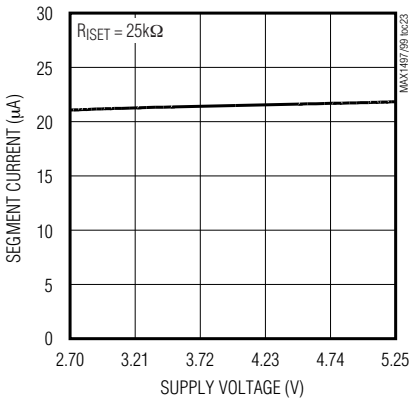
V_{NEG} STARTUP SCOPE SHOT



CHARGE-PUMP OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



SEGMENT CURRENT vs. SUPPLY VOLTAGE



3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Pin Description

PIN		NAME	FUNCTION
MAX1497	MAX1499		
1	31	VNEG	-2.5V Charge-Pump Voltage-Output. Connect a 0.1µF capacitor to GND.
2	32	REF-	Negative Reference Voltage Input. For internal reference operation, connect REF- to GND. For external reference operation, bypass REF- to GND with a 0.1µF capacitor and set V_{REF-} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
3	1	REF+	Positive Reference Voltage Input. For internal reference operation, connect a 4.7µF capacitor from REF+ to GND. For external reference operation, bypass REF+ to GND with a 0.1µF capacitor and set V_{REF+} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
4	2	AIN+	Positive Analog Input. Positive side of fully differential analog input. Bypass AIN+ to GND with a 0.1µF or greater capacitor.
5	3	AIN-	Negative Analog Input. Negative side of fully differential analog input. Bypass AIN- to GND with a 0.1µF or greater capacitor.
6	4	I_{SET}	Segment Current Controller. Connect to ground through a resistor to set the segment current. See Table 6 for segment current selection.
7	5	GND	Ground
8	—	V_{DD}	Analog and Digital Circuit Supply Voltage. Connect V_{DD} to a +2.7V to +5.25V power supply. Bypass V_{DD} to GND with a 0.1µF and a 4.7µF capacitor.
9	8	CLK	External Clock Input. When the EXTCLK register bit is set to one, CLK is the master clock input (frequency = 4.9152MHz) for the modulator and the filter. When the EXTCLK register bit is reset to zero, the internal clock is used. Connect CLK to GND or DV_{DD} (MAX1499) or V_{DD} (MAX1497) when the internal oscillator is used.
10	9	$\overline{EOC}$	Active-Low End-of-Conversion Logic Output. A logic low at EOC indicates that a new ADC result is available in the ADC result register.
11	10	$\overline{CS}$	Active-Low Chip Select Input. Forcing $\overline{CS}$ low activates the serial interface.
12	11	DIN	Serial Data Input. Data present at DIN is shifted into the internal registers in response to a rising edge at SCLK when $\overline{CS}$ is low.
13	12	SCLK	Serial Clock Input. Apply an external clock to SCLK to facilitate communication through the serial bus. SCLK may idle high or low.
14	13	DOUT	Serial Data Output. DOUT presets serial data in response to register queries. Data shifts out on the falling edge of SCLK. DOUT goes high impedance when $\overline{CS}$ is high.
15	14	DIG0	Digit 0 Driver
16	15	DIG1	Digit 1 Driver
17	16	GLED	Ground for LED-Display Segment Driver
18	17	DIG2	Digit 2 Driver
19	18	DIG3	Digit 3 Driver
20	20	SEGA	Segment A Driver
21	21	SEGB	Segment B Driver
22	22	SEGC	Segment C Driver
23	23	SEGD	Segment D Driver
24	24	SEGE	Segment E Driver

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1497	MAX1499		
25	25	VLED	LED-Display Segment-Driver Supply. Connect to a +2.7V to +5.25V supply. Bypass with a 0.1µF capacitor to GLED.
26	26	SEGF	Segment F Driver
27	27	SEGG	Segment G Driver
28	28	SEGDP	Segment DP Driver
—	6	AV_{DD}	Analog Positive Supply Voltage. Connect AV_{DD} to a +2.7V to +5.25V power supply. Bypass AV_{DD} to GND with a 0.1µF capacitor.
—	7	DV_{DD}	Digital Positive Supply Voltage. Connect DV_{DD} to a +2.7V to +5.25V power supply. Bypass DV_{DD} to GND with a 0.1µF capacitor.
—	19	DIG4	Digit 4 Driver
—	29	LED_EN	Active-High LED Enable. The MAX1499 LED display driver turns off when LED_EN is driven to logic low. The MAX1499 LED display driver turns on when LED_EN is driven to logic high.
—	30	LOWBATT	Low-Battery Voltage Monitor. When the LOWBATT input voltage is lower than 2.048V, the LOWBATT bit in the status register is set to one.

Detailed Description

The MAX1497/MAX1499 low-power, highly integrated ADCs with LED drivers convert a ±2V differential input voltage (one count is equal to 100µV for the MAX1499 and 1mV for the MAX1497) with a sigma-delta ADC and output the result to an LED or µC. An additional ±200mV input range (one count is equal to 10µV for the MAX1499 and 100µV for the MAX1497) is available to measure small signals with increased resolution.

The devices operate from a single 2.7V to 5.25V power supply and offer 3.5-digit (MAX1497) or 4.5-digit (MAX1499) conversion results. An internal 2.048V reference, internal charge pump, and a high-accuracy on-chip oscillator eliminate external components.

The MAX1497/MAX1499 interface with a µC using an SPI-/QSPI-/MICROWIRE-compatible serial interface. Data can either be sent directly to the display or to the µC first for processing before being displayed.

The devices also feature on-chip buffers for the differential input signal and external reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset-calibration and offer >100dB of 50Hz and 60Hz line noise rejection. Other features include data hold and peak detection, overrange and underrange detection. The MAX1499 also provides a low-battery monitor.

Analog Input Protection

Internal protection diodes limit the analog input range from VNEG to (AV_{DD} + 0.3V) for the MAX1499, and from VNEG to (V_{DD} to 0.3V) for the MAX1497. If the analog input exceeds this range, limit the input current to 10mA.

Internal Analog Input/Reference Buffers

The MAX1497/MAX1499 analog input/reference buffers allow the use of high-impedance signal sources. The input buffers' common-mode input range allows the analog inputs and the reference to range from -2.2V to +2.2V.

Modulator

The MAX1497/MAX1499 perform analog-to-digital conversions using a single-bit, 3rd-order, sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input.

The MAX1497/MAX1499 modulator provides 3rd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. A single-bit data stream is then presented to the digital filter to remove the frequency-shaped quantization noise.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

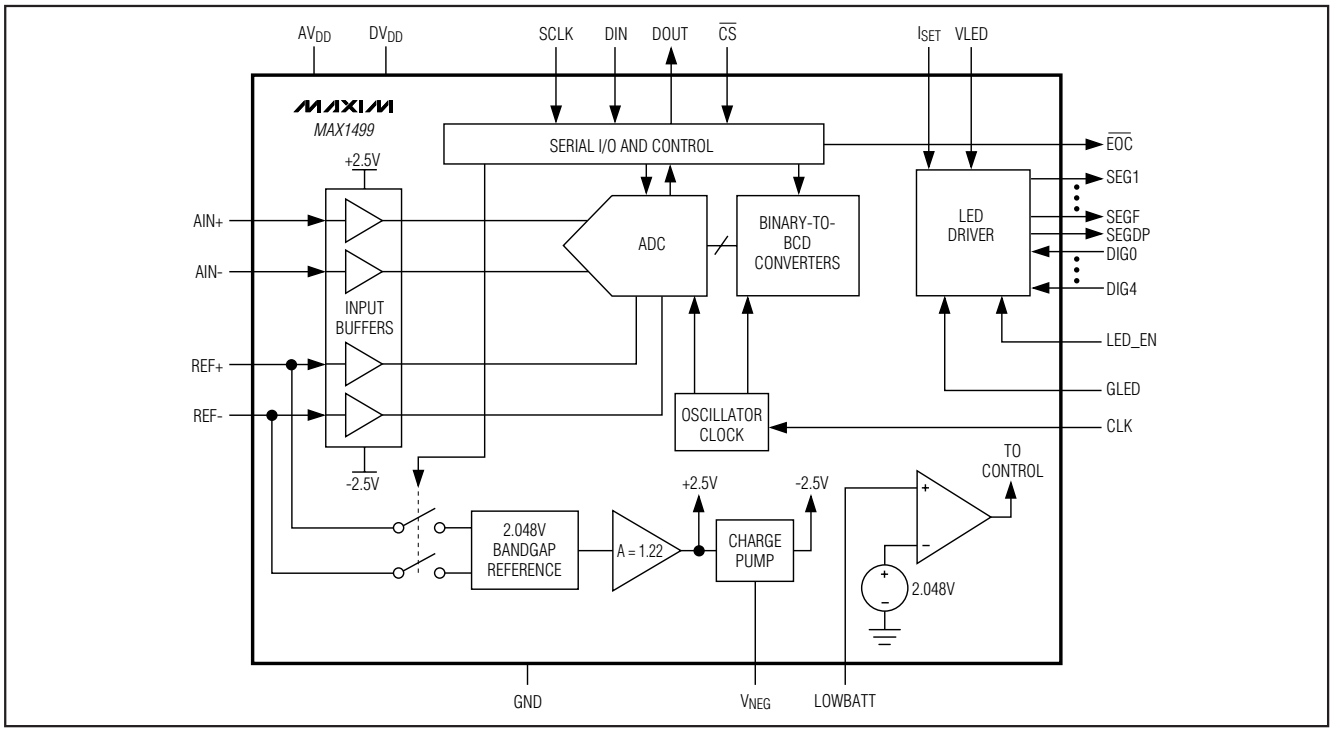


Figure 1. MAX1499 Functional Diagram

Digital Filtering

The MAX1497/MAX1499 contain an on-chip digital low-pass filter that processes the data stream from the modulator using a SINC^4 response:

$$\left(\frac{\sin(x)}{x}\right)^4$$

The SINC^4 filter has a settling time of four output data periods (4 x 200ms).

The MAX1497/MAX1499 have 25% overrange capability built into the modulator and digital filter. The digital filter is optimized for the f_{CLK} equal to 4.9152MHz. Other clock frequencies can be used; however, 50Hz/60Hz noise rejection decreases. The frequency response of the SINC^4 filter is calculated as follows:

$$H(z) = \left[\frac{1}{N}\frac{(1 - Z^{-N})}{(1 - Z^{-1})}\right]^4$$

$$H(f) = \frac{1}{N}\left[\frac{\sin\left(N\pi\frac{f}{f_m}\right)}{\sin\left(\frac{\pi f}{f_m}\right)}\right]^4$$

where N is the oversampling ratio, and f_m = N x output data rate = 5Hz.

Filter Characteristics

Figure 2 shows the filter frequency response. The SINC^4 characteristic -3dB cutoff frequency is 0.228 times the first notch frequency (5Hz). The oversampling ratio (OSR) for the MAX1497 is 128 and the OSR for the MAX1499 is 1024.

The output data rate for the digital filter corresponds to the positioning of the first notch of the filter's frequency response. The notches of the SINC^4 filter are repeated at multiples of the first notch frequency. The SINC^4 filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to 10 times the first notch frequency and 60Hz is equal to 12 times the first notch frequency.

For large step changes at the input, allow a settling time of 800ms before valid data is read.

Clock Modes

Configure the MAX1497/MAX1499 to use either the internal oscillator or an externally applied clock to drive the modulator and filter. Set the EXTCLK bit in the control register to zero to put the device in internal-clock mode. Set the EXTCLK bit to one to put the device in

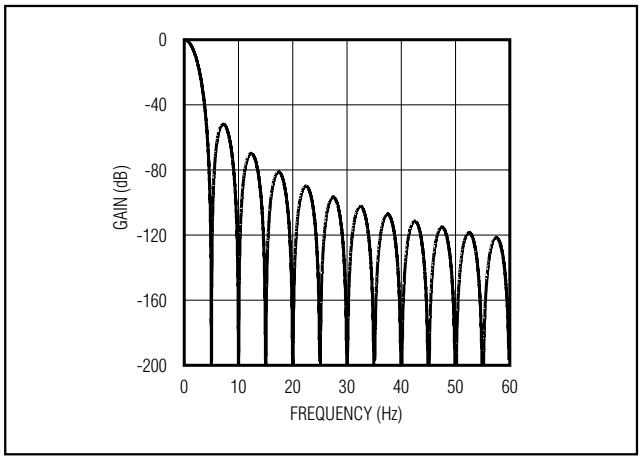


Figure 2. Frequency Response of the SINC^4 Filter (Notch at 60Hz)

external-clock mode. When using the internal oscillator, connect CLK to GND or DV_{DD} for the MAX1499, or connect CLK to V_{DD} for the MAX1497. The MAX1497/MAX1499 ideally operate with a 4.9152MHz clock to achieve maximum rejection of 50Hz/60Hz common-mode, power-supply, and normal-mode noise.

Internal-Clock Mode

The MAX1497/MAX1499 contain an internal oscillator. The power-up condition for the MAX1497/MAX1499 is internal clock operation with the EXTCLK bit in the control register equal to zero. Using the internal oscillator saves board space by removing the need for an external clock source.

External-Clock Mode

For external clock operation, set the EXTCLK bit in the control register to one and drive CLK with a 4.9152MHz clock source for best 50Hz/60Hz rejection ratio. Other external clock frequencies allow for custom conversion rates. A 2.4576MHz clock signal reduces the conversion rate and the LED update rate by a factor of two while keeping good 50Hz/60Hz noise rejection. The MAX1497/MAX1499 operate with an external clock source of up to 5.05MHz.

Charge Pump

The MAX1497/MAX1499 contain an internal charge pump to provide the negative supply voltage for the internal analog input/reference buffers. The bipolar input range of the analog input/reference buffers allows this device to accept negative inputs with high source impedances. Connect a 0.1µF capacitor from VNEG to GND.

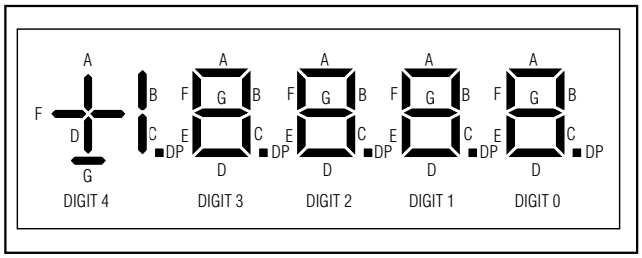


Figure 3. Segment Connection for the MAX1499 (4.5 Digits)

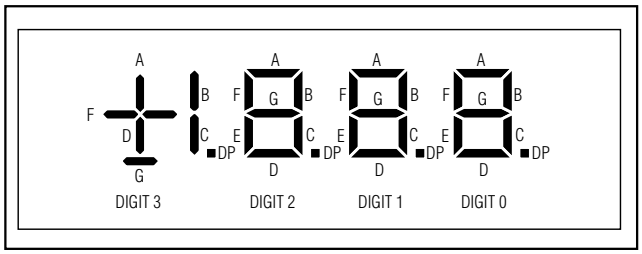


Figure 4. Segment Connection for the MAX1497 (3.5 Digits)

Table 1. LED Priority Table

SEG_SEL	SPI/$\overline{ADC}$	HOLD	PEAK	DISPLAY VALUES FORM
1	X	X	X	LED segment registers
0	1	X	X	LED display register (user written)
0	0	1	X	LED display register
0	0	0	1	Peak register
0	0	0	0	ADC result register

X = *Don't care.*

LED Driver

The MAX1499 has a 4.5-digit common-cathode display driver and the MAX1497 has a 3.5-digit common-cathode display driver. Figures 3 and 4 show the connection schemes for a standard seven-segment LED display. The LED update rate is 2.5Hz. The MAX1497/MAX1499 automatically display the results of the ADC, if desired (Table 1). The MAX1497/MAX1499 also allow independent control of the LED driver through the serial interface, allowing for data processing of the ADC result before showing the result on the LED. Additionally, each LED segment can be individually controlled (see the LED segment-display register sections).

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Table 2. Decimal-Point Control Table—MAX1499

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	0	18888	0
0	0	1	18888	0
0	1	0	18888	0
0	1	1	18888	0
1	0	0	1888.8	0.0
1	0	1	188.88	0.00
1	1	0	18.888	0.000
1	1	1	1.8888	0.0000

Table 3. Decimal-Point Control Table—MAX1497

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
X	0	0	188.8	0.0
X	0	1	18.88	0.00
X	1	0	1888	0
X	1	1	1.888	0.000

X = *Don't care.*

Table 4. LED During Overrange and Underrange Conditions

CONDITION	MAX1497	MAX1499
Overrange	1---	1----
Underrange	-1---	-1----

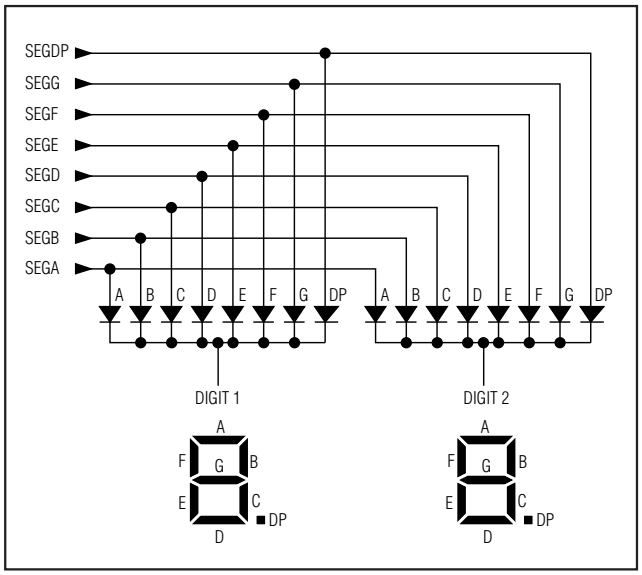


Figure 5. Two-Digit Common-Cathode Configuration

Figure 5 shows a typical common-cathode configuration for two digits. In common-cathode configuration, the cathodes of all LEDs in a digit are connected together. Each segment driver of the MAX1497/MAX1499 connects to its corresponding LEDs anodes. For example, segment driver SEGA connects to all LED segments designated as A. Similar configurations are followed for other segment drivers.

The MAX1497/MAX1499 use a multiplexing scheme to drive one digit at a time. The scan rate is fast enough to make the digits appear to be lit. Figures 6 and 7 show data timing diagrams for the MAX1497/MAX1499 where T is the display scan period typically around 1/512Hz or 1.9531ms for the MAX1499 and 1/640Hz or 1.5625ms for the MAX1497. T_{ON} in Figures 6 and 7 denotes the amount of time each digit is on and is calculated as follows:

$$T_{ON} = \frac{T}{5} = \frac{1.95312ms}{5} = 390.60\mu s \quad (MAX1499)$$

$$T_{ON} = \frac{T}{4} = \frac{1.5625ms}{4} = 390.60\mu s \quad (MAX1497)$$

The MAX1497/MAX1499 allow for full decimal-point control and feature leading-zero suppression. Use the DPON, DPSET1, and DPSET2 bits in the control register to set the value of the decimal point (Tables 2 and 3). The MAX1497/MAX1499 overrange and underrange display is shown in Table 4.

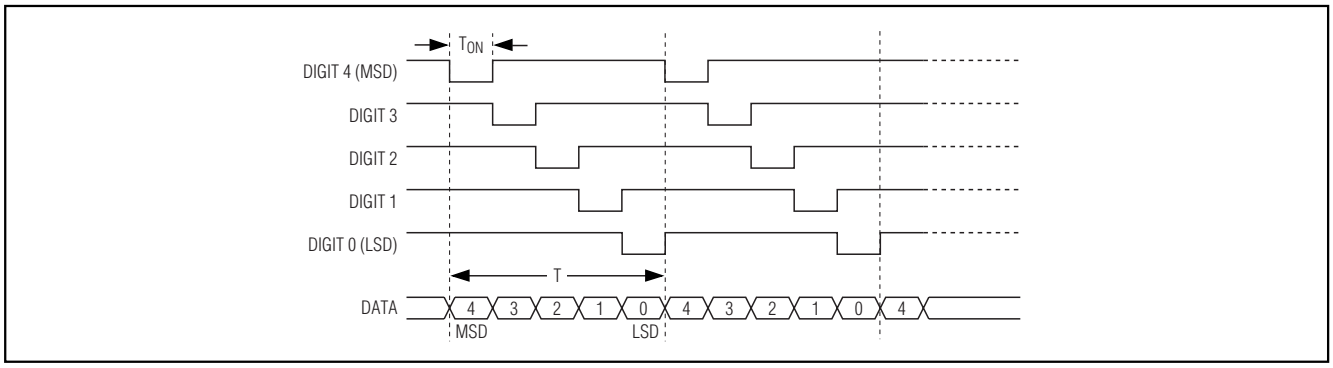


Figure 6. LED Voltage Waveform—MAX1499

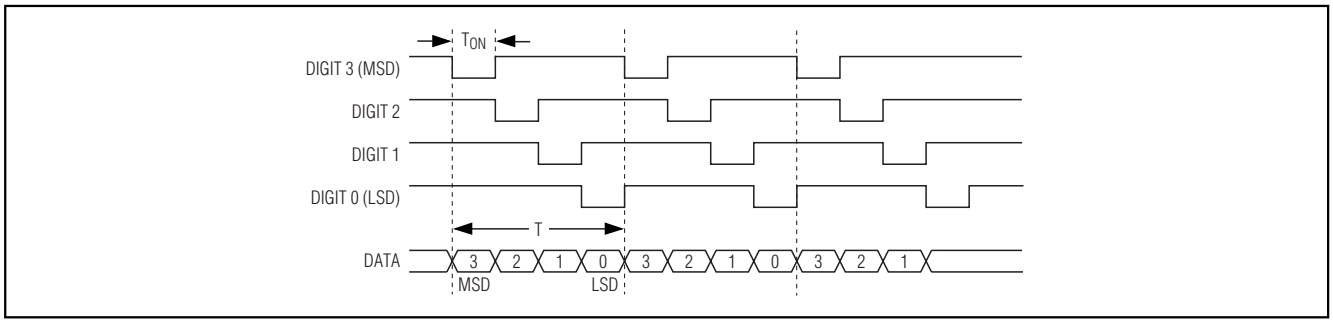


Figure 7. LED Voltage Waveform—MAX1497

Leading-Zero Suppression

The MAX1497/MAX1499 include a leading-zero suppression circuitry to turn off unnecessary zeros. For example, when DPSET1 and DPSET2 = [0,0], 0.0 is displayed instead of 000.0. This feature saves a substantial amount of power from being wasted.

Interdigit Blanking

The MAX1497/MAX1499 also include an interdigit blanking circuitry. Without this feature, it is possible to see a faint digit next to a digit that is completely on. The interdigit blanking circuitry prevents bleeding over into the next digit for a short period of time. The typical interdigit blanking time is 4µs.

Reference

The MAX1497/MAX1499 reference sets the full-scale range of the ADC transfer function. With a nominal 2.048V reference, the ADC full-scale range is ±2V with the RANGE bit equal to zero. With the RANGE bit set to one, the full-scale range is ±200mV. A decreased reference voltage decreases full-scale range (see the *Transfer Functions* section).

The MAX1497/MAX1499 accept either an external reference or an internal reference. The INTREF bit selects the reference mode (see the *Control Register (Read/Write)* section).

For internal reference operation, set the INTREF bit to one, connect REF- to GND, and bypass REF+ to GND with a 4.7µF capacitor. The internal reference provides a nominal 2.048V source between REF+ and GND. The internal reference temperature coefficient is typically 40ppm/°C.

The default power-on state sets the MAX1497/MAX1499 to use the external reference with the INTREF bit cleared to zero. The external reference inputs, REF+ and REF-, are fully differential. For a valid external reference input, V_{REF+} must be greater than V_{REF-}. Bypass REF+ and REF- with a 0.1µF or greater capacitor to GND in external reference mode.

Figure 16 shows the MAX1497/MAX1499 operating with an external single-ended reference. In this mode, REF- is connected to GND and REF+ is driven with an external 2.048V reference. Bypass REF+ to GND with a 0.47µF capacitor.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Figure 15 shows the MAX1497/MAX1499 operating with an external differential reference. In this mode, REF- is connected to the top of the strain gauge and REF+ is connected to the midpoint of the resistor-divider of the supply.

Applications Information

Serial Interface

The SPI/QSPI/MICROWIRE serial interface consists of a chip select ($\overline{CS}$), a serial clock (SCLK), a data in (DIN), a data out (DOUT), and an asynchronous $\overline{EOC}$ output. $\overline{EOC}$ provides an asynchronous end-of-conversion signal with a period of 200ms (f_{CLK} = 4.9152MHz). The MAX1497 updates the data register when $\overline{EOC}$ goes high. Data is valid in the ADC result registers when $\overline{EOC}$ returns low. The serial interface provides access to 12 on-chip registers, allowing control to all the power modes and functional blocks. Table 5 lists the address and read/write accessibility of all the registers.

A logic high on $\overline{CS}$ tri-states DOUT and causes the MAX1497/MAX1499 to ignore any signals on SCLK and DIN. To clock data in or out of the internal shift register, drive $\overline{CS}$ low. SCLK synchronizes the data transfer. The rising edge of SCLK clocks DIN into the shift register, and the falling edge of SCLK clocks DOUT out of the shift register. DIN and DOUT are transferred MSB first (data is left justified). Figures 8–12 show the detailed serial interface timing diagrams for the 8- and 16-bit read/write operations.

All communication with the MAX1497/MAX1499 begins with a command byte on DIN, where the first logic one on DIN is recognized as the START bit (MSB) for the command byte. The following seven clock cycles load the command into a shift register. These 7 bits specify which of the registers are accessed next, and whether a read or write operation takes place. Transitions on the serial clock after the command byte transfer, cause a write or read from the device until the correct number of

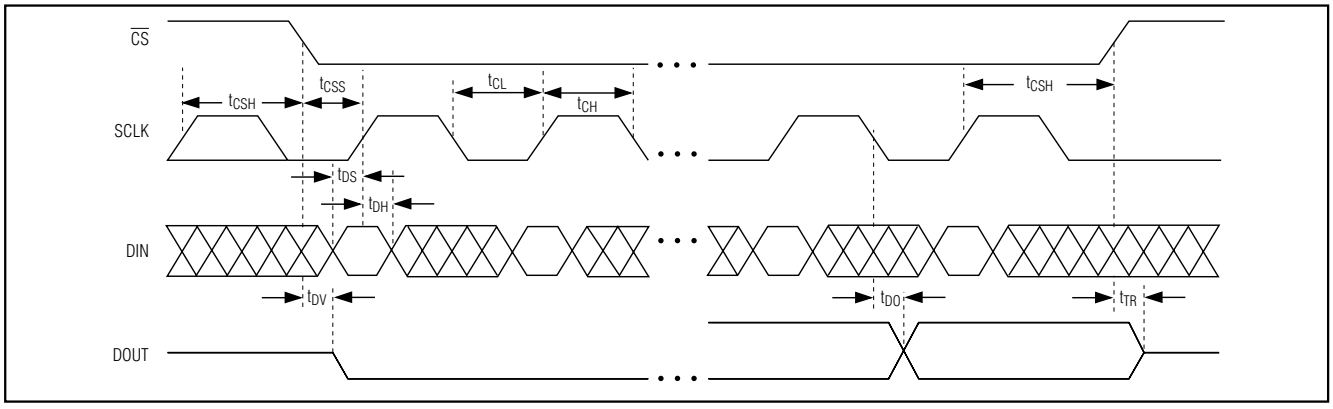


Figure 8. Detailed Timing Diagram

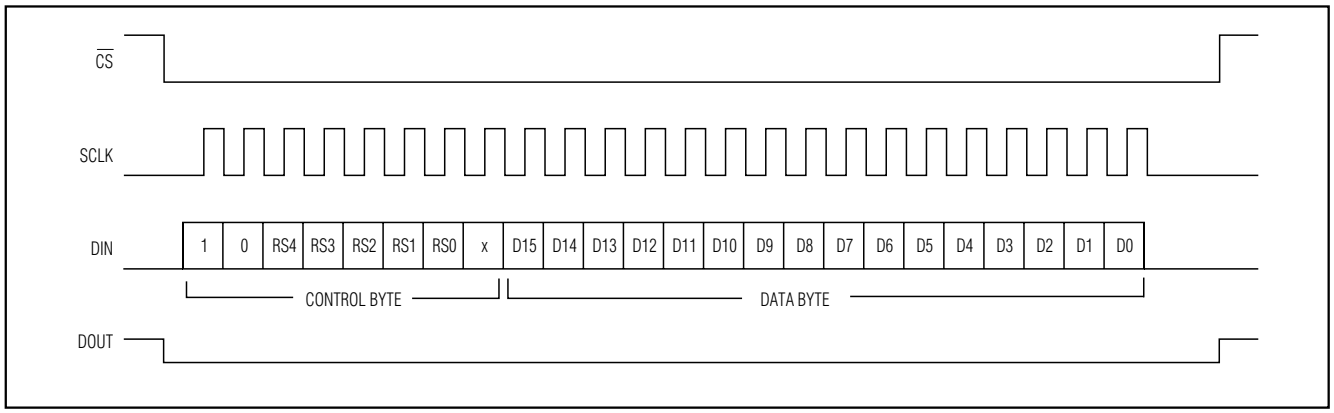


Figure 9. Serial-Interface, 16-Bit, Write Timing Diagram

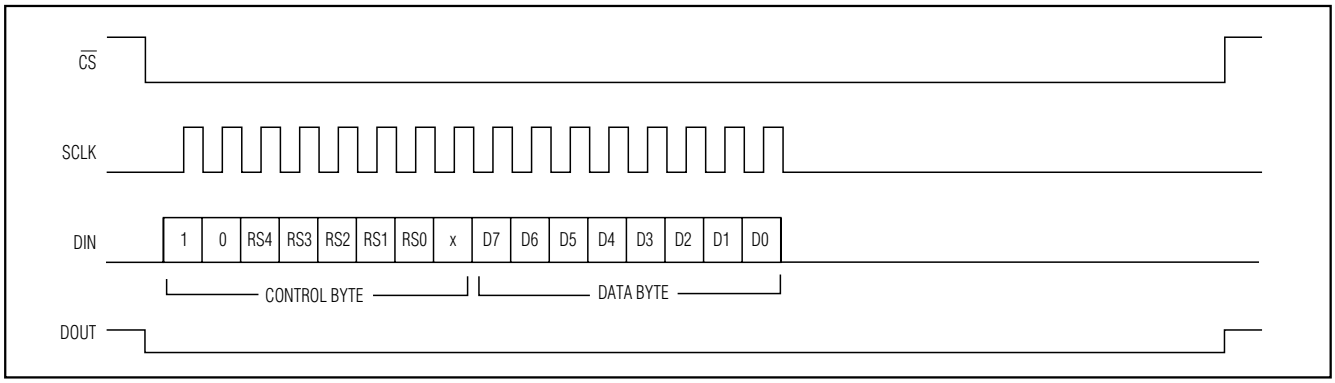


Figure 10. Serial-Interface, 8-Bit, Write Timing Diagram

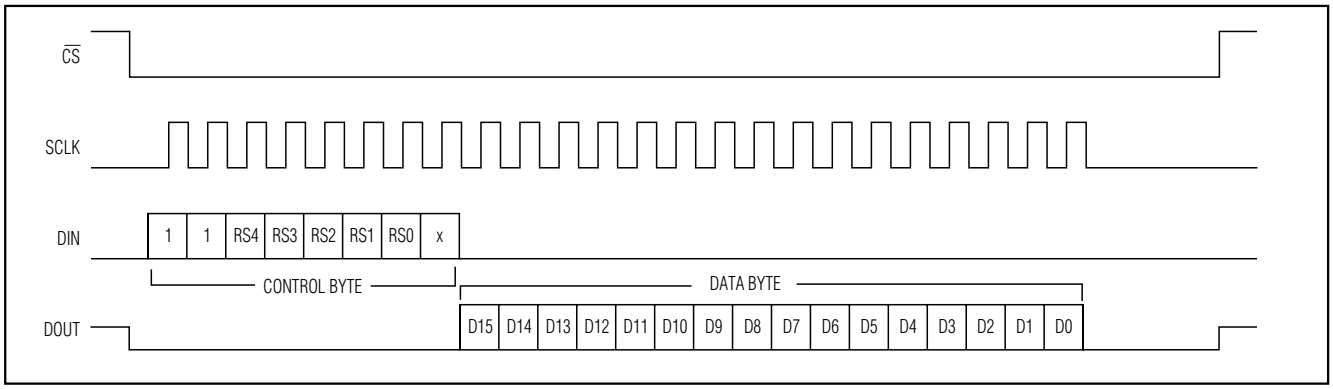


Figure 11. Serial-Interface, 16-Bit, Read Timing Diagram

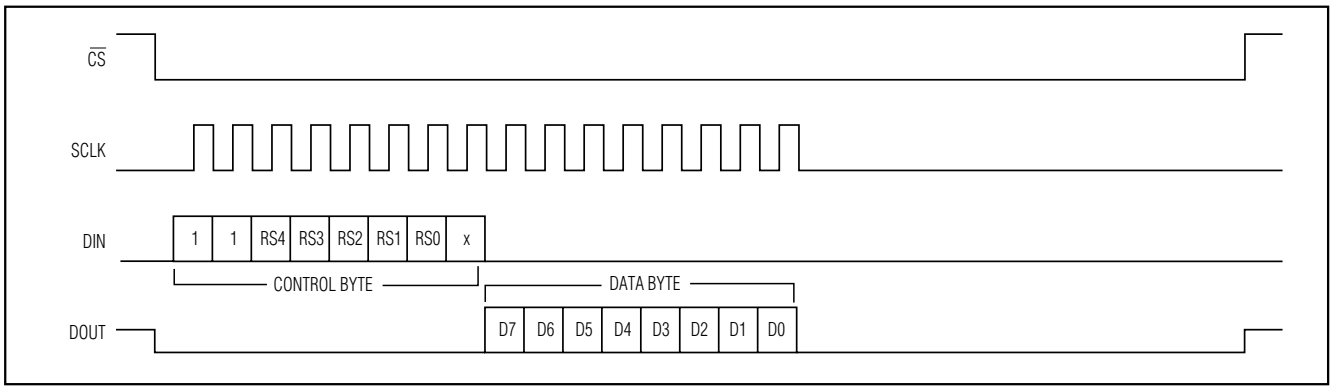


Figure 12. Serial-Interface, 8-Bit, Read Timing Diagram

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Table 5. Register Address Table

REGISTER N0.	ADDRESS RS [4:0]	NAME	WIDTH	ACCESS
1	00000	Status register	8	Read only
2	00001	Control register	16	R/$\overline{W}$
3	00010	Overrange register	16	R/$\overline{W}$
4	00011	Underrange register	16	R/$\overline{W}$
5	00100	LED segment-display register 1	16	R/$\overline{W}$
6	00101	LED segment-display register 2	16	R/$\overline{W}$
7	00110	LED segment-display register 3	8	R/$\overline{W}$
8	00111	ADC custom offset register	16	R/$\overline{W}$
9	01000	ADC result register 1 (16 MSBs)	16	Read only
10	01001	LED data register	16	R/$\overline{W}$
11	01010	Peak register	16	Read only
12	10100	ADC result register 2 (4 LSBs)	8	Read only
—	All other addresses	Reserved	—	—

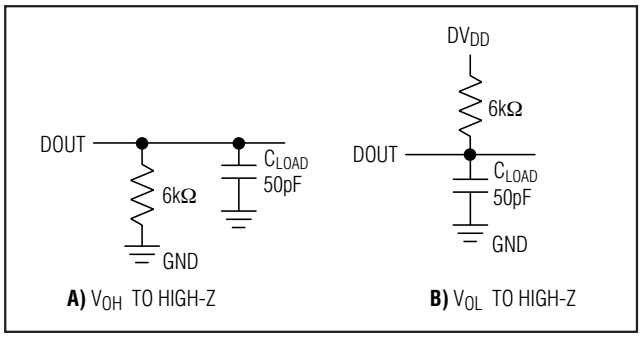


Figure 13. Load Circuits for Disable Time

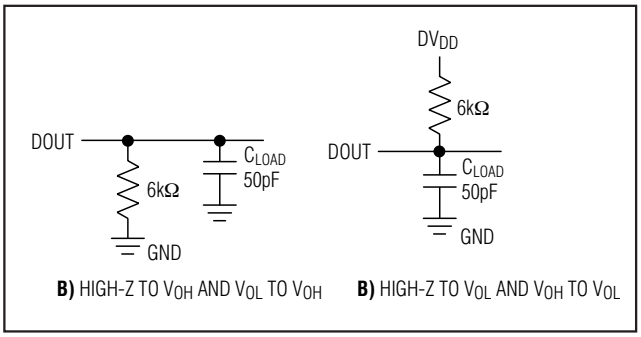


Figure 14. Load Circuits for Enable Time

bits have been transferred (8 or 16). Once this has occurred, the MAX1497/MAX1499 wait for the next command byte. $\overline{CS}$ must not go high between data transfers. If $\overline{CS}$ is toggled before the end of a write or read operation, the device mode may be unknown. Clock in 32 zeros to clear the device state and reset the interface so it is ready to receive a new command byte.

On-Chip Registers

The MAX1497/MAX1499 contain 12 on-chip registers. These registers configure the various functions of the device and allow independent reading of the ADC results and writing to the LED display. Table 5 lists the address and size of each register.

The first of these registers is the status register. The 8-bit status register contains the status flags for the ADC. The second register is the 16-bit control register. This register sets the LED display controls, range modes, power-down modes, offset calibration, and the reset register function (CLR). The third register is the 16-bit overrange register, which sets the overrange limit of the analog input. The fourth register is the 16-bit underrange register, which sets the underrange limit of the analog input. Registers 5 through 7 contain the display data for the individual segments of the LED. The eighth register contains the custom offset value. The ninth register contains the 16 MSBs of the ADC conversion result. The 10th register contains the LED data. The 11th register contains the peak analog input value. The last register contains the lower four LSBs of the 20-bit ADC conversion result.

Control and Status Registers

Command Byte (Write Only)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
START(1)	R/$\overline{W}$	RS4	RS3	RS2	RS1	RS0	X

START: Start bit. The first 1 clocked into the MAX1497/MAX1499 is the first bit of the command byte.

(R/$\overline{W}$): Read/$\overline{Write}$. Set this bit to 1 to read from the specified register. Set this bit to zero to write to the selected register. Note that certain registers are read only. Write commands to a read-only register are ignored.

(RS4–RS0): Register address bits. RS4 to RS0 specify which register is accessed.

X: Don't care.

Status Register (Read Only)

MSB							LSB
SIGN	OVER	UNDER	LOW_BATT	DRDY	0	0	0

Default values: 00h

This register contains the status of the conversion results.

SIGN: Latched negative-polarity indicator. Latches high when the result is negative. Clears by reading the status register, unless the condition remains true.

OVER: Overrange bit. Latches high if an overrange condition occurs (the ADC result is larger than the value in the overrange register). Clears by reading the status register, unless the condition remains true.

UNDER: Underrange bit. Latches high if an underrange condition occurs (the ADC result is less than the value in the underrange register). Clears by reading the status register, unless the condition remains true.

LOW_BATT: Low-battery bit. Latches high if the voltage at the LOWBATT is lower than 2.048V (typ). Clears by reading the status register, unless the condition remains true. For the MAX1497, LOWBATT is not used and the LOWBATT bit always returns to zero.

DRDY: Data ready bit. Latches high to indicate a completed conversion result with valid data. Read the ADC result register to clear this bit.

Control Register (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPI/$\overline{ADC}$	EXTCLK	INTREF	DPON	DPSET2	DPSET1	PD_DIG	PD_ANA
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOLD	PEAK	RANGE	CLR	SEG_SEL	$\overline{OFFSET_CAL1}$	OFFSET_ CAL2	ENABLE

Default values: 0001h

This register is the primary control register for the MAX1497/MAX1499. It is a 16-bit read/write register. It is used to indicate the desired clock and reference source. It sets the LED display controls, range modes, power-down modes, offset calibration, and the reset register function (CLR).

ENABLE: (default = 1) LED driver enable bit. When set to 1, the MAX1497/MAX1499 enables the LED display drivers. A 0 in this location disables the LED display drivers.

OFFSET_CAL2: (default = 0) Enhanced offset-calibration start bit (MAX1499, RANGE = 1). To achieve the lowest possible offset in the ±200mV input range, perform an enhanced offset calibration by setting this bit to

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1. The calibration takes about nine cycles (1800ms). After the calibration completes, set this bit to zero to resume ADC conversions.

OFFSET_CAL1: (default = 0) Automatic offset calibration enable bit. When set to 1, the MAX1497/MAX1499 disable automatic offset calibration. When this bit is set to zero, automatic offset calibration is enabled.

SEG_SEL: (default = 0) SEG_SEL segment selection bit. When set to 1, the LED segment drivers use the LED segment registers to display individual segments that can form letters or numbers or other information on the display. The LED data register is not displayed. Send the data first to the LED segment-display registers and then set this bit high.

CLR: (default = 0) Clear all registers bit. When set to 1, all registers reset to their power-on reset states after CS makes a low-to-high transition.

RANGE: (default = 0) Input range select bit. When set to zero, the input voltage range is ±2V. When set to 1, the input voltage range is ±200mV.

PEAK: (default = 0) Peak bit. When set to 1 (and the HOLD bit is set to zero), the LED shows the result stored in the peak register (see Table 6).

HOLD: (default = 0) Hold bit. When set to 1, the LED register does not update from the ADC conversion results and holds the last result on the LED. The MAX1497/MAX1499 continue to perform conversions during HOLD (Table 1).

PD_ANA: (default = 0) Power-down analog select bit. When set to 1, the analog circuits (analog modulator and ADC input buffers) go into the power-down mode. When set to zero, the device is in full power-up mode.

PD_DIG: (default = 0) Power-down digital select bit. When set to 1, the digital circuits (digital filter and LED drivers) go into power-down mode. This also resets the values of the internal SRAM in the digital filter to zeros. When set to zero, the device returns to full power-up mode. When powering down PD_DIG, power down the LED segment drivers by clearing the ENABLE bit to zero.

DPSET[2:1]: (default = 00) Decimal-point selection bits (Table 2 and 3).

DPON: (default = 0) Decimal-point enable bit (Tables 2 and 3).

INTREF: (default = 0) Reference select bit. For internal reference operation, set INTREF to 1. For external reference operation, set INTREF to zero.

EXTCLK: (default = 0) External clock select bit. The EXTCLK bit controls selection of the internal clock or an external clock source. A 1 in this location selects the signal at the CLK input as the clock source. A zero in this location selects and powers up the internal clock oscillator.

SPI/ADC: (default = 0) Display select bit. The SPI/ADC bit controls selection of the data fed into LED data register. A 1 in this location selects SPI/QSPI/ MICROWIRE data (user writes this data to the LED data register). A zero in this location selects the ADC result register data, unless hold or peak functions are active (Table 1).

Note: When changing any one of the following control bits: OFFSET_CAL1, RANGE, PD_ANA, PD_DIG, INTREF, and EXTCLK, wait 800ms before reading the ADC results.

Overrange Register (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 7CF0h (for 3.5-digit, +1999)

4E1Fh (for 4.5-digit, +19,999)

The overrange register is a 16-bit read/write register (D15 is the MSB). When the conversion result exceeds the value in the overrange register, the OVER bit in the status register latches to 1. The LED shows a 1 followed by four dashes for the MAX1499 or a 1 followed by three dashes for the MAX1497 (Table 4).

The data is represented in two's complement format.

Underrange Register (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 8300h (for 3.5-digit, -2000)

B1E0h (for 4.5-digit, -20,000)

The underrange data register is 16-bit read/write register (D15 is the MSB). When the conversion result falls below the value in the underrange register, the UNDR bit in the status register sets to 1. The LED shows a -1 followed by four dashes for the MAX1499 or a -1 followed by three dashes for the MAX1497 (Table 4).

The data is represented in two's complement format.

Default values: 0000h

LED Segment-Display Register 1 (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 1	Bit 11	Bit 10	Bit 9	Bit 8
$\overline{A1}$	$\overline{G1}$	$\overline{D1}$	$\overline{F1}$	$\overline{E1}$	$\overline{DP2}$	X	$\overline{B0}$
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{C0}$	$\overline{A0}$	$\overline{G0}$	$\overline{D0}$	$\overline{F0}$	$\overline{E0}$	$\overline{DP1}$	0

LED segment-display register 1 is a 16-bit read/write register. When the LED bit (in the control register) is set to 1, the MAX1497/MAX1499 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{DP1}$: Segment DP driver bit of digit 1. The default value turns on the LED segment.

$\overline{E0}$: Segment E driver bit of digit 0. The default value turns on the LED segment.

$\overline{F0}$: Segment F driver bit of digit 0. The default value turns on the LED segment.

$\overline{D0}$: Segment D driver bit of digit 0. The default value turns on the LED segment.

$\overline{G0}$: Segment G driver bit of digit 0. The default value turns on the LED segment.

$\overline{A0}$: Segment A driver bit of digit 0. The default value turns on the LED segment.

$\overline{C0}$: Segment C driver bit of digit 0. The default value turns on the LED segment.

$\overline{B0}$: Segment B driver bit of digit 0. The default value turns on the LED segment.

X: Don't care.

$\overline{DP2}$: Segment DP driver bit of digit 2. The default value turns on the LED segment.

$\overline{E1}$: Segment E driver bit of digit 1. The default value turns on the LED segment.

$\overline{F1}$: Segment F driver bit of digit 1. The default value turns on the LED segment.

$\overline{D1}$: Segment D driver bit of digit 1. The default value turns on the LED segment.

$\overline{G1}$: Segment G driver bit of digit 1. The default value turns on the LED segment.

$\overline{A1}$: Segment A driver bit of digit 1. The default value turns on the LED segment.

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LED Segment-Display Register 2 (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 1	Bit 11	Bit 10	Bit 9	Bit 8
$\overline{F3}$	$\overline{E3}$	$\overline{DP4}$	$\overline{MINUS}$	$\overline{B2}$	$\overline{C2}$	$\overline{A2}$	$\overline{G2}$
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{D2}$	$\overline{F2}$	$\overline{E2}$	$\overline{DP3}$	X	$\overline{B1}$	$\overline{C1}$	0

Default values: 0000h

LED segment-display register 2 is a 16-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1497/MAX1499 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{C1}$: Segment C driver bit of digit 1. The default value turns on the LED segment.

$\overline{B1}$: Segment B driver bit of digit 1. The default value turns on the LED segment.

$\overline{MINUS}$: Segment minus driver bit. The default value turns on the LED minus segment. Setting this bit to 1 enables the plus sign on the LED display.

$\overline{DP3}$: Segment DP driver bit of digit 3. The default value turns on the LED segment.

$\overline{E2}$: Segment E driver bit of digit 2. The default value turns on the LED segment.

$\overline{F2}$: Segment F driver bit of digit 2. The default value turns on the LED segment.

$\overline{D2}$: Segment D driver bit of digit 2. The default value turns on the LED segment.

$\overline{G2}$: Segment G driver bit of digit 2. The default value turns on the LED segment.

$\overline{A2}$: Segment A driver bit of digit 2. The default value turns on the LED segment.

$\overline{C2}$: Segment C driver bit of digit 2. The default value turns on the LED segment.

$\overline{B2}$: Segment B driver bit of digit 2. The default value turns on the LED segment.

$\overline{DP4}$: Segment DP driver bit of digit 4. The default value turns on the LED segment (MAX1499 only).

$\overline{E3}$: Segment E driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{F3}$: Segment F driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

LED Segment-Display Register 3 (Read/Write)

MSB							LSB
X	X	$\overline{BC_}$	$\overline{B3}$	$\overline{C3}$	$\overline{A3}$	$\overline{G3}$	$\overline{D3}$

Default values: 00h

LED segment-display register 3 is an 8-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1497/MAX1499 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{D3}$: Segment D driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{G3}$: Segment G driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{A3}$: Segment A driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{C3}$: Segment C driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{B3}$: Segment B driver bit of digit 3. The default value turns on the LED segment (MAX1499 only).

$\overline{BC_}$: Segment B and C driver bit of digit 3 (3.5 digits) or Digit 4 (4.5 digits). The default value turns on the LED segment.

X: Don't care.

ADC Custom Offset-Calibration Register (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

In addition to automatic offset calibration, the MAX1497/MAX1499 offer a user-defined custom offset 16-bit read/write register. The final result of the ADC conversion is the input after autocalibration minus the value in the custom offset. The custom offset value is stored in this register. D15 is the MSB. The data is represented in two's complement format.

ADC Result Register 1 (Read Only)

MSB											LSB (MAX1497)				LSB (MAX1499)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

ADC result register 1 is a 16-bit read-only register. This register stores the 16 MSBs of the ADC result. The data is represented in two's complement format.

For the MAX1499, the data is 16-bit and D15 is the MSB. For the MAX1497, the data is 12-bit, D15 is the MSB, and D4 is the LSB.

ADC Result Register 2 (Read Only)

MSB			LSB				
D3	D2	D1	D0	0	0	0	0

Default values: 00h

ADC result register 2 is an 8-bit read-only register. This register stores the 4 LSBs of the ADC result. Use this result with the result in ADC result-register 1 to form a 20-bit two's complement conversion result.

LED Data Register (Read/Write)

MSB											LSB (MAX1497)				LSB (MAX1499)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

The LED data register is a 16-bit read/write register. This register updates from ADC result register 1 or from the serial interface by selecting the SPI/$\overline{\text{ADC}}$ bit in the control register. The data is represented in two's complement format.

For the MAX1499, the data is 16-bit and D15 is the MSB. For the MAX1497, the data is 12-bit, D15 is the MSB, and D4 is the LSB, followed by 4 trailing sub-bits.

PEAK Register (Read Only)

MSB											LSB (MAX1497)				LSB (MAX1499)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: B1E0h

The peak data register is a 16-bit read only register. Set the PEAK bit to 1 to enable the PEAK function. This register stores the peak value of the ADC conversion result. First, the current ADC result is saved to the PEAK register, then the new ADC conversion result is compared to this value. If the new value is larger than the value in the peak register, the MAX1497/MAX1499 save the new value to the peak register. If the new value is less than the value in the peak register, the value in the peak register remains unchanged. Set the PEAK bit to zero to clear the value in the PEAK register.

The data is represented in two's complement format.

For the MAX1499, the data is 16-bit and D15 is the MSB. For the MAX1497, the data is 12-bit, D15 is the MSB, and D4 is the LSB followed by 4 trailing sub-bits.

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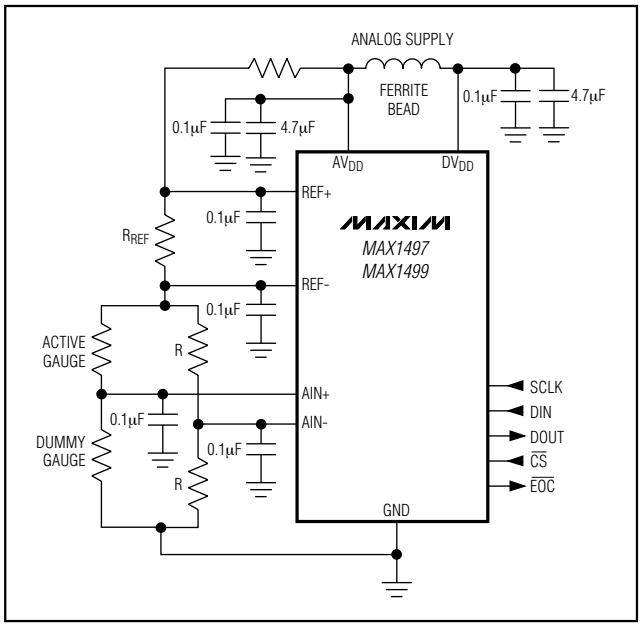


Figure 15. Strain-Gauge Application with the MAX1497/MAX1499

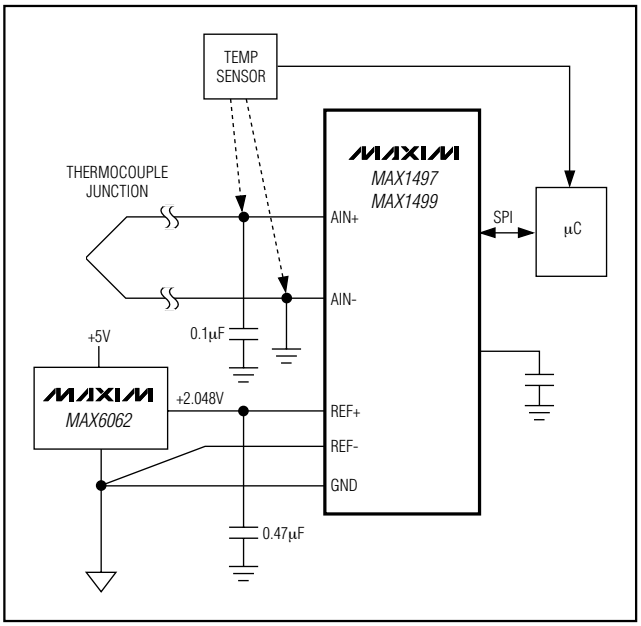


Figure 16. Thermocouple Application with the MAX1497/MAX1499

Power-On Reset

At power-on, the serial interface, logic LED drivers, digital filter, and modulator circuits reset. The registers return to their default values. Allow time for the reference to settle before starting calibration.

Offset Calibration

The MAX1497/MAX1499 offer on-chip offset calibration. The device offset calibrates during every conversion when the OFFSET_CAL1 bit is zero in the control register. Enhanced offset calibration is only needed in the MAX1499 when the RANGE bit = 1. It is performed on demand by setting the OFFSET_CAL2 bit to 1.

Enhanced Offset Calibration

Enhanced offset calibration is a more accurate calibration method that is needed in the case of the ±200mV range and 4.5-digit resolution. The MAX1499 performs the enhanced calibration on demand by setting the OFFSET_CAL2 bit to 1.

Power-Down Modes

The MAX1497/MAX1499 feature independent power-down control of the analog and digital LED drivers circuitry. Writing a 1 to the PD_DIG and PD_ANA bits in the control word, powers down the analog and digital circuitry, reducing the supply current to 268µA (typ). PD_DIG powers down the digital filter, while PD_ANA powers down the analog modulator and ADC input buffers. Writing a zero to the ENABLE bit in the control word, powers down the LED drivers.

Peak

The MAX1497/MAX1499 feature peak detection circuitry. When activated (PEAK bit = 1), the devices display only the highest voltage measured to the LED.

Hold

The MAX1497/MAX1499 feature data-hold circuitry. When activated (HOLD bit = 1), the device displays the current reading on the LED.

Low Battery

The MAX1499 features a low-battery detection input. When the voltage at LOWBATT drops below 2.048V (typ), the LOWBATT bit of the status register goes high.

Strain-Gauge Measurement

Connect the differential inputs of the MAX1497/MAX1499 to the bridge network of the strain gauge. In Figure 15, the analog supply voltage powers the bridge network and the MAX1497/MAX1499 along with the reference voltage. The MAX1497/MAX1499 handle an analog input voltage range of ±200mV and ±2V full scale. The analog/reference inputs of the parts allow the analog input range to have an absolute value of anywhere between -2.2V and +2.2V.

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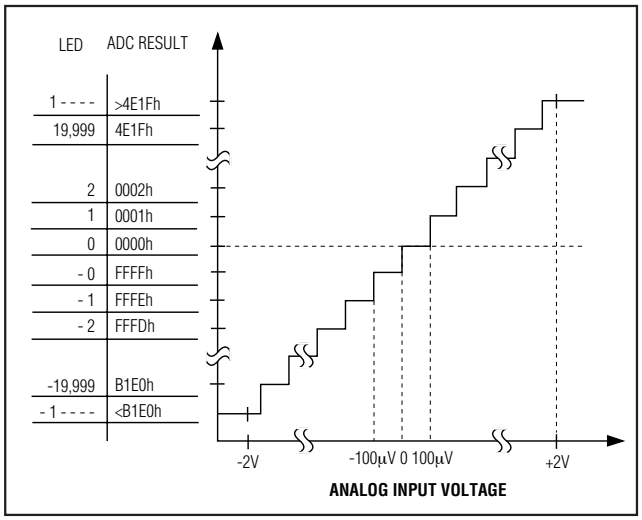


Figure 17. MAX1499 Transfer Function, ±2V Range

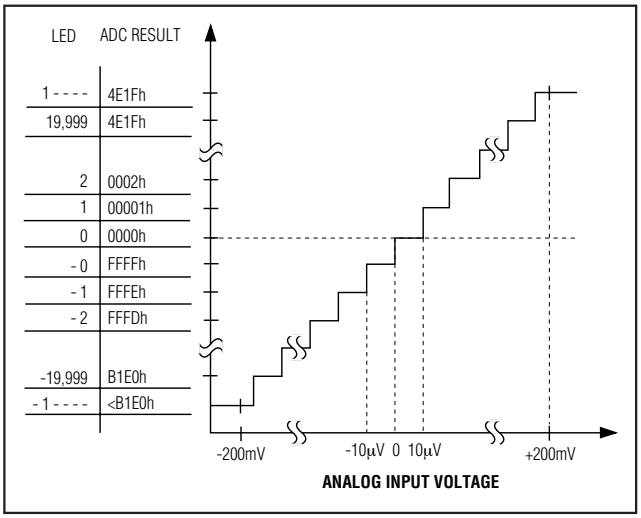


Figure 18. MAX1499 Transfer Function, ±200mV Range

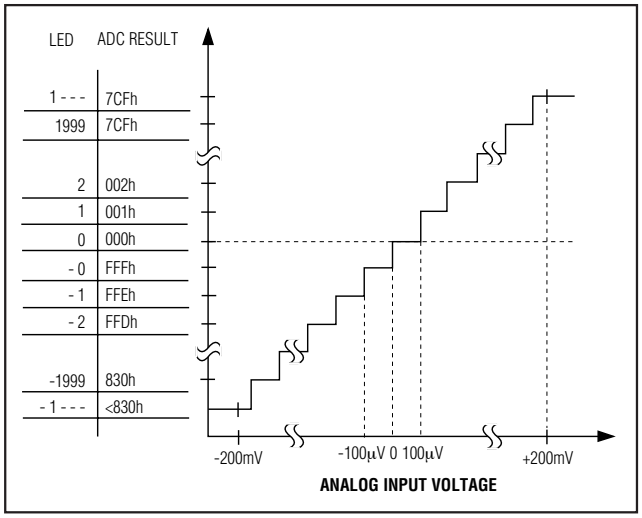


Figure 19. MAX1497 Transfer Function, ±200mV Range

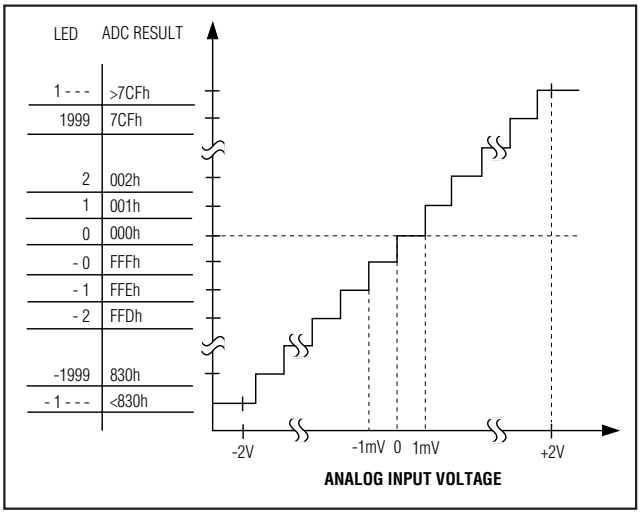


Figure 20. MAX1497 Transfer Function, ±2V Range

Thermocouple Measurement

Figure 16 shows a connection from a thermocouple to the MAX1497/MAX1499. In this application, the MAX1497/MAX1499 take advantage of the on-chip input buffers that allow large source impedances on the front end. The decoupling capacitors reduce noise pickup from the thermocouple leads. To place the differential voltage from the thermocouple at a suitable common-mode voltage, the AIN- input of the MAX1497/MAX1499 is biased to GND. Use an external temperature sensor, such as the DS75, and a µC to perform cold-junction temperature compensation.

Transfer Functions

Figures 17–20 show the transfer functions of the MAX1497/MAX1499. The output data is stored in the ADC data register in two's complement.

The transfer function for the MAX1499 with AIN+ - AIN- ≥ 0, RANGE = 0 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}}\right) \times 20{,}000$$

The transfer function for the MAX1499 with AIN+ - AIN- < 0, RANGE = 0 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) + 1$$

The transfer function for the MAX1497 with AIN+ - AIN- ≥ 0, RANGE = 0 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right)$$

The transfer function for the MAX1497 with AIN+ - AIN- < 0, RANGE = 0 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) + 1$$

The transfer function for the MAX1499 with AIN+ - AIN- ≥ 0, RANGE = 1 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}}\right) \times 20{,}000 \times 10$$

The transfer function for the MAX1499 with AIN+ - AIN- < 0, RANGE = 1 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10 + 1$$

The transfer function for the MAX1497 with AIN+ - AIN- ≥ 0, RANGE = 1 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10$$

The transfer function for the MAX1497 with AIN+ - AIN- < 0, RANGE = 1 is:

$$COUNTS = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10 + 1$$

Table 6. Segment Current Selection

R_{ISET} (kΩ)	I_{SEG} (mA)
25	20
50	10
100	5
500	1
>2500	LED driver disabled

Supplies, Layout, and Bypassing

Power up AVDD and DVDD (MAX1499) and VDD (MAX1497) before applying an analog input and external reference voltage to the device. If this is not possible, limit the current into these inputs to 50mA. When the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10Ω) or ferrite bead. For best performance, ground the MAX1497/MAX1499 to the analog ground plane of the circuit board.

Avoid running digital lines under the device, because they may couple noise onto the die. Run the analog ground plane under the MAX1497/MAX1499 to minimize coupling of digital noise. Make the power-supply lines to the MAX1497/MAX1499 as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line.

Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals. Running traces that are on opposite sides of the board at right angles to each other reduces feedthrough effects. A microstrip technique is best, but is not always possible with double-sided boards. With this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high-resolution ADCs. Decouple the supplies with 0.1µF ceramic capacitors to GND. Place these components as close to the device as possible to achieve the best decoupling.

Segment-Current Selection

A resistor from ISET to ground sets the current for each LED segment. See Table 6 for more detail. Use the following formula to set the segment current:

$$I_{SEG} = \left(\frac{1.25V}{R_{ISET}}\right) \times 400$$

R_{ISET} values below 25kΩ increase the I_{SEG}. However, the internal current-limit circuit limits the I_{SEG} to less than 30mA. At higher I_{SEG} values, the proper operation of the device is not guaranteed. In addition, the power dissipated may exceed the package power dissipation limit.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Choosing Supply Voltage to Minimize Power Dissipation

The MAX1497/MAX1499 drive a peak current of 25.5mA into LEDs with a 2.2V forward-voltage drop when operated from a supply voltage of at least 3.0V. Therefore, the minimum voltage drop across the internal LED drivers is (3.0V - 2.2V) = 0.8V. The MAX1497/MAX1499 sink (8 x 25.5mA = 204mA) when the outputs are operating and LED segment drivers are at full current. For a 3.3V supply, the MAX1497/MAX1499 dissipate (3.3V - 2.2V) x 204 = 224.4mW. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.8V headroom.

For a VLED supply voltage of 2.7V, the maximum LED forward voltage is 1.9V to ensure 0.8V driver headroom. The voltage drop across the drivers with a nominal +5V supply (5.0V - 2.2V = 2.8V) is almost three times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V = 1.1V). Therefore, the driver's power dissipation increases three times. The power dissipation in the part causes the junction temperature to rise accordingly. In the high ambient temperature case, the total junction temperature may be very high (>+125°C). At higher junction temperatures, the ADC performance degrades. To ensure the dissipation limit for the MAX1497/MAX1499 is not exceeded and the ADC performance is not degraded, a diode can be inserted between the power supply and VLED.

Computing Power Dissipation

The following can be used to compute power dissipation:

$$PD = (VLED \times I_{VLED}) + (VLED - V_{DIODE})(DUTY \times I_{SEG} \times N) + V_{SUPPLY} \times I_{SUPPLY}$$

VLED = LED driver supply voltage

I_{VLED} = VLED bias current

V_{DIODE} = LED forward voltage

DUTY = segment ON time during each digit ON time

I_{SEG} = segment current set by R_{ISET}

N = number of segments driven (worst case is eight)

V_{SUPPLY} = supply voltage of the part

I_{SUPPLY} = supply current from V_{DD} for the MAX1497 or $AV_{DD} + DV_{DD}$ for the MAX1499

Dissipation Example

For I_{SEG} = 25.5mA, N = 8, DUTY = 127 / 128, V_{DIODE} = 1.5V at 25.5mA, VLED = V_{SUPPLY} = 5.25V:

$$PD = (5.25 \times 2mA) + (5.25V - 1.5)[(127 / 128) \times 25.5mA \times 8)] + 5.25 \times 1.080mA$$

$$PD = 0.7751W$$

28-Pin SSOP Package Example

For the 28-pin SSOP package (TJA = 1 / 0.009496 = +105.3°C/W), the maximum allowed ambient temperature T_A is given by:

$$TJ\ (max) = T_A + (PD \times TJA) = +125°C = T_A + (0.7751W \times +105.3°C/W)$$

$$T_A = +43°C$$

Thus, the device cannot operate safely at a maximum package temperature of +85°C. The power dissipates in the part need to be lowered.

$$(PD \times TJA)\ max = (+125°C) - (+85°C) = +40°C$$

$$PD\ (max) = +40°C / +105.3°C/W = 380mW$$

$$(VLED - V_{DIODE}) = [380mW - (5.25V \times 2mA) - 5.25V \times 1.080mA] / [(127 / 128) \times 25.5mA \times 8]$$

$$VLED - V_{DIODE} = 1.854V$$

$VLED - V_{DIODE}$ should have the following condition to ensure it operates safely:

$$0.8V < VLED - V_{DIODE} < 2.08V$$

28-Pin PDIP Package Example

$$PD \times TJA\ (max) = (+125°C) - (+85°C) = +40°C$$

$$PD\ (max) = +40°C / +70°C/W = 571mW$$

$$VLED - V_{DIODE} = [571mW - (5.25V \times 2mA) - 5.25V \times 1.080mA] / [(127 / 128) \times 25.5mA \times 8]$$

$$VLED - V_{DIODE} = 2.80V$$

For a 28-pin PDIP package, $VLED - V_{DIODE}$ should have the following condition to ensure it operates safely:

$$0.8V < VLED - V_{DIODE} < 3.18V$$

32-Pin TQFP Package

The MAX1499 TQFP package can operate safely for all supply voltages provided V_{DIODE} > 1.5V.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Definitions

INL

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1497/MAX1499 is measured using the endpoint method.

DNL

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of ±1 LSB. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Rollover Error

Rollover error is defined as the absolute-value difference between a near positive full-scale reading and near negative full-scale reading. Rollover error is tested by applying a full-scale positive voltage, swapping AIN+ and AIN-, and adding the results.

Zero Input Reading

Ideally, with AIN+ connected to AIN-, the MAX1497/MAX1499 digital ADC result is 0000h. Zero input reading is the measured deviation from the ideal 0x0000 and the actual measured point.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

Common-Mode Rejection

Common-mode rejection (CMR) is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

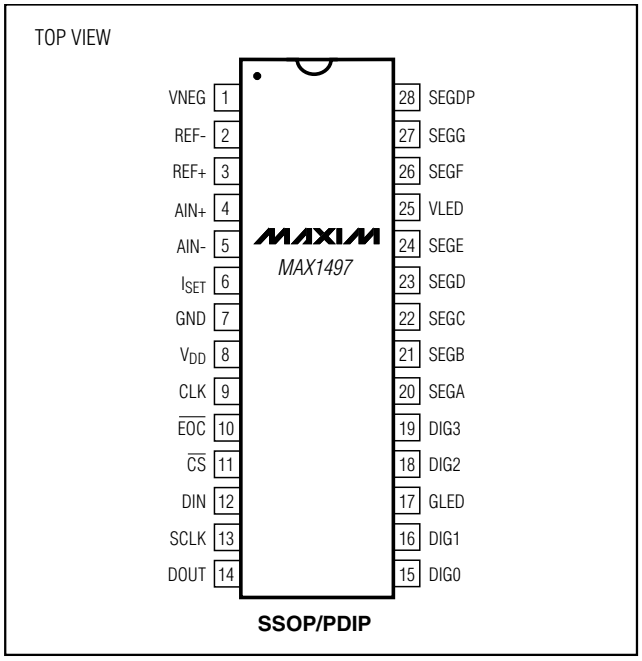
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)

Normal-mode rejection is a measure of how much output changes when a 50Hz and a 60Hz signal is injected into only one of the differential inputs. The MAX1497/MAX1499 sigma-delta converter uses its internal digital filter to provide normal-mode rejection to both 50Hz and 60Hz power-line frequencies simultaneously.

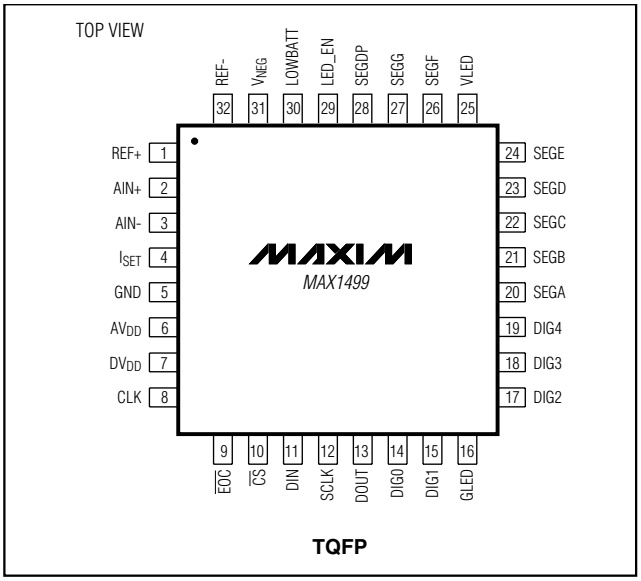
Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is the ratio of the input supply change (in volts) to the change in the converter output (in volts). It is typically measured in decibels.

Pin Configurations



SSOP/PDIP



TQFP

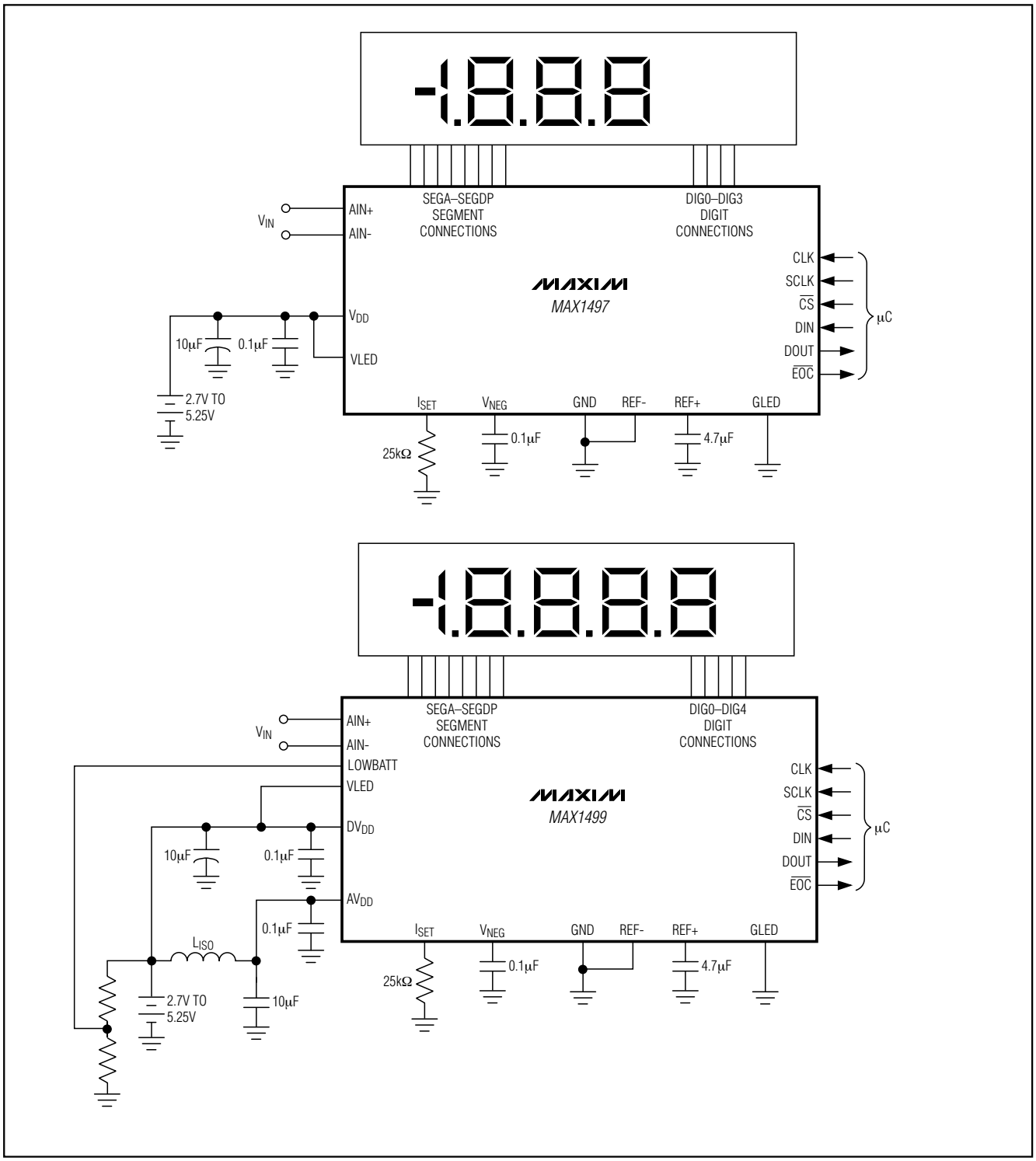
Chip Information

TRANSISTOR COUNT: 80,000

PROCESS: BiCMOS

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Typical Operating Circuits

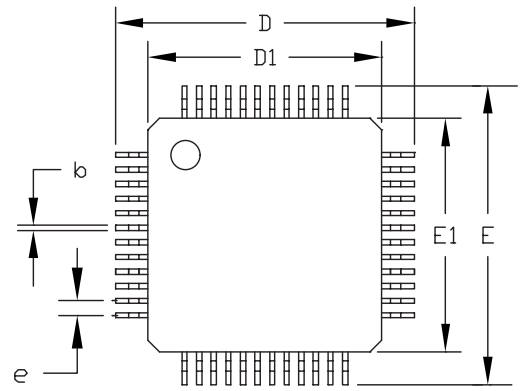


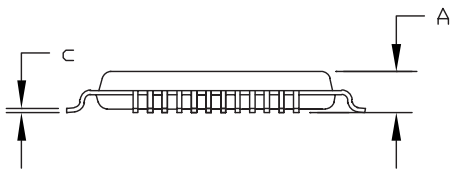
3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

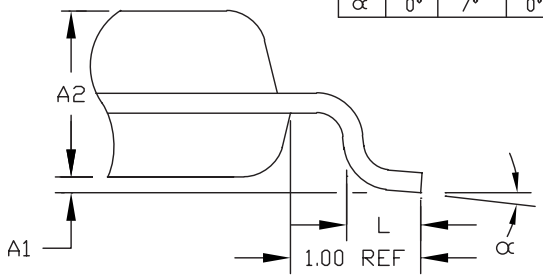
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L/48L,TQFP.EPS







JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

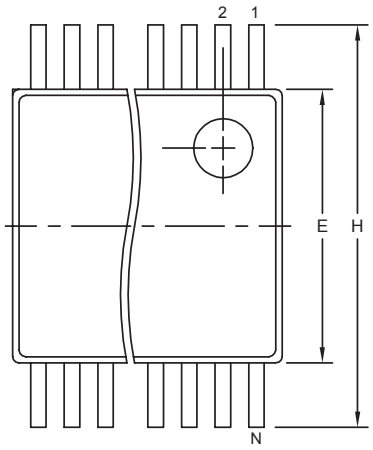
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	D	1/1

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

Package Information (continued)

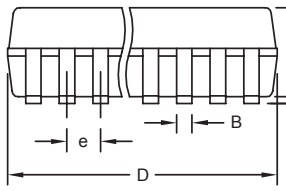
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

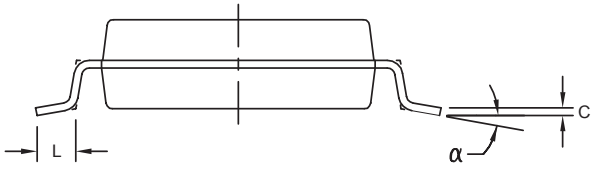
SSOP.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

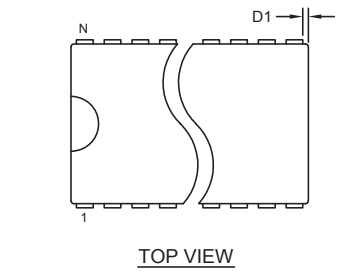
APPROVAL	DOCUMENT CONTROL NO.	REV.	
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3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers and µC Interface

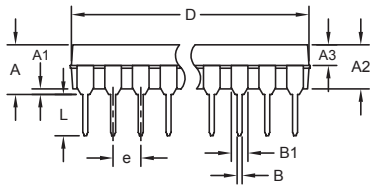
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

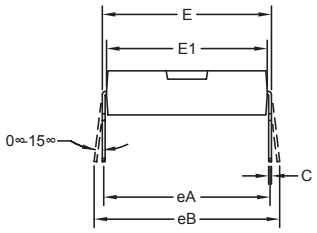
PDIPW.EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.200	-	5.08
A1	0.015	-	0.39	-
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.21	0.30
D1	0.005	0.009	0.13	0.22
E	0.600	0.625	15.24	15.87
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	-	0.700	-	17.78
L	0.120	0.150	3.05	3.81

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS011
D	1.230	1.270	31.24	32.26	24	AA
D	1.430	1.470	36.32	37.34	28	AB
D	2.025	2.075	51.44	52.71	40	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MS011.
5. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .600" PDIP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0044	B	1/1

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