MAX15021

Dual, 4A/2A, 4MHz, Step-Down DC-DC Regulator withTracking/ Sequencing Capability

General Description

The MAX15021 is a dual-output, pulse-width-modulated (PWM), step-down DC-DC regulator with tracking (coincident and ratiometric) and sequencing options. The device operates from 2.5V to 5.5V and each output can be adjusted from 0.6V to the input supply (V_{AVIN}). The MAX15021 delivers up to 4A (regulator 1) and 2A (regulator 2) of output current. This device offers the ability to adjust the switching frequency from 500kHz to 4MHz and provides the capability of optimizing the design in terms of size and performance.

The MAX15021 utilizes a voltage-mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types. The dual switching regulators operate 180° out-of-phase, thereby reducing the RMS input ripple current and thus the size of the input bypass capacitor significantly.

The MAX15021 offers the ability to track (coincident or ratiometric) or sequence during power-up and power-down operation. When sequencing, it powers up glitch-free into a prebiased output.

Additional features include an internal undervoltage lockout with hysteresis and a digital soft-start/soft-stop for glitch-free power-up and power-down. Protection features include lossless cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

The MAX15021 is available in a space-saving, 5mm x 5mm, 28-pin TQFN-EP package and is specified for operation from -40°C to +125°C temperature range.

Applications

RFID Reader Cards

Power-over-Ethernet (PoE) IP Phones

Automotive Multimedia

Multivoltage Supplies

Networking/Telecom

Ordering Information

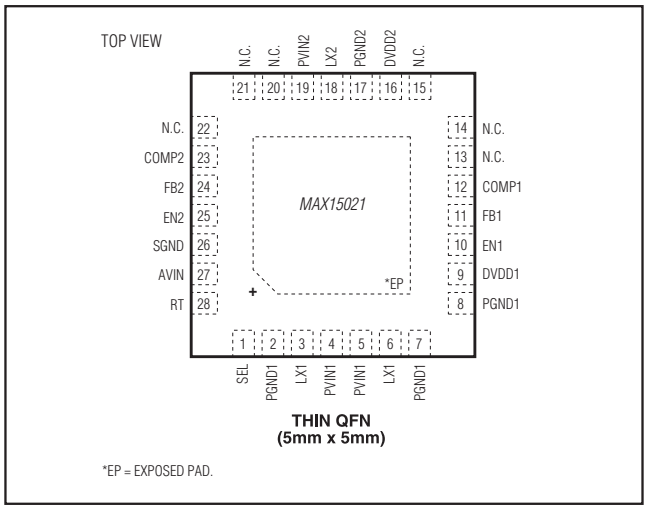
PART	TEMP RANGE	PIN-PACKAGE
MAX15021ATI/V+	-40°C to +125°C	28 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Benefits and Features

- Integration Reduces Power-Supply Footprint for Space-Constrained Designs
  - Dual-Output Synchronous Buck Regulators
  - Integrated Switches for 4A and 2A Output Currents
  - Programmable Switching Frequency from 500kHz to 4MHz
  - 28-Pin TQFN Package (5mm x 5mm)
  - 180° Out-Of-Phase Operation Reduces Input Ripple Current and Thus the Size of the Input Bypass Capacitors
- Sophisticated Tracking/Sequencing Functions Facilitate Reliable Processor Operation
  - Digital Soft-Start and Soft-Stop for Tracking Applications
  - Digital Soft-Start into a Prebiased Load for Sequencing Applications
  - Sequencing or Coincident/Ratiometric Tracking
- Flexible Enough for Use in a Range of Designs
  - 2.5V to 5.5V Input Voltage Range
  - Output-Voltage Adjustable from 0.6V to V_{AVIN}
  - External Compensation for Maximum Flexibility
  - 100% Maximum Duty Cycle
- Integrated Protection Features Save Space and Increase Reliability
  - Lossless, Cycle-by-Cycle Current Sensing
  - Thermal Shutdown and Hiccup-Mode Short-Circuit Protection
- 20µA Shutdown Current Extends Battery Life in Portable Applications

Pin Configuration



19-4106; Rev 2; 4/15

maxim integrated™

Absolute Maximum Ratings

AVIN, PVIN_, DVDD_, EN_, FB_, RT, SEL to SGND .....-0.3V to +6V
COMP_ to SGND .....-0.3V to (V_{AVIN} + 0.3V)
PGND_ to SGND .....-0.3V to +0.3V
LX_ Current (Note 1)
Regulator 1.....6A
Regulator 2.....3A
Current into Any Pin other than PVIN_, LX_, and PGND_.....50mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
Junction-to-Case Thermal Resistance (θ_{JC})(Note 2).....2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})(Note 2) ..29°C/W
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX_ has internal diodes to PGND_ and PVIN_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations see **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AVIN} = $V_{PVIN_}$ = $V_{DVDD_}$ = 3.3V, $V_{PGND_}$ = $V_{SGND_}$ = 0V, R_T = 25kΩ, and T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input-Voltage Range		V_{AVIN} = V_{PVIN1} = V_{PVIN2} = V_{DVDD1} = V_{DVDD2}	2.5		5.5	V
Undervoltage Lockout Threshold		AVIN rising	2.1	2.2	2.3	V
Undervoltage Lockout Hysteresis				0.12		V
Operating Supply Current		$V_{EN_}$= 1.3V, $V_{FB_}$ = 0.8V		3.5	6	mA
Shutdown Supply Current		$V_{EN_}$ = 0V		20	65	µA
PWM DIGITAL SOFT-START/SOFT-STOP						
Soft-Start/Soft-Stop Duration				4096		Clock Cycles
Reference Voltage Steps				64		Steps
PWM ERROR AMPLIFIERS						
FB1, FB2 Input Bias Current			-1		+1	µA
FB1, FB2 Voltage Set-Point			0.593	0.599	0.605	V
COMP1, COMP2 Voltage Range		$I_{COMP_}$ = -250µA to +250µA	0.3		V_{AVIN} - 0.5	V
Error-Amplifier Open-Loop Gain				80		dB
Error-Amplifier Unity-Gain				12		MHz
POWER MOSFETs						
Regulator 1 p-Channel MOSFET		V_{DVDD1} = 5V		50	90	mΩ
Regulator 1 n-Channel MOSFET		V_{DVDD1} = 5V		30	50	mΩ
Regulator 1 Gate Charge		V_{DVDD1} = 5V		8		nC
Maximum LX1 RMS Current				4		A
Regulator 2 p-Channel MOSFET		V_{DVDD2} = 5V		100	180	mΩ
Regulator 2 n-Channel MOSFET		V_{DVDD2} = 5V		60	100	mΩ
Regulator 2 Gate Charge		V_{DVDD2} = 5V		4		nC
Maximum LX2 RMS Current				2		A

Electrical Characteristics (continued)

(V_{AVIN} = $V_{PVIN_}$ = $V_{DVDD_}$ = 3.3V, $V_{PGND_}$ = $V_{SGND_}$ = 0V, R_T = 25kΩ, and T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM CURRENT LIMIT AND HICCUP MODE						
Regulator 1 Peak Current Limit		V_{AVIN} = 3.3V	4.5	4.9	5.3	A
		V_{AVIN} = 2.5V	3.4	3.65	3.95	
Regulator 1 Valley Current Limit		V_{AVIN} = 3.3V	4.0	4.9	5.65	A
		V_{AVIN} = 2.5V	3.0	3.7	4.25	
Regulator 2 Peak Current Limit		V_{AVIN} = 3.3V	2.25	2.45	2.65	A
		V_{AVIN} = 2.5V	1.70	1.85	1.98	
Regulator 2 Valley Current Limit		V_{AVIN} = 3.3V	2.0	2.5	2.83	A
		V_{AVIN} = 2.5V	1.5	1.85	2.13	
Number of Cumulative Current-Limit Events to Hiccup	N_{CL}			4		Clock Cycles
Number of Consecutive Noncurrent Limit Cycles to Clear N_{CL}	N_{CLR}			3		Clock Cycles
Hiccup Timeout	N_{HT}			8192		Clock Cycles
ENABLE/SEL						
EN_ Threshold		$V_{EN_}$ rising	1.207	1.225	1.243	V
EN_ Hysteresis				0.12		V
EN_ Input Current			-2.5		+2.5	µA
SEL High Threshold			0.85 x V_{AVIN}			V
SEL Low Threshold					0.2 x V_{AVIN}	V
SEL Input Bias Current		Present only during startup	-100		+100	µA
OSCILLATOR						
Switching Frequency Range	f_{SW}	f_{SW} = 3MHz x [V_{RT}(V)/1.067(V)] (Note 4)	500		4000	kHz
Oscillator Accuracy		f_{SW} ≤ 1500kHz	-6		+6	%
		f_{SW} > 1500kHz	-10		+10	
Phase Shift Between Regulators				180		Degrees
RT Current		0 < V_{RT} < 1.067V	31.30	32	32.58	µA
RT Voltage Range	V_{RT}		0.13		1.067	V
Minimum Controllable On-Time				60		ns
Minimum Controllable Off-Time				60		ns
PWM Ramp Amplitude				V_{AVIN}/4		V
PWM Ramp Valley				0.3		V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		Temperature rising		+160		°C
Thermal Shutdown Hysteresis				15		°C

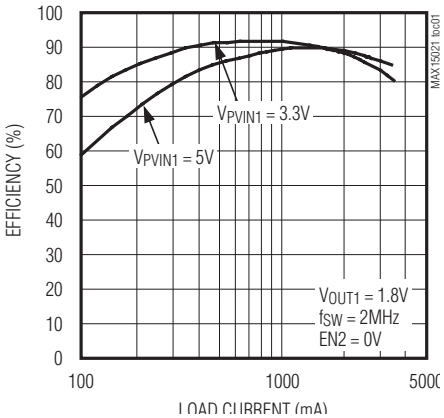
Note 3: Specifications are 100% production tested at T_A = +25°C and T_A = +125°C. Maximum and minimum specifications over temperature are guaranteed by design.

Note 4: When operating with V_{AVIN} = 2.5V, the maximum switching frequency should be derated to 3MHz.

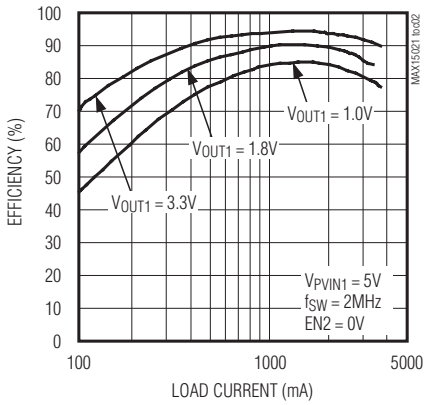
Typical Operating Characteristics

(V_{AVIN} = V_{DVDD1} = V_{DVDD2} = V_{PVIN1} = V_{PVIN2} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, $V_{PGND_}$ = 0V, R_T = 16.5kΩ. T_A = +25°C, unless otherwise noted.)

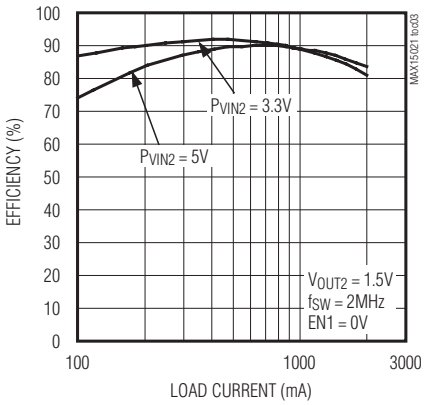
CHANNEL 1 EFFICIENCY vs. LOAD CURRENT



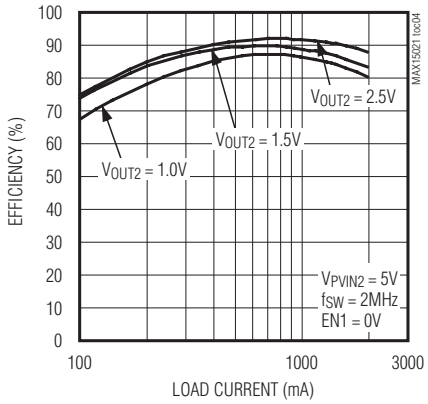
CHANNEL 1 EFFICIENCY vs. LOAD CURRENT



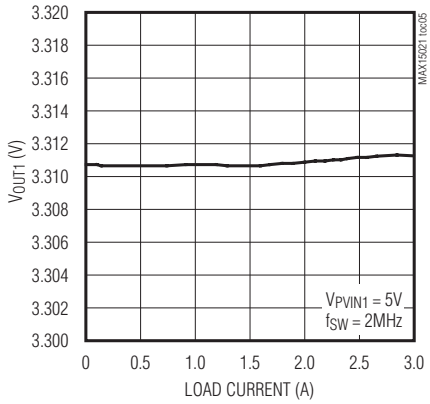
CHANNEL 2 EFFICIENCY vs. LOAD CURRENT



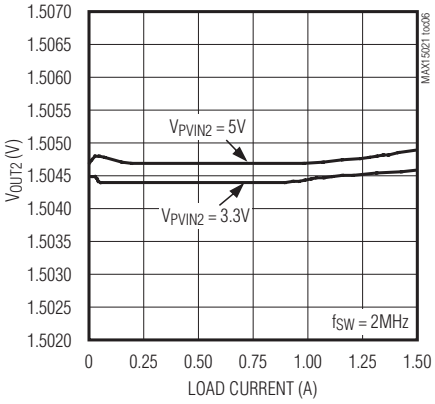
CHANNEL 2 EFFICIENCY vs. LOAD CURRENT



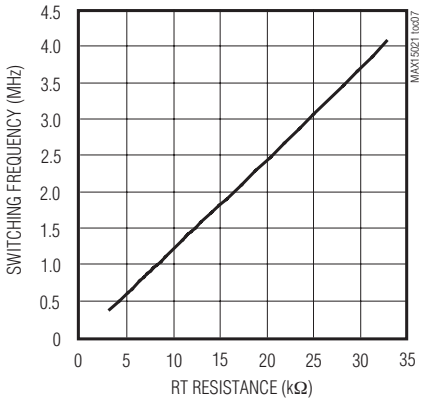
CHANNEL 1 LOAD REGULATION



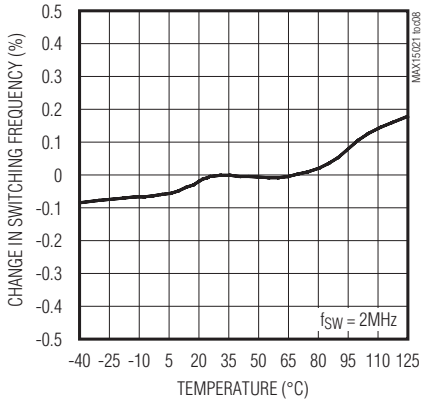
CHANNEL 2 LOAD REGULATION



SWITCHING FREQUENCY vs. RT RESISTANCE



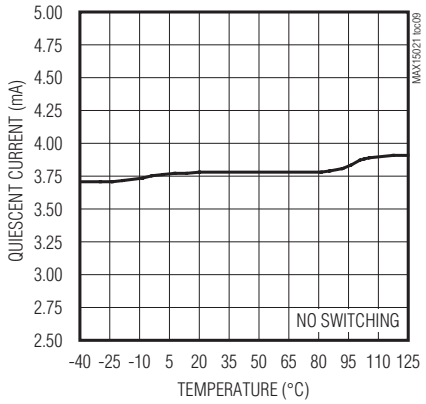
SWITCHING FREQUENCY vs. TEMPERATURE



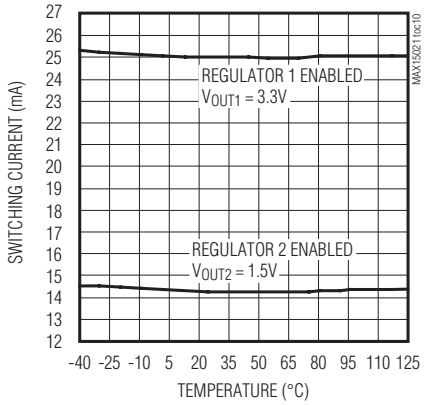
Typical Operating Characteristics (continued)

(V_{AVIN} = V_{DVDD1} = V_{DVDD2} = V_{PVIN1} = V_{PVIN2} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, $V_{PGND_}$ = 0V, R_T = 16.5kΩ. T_A = +25°C, unless otherwise noted.)

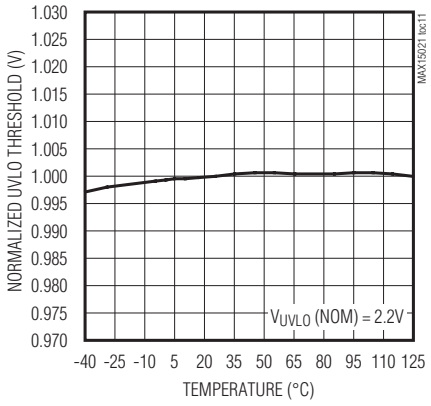
QUIESCENT CURRENT vs. TEMPERATURE



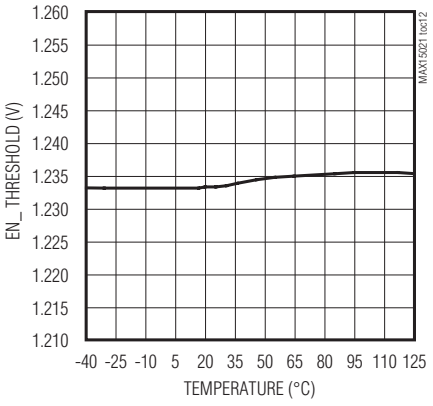
SWITCHING CURRENT vs. TEMPERATURE



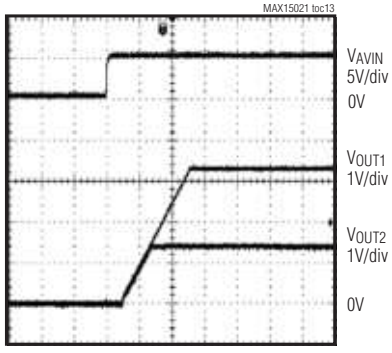
NORMALIZED UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



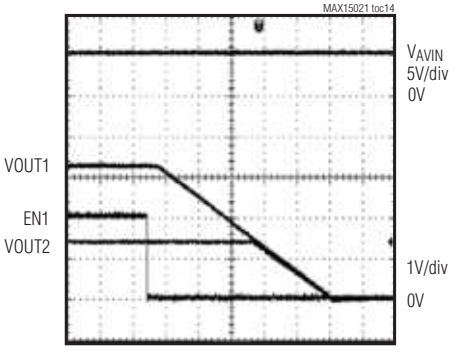
EN_ THRESHOLD vs. TEMPERATURE



COINCIDENT TRACKING SOFT-START



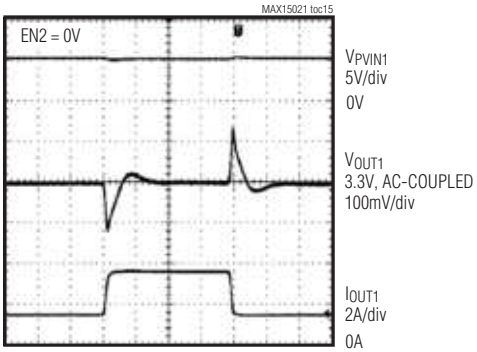
COINCIDENT TRACKING SOFT-STOP



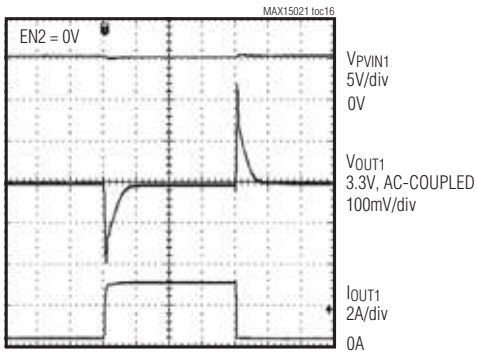
Typical Operating Characteristics (continued)

(V_{AVIN} = V_{DVDD1} = V_{DVDD2} = V_{PVIN1} = V_{PVIN2} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, $V_{PGND_}$ = 0V, R_T = 16.5kΩ. T_A = +25°C, unless otherwise noted.)

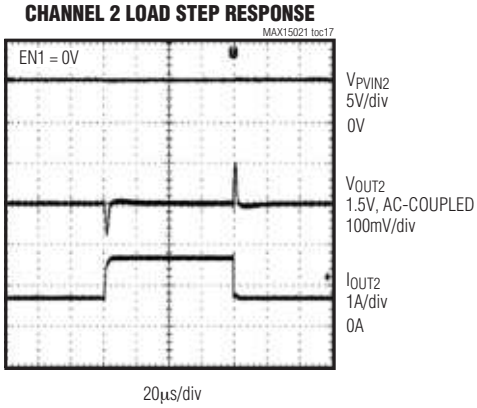
CHANNEL 1 LOAD STEP RESPONSE



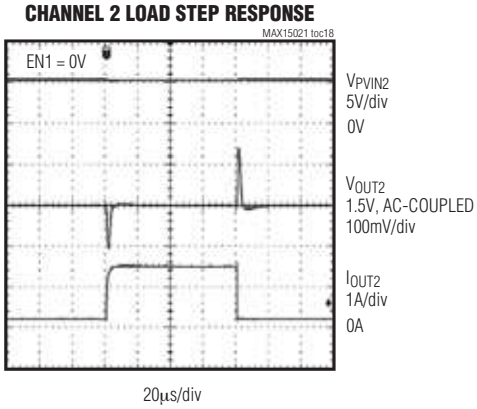
CHANNEL 1 LOAD STEP RESPONSE



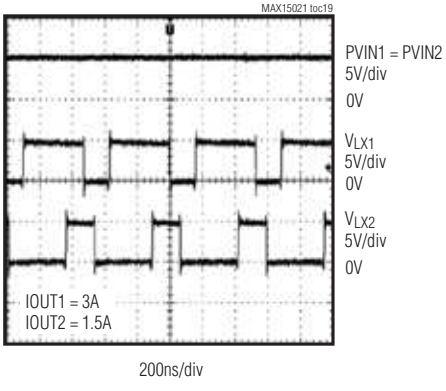
CHANNEL 2 LOAD STEP RESPONSE



CHANNEL 2 LOAD STEP RESPONSE



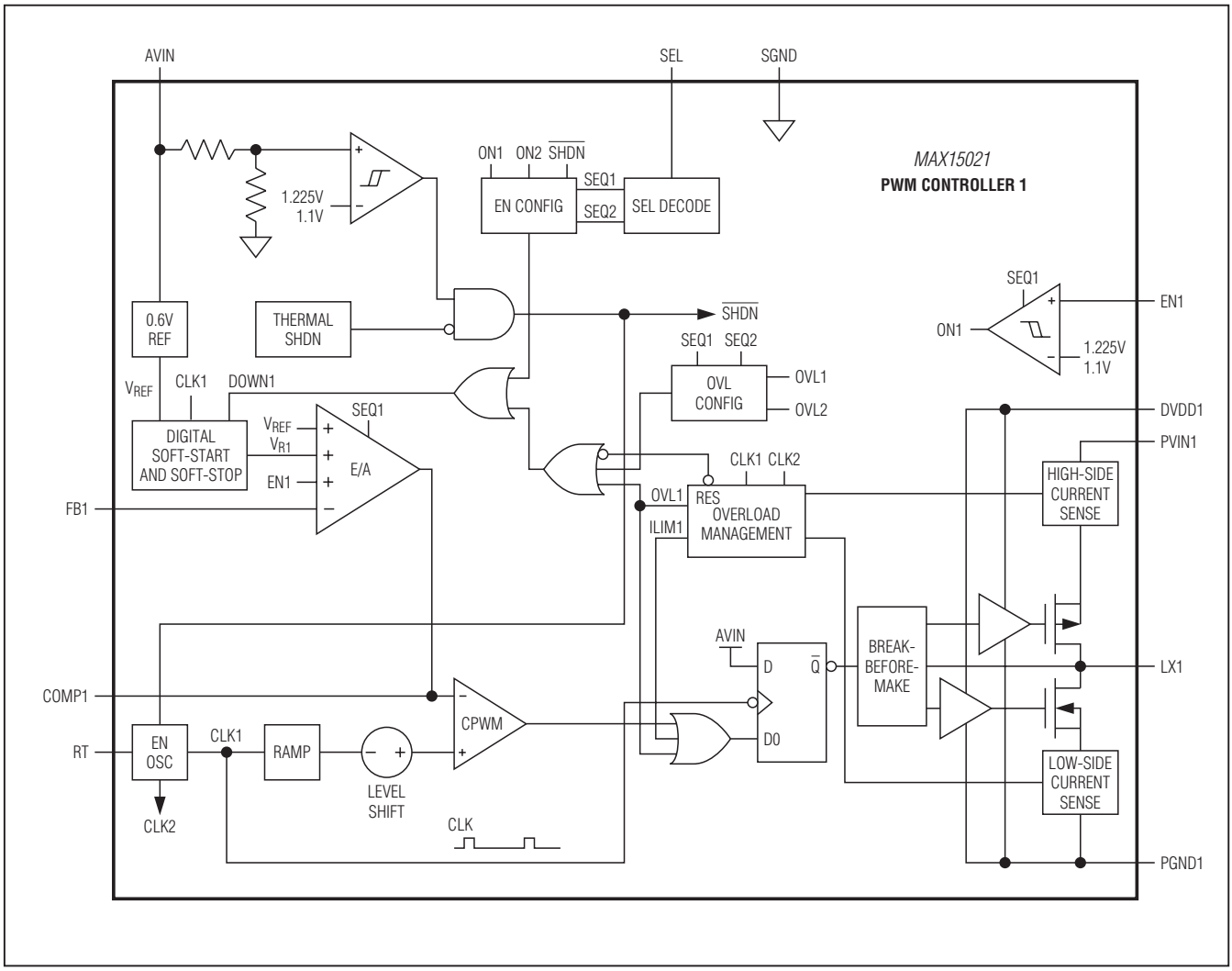
180° OUT-OF-PHASE OPERATION



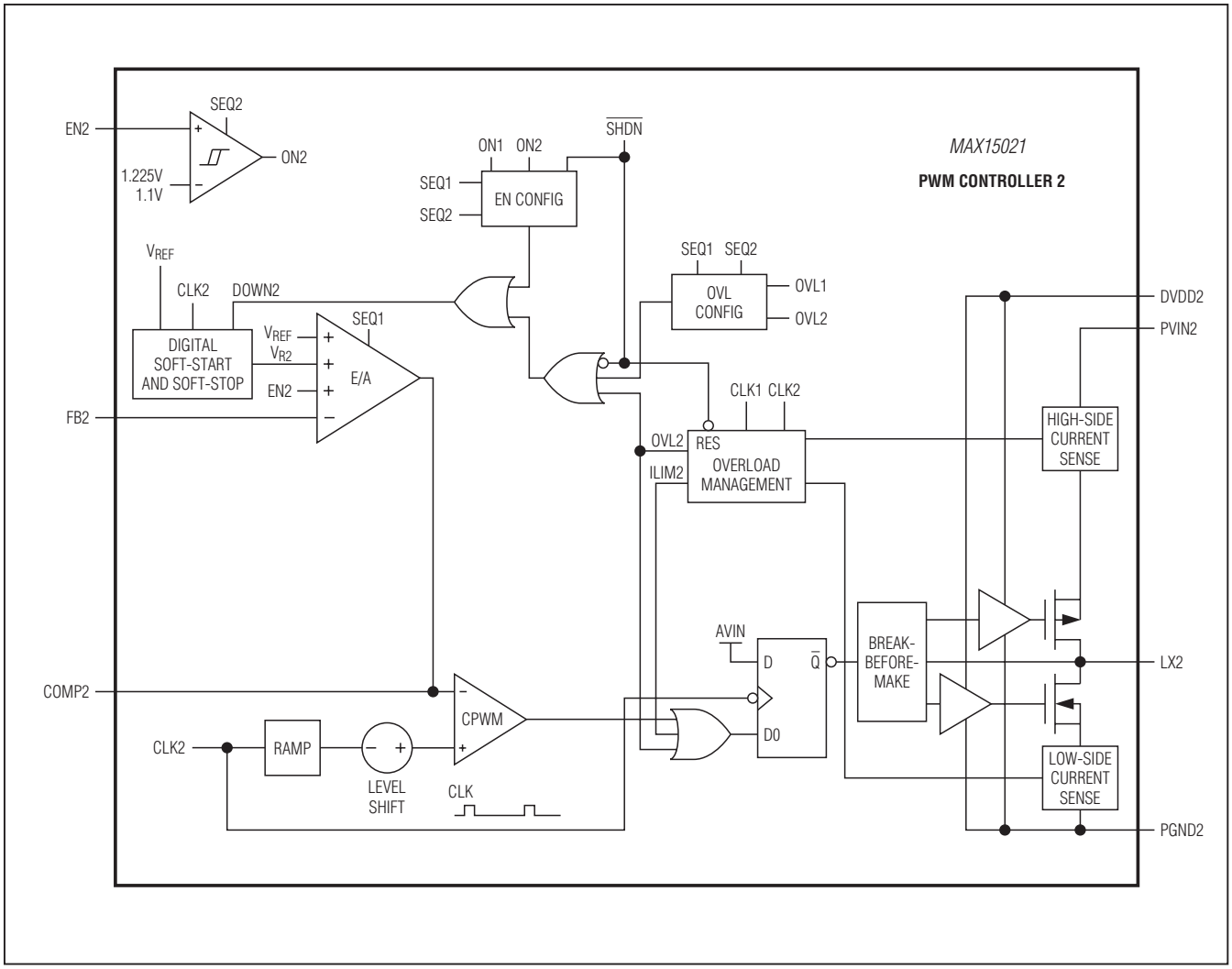
Pin Description

PIN	NAME	FUNCTION
1	SEL	Track/Sequence Select Input. Connect SEL to ground to configure the device as a sequencer. Connect SEL to AVIN for tracking with output 1 as the master. Leave SEL unconnected for tracking with output 2 as the master. Use the output with the higher voltage as the master and the output with the lower voltage as the slave.
2, 7, 8	PGND1	Power Ground Connection for Regulator 1. Connect the negative terminals of the input and output filter capacitor to PGND1. Connect PGND1 externally to SGND at a single point, typically at the negative terminal of the input capacitor.
3, 6	LX1	Inductor Connection for Regulator 1. LX1 is the drain connection of the internal high-side p-channel MOSFET and the drain connection of the internal synchronous n-channel MOSFET for regulator 1.
4, 5	PVIN1	Input Supply Voltage for Regulator 1. Connect to an external voltage source from 2.5V to 5.5V. Bypass PVIN1 to PGND1 with a 1µF (min) ceramic capacitor.
9	DVDD1	Switch Driver Supply for Regulator 1. Connect externally to PVIN1.
10	EN1	Enable Input for Regulator 1. When configured as a sequencer, EN1 must exceed 1.225V (typ) for the PWM controller to begin regulating output 1. When configured as a tracker, connect EN1 to the center tap of a resistive divider from the regulator 2 output.
11	FB1	Feedback Regulation Point for Regulator 1. Connect FB1 to the center tap of a resistive divider from the regulator 1 output to SGND to set the output voltage. The FB1 voltage regulates to 0.6V (typ).
12	COMP1	Error-Amplifier Output for Regulator 1. Connect COMP1 to the compensation feedback network.
13, 14, 15, 20, 21, 22	N.C.	No Connection. Do not connect.
16	DVDD2	Switch Driver Supply for Regulator 2. Connect externally to PVIN2.
17	PGND2	Power Ground Connection for Regulator 2. Connect the negative terminals of the input and output filter capacitors to PGND2. Connect PGND2 externally to SGND at a single point, typically at the negative terminal of the input capacitor.
18	LX2	Inductor Connection for Regulator 2. LX2 is the drain connection of the internal high-side p-channel MOSFET and the drain connection of the internal synchronous n-channel MOSFET for regulator 2.
19	PVIN2	Input Supply Voltage for Regulator 2. Connect to an external voltage source from 2.5V to 5.5V. Bypass PVIN2 to PGND2 with a 1µF (min) ceramic capacitor.
23	COMP2	Error-Amplifier Output for Regulator 2. Connect COMP2 to the compensation feedback network.
24	FB2	Feedback Regulation Point for Regulator 2. Connect to the center tap of a resistive divider from the regulator 2 output to SGND to set the output voltage. The FB2 voltage regulates to 0.6V (typ).
25	EN2	Enable Input for Regulator 2. When configured as a sequencer, EN2 must exceed 1.225V (typ) for the PWM controller to begin regulating output 2. When configured as a tracker, connect EN2 to the center tap of a resistive divider from the regulator 1 output.
26	SGND	Signal Ground. Connect SGND to PGND_ at a single point, typically near negative terminal of the input bypass capacitor.
27	AVIN	Input Voltage. Bypass AVIN to SGND with a 100nF (min) ceramic capacitor.
28	RT	Oscillator Timing Resistor Connection. Connect a 4.2kΩ to 33kΩ resistor from RT to SGND to program the switching frequency from 500kHz to 4MHz.
—	EP	Exposed Pad. Connect EP to a large copper plane at SGND potential to improve thermal dissipation. Do not use as the main SGND connection.

Functional Diagrams



Functional Diagrams (continued)



Detailed Description

The MAX15021 incorporates dual-output, PWM, step-down, DC-DC regulators with tracking and sequencing options. The device operates over the input-voltage range of 2.5V to 5.5V. Each PWM regulator provides an adjustable output down to 0.6V and delivers up to 4A (regulator 1) and 2A (regulator 2) of load current. The high switching frequency (up to 4MHz) and integrated power switches optimize the MAX15021 for high-performance and small-size power management solutions.

Each of the MAX15021 PWM regulator sections utilizes a voltage-mode control scheme for good noise immunity and offers external compensation allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The device operates at a fixed switching frequency that is programmable from 500kHz to 4MHz with a single resistor. Operating the regulators with 180° out-of-phase clocking, and at frequencies up to 4MHz, significantly reduces the RMS input ripple current. The resulting peak input current reduction (and increase in the ripple frequency) significantly reduces the required amount of input bypass capacitance.

The MAX15021 provides coincident tracking, ratiometric tracking, or sequencing to allow tailoring of power-up/power-down sequence depending on the system requirements. When sequencing, it powers up glitch-free into a prebiased output.

The MAX15021 includes internal undervoltage lockout with hysteresis, digital soft-start/soft-stop for “glitch-free” power-up and power-down. Protection features include lossless, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

Undervoltage Lockout (UVLO)

The supply voltage (V_{AVIN}) must exceed the default UVLO threshold before any operation starts. The UVLO circuitry keeps the MOSFET drivers, oscillator, and all the internal circuitry shut down to reduce current consumption. The UVLO rising threshold is 2.2V (typ) with a 120mV (typ) hysteresis.

Digital Soft-Start/Soft-Stop

The MAX15021 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after V_{AVIN} exceeds the undervoltage lockout threshold and the enable input is above 1.225V (typ). The soft-start circuitry ramps up the reference voltage, controlling the rate of rise of the output voltage, and reducing input surge currents during startup. The soft-start duration is 4096 clock cycles. The output voltage is incremented through 64 equal steps. The output reaches regulation when soft-start is completed, regardless of the output capacitance and load.

For tracking applications, soft-stop commences when the enable input falls below 1.1V (typ). The soft-stop circuitry ramps down the reference voltage controlling the output-voltage rate of fall. The output voltage is decremented through 64 equal steps in 4096 clock cycles.

Oscillator

Use an external resistor at RT to program the MAX15021 switching frequency from 500kHz to 4MHz. Calculate the appropriate resistor at RT for the desired output switching frequency (f_{SW}):

$$R_T[k\Omega] = \frac{f_{SW}[kHz] \times 1.067[V]}{32[\mu A] \times 4[MHz]}$$

Tracking/Sequencing

The MAX15021 features coincident/ratiometric tracking and sequencing (see Figure 1). Connect SEL to ground to configure the device as sequencer. Connect SEL to AVIN for tracking with output 1 as the master. Leave SEL unconnected for tracking with output 2 as the master. Assign the output with the higher voltage as the master.

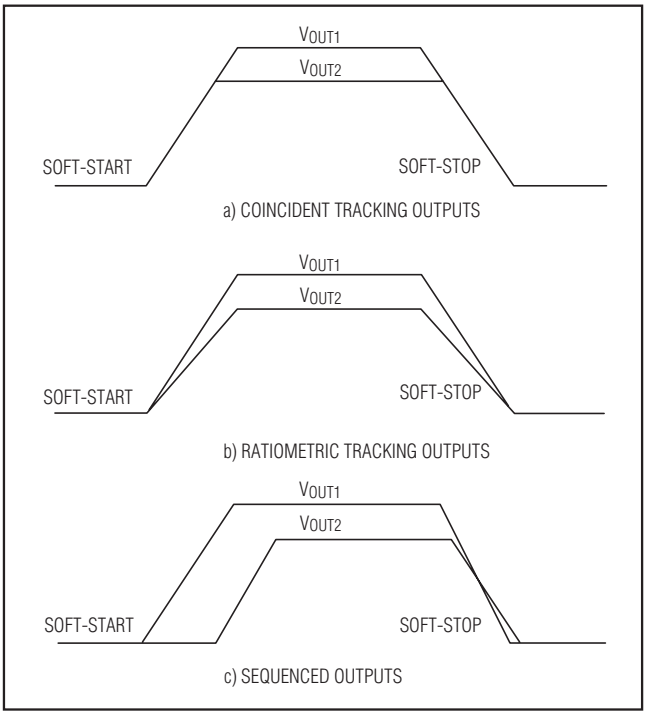


Figure 1. Graphical Representation of Coincident Tracking, Ratiometric Tracking, and Sequencing

Coincident/Ratiometric Tracking

The enable inputs in conjunction with digital soft-start and soft-stop provide coincident/ratiometric tracking. Track an output voltage by connecting a resistive divider from the output being tracked to its enable input. For example, for V_{OUT2} to coincidentally track V_{OUT1}, connect the same resistive divider used for FB2, from V_{OUT1} to EN2 to SGND (see Figure 2).

Track ratiometrically by connecting EN_ to SGND. This synchonizes the soft-start and soft-stop of all the regulator references, and hence their respective output voltages will track ratiometrically (see Figure 2).

When the MAX15021 regulators are configured as voltage trackers, output short-circuit fault conditions at either master or slave output are handled carefully—neither the master nor slave output will remain energized when the other output is shorted to ground. When the slave is shorted and enters hiccup mode, the master will soft-stop. When the master is shorted and the part enters in hiccup mode, the slave will ratiometrically soft-stop. Coming out of hiccup mode, both outputs will soft-start coincidently or ratiometrically depending on their initial configuration. During the thermal shutdown or power-off when the input falls below its UVLO, the output voltages decrease at a rate depending on the respective output capacitance and load.

See Figure 1 for a graphical representation of coincident/ratiometric tracking.

Sequencing

When sequencing, the voltage at the enable inputs must exceed 1.225V (typ) for each PWM controller to start (see Figure 1c).

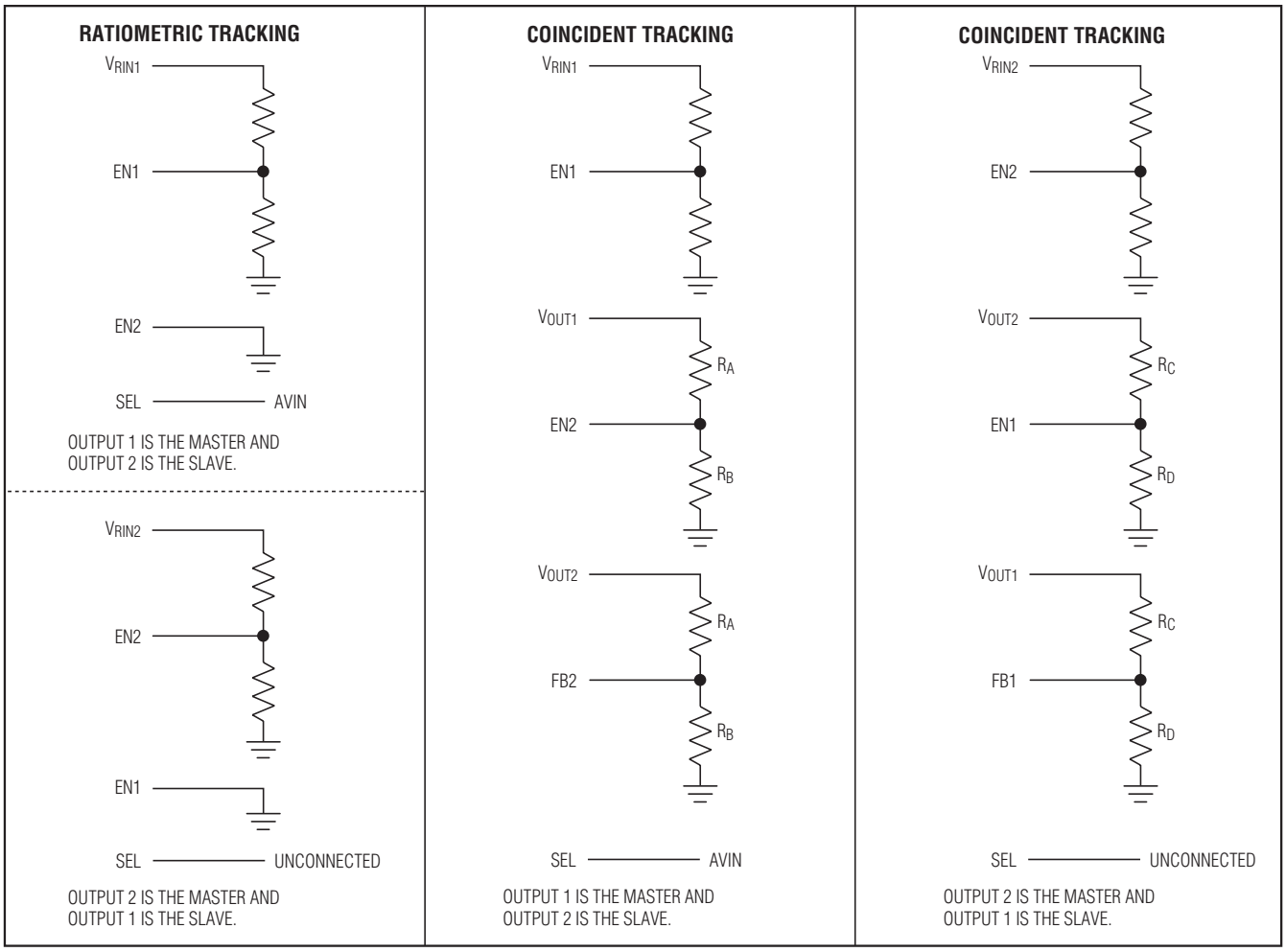


Figure 2. Ratiometric Tracking and Coincident Tracking Configurations

Error Amplifier

The output of the internal voltage-mode error amplifier (COMP_) is provided for frequency compensation (see the *Compensation-Design Guidelines* section). FB_ is the inverting input of the error amplifier. The error amplifier has an 80dB open-loop gain and a 12MHz gain bandwidth (GBW) product.

Output Short-Circuit Protection (Hiccup Mode)

The MAX15021 features lossless, high-side peak current limit and low-side, valley current limit. At short duty cycles, both limits are active. At high duty cycles, only the high-side peak current limit is active. Either limit causes the hiccup mode count (N_{CL}) to increment.

For duty cycles less than 50%, the low-side valley current limit is active. Once the high-side MOSFET turns off, the voltage across the low-side MOSFET is monitored. If this voltage does not exceed the current-limit threshold at the end of the cycle, the high-side MOSFET turns on normally at the start of the next cycle. If the voltage exceeds the current-limit threshold just before the beginning of a new PWM cycle, the controller skips that cycle. During severe overload or short-circuit conditions, the switching frequency of the device appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

If the current-limit threshold is exceeded for more than four cumulative clock cycles (N_{CL}), the device shuts down for 8192 clock cycles (hiccup timeout) and then restarts with a soft-start sequence. If three consecutive cycles pass without a current-limit event, the count of N_{CL} is cleared (see Figure 3). Hiccup mode protects the device against a continuous output short circuit.

The internal current limit is constant from 5.5V down to 3V and decreases linearly by 50% from 3V to 2V. See the *Electrical Characteristics* table.

Thermal-Overload Protection

The MAX15021 features an integrated thermal-overload protection with temperature hysteresis. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, an internal thermal sensor shuts down the device, turning off the internal power MOSFETs and allowing the die to cool. After the die temperature falls by +15°C, the part restarts with a soft-start sequence.

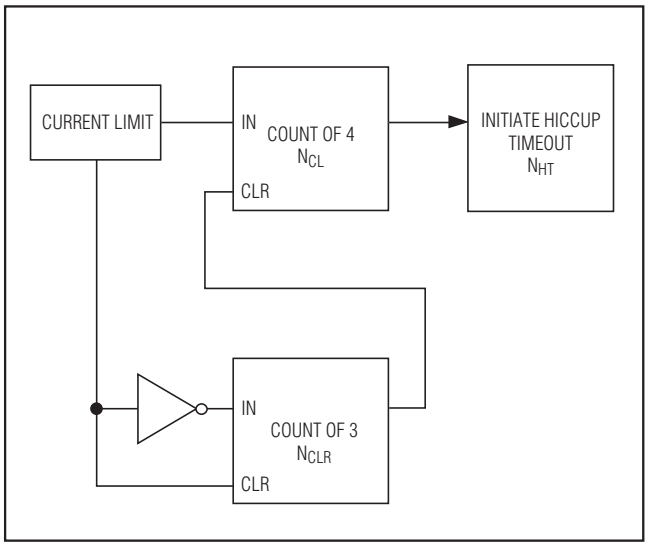


Figure 3. Hiccup-Mode Block Diagram

Startup into a Prebiased Output (Sequencing Mode)

In sequencing mode, the regulators start into a prebiased output and soft-stop is disabled. During soft-start, the complementary switching sequence is inhibited until the PWM comparator commands its first PWM pulse. Until then, the converters do not sink current from the outputs. The first PWM pulse occurs when the ramping reference voltage increases above the FB_ voltage.

PWM Controllers Design Procedure

Setting the Switching Frequency

Connect a 4.2kΩ to 33kΩ resistor from RT to SGND to program the switching frequency from 500kHz to 4MHz. Calculate the resistor connected to RT using the following equation:

$$R_T[k\Omega] = \frac{f_{SW}[kHz] \times 1.067[V]}{32[\mu A] \times 4[MHz]}$$

Higher frequencies allow designs with lower inductor values and less output capacitance. At higher switching frequencies core losses, gate-charge currents, and switching losses increase. When operating from V_{AVIN} ≤ 3V, the switching frequency (f_{SW}) should be derated to 3MHz (maximum).

Effective Input-Voltage Range

Although the MAX15021's regulators can operate from input supplies ranging from 2.5V to 5.5V, the input-voltage range can be effectively limited by the MAX15021's duty-cycle limitations for a given output voltage ($V_{OUT_}$). The maximum input voltage (V_{PVIN_MAX}) can be effectively limited by the controllable minimum on-time ($t_{ON(MIN)}$):

$$V_{PVIN_MAX}[V] \le \frac{V_{OUT_}[V]}{t_{ON(MIN)}[\mu s] \times f_{SW}[MHz]}$$

where $t_{ON(MIN)}$ is 0.06µs (typ).

The minimum input voltage (V_{PVIN_MIN}) can be effectively limited by the maximum controllable duty cycle and is calculated using the following equation:

$$V_{PVIN_MIN}[V] \ge \frac{V_{OUT_}[V]}{1-(t_{OFF(MIN)}[\mu s] \times f_{SW}[MHz])}$$

where $V_{OUT_}$ is the regulator output voltage and $t_{OFF(MIN)}$ is the 0.06µs (typ) controllable off-time.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15021: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value. A lower inductance minimizes size and cost and improves large-signal and transient response. However, efficiency is reduced due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. A higher inductance increases efficiency by reducing the ripple current; however, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. Choose the inductor's peak-to-peak current, ΔI_{P-P}, in the range of 20% to 50% of the full load current; as a rule of thumb 30% is typical.

Calculate the inductance, L, using the following equation:

$$L[\mu H] = \frac{V_{OUT_}[V] \times (V_{PVIN_}[V] - V_{OUT_}[V])}{V_{PVIN_}[V] \times f_{SW}[MHz] \times \Delta I_{P-P}[A]}$$

where $V_{PVIN_}$ is the input supply voltage, $V_{OUT_}$ is the regulator output voltage, and f_{SW} is the switching frequency. Use typical values for $V_{PVIN_}$ and $V_{OUT_}$ so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is programmable between 500kHz and 4MHz (see the *Oscillator* section).

The peak-to-peak inductor current (ΔI_{P-P}), which reflects the peak-to-peak output ripple, is largest at the maximum input voltage. See the *Output-Capacitor Selection* section to verify that the worst-case output current ripple is acceptable.

Select an inductor with a saturation current, I_{SAT}, higher than the maximum peak current to avoid runaway current during continuous output short-circuit conditions. Also, confirm that the inductor's thermal performances and projected temperature rise above ambient does not exceed its thermal capacity. Many inductor manufacturers provide bias/load current versus temperature rise performance curves (or similar) to obtain this information.

Input-Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents and therefore, the input capacitor must be carefully chosen to withstand the input ripple current and keep the input-voltage ripple within design requirements.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} which peaks at the end of the on-cycle. Calculate the required input capacitance and ESR for a specified ripple using the following equations:

$$ESR[m\Omega] = \frac{\Delta V_{ESR}[mV]}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)[A]}$$

$$C_{PVIN_}[\mu F] = \frac{I_{LOAD(MAX)}[A] \times \left(\frac{V_{OUT_}[V]}{V_{PVIN_}[V]}\right)}{\Delta V_Q[V] \times f_{SW}[MHz]}$$

$$\Delta I_{P-P}[A] = \frac{\left(V_{PVIN_} - V_{OUT_}\right)[V] \times V_{OUT_}[V]}{V_{PVIN_}[V] \times f_{SW}[MHz] \times L[\mu H]}$$

$I_{LOAD(MAX)}$ is the maximum output current, ΔI_{P-P} is the peak-to-peak inductor current, and $V_{PVIN_}$ is the input supply voltage, $V_{OUT_}$ is the regulator output voltage, and f_{SW} is the switching frequency.

Use the following equation to calculate the input ripple when only one regulator is enabled:

$$I_{CIN(RMS)}[A] = I_{LOAD(MAX)}[A] \times \frac{\sqrt{V_{OUT_}[V] \times (V_{PVIN_} - V_{OUT_})[V]}}{V_{PVIN_}[V]}$$

The MAX15021 includes UVLO hysteresis to avoid possible unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. If using a lower input voltage, additional input capacitance helps to avoid possible undershoot below the undervoltage lockout threshold during transient loading.

Output-Capacitor Selection

The allowed output-voltage ripple and the maximum deviation of the output voltage during load steps determine the required output capacitance and its ESR. The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the equivalent series resistance of the output capacitor). The equations for calculating the output capacitance and its ESR are:

$$C_{OUT}[\mu F] = \frac{\Delta I_{P-P}[A]}{8 \times \Delta V_Q[V] \times f_{SW}[MHz]}$$

$$ESR[m\Omega] = \frac{2 \times \Delta V_{ESR}[mV]}{\Delta I_{P-P}[A]}$$

where ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

ΔV_{ESR} and ΔV_Q are not directly additive since they are out of phase from each other. If using ceramic capacitors, which generally have low ESR, ΔV_Q dominates. If using electrolytic capacitors, ΔV_{ESR} dominates.

The allowable deviation of the output voltage during fast load transients also affects the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with an increased duty cycle. The response time ($t_{RESPONSE}$) depends on the gain bandwidth of the controller (see the *Compensation-Design Guidelines* section). The resistive drop across the output capacitor's ESR (ΔV_{ESR}), the drop across the capacitor's ESL (ΔV_{ESL}), and the capacitor discharge (ΔV_Q) cause a voltage droop during the load-step (I_{STEP}). Use a combination of low-ESR tantalum/aluminum electrolyte and ceramic capacitors for better load transient and voltage ripple performance. Nonleaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the electronics being powered.

Use the following equations to calculate the required output capacitance, ESR, and ESL for minimal output deviation during a load step:

$$ESR[m\Omega] = \frac{\Delta V_{ESR}[mV]}{I_{STEP}[A]}$$

$$C_{OUT}[\mu F] = \frac{I_{STEP}[A] \times t_{RESPONSE}[\mu s]}{\Delta V_Q[V]}$$

$$ESL[nH] = \frac{\Delta V_{ESL}[mV] \times t_{STEP}[\mu s]}{I_{STEP}[A]}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller.

Compensation-Design Guidelines

The MAX15021 uses a fixed-frequency, voltage-mode control scheme that regulates the output voltage by comparing the output voltage against a fixed reference. The subsequent "error" voltage that appears at the error-amplifier output (COMP_) is compared against an internal ramp voltage to generate the required duty cycle of the pulse-width modulator. A second-order lowpass LC filter removes the switching harmonics and passes the DC component of the pulse-width-modulated signal to the output. The LC filter has an attenuation slope of -40dB/decade and introduces 180° of phase shift at frequencies above the LC resonant frequency. This phase shift in addition to the inherent 180° of phase shift of the regulator's negative feedback system turns the feedback into unstable positive feedback. The error amplifier and its associated circuitry must be designed to achieve a stable closed-loop system.

The basic controller loop consists of a power modulator (comprised of the regulator's pulse-width modulator, associated circuitry, and LC filter), an output feedback divider, and an error amplifier. The power modulator has a DC gain set by V_{AVIN}/V_{RAMP} where the ramp voltage (V_{RAMP}) is a function of the V_{AVIN} and results in a fixed DC gain of 4V/V, providing effective feed-forward compensation of input-voltage supply DC variations. The feed-forward compensation eliminates the dependency of the power modulator's gain on the input voltage such that the feedback compensation of the error amplifier requires no modifications for nominal input-voltage changes. The output filter is effectively modeled as a double-pole and a single zero set by the output inductance (L), the DC resistance of the inductor (DCR), the output capacitance (C_{OUT}) and its equivalent series resistance (ESR).

Below are equations that define the power modulator:

$$Gain_{MOD(DC)} = \frac{V_{AVIN}}{V_{RAMP}} = \frac{V_{AVIN}}{\frac{V_{AVIN}}{4}} = 4V/V$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT} \times \left(\frac{R_{OUT} + ESR}{R_{OUT} + DCR}\right)}} \approx \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

R_{OUT} is the load resistance of the regulator, f_{LC} is the resonant break frequency of the filter, and f_{ESR} is the ESR zero of the output capacitor. See the *Closed-Loop Response and Compensation of Voltage-Mode Regulators* section for more information on f_{LC} and f_{ESR}.

The switching frequency (f_{SW}) is programmable between 500kHz and 4MHz. Typically, the crossover frequency (f_{CO})—the frequency at which the system's closed-loop gain is equal to unity (crosses 0dB)—should be set at or below one-tenth the switching frequency (f_{SW}/10) for stable closed-loop response.

The MAX15021 provides an internal voltage-mode error amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each controller offers a wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use aluminum electrolytic capacitors while for space-sensitive applications, use low-ESR tantalum or multilayer ceramic chip (MLCC) capacitors at the output. The higher switching frequencies of the MAX15021 allow the use of MLCC as the primary filter capacitor(s).

First, select the passive and active power components that meet the application output ripple, component size, and component cost requirements. Second, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined below.

Closed-Loop Response and Compensation of Voltage-Mode Regulators

The power modulator's LC lowpass filter exhibits a variety of responses, dependent on the value of the L and C and their parasitics. Higher resistive parasitics reduce the Q of the circuit, reducing the peak gain and phase of the system; however, efficiency is also reduced under these circumstances.

One such response is shown in Figure 4a. In this example, the ESR zero occurs relatively close to the filter's resonant break frequency, f_{LC}. As a result, the power modulator's uncompensated crossover is approximately one-third the desired crossover frequency, f_{CO}. Note also, the uncompensated rolloff through the 0dB plane follows a single-pole, -20dB/decade slope, and 90° of phase lag. In this instance, the inherent phase margin ensures a stable system; however, the gain-bandwidth product is not optimized.

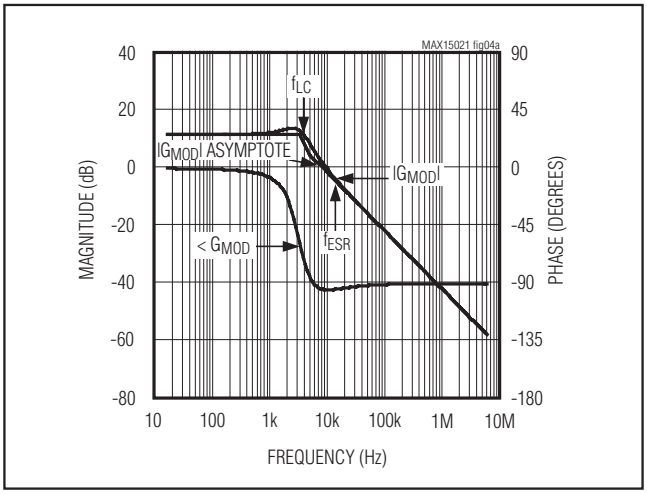


Figure 4a. Power Modulator Gain and Phase Response with Lossy Bulk Output Capacitor(s) (Aluminum)

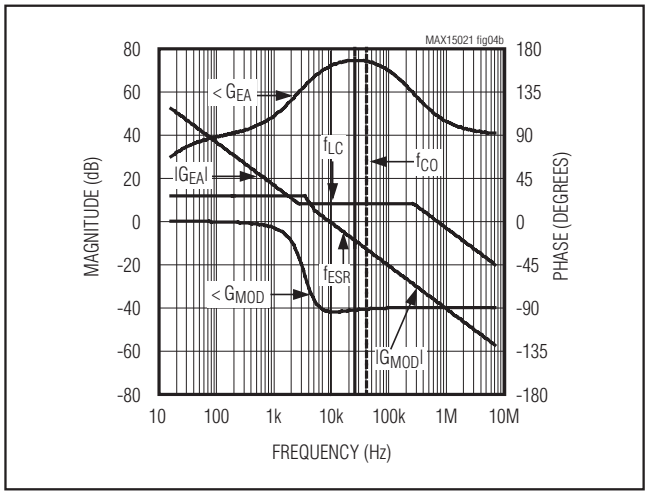


Figure 4b. Power Modulator and Type II Compensator Gain and Phase Response with Lossy Bulk Output Capacitor(s) (Aluminum)

As seen in Figure 4b, a Type II compensator provides for stable closed-loop operation, leveraging the +20dB/decade slope of the capacitor's ESR zero, while extending the closed-loop gain-bandwidth of the regulator. The zero crossover now occurs at approximately three times the uncompensated crossover frequency, f_{CO}.

The Type II compensator's midfrequency gain (approximately 12dB shown here) is designed to compensate for the power modulator's attenuation at the desired crossover frequency, f_{CO} ($Gain_{E/A}$ + $Gain_{MOD}$ = 0dB at f_{CO}). In this example, the power modulator's inherent -20dB/decade rolloff above the ESR zero ($f_{ZERO,ESR}$) is leveraged to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 4b, the net result is a three times increase in the regulator's gain bandwidth while providing greater than 75° of phase margin (the difference between $Gain_{E/A}$ and $Gain_{MOD}$ respective phases at crossover, f_{CO}).

Other filter schemes pose their own problems. For instance, when choosing high-quality filter capacitor(s), e.g. MLCCs, the inherent ESR zero may occur at a much higher frequency, as shown in Figure 4c.

As with the previous example, the actual gain and phase response is overlaid on the power modulator's asymptotic gain response. One readily observes the more dramatic gain and phase transition at or near the power modulator's resonant frequency, f_{LC}, versus the gentler response of the previous example. This is due to the filter components' lower parasitic (DCR and ESR) and corresponding higher frequency of the inherent ESR zero. In this example, the desired crossover frequency occurs below the ESR zero frequency.

In this example, a compensator with an inherent midfrequency double-zero response is required to mitigate the effects of the filter's double-pole phase lag. This is available with the Type III topology.

As demonstrated in Figure 4d, the Type III's midfrequency double-zero gain (exhibiting a +20dB/dec slope, noting the compensator's pole at the origin) is designed to compensate for the power modulator's double-pole -40dB/decade attenuation at the desired crossover frequency, f_{CO} (again, $Gain_{E/A}$ + $Gain_{MOD}$ = 0dB at f_{CO}) (see Figure 4d).

In the above example the power modulator's inherent (midfrequency) -40dB/decade rolloff is mitigated by the midfrequency double zero's +20dB/decade gain to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 4d, the net result is an approximate doubling in the controller's gain bandwidth while providing greater than 55 degrees of phase margin (the difference between $Gain_{E/A}$ and $Gain_{MOD}$ respective phases at crossover, f_{CO}).

Design procedures for both Type II and Type III compensators are shown below.

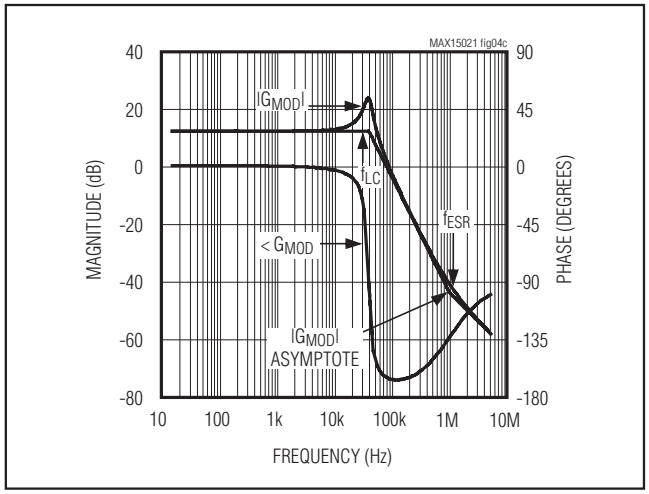


Figure 4c. Power Modulator Gain and Phase Response with Low-Parasitic Capacitor(s) (MLCCs)

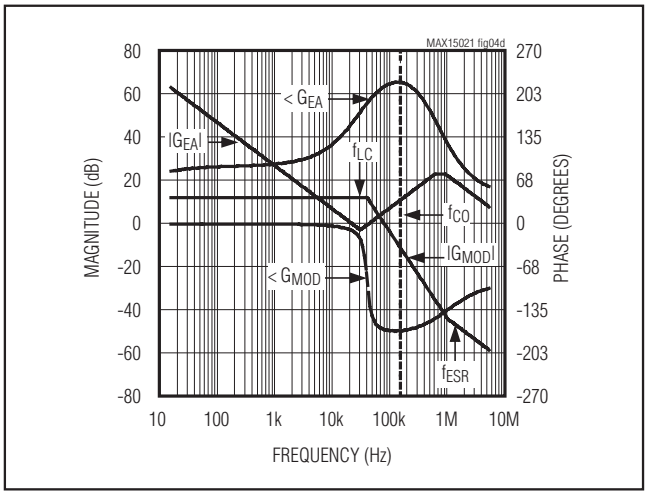


Figure 4d. Power Modulator and Type III Compensator Gain and Phase Response with Low Parasitic Capacitors (MLCCs)

Type II: Compensation when fCO > fZERO,ESR

When the f_{CO} is greater than f_{ESR}, a Type II compensation network provides the necessary closed-loop compensated response. The Type II compensation network provides a midband compensating zero and a high-frequency pole (see Figures 5a and 5b).

R_FC_F provides the midband zero $f_{MID,ZERO}$, and R_FC_{CF} provides the high-frequency pole, $f_{HIGH,POLE}$. Use the following procedure to calculate the compensation network components.

Calculate the f_{ESR} and LC double pole, f_{LC}:

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} \approx \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

where C_{OUT} is the regulator output capacitor and ESR is the series resistance of C_{OUT}. See the *Output-Capacitor Selection* section for more information on calculating C_{OUT} and ESR.

Set the compensator's leading zero, f_{Z1}, at or below the filter's resonant double-pole frequency from:

$$f_{Z1} \le f_{LC}$$

Set the compensator's high-frequency pole, f_{P1}, at or below one-half the switching frequency, f_{SW}:

$$f_{P1} \le \frac{f_{SW}}{2}$$

To maximize the compensator's phase lead, set the desired crossover frequency, f_{CO}, equal to the geometric mean of the compensator's leading zero, f_{Z1}, and high-frequency pole, f_{P1}, as follows:

$$f_{CO} = \sqrt{f_{Z1} \times f_{P1}}$$

Select the feedback resistor, R_F, in the range of 3.3kΩ to 30kΩ.

Calculate the gain of the modulator ($Gain_{MOD}$)—comprised of the regulator's pulse-width modulator, LC filter, feedback divider, and associated circuitry—at the desired crossover frequency, f_{CO}, using the following equation:

$$Gain_{MOD} = 4(V/V) \times \frac{ESR\ [m\Omega]}{(2\pi \times f_{CO}[kHz] \times L[\mu H])} \times \frac{V_{FB}[V]}{V_{OUT_}[V]}$$

where V_{FB} is the 0.6V (typ) FB_ input-voltage set-point, L is the value of the regulator inductor, ESR is the series resistance of the output capacitor, and $V_{OUT_}$ is the desired output voltage.

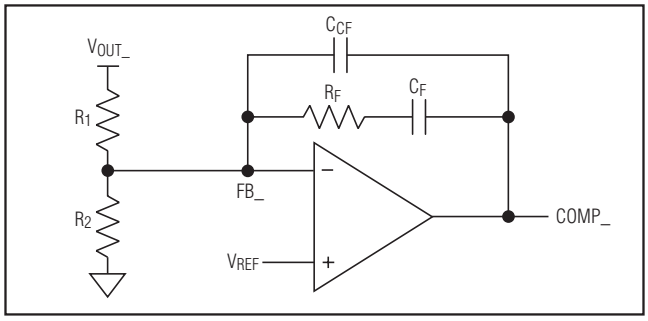


Figure 5a. Type II Compensation Network

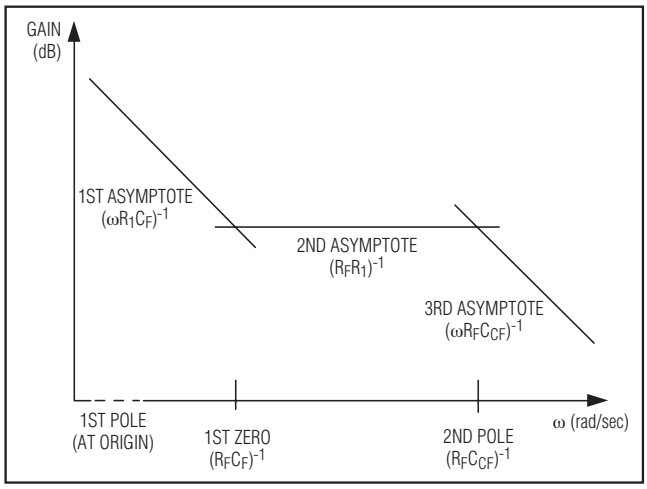


Figure 5b. Type II Compensation Network Response

The gain of the error amplifier ($Gain_{E/A}$) in the midband frequencies is:

$$Gain_{E/A} = \frac{R_F\ [k\Omega]}{R_1\ [k\Omega]}$$

The total loop gain is the product of the modulator gain and the error amplifier gain at f_{CO} and should be set equal to 1 as follows:

$$Gain_{MOD} \times Gain_{E/A} = 1$$

So:

$$20 \times \log_{10}\left[\frac{R_F}{R_1}\right] + 20 \times \log_{10}\left[\frac{4 \times ESR \times V_{FB}}{2\pi \times f_{CO} \times L \times V_{OUT_}}\right] = 0dB$$

$$\frac{R_F}{R_1} \times \frac{4 \times ESR \times V_{FB}}{2\pi \times f_{CO} \times L \times V_{OUT_}} = 1$$

Solving for R_1:

$$R_1\,[k\Omega] = \frac{R_F[k\Omega] \times 4 \times ESR[m\Omega] \times V_{FB}[V]}{2\pi \times f_{CO}[kHz] \times L[\mu H] \times V_{OUT_}[V]}$$

where V_{FB} is the 0.6V (typ) FB_ input-voltage set-point, L is the value of the regulator inductor, ESR is the series resistance of the output capacitor, and $V_{OUT_}$ is the desired output voltage.

1) C_F is determined from the compensator's leading zero, f_{Z1}, and R_F as follows:

$$C_F[\mu F] = \frac{1}{2\pi \times R_F[k\Omega] \times f_{Z1}[kHz]}$$

2) C_{CF} is determined from the compensator's high-frequency pole, f_{P1}, and R_F as follows:

$$C_{CF}[\mu F] = \frac{1}{2\pi \times R_F[k\Omega] \times f_{P1}[kHz]}$$

3) Calculate R_2 using the following equation:

$$R_2[k\Omega] = R_1[k\Omega] \times \frac{V_{FB}\,[V]}{V_{OUT_}[V] - V_{FB}[V]}$$

where V_{FB} = 0.6V (typ) and $V_{OUT_}$ is the output voltage of the regulator.

Type III: Compensation when fCO < fESR

As indicated above, the position of the output capacitor's inherent ESR zero is critical in designing an appropriate compensation network. When low-ESR ceramic output capacitors (MLCCs) are used, the ESR zero frequency (f_{ESR}) is usually much higher than the desired crossover frequency (f_{CO}). In this case, a type III compensation network is recommended (see Figure 6a).

As shown in Figure 6b, the Type III compensation network introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole at the origin, two zeros, and two higher frequency poles at the following frequencies:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$$

$$f_{Z2} = \frac{1}{2\pi \times C_I \times (R_1 + R_I)}$$

Two midband zeros (f_{Z1} and f_{Z2}) are designed to compensate for the pair of complex poles introduced by the LC filter.

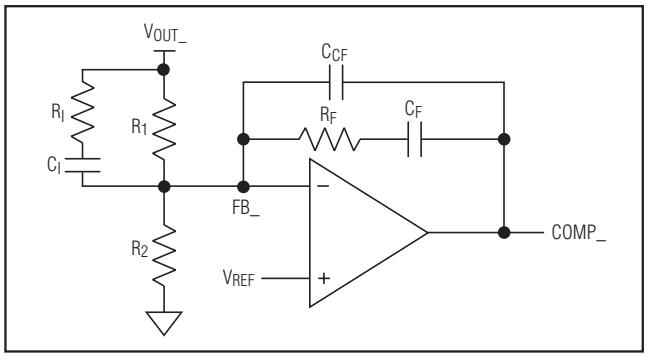


Figure 6a. Type III Compensation Network

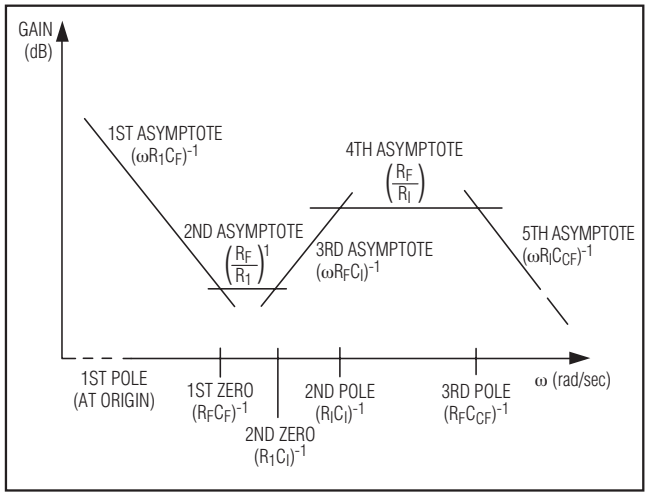


Figure 6b. Type III Compensation Network Response

f_{P1} introduces a pole at zero frequency (integrator) for nulling DC output voltage errors.

f_{P1}= at the origin (0Hz)

Depending on the location of the ESR zero (f_{ESR}), f_{P2} can be used to cancel it, or to provide additional attenuation of the high-frequency output ripple.

$$f_{P2} = \frac{1}{2\pi \times R_I \times C_I}$$

f_{P3} attenuates the high-frequency output ripple.

$$f_{P3} = \frac{1}{2\pi \times R_F \times \left(C_F \| C_{CF}\right)} = \frac{1}{2\pi \times R_F \times \frac{C_F \times C_{CF}}{C_F + C_{CF}}}$$

Since $C_{CF} << C_F$ then:

$$f_{P3} = \frac{1}{2\pi \times R_F \times C_{CF}}$$

The locations of the zeros and poles should be such that the phase margin peaks around f_{CO}.

Set the ratios of f_{CO}-to-f_Z and f_P-to-f_{CO} equal to one another, e.g., $\frac{f_{CO}}{f_Z} = \frac{f_P}{f_{CO}} = 5$ is a good number to get approximately 60° of phase margin at f_{CO}. Whichever technique, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

The following procedure is recommended:

1) Select a crossover frequency, f_{CO}, at or below one-tenth the switching frequency (f_{SW}):

$$f_{CO}[kHz] \le \frac{f_{SW}[kHz]}{10}$$

2) Calculate the LC double-pole frequency, f_{LC} :

$$f_{LC}[MHz] \approx \frac{1}{2\pi \times \sqrt{L[\mu H] \times C_{OUT}[\mu F]}}$$

where C_{OUT} is the output capacitor of the regulator.

3) Select the feedback resistor, R_F, in the range of 3.3kΩ to 30kΩ.

4) Place the compensator's first zero at or below the output filter's double-pole, f_{LC} , as follows:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$$

$$C_F[\mu F] = \frac{1}{2\pi \times R_F[k\Omega] \times 0.5 \times f_{LC}[kHz]}$$

5) The gain of the modulator ($Gain_{MOD}$)—comprised of the regulator's pulse-width modulator, LC filter, feedback divider, and associated circuitry—at the crossover frequency is:

$$Gain_{MOD} = 4 \times \frac{1}{(2\pi \times f_{CO}[MHz])^2 \times L[\mu H] \times C_{OUT}[\mu F]}$$

The gain of the error amplifier ($Gain_{E/A}$) in midband frequencies is:

$$Gain_{E/A} = 2\pi \times f_{CO}[kHz] \times C_I[\mu F] \times R_F[k\Omega]$$

The total loop gain is the product of the modulator gain and the error amplifier gain at f_{CO} should be equal to 1, as follows:

$$Gain_{MOD} \times Gain_{E/A} = 1$$

So:

$$4 \times \frac{1}{(2\pi \times f_{CO}[kHz])^2 \times C_{OUT}[\mu F] \times L[\mu H]} \times 2\pi \times f_{CO}[kHz] \times C_I[pF] \times R_F[k\Omega] = 1$$

Solving for C_I:

$$C_I[pF] = \frac{(2\pi \times f_{CO}[kHz] \times L[\mu H] \times C_{OUT}[\mu F])}{4 \times R_F[k\Omega]}$$

6) For those situations where $f_{LC} < f_{CO} < f_{ESR} < f_{SW}/2$, as with low-ESR tantalum capacitors, the compensator's second pole (f_{P2}) should be used to cancel f_{ESR}. This provides additional phase margin. On the system Bode plot, the loop gain maintains its +20dB/decade slope up to $^1/_2$ of the switching frequency verses flattening out soon after the 0dB crossover. Then set:

$$f_{P2} = f_{ESR}$$

If a ceramic capacitor is used, then the capacitor ESR zero, f_{ESR}, is likely to be located even above one-half of the switching frequency, that is $f_{LC} < f_{CO} < f_{SW}/2 < f_{ESR}$. In this case, the frequency of the second pole (f_{P2}) should be placed high enough not to significantly erode the phase margin at the crossover frequency. For example, f_{P2} can be set at 5 x f_{CO}, so that its contribution to phase loss at the crossover frequency f_{CO} is only about 11°:

$$f_{P2} = 5 \times f_{CO}$$

Once f_{P2} is known, calculate R_I:

$$R_I[k\Omega] = \frac{1}{2\pi \times f_{P2}[kHz] \times C_I[\mu F]}$$

7) Place the second zero (f_{Z2}) at 0.2 x f_{CO} or at f_{LC}, whichever is lower, and calculate R_1 using the following equation:

$$R_1[k\Omega] = \frac{1}{2\pi \times f_{Z2}[kHz] \times C_I[\mu F]}$$

8) Place the third pole (f_{P3}) at 1/2 the switching frequency and calculate C_{CF} from:

$$C_{CF}[nF] = \frac{1}{(2\pi \times 0.5 \times f_{SW}[MHz] \times R_F[k\Omega])}$$

9) Calculate R_2 as:

$$R_2[k\Omega] = R_1[k\Omega] \times \frac{V_{FB}[V]}{V_{OUT_}[V] - V_{FB}[V]}$$

where V_{FB} = 0.6V (typ).

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close as possible to the IC pins.
2) Keep SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
3) Route high-speed switching nodes away from sensitive analog areas (FB_, COMP_, and EN_).
4) Distribute the power components evenly across the board for proper heat dissipation.
5) Ensure timing resistor and all feedback connections are short and direct. Place feedback resistors as close as possible to the IC.
6) Place the bank of the output capacitors close to the load.
7) Connect the MAX15021 exposed pad to a large copper plane to maximize its power dissipation capability. Connect the exposed pad to SGND plane. Do not connect the exposed pad to the SGND pin directly underneath the IC.
8) Use 2oz. copper to keep trace inductance and resistance to a minimum. Thin copper PCBs can compromise efficiency since high currents are involved in the application. Also thicker copper conducts heat more effectively, thereby reducing thermal impedance.
9) A reference PCB layout included in the MAX15021 Evaluation Kit is also provided to further aid layout.

Typical Operating Circuits

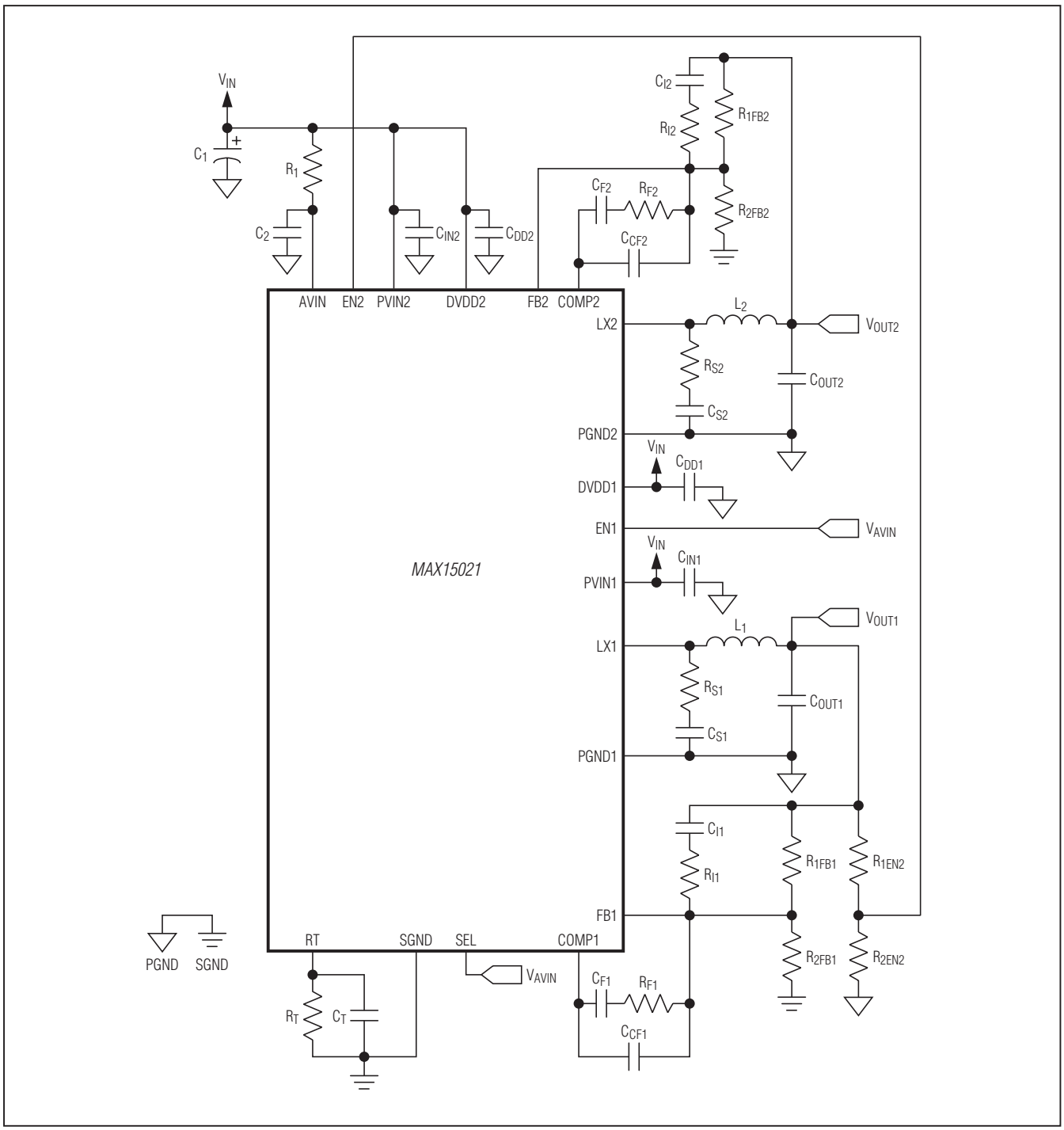


Figure 7. MAX15021 Double Buck with Tracking

Typical Operating Circuits (continued)

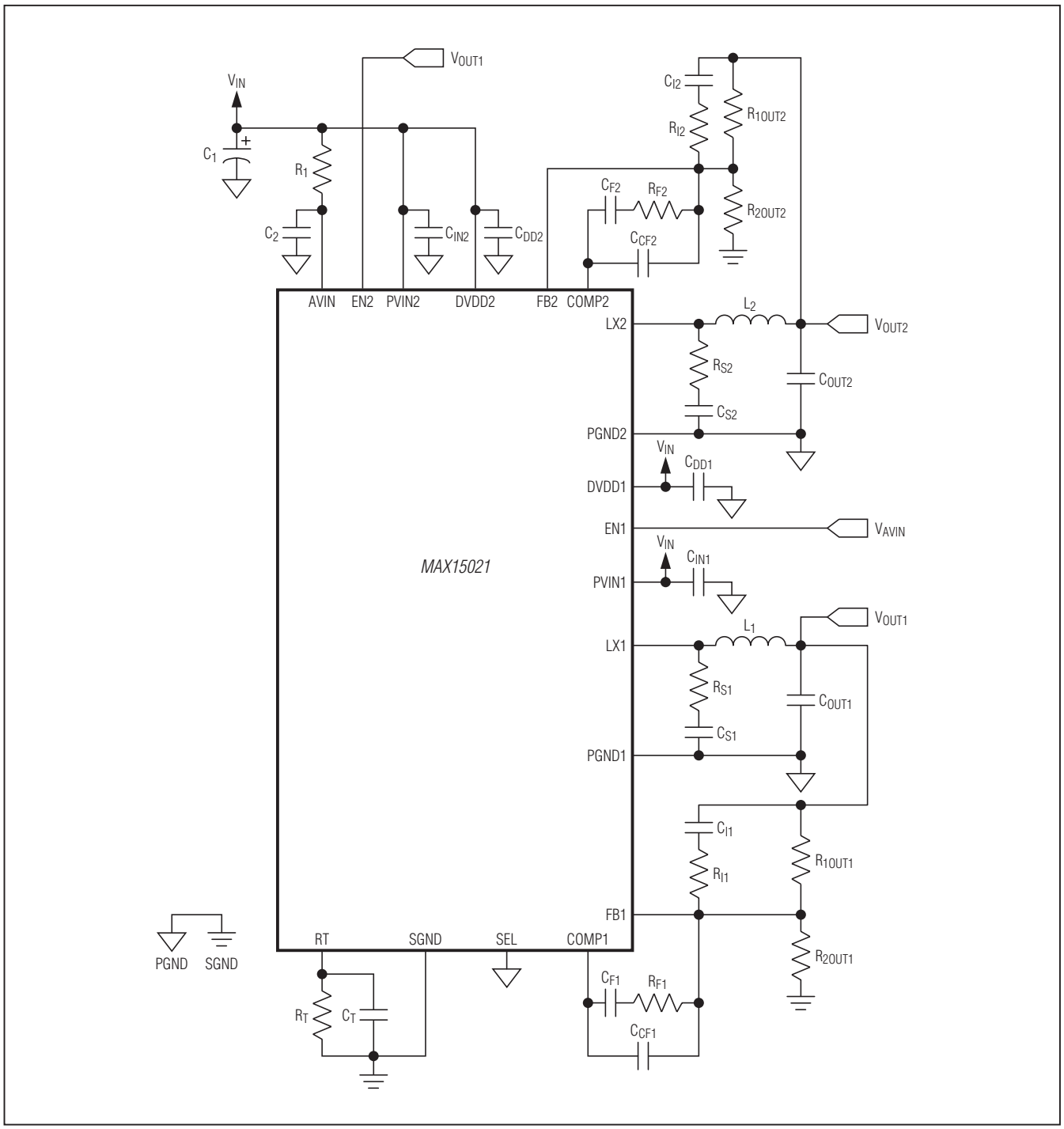


Figure 8. MAX15021 Double Buck with Sequencing

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+6	**21-0140**	**90-0026**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	8/12	Added automotive qualified part to *Ordering Information*	1
2	4/15	Updated *Benefits and Features* section	1

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