# MAX15023

# Wide 4.5V to 28V Input, Dual-Output Synchronous Buck Controller

## General Description

The MAX15023 dual, synchronous step-down controller operates from a 5.5V to 28V or 5V ±10% input voltage range and generates two independent output voltages. Each output is adjustable from 85% of the input voltage down to 0.6V and supports loads of 12A or higher. Input voltage ripple and total RMS input ripple current are reduced by interleaved 180° out-of-phase operation.

The MAX15023 offers the ability to adjust the switching frequency from 200kHz to 1MHz with an external resistor. The MAX15023's adaptive synchronous rectification eliminates the need for external freewheeling Schottky diodes. The device also utilizes the external low-side MOSFET's on-resistance as a current-sense element, eliminating the need for a current-sense resistor. This protects the DC-DC components from damage during output overloaded conditions or output short-circuit faults without requiring a current-sense resistor. Hiccup-mode current limit reduces power dissipation during short-circuit conditions. The MAX15023 includes two independent power-good outputs and two independent enable inputs with precise turn-on/turn-off thresholds, which can be used for supply monitoring and for power sequencing.

Additional protection features include cycle-by-cycle, low-side, sink peak current limit, and thermal shutdown. Cycle-by-cycle, low-side, sink peak current limit prevents reverse inductor current from reaching dangerous levels when the device is sinking current from the output. The MAX15023 also allows prebiased startup without discharging the output and features adaptive internal digital soft-start. This new proprietary feature enables monotonic charging of externally large output capacitors at startup, and achieves good control of the peak inductor current during hiccup-mode short-circuit protection.

The MAX15023 is available in a space-saving and thermally enhanced 4mm x 4mm, 24-pin TQFN-EP package. The device operates over the -40°C to +85°C extended temperature range.

## Applications

- Point-of-Load Regulators
- Set-Top Boxes
- LCD TV Secondary Supplies
- Switches/Routers
- Power Modules
- DSP Power Supplies

## Features

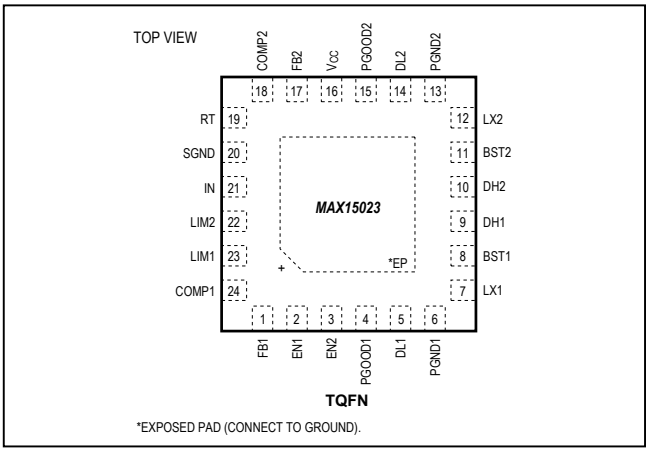
- 5.5V to 28V or 5V ±10% Input Supply Range
- 0.6V to (0.85 x $V_{IN}$) Adjustable Outputs
- Adjustable 200kHz to 1MHz Switching Frequency
- Guaranteed Monotonic Startup into a Prebiased Load
- Lossless, Cycle-by-Cycle, Low-Side, Source Peak Current Limit with Adjustable, Temperature-Compensated Threshold
- Cycle-by-Cycle, Low-Side, Sink Peak Current-Limit Protection
- Proprietary Adaptive Internal Digital Soft-Start
- ±1% Accurate Voltage Reference
- Internal Boost Diodes
- Adaptive Synchronous Rectification Eliminates External Freewheeling Schottky Diodes
- Hiccup-Mode Short-Circuit Protection and Thermal Shutdown
- Power-Good Outputs and Analog Enable Inputs for Power Sequencing

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX15023ETG+ | -40°C to +85°C | 24 TQFN-EP* |
| MAX15023ETG/V+ | -40°C to +85°C | 24 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*
*/V denotes an automotive qualified package.*

## Pin Configuration






maxim integrated™

## Absolute Maximum Ratings

IN to SGND ..... -0.3V to +30V
BST_ to $V_{CC}$ ..... -0.3V to +30V
LX_ to SGND ..... -1V to +30V
EN_ to SGND ..... -0.3V to +6V
PGOOD_ to SGND ..... -0.3V to +30V
BST_ to LX_ ..... -0.3V to +6V
DH_ to LX_ ..... -0.3V to ($V_{BST_}$ + 0.3V)
DL_ to PGND_ ..... -0.3V to ($V_{CC}$ + 0.3V)
SGND to PGND_ ..... -0.3V to +0.3V
$V_{CC}$ to SGND ..... -0.3V to the lower of +6V or ($V_{IN}$ + 0.3V)
All Other Pins to SGND ..... -0.3V to ($V_{CC}$ + 0.3V
$V_{CC}$ Short Circuit to SGND ..... Continuou
$V_{CC}$ Input Current (IN = $V_{CC}$, internal LDO not used) ..... 600mA
PGOOD_ Sink Current ..... 20mA
Continuous Power Dissipation ($T_A$ = +70°C)(Note 1)
24-Pin TQFN-EP (derate 27.8mW/°C above +70°C) .. 2222.2mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: These power limits are due to the thermal characteristics of the package, absolute maximum junction temperature (150°C), and the JEDEC 51-7 defined setup. Maximum power dissipation could be lower, limited by the thermal shutdown protection included in this IC.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 2)

24 TQFN-EP
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....+36°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....+8°C/W

**Note 2**: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **http://www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{IN}$ = 12V, $R_T$ = 33kΩ, $C_{VCC}$ = 4.7µF, $C_{IN}$ = 1µF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 5.5 | | 28 | V |
| | | $V_{IN}$ = $V_{CC}$ | 4.5 | | 5.5 | |
| Quiescent Supply Current | $I_{IN}$ | $V_{FB1}$ = $V_{FB2}$ = 0.9V, no switching | | 4.5 | 6 | mA |
| Standby Supply Current | $I_{IN_SBY}$ | $V_{EN1}$ = $V_{EN2}$ = $V_{SGND}$ | | 0.21 | 0.35 | mA |
| **$V_{CC}$ REGULATOR** | | | | | | |
| Output Voltage | $V_{CC}$ | 6V < $V_{IN}$ < 28V, $I_{LOAD}$ = 5mA | 5.00 | 5.2 | 5.50 | V |
| | | $V_{IN}$ = 6V, 1mA < $I_{LOAD}$ < 100mA | | | | |
| $V_{CC}$ Regulator Dropout | | $I_{LOAD}$ = 100mA | | 0.07 | | V |
| $V_{CC}$ Short-Circuit Output Current | | $V_{IN}$ = 5V | 150 | 250 | | mA |
| $V_{CC}$ Undervoltage Lockout | $V_{CC_UVLO}$ | $V_{CC}$ falling | 3.6 | 3.8 | 4 | V |
| $V_{CC}$ Undervoltage Lockout Hysteresis | | | | 430 | | mV |
| **ERROR AMPLIFIER (FB_, COMP_)** | | | | | | |
| FB_ Input Voltage Set-Point | $V_{FB_}$ | | 594 | 600 | 606 | mV |
| FB_ Input Bias Current | $I_{FB_}$ | $V_{FB_}$ = 0.6V | -250 | | +250 | nA |

## Electrical Characteristics (continued)

($V_{IN}$ = 12V, $R_T$ = 33kΩ, $C_{VCC}$ = 4.7µF, $C_{IN}$ = 1µF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| FB to COMP Transconductance | $g_m$ | $I_{COMP}$ = ±40µA | | 650 | 1200 | 1900 | µS |
| Amplifier Open-Loop Gain | | No load | | | 80 | | dB |
| Amplifier Unity-Gain Bandwidth | | | | | 10 | | MHz |
| COMP_ Swing (High) | | | | | 2.4 | | V |
| COMP_ Swing (Low) | | No load at COMP_ | | | 0.6 | | V |
| COMP_ Source/Sink Current | $I_{COMP_}$ | $\lvert I_{COMP_} \rvert$, $V_{COMP_}$ = 1.5V | | 45 | 80 | 120 | µA |
| ENABLE (EN_) | | | | | | | |
| EN_ Input High | $V_{EN_H}$ | EN_ rising | | 1.15 | 1.20 | 1.25 | V |
| EN_ Input Hysteresis | $V_{EN_HYS}$ | | | | 150 | | mV |
| EN_ Input Leakage Current | $I_{LEAK_EN_}$ | | | -250 | | +250 | nA |
| **OSCILLATOR** | | | | | | | |
| Switching Frequency | $f_{SW}$ | Each converter | | 460 | 500 | 540 | kHz |
| Switching Frequency Adjustment Range | | (Note 4) | | 200 | | 1000 | kHz |
| PWM Ramp Peak-to-Peak Amplitude | $V_{RAMP}$ | | | | 1.42 | | V |
| PWM Ramp Valley | $V_{VALLEY}$ | | | | 0.72 | | V |
| Phase Shift Between Channels | | From DH1 to DH2 rising edges | | | 180 | | Degrees |
| Minimum Controllable On-Time | | | | | 60 | 100 | ns |
| Maximum Duty Cycle | | | | 86 | 87.5 | | % |
| **OUTPUT DRIVERS** | | | | | | | |
| DH_ On-Resistance | | Low, sinking 100mA, $V_{BST_}$ - $V_{LX_}$ = 5V | | | 1 | | Ω |
| | | High, sourcing 100mA, $V_{BST_}$ - $V_{LX_}$ = 5V | | | 1.2 | | |
| DL_ On-Resistance | | Low, sinking 100mA, $V_{CC}$ = 5.2V | | | 0.75 | | Ω |
| | | High, sourcing 100mA, $V_{CC}$ = 5.2V | | | 1.4 | | |
| DH_ Peak Current | | $C_{LOAD}$ = 10nF | Sinking | | 3 | | A |
| | | | Sourcing | | 2 | | |
| DL_ Peak Current | | $C_{LOAD}$ = 10nF | Sinking | | 3 | | A |
| | | | Sourcing | | 2 | | |
| DH_, DL_ Break-Before-Make Time (Dead Time) | | | | | 15 | | ns |
| **SOFT-START** | | | | | | | |
| Soft-Start Duration | | | | | 2048 | | Switching cycles |
| Reference Voltage Steps | | | | | 64 | | Steps |

## Electrical Characteristics (continued)

($V_{IN}$ = 12V, $R_T$ = 33kΩ, $C_{VCC}$ = 4.7µF, $C_{IN}$ = 1µF, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT/HICCUP** | | | | | | |
| Cycle-by-Cycle, Low-Side, Source Peak Current-Limit Threshold Adjustment Range | | Source peak limit = $V_{LIM_}$/10 | 30 | | 300 | mV |
| LIM_ Reference Current | $I_{LIM_}$ | $V_{LIM_}$ = 0.3V to 3V, $T_A$ = +25°C | 45 | 50 | 55 | µA |
| LIM_ Reference Current TC | | $V_{LIM_}$ = 0.3V | | 2400 | | ppm/°C |
| Number of Consecutive Current-Limit Events to Hiccup | | | | 7 | | Events |
| Hiccup Timeout | | Out of soft-start | | 7936 | | Switching cycles |
| Cycle-by-Cycle, Low-Side, Sink Peak Current-Limit Sense Voltage | | | | $V_{LIM_}$/20 | | V |
| **BOOST** | | | | | | |
| Boost Switch Resistance | | $V_{IN}$ = $V_{CC}$ = 5.2V, $I_{BST_}$ = 10mA | | 4.5 | 8 | Ω |
| **POWER-GOOD OUTPUTS** | | | | | | |
| PGOOD_ Threshold | | $V_{FB_}$ rising | 88.5 | 92.5 | 96.5 | % $V_{FB(NOMINAL)}$ |
| | | $V_{FB_}$ falling | 85.5 | 89.5 | 93.5 | |
| PGOOD_ Output Leakage | $I_{LEAK_PGD}$ | $V_{PGOOD_}$ = 28V, $V_{EN_}$ = 5V, $V_{FB_}$ = 0.8V | | | 1 | µA |
| PGOOD_ Output Low Voltage | $V_{PGOOD_L}$ | $I_{PGOOD_}$ = 2mA, EN_ = SGND | | | 0.4 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Threshold | | | | +150 | | °C |
| Thermal Shutdown Hysteresis | | Temperature falling | | 20 | | °C |

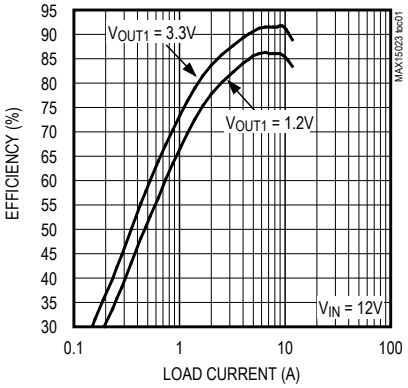
**Note 3:** All *Electrical Characteristics* limits over temperature are 100% tested at room tempture and guaranteed by design over the specified temperature range.

**Note 4:** Select $R_T$ as $R_T(k\Omega) = \frac{24806}{(f_{SW}(kHz))1.0663}$ (24806 has a $\frac{1}{farad}$ unit).

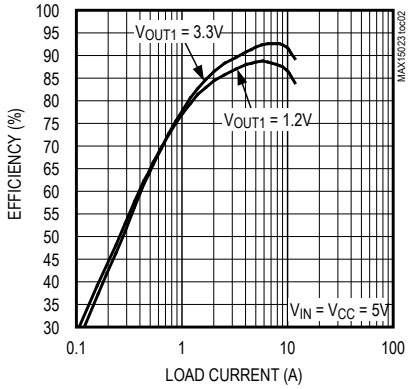
## Typical Operating Characteristics

(Supply = IN = 12V, unless otherwise noted. See *Typical Application Circuit* of Figure 6.)

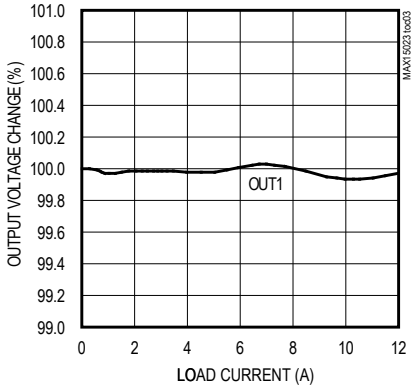
**EFFICIENCY vs. LOAD CURRENT**



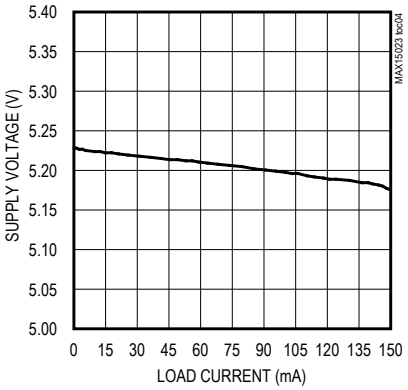

**EFFICIENCY vs. LOAD CURRENT**



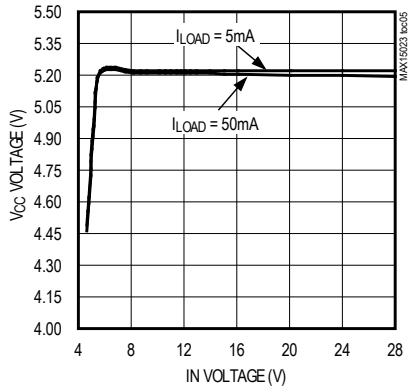

**OUTPUT VOLTAGE CHANGE vs. LOAD CURRENT**



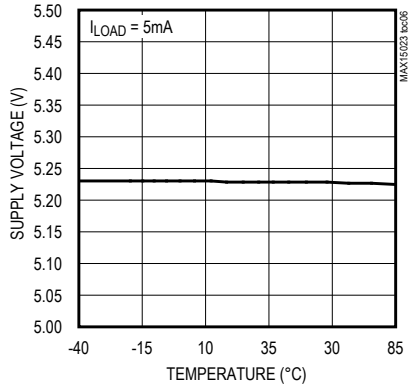

**VCC VOLTAGE vs. LOAD CURRENT**



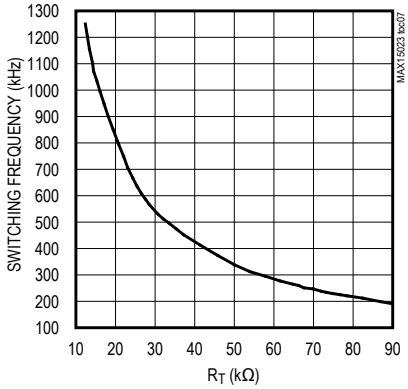

**VCC VOLTAGE vs. IN VOLTAGE**



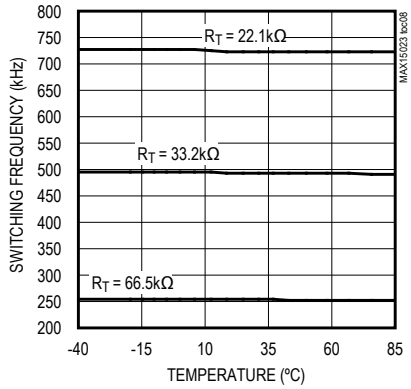

**VCC VOLTAGE vs. TEMPERATURE**



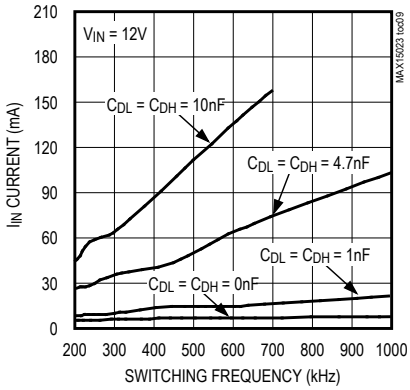

**SWITCHING FREQUENCY vs. RT**




**SWITCHING FREQUENCY vs. TEMPERATURE**



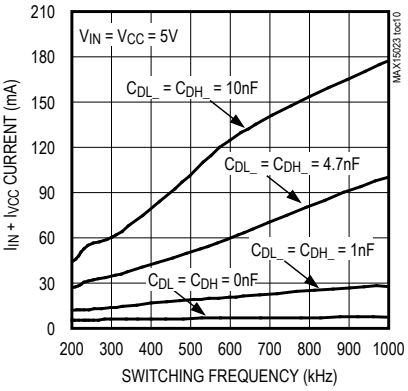

**IIN CURRENT vs. SWITCHING FREQUENCY**



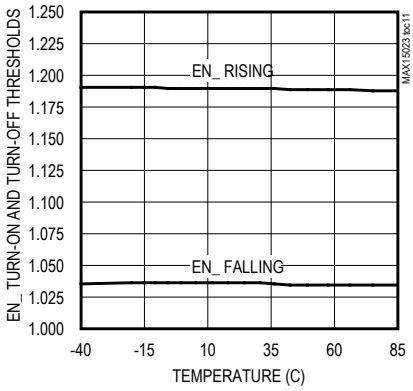
## Typical Operating Characteristics (continued)

(Supply = IN = 12V, unless otherwise noted. See *Typical Application Circuit* of Figure 6.)

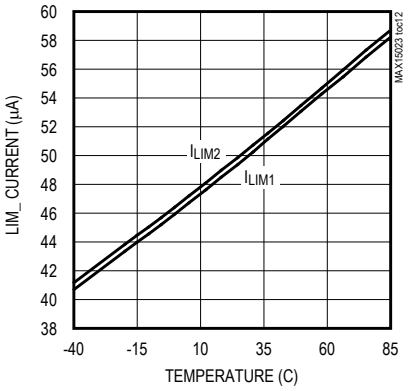
**$I_{IN}$ + $I_{VCC}$ CURRENT vs. SWITCHING FREQUENCY**



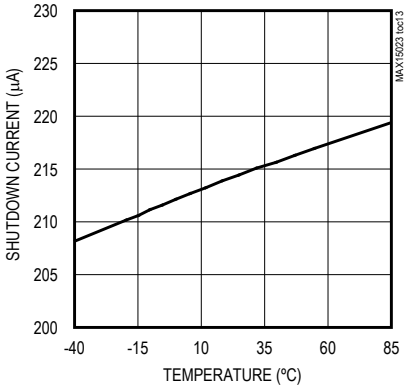

**EN_ TURN-ON AND TURN-OFF THRESHOLD vs. TEMPERATURE**



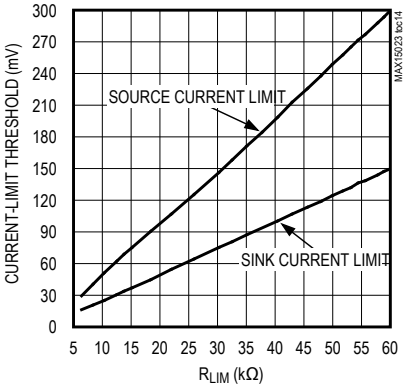

**LIM_ CURRENT vs. TEMPERATURE**



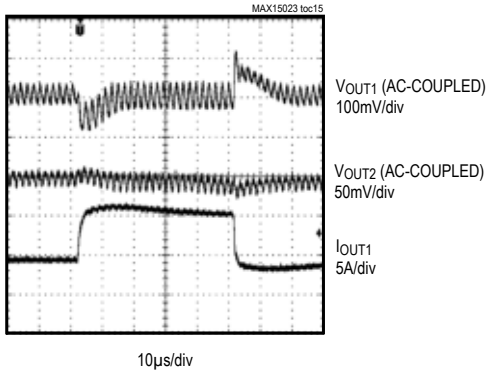

**SHUTDOWN CURRENT vs. TEMPERATURE**



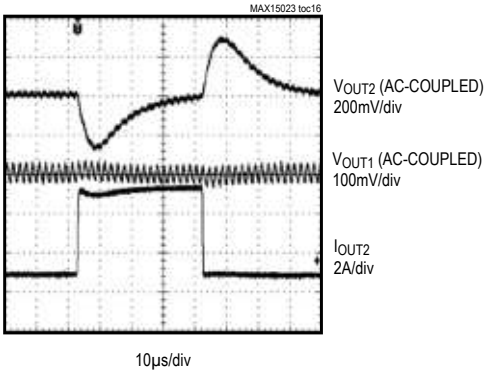

**CURRENT-LIMIT THRESHOLD vs. $R_{LIM}$**




**LOAD TRANSIENT ON OUT1**



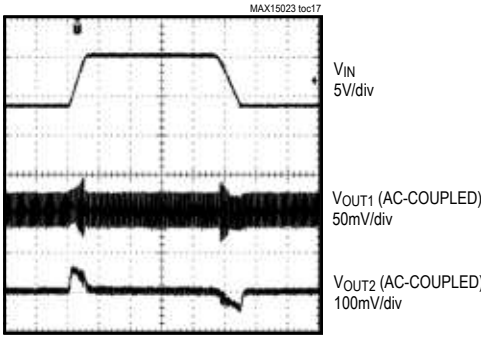

**LOAD TRANSIENT ON OUT2**



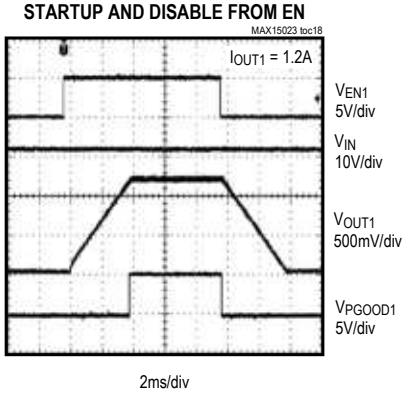
## Typical Operating Characteristics (continued)

(Supply = IN = 12V, unless otherwise noted. See *Typical Application Circuit* of Figure 6.)

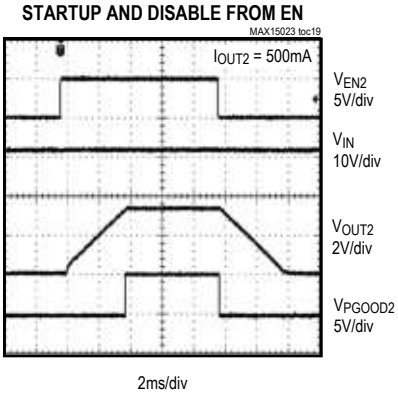
**LINE-TRANSIENT RESPONSE**



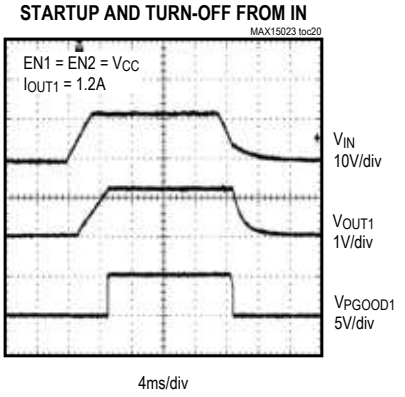

**STARTUP AND DISABLE FROM EN**



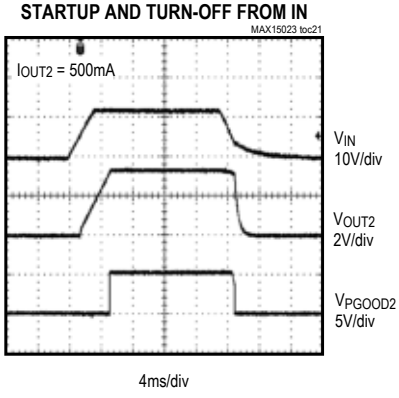

**STARTUP AND DISABLE FROM EN**



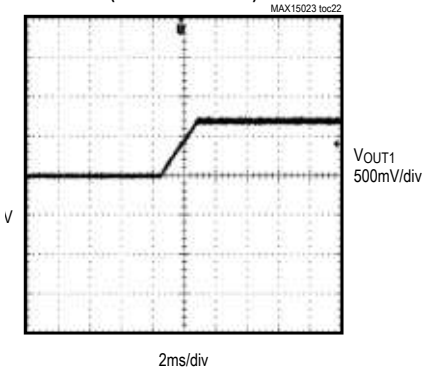

**STARTUP AND TURN-OFF FROM IN**




**STARTUP AND TURN-OFF FROM IN**



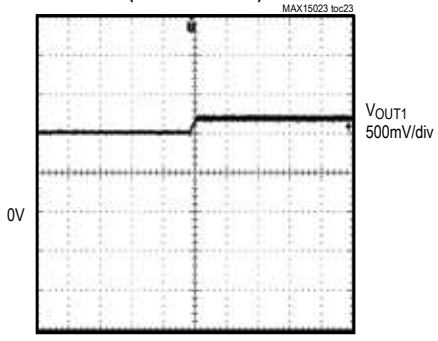

**STARTUP INTO PREBIASED OUTPUT (0.5V PREBIASED)**



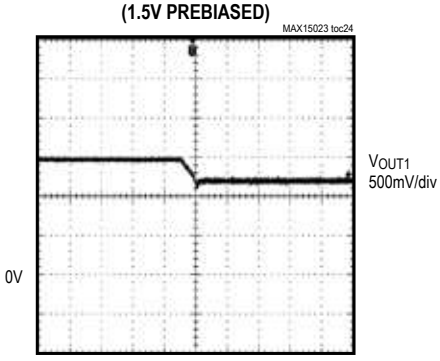
## Typical Operating Characteristics (continued)

(Supply = IN = 12V, unless otherwise noted. See *Typical Application Circuit* of Figure 6.)

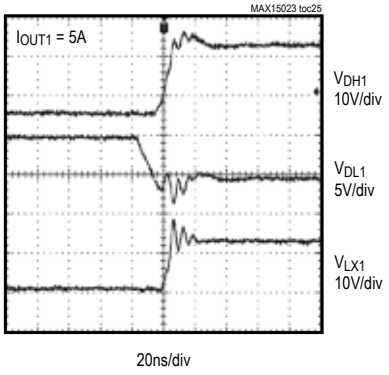
**STARTUP INTO PREBIASED OUTPUT (1V PREBIASED)**



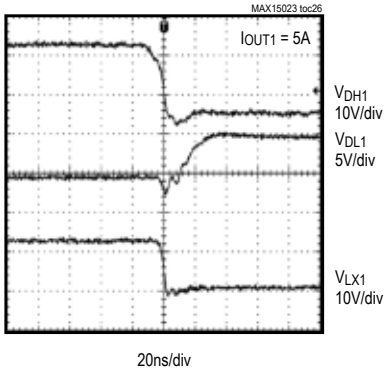

**STARTUP INTO PREBIASED OUTPUT (1.5V PREBIASED)**



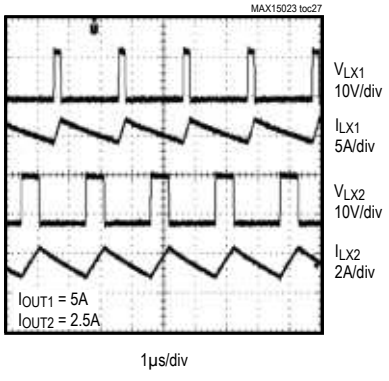

**DH_ AND DL_ DISOVERLAP**



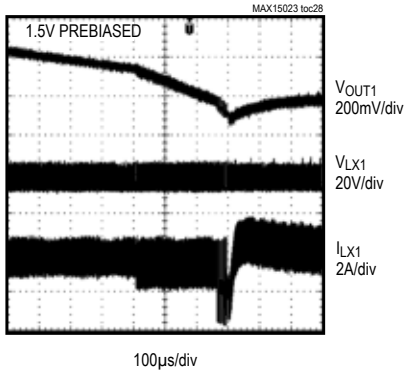

**DH_ AND DL_ DISOVERLAP**




**OUT-OF-PHASE SWITCHING FORMS**




**SINK CURRENT-LIMIT WAVEFORMS**



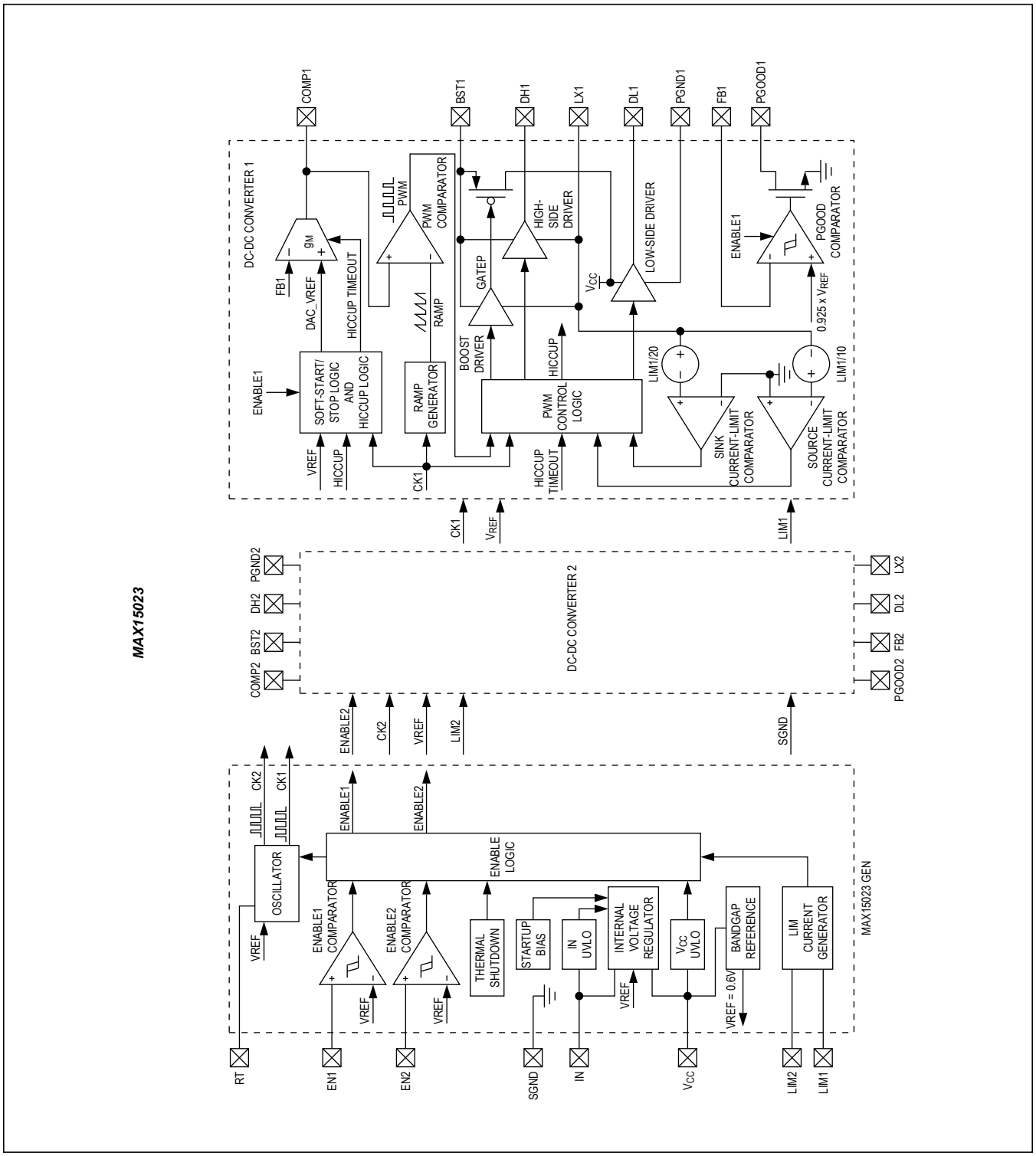
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | FB1 | Feedback Input for Regulator 1. Connect FB1 to a resistive divider between Output 1 and SGND to adjust the output voltage between 0.6V and (0.85 x input voltage (V)). See the *Setting the Output Voltage* section. |
| 2 | EN1 | Active-High Enable Input for Regulator 1. When the voltage at EN1 exceeds 1.2V (typ), the controller begins regulating OUT1. When the voltage falls below 1.05V (typ), the regulator is turned off. The EN1 input can be used for power sequencing and as a secondary UVLO. Connect EN1 to $V_{CC}$ for always-on applications. |
| 3 | EN2 | Active-High Enable Input for Regulator 2. When the voltage at EN2 exceeds 1.2V (typ), the controller begins regulating OUT2. When the voltage falls below 1.05V (typ), the regulator is turned off. The EN2 input can be used for power sequencing and as a secondary UVLO. Connect EN2 to $V_{CC}$ for always-on applications. |
| 4 | PGOOD1 | Power-Good Output (Open Drain) for Channel 1. To obtain a logic signal, pull up PGOOD1 with an external resistor connected to a positive voltage below 28V. |
| 5 | DL1 | Low-Side Gate-Driver Output for Regulator 1. DL1 swings from $V_{CC}$ to PGND1. DL1 is low before $V_{CC}$ reaches the UVLO rising threshold voltage. |
| 6 | PGND1 | Low-Side Gate-Driver Supply Return (Regulator 1). Connect to the source of the low-side MOSFET of Regulator 1. |
| 7 | LX1 | External Inductor Connection for Regulator 1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver and as sensing input of the synchronous MOSFET's $V_{DS}$ drop (drain terminal). |
| 8 | BST1 | Boost Flying-Capacitor Connection for Regulator 1. Connect a ceramic capacitor with a minimum value of 100nF between BST1 and LX1. |
| 9 | DH1 | High-Side Gate-Driver Output for Regulator 1. DH1 swings from LX1 to BST1. DH1 is low before $V_{CC}$ reaches the UVLO rising threshold voltage. |
| 10 | DH2 | High-Side Gate-Driver Output for Regulator 2. DH2 swings from LX2 to BST2. DH2 is low before $V_{CC}$ reaches the UVLO rising threshold voltage. |
| 11 | BST2 | Boost Flying-Capacitor Connection for Regulator 2. Connect a ceramic capacitor with a minimum value of 100nF between BST2 and LX2. |
| 12 | LX2 | External Inductor Connection for Regulator 2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver and as sensing input of the synchronous MOSFET's $V_{DS}$ drop (drain terminal). |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 13 | PGND2 | Low-Side Gate-Driver Supply Return (Regulator 2). Connect to the source of the low-side MOSFET of Regulator 2. |
| 14 | DL2 | Low-Side Gate-Driver Output for Regulator 2. DL2 swings from $V_{CC}$ to PGND2. DL2 is low before $V_{CC}$ reaches the UVLO rising threshold voltage. |
| 15 | PGOOD2 | Power-Good Output (Open Drain) for Channel 2. To obtain a logic signal, pull up PGOOD2 with an external resistor connected to a positive voltage below 28V. |
| 16 | $V_{CC}$ | Internal 5.2V Linear Regulator Output and the Device's Core Supply. When using the internal regulator, bypass $V_{CC}$ to SGND with a 4.7µF minimum low-ESR ceramic capacitor. If $V_{CC}$ is connected to IN for 5V operation, then a 2.2µF ceramic capacitor is adequate for decoupling (see the *Typical Application Circuits*). |
| 17 | FB2 | Feedback Input for Regulator 2. Connect FB2 to a resistive divider between output 2 and SGND to adjust the output voltage between 0.6V and (0.85 x input voltage (V)). See the *Setting the Output Voltage* section. |
| 18 | COMP2 | Compensation Pin for Regulator 2. See the *Compensation* section. |
| 19 | RT | Oscillator-Timing Resistor Input. Connect a resistor from RT to SGND to set the oscillator frequency from 200kHz to 1MHz (see the *Setting the Switching Frequency* section). |
| 20 | SGND | Signal Ground. Connect SGND to the SGND plane. SGND also serves as sensing input of the synchronous MOSFET's $V_{DS}$ drop (source terminals) for both channels. |
| 21 | IN | Internal $V_{CC}$ Regulator Input. Bypass IN to SGND with a 1µF minimum ceramic capacitor when the internal linear regulator ($V_{CC}$) is used. When operating in the 5V ±10% range, connect IN to $V_{CC}$. |
| 22 | LIM2 | Current-Limit Adjustment for Regulator 2. Connect a resistor ($R_{LIM2}$) from LIM2 to SGND to adjust the current-limit threshold ($V_{ITH2}$) from 30mV ($R_{LIM2}$ = 6kΩ) to 300mV ($R_{LIM2}$ = 60kΩ). See the *Setting the Cycle-by-Cycle Low-Side Source Peak Current Limit* section. |
| 23 | LIM1 | Current-Limit Adjustment for Regulator 1. Connect a resistor ($R_{LIM1}$) from LIM1 to SGND to adjust the current-limit threshold ($V_{ITH1}$) from 30mV ($R_{LIM1}$ = 6kΩ) to 300mV ($R_{LIM1}$ = 60kΩ). See the *Setting the Cycle-by-Cycle Low-Side Source Peak Current Limit* section. |
| 24 | COMP1 | Compensation Pin for Regulator 1. See the *Compensation* section. |
| — | EP | Exposed Paddle. Connect EP to a large copper plane at SGND potential to improve thermal dissipation. Do not use as the main IC's SGND ground connection. |

## Functional Diagram



## Detailed Description

The MAX15023 dual, synchronous, step-down controller operates from a 5.5V to 28V or 5V ±10% input voltage range and generates two independent output voltages. As long as the controller's input bias voltage is within the specified range, the input power bus can also be lower than 4.5V and step-down conversion from a 3.3V rail is also possible. Both output voltages can be set from 0.6V to 85% of regulator's input voltage. Each output can support loads of 12A or higher. The switching sequence of the regulators is interleaved with 180° out-of-phase operation, so that input voltage ripple and total RMS input ripple current are reduced.

Enable inputs with precise turn-on/off threshold (±4.2%) allow accurate external UVLO settings. Power-good (PGOOD) open-drain outputs can be used for supply sequencing.

The MAX15023's capability to provide low output voltages (down to 0.6V) and high output current (in excess of 12A) makes it ideal for applications where a 5V or 12V bus is postregulated to deliver low voltages and high currents, such as in set-top boxes.

The switching frequency is adjustable from 200kHz to 1MHz using an external resistor. The MAX15023's adaptive synchronous rectification eliminates the need for external freewheeling Schottky diodes.

The MAX15023 utilizes voltage-mode control and external compensation. The device also utilizes cycle-by-cycle low-side source peak current limit for overcurrent protection, where the external low-side MOSFET's on-resistance is used as a current-sense element during the inductor freewheeling time, eliminating the need for a current-sense resistor. The current-limit threshold voltage is resistor adjustable independently on each regulator from 30mV to 300mV and is temperature compensated, so that the effects of the MOSFET's RDS(ON) variation over temperature are reduced. Hiccup-mode current limit reduces average current and power dissipation during a prolonged short-circuit condition.

The MAX15023 also features a proprietary adaptive internal digital soft-start and allows prebias startup without discharging the output. Adaptive digital soft-start, by acting on the loop voltage reference, automatically prolongs the soft-start time, if the current-limit threshold is reached during the soft-start sequence. This increases the ability to smoothly bring up a large, unknown amount of output capacitance. Also, since soft-start is invoked during hiccup-mode short-circuit protection, the same voltage reference rollback algorithm achieves good control of the peak inductor current during steady short-circuit or overload conditions.

An additional protection feature (cycle-by-cycle low-side sink peak current limit) prevents the regulators from sinking excessive amount of current if the prebias voltage exceeds the programmed steady-state regulation level, or if another voltage source is trying to force the output above that. This way, the synchronous rectifier MOSFET and the body diode of the high-side MOSFET do not experience dangerous levels of current stress while the regulator is sinking current from the output.

Thermal shutdown protects the MAX15023 from excessive power dissipation.

### DC-DC PWM Controller

The MAX15023 step-down controller uses a PWM voltage-mode control scheme (see the *Functional Diagram*) for each channel. Control loop compensation is external for providing maximum flexibility in choosing the operating frequency and output LC filter components. An internal transconductance error amplifier produces an integrated error voltage at COMP_ that helps provide higher DC accuracy. The voltage at COMP_ sets the duty cycle using a PWM comparator and a ramp generator. On the rising edge of its internal clock, the high-side n-channel MOSFET of each regulator turns on and remains on until either the appropriate duty cycle or the maximum duty cycle is reached. During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side n-channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down, providing current to the output. Under overload conditions, when the inductor current exceeds the selected cycle-by-cycle low-side source peak current-limit threshold (see the *Current-Limit Circuit (LIM_)* section), the high-side MOSFET does not turn on at the subsequent clock rising edge and the low-side MOSFET remains on to let the inductor current ramp down.

### Interleaved Out-of-Phase Operation

The two independent regulators in the MAX15023 operate 180° out-of-phase to reduce input filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component cost and saves board space, making the MAX15023 ideal for cost-sensitive applications.

The internal oscillator frequency is divided down to obtain separated clock signals for each regulator. The phase difference of the two clock signals is 180°, so that the high-side MOSFETs turn on out-of-phase. The instantaneous input current peaks of both regulators no longer overlap, resulting in reduced RMS ripple current and input voltage ripple. As a result, this allows an input capacitor with a lower ripple-current rating to be used or allows the use of fewer or less expensive capacitors, as well as reduces EMI filtering and shielding requirements.

### Internal 5.2V Linear Regulator

The MAX15023's internal functions and MOSFET drivers are designed to operate from a 5V ±10% supply voltage. If the available supply voltage exceeds 5.5V, a 5.2V internal low-dropout linear regulator is used to power internal functions and the MOSFET drivers at $V_{CC}$. If an external 5V ±10% supply voltage is available, then IN and $V_{CC}$ can be tied to the 5V supply. The maximum regulator input voltage ($V_{IN}$) is 28V. The regulator's input (IN) must be bypassed to SGND with a 1µF ceramic capacitor when the regulator is used. Bypass the regulator's output ($V_{CC}$) with a 4.7µF ceramic capacitor to SGND. The $V_{CC}$ dropout voltage is typically 70mV, so when $V_{IN}$ is greater than 5.5V, $V_{CC}$ is typically 5.2V. The MAX15023 also employs a UVLO circuit that disables both regulators when $V_{CC}$ falls below 3.8V (typ). The 430mV UVLO hysteresis prevents chattering on power-up/power-down.

The internal $V_{CC}$ linear regulator can source up to 100mA to supply the IC, power the low-side gate drivers, recharge the external boost capacitors, and supply small external loads. The current available for external loads depends on the current consumed for the MOSFET gate drive.

For example, when switched at 600kHz, a single MOSFET with 18nC total gate charge (at $V_{GS}$ = 5V) requires 18nC x 600kHz ≅ 11mA. Since four MOSFETs are driven and 6mA (max) is used by the internal control functions, the current available for external loads is:

$$(100 – (4 \times 11) – 6)\text{mA} \cong 50\text{mA}$$

### MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving large size n-channel power MOSFETs. Under normal operating conditions and after startup, the DL_ low-side drive waveform is always the complement of the DH_ high-side drive waveform (with controlled dead time to prevent cross-conduction or shoot-through). On each channel, an adaptive dead-time circuit monitors the DH and DL outputs and prevents the opposite-side MOSFET from turning on until the other MOSFET is fully off. Thus, the circuit allows the high-side driver to turn on only when the DL_ gate driver has been turned off. Similarly, it prevents the low-side (DL_) from turning on until the DH_ gate driver has been turned off.

The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays, and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly. Otherwise, because of the stray impedance in the gate discharge path, the sense circuitry could interpret the MOSFET gates as off while the VGS of the MOSFET is still high. To minimize stray impedance, use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal low-side Schottky catch diode with a low-resistance MOSFET switch. The internal pulldown transistor that drives DL_ low is robust, with a 0.75Ω (typ) on-resistance. This low on-resistance helps prevent DL_ from being pulled up during the fast rise time of the LX_ node, due to capacitive coupling from the drain to the gate of the low-side synchronous rectifier MOSFET.

### High-Side Gate-Drive Supply (BST_) and Internal Boost Switches

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_. This provides the necessary gate-to-source voltage to turn on the high-side MOSFET, an action that boosts the gate drive signal above $V_{IN}$. The boost capacitor connected between BST_ and LX_ holds up the voltage across the gate driver during the high-side MOSFET on-time.

The charge lost by the boost capacitor for delivering the gate charge is refreshed when the high-side MOSFET is turned off and LX_ node swings down to ground. When the corresponding LX_ node is low, an internal high-voltage switch connected between $V_{CC}$ and BST_ recharges the boost capacitor to the $V_{CC}$ voltage. The need for external boost diodes is negated. See the *Boost Flying-Capacitor Selection* section in the Design Procedure section to choose the right size of the boost capacitor.

### Enable Inputs (EN_), Adaptive Soft-Start and Soft-Stop

The MAX15023 can be used regulate two independent outputs. Each of the two outputs can be turned on and off independently of one another by controlling the enable input of each phase (EN1 and EN2).

A logic-high on each enable pin turns on the corresponding channel. Then, the soft-start sequence is initiated by step-wise increasing the reference voltage of the error

amplifier. The duration of the soft-start ramp is 204witching cycles and the resolution is 1/64 of the steady-state regulation voltage. This allows a smooth increase of the output voltage. A logic-low on each EN_ initiates a soft-stop sequence by stepping down the reference voltage of the error amplifier. After the soft-stop sequence is completed, the MOSFET drivers are both turned off. See Figure 1 for more detail.

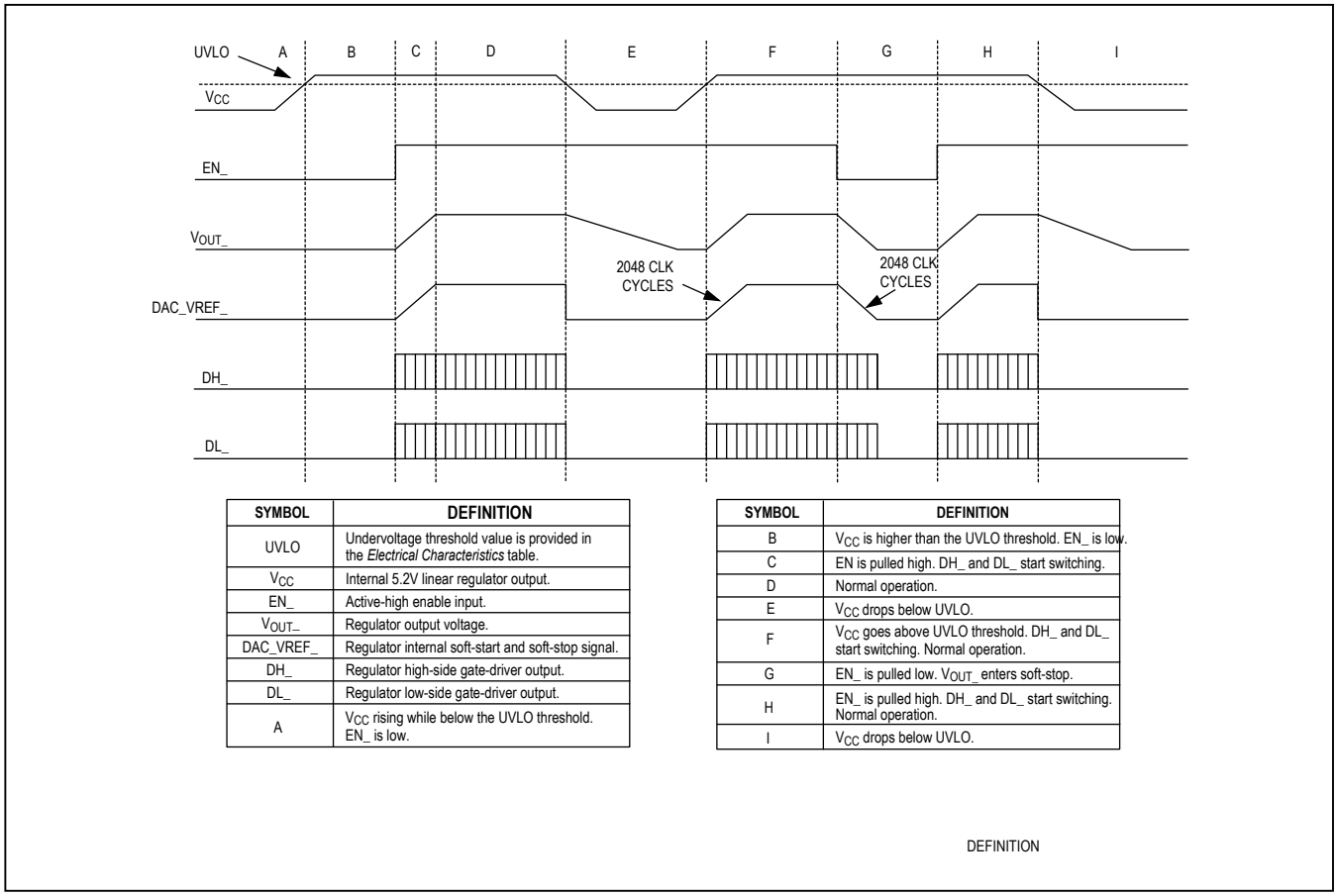
Connect EN1 and EN2 to $V_{CC}$ for always-on operation. Owing to their accurate turn-on and turn–off thresholds, EN1 and EN2 can be used as a UVLO adjustment input and for power sequencing together with the PGOOD_ outputs. (See the *Setting the Enable Input (EN_)* section).

The adaptive action in the soft-start becomes visible if the cycle-by-cycle, low-side, source peak current limit is reached during the soft-start ramping sequence. In this case, the rate-of-rise of the internal reference is decreased, so that the PWM controller tries to regulate to the inductor current around its limit value, rather than the output voltage. The soft-start time can be prolonged up to 4096 clock cycles (twice the normal soft-start duration). This implementation allows the soft-start time to be automatically adapted to the time necessary to keep the LX current below the limit while charging the output capacitor.

Since soft-start is invoked by the hiccup-mode short-circuit protection, also see the *Hiccup Mode Overcurrent Protection* section for additional details.

## Power-Good Outputs (PGOOD_)

The MAX15023 includes two power-good comparators to monitor the regulators' output voltages and detect the power-good threshold, fixed at 92.5% of the nominal FB voltage. The PGOOD_ outputs are open-drain and should be pulled up with an external resistor to the supply voltage of the logic input they drive. This voltage should not exceed 28V. They can sink up to 2mA of current while low.




| SYMBOL | DEFINITION |
|---|---|
| UVLO | Undervoltage threshold value is provided in the *Electrical Characteristics* table. |
| $V_{CC}$ | Internal 5.2V linear regulator output. |
| EN_ | Active-high enable input. |
| $V_{OUT_}$ | Regulator output voltage. |
| DAC_VREF_ | Regulator internal soft-start and soft-stop signal. |
| DH_ | Regulator high-side gate-driver output. |
| DL_ | Regulator low-side gate-driver output. |
| A | $V_{CC}$ rising while below the UVLO threshold. EN_ is low. |

| SYMBOL | DEFINITION |
|---|---|
| B | $V_{CC}$ is higher than the UVLO threshold. EN_ is low. |
| C | EN is pulled high. DH_ and DL_ start switching. |
| D | Normal operation. |
| E | $V_{CC}$ drops below UVLO. |
| F | $V_{CC}$ goes above UVLO threshold. DH_ and DL_ start switching. Normal operation. |
| G | EN_ is pulled low. $V_{OUT_}$ enters soft-stop. |
| H | EN_ is pulled high. DH_ and DL_ start switching. Normal operation. |
| I | $V_{CC}$ drops below UVLO. |

DEFINITION

*Figure 1. MAX15023 Detailed Power-On/-Off Sequencing*

Each PGOOD_ goes high (high impedance) when the corresponding regulator output increases above 92.5% of its nominal regulated voltage. Each PGOOD_ goes low when the corresponding regulator output voltage drops typically below 89.5% of its nominal regulated voltage. PGOOD_ can be used as power-on-reset or power sequencing for the two regulators.

PGOOD_ asserts low during the hiccup timeout pod.

### Startup into a Prebiased Output

When the controller starts into a prebiased output, the DH_/DL_ complementary switching sequence is inhibited until the PWM comparator commands its first PWM pulse. Until then, DH_ and DL_ are kept off so that the converter does not sink current from the output. The first PWM pulse occurs when the ramping reference voltage increases above the FB_ voltage or the internal soft-start time is over.

### Current-Limit Circuit (LIM_)

The current-limit circuit employs a cycle-by-cycle low-side source peak and sink current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element, so that costly sense resistors are not required. The current-limit circuit is also temperature compensated to track the MOSFET's on-resistance variation over temperature. The current limit is adjustable on each channel with an external resistor at LIM_ (see the *Typical Application Circuits*), and accommodates MOSFETs with a wide range of on-resistance characteristics (see the Design Procedure section). The adjustment range is from 30mV to 300mV for the cycle-by-cycle, low-side, source peak current limit, corresponding to resistor values of 6kΩ to 60kΩ. The cycle-by-cycle, low-side, source peak current-limit threshold across the low-side MOSFET is precisely 1/10 the voltage seen LIM_, while the cycle-by-cycle, low-side, sink peak current-limit threshold is 1/20 the voltage seen at LIM_.

The MAX15023 uses SGND to sense the voltage of the source terminals of the low-side MOSFETs for both channels, and LX_ to sense the drain voltage of each low-side MOSFET. Carefully observe the *PCB Layout Guidelines* section to ensure that noise and systematic errors do not corrupt the current-sense signals seen by LX_ and SGND on each channel.

Cycle-by-cycle, low-side, source peak current limit acts when the inductor current flows in the normal direction, and the drain (LX_) is more negative than source (sensed by SGND) during the low-side MOSFET on-time. If the magnitude of current-sense signal exceeds the cycle-by-cycle, low-side, source peak current-limit threshold during the low-side MOSFET on-time, the controller does not initiate a new PWM cycle and lets the inductor current decay in the next cycle. Since cycle-by-cycle, low-side, source peak current sensing is employed, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are functions of the low-side MOSFET's on-resistance, current-limit threshold, inductor value, and input voltage.

Cycle-by-cycle, low-side, sink peak current limit is also implemented by monitoring the voltage drop across the low-side MOSFET, but with opposite polarity (drain more positive than source). If this drop exceeds 1/20 the voltage at the corresponding LIM_ pin at any time during the low-side MOSFET on-time, the low-side MOSFET is turned off and the inductor current flows from the output through the high-side MOSFET back. If the cycle-by-cycle, low-side, sink peak current limit is activated, the DH_ and DL_ switching sequence is no longer complementary.

### Hiccup Mode Overcurrent Protection

Hiccup mode overcurrent protection reduces power dissipation during prolonged short-circuit or deep overload conditions.

After the soft-start sequence has been completed, on each switching cycle where the cycle-by-cycle, low-side, source peak current-limit threshold is reached, a 3-bit counter is incremented. The counter is decremented on each switching cycle where the threshold is not reached, and stopped at zero (000).

If the cycle-by-cycle, low-side, source peak current-limit condition persists, the counter fills up reaching 111 (= 7 events). Then, the controller stops both DL_ and DH_ drivers and waits for 7936 switching cycles (hiccup timeout delay). After this delay, the controller initiates a new soft-start sequence.

If cycle-by-cycle low-side, source peak current-limit events occur during theft-start time, turn-on cycles are still skipped to control the inductor current, but the fill-up of the 3-bit counter does not terminate the soft-start sequence. Rather, the soft-start ramp is slowed down or rolled back based on the cycle-by-cycle, low-side, source peak current-limit events occurrences, so that the PWM controller tries to regulate the inductor current around its limit value, rather than the output voltage.

This proprietary technique prevents the duty cycle from saturating, and limits the on-time and thus, the peak inductor current is reached every time the high-side MOSFET is turned on.

In case of a nonideal short circuit applied at the output, the out voltage equals the output impedance times the limited inductor current during this phase. Ar reaching the maximum allowable limit of the soft-start duration (twice the normal soft-start ti, the controller remains off for 7936 clock cycles before trying to soft-start again.

### Undervoltage Lockout

The MAX15023 has an internal undervoltage lockout (UVLO) circuit to monitor the voltage on $V_{CC}$. The UVLO circuit prevents the MAX15023 from operating if the voltages for the MOSFET drivers or for the internal control functions are too low. The $V_{CC}$ falling threshold is 3.8V (typ), with 430mV hysteresis to prevent chattering on the rising/falling edge of the supply voltage. Before $V_{CC}$ reaches UVLO rising threshold voltage, DL_ and DH_ stay low to inhibit switching.

### Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX15023. When the device's die-junction temperature exceeds $T_J$ = +150°C, an on-chip thermal sensor shuts down the device, forcing DL_ and DH_ low, allowing the IC to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. During thermal shutdown, the regulators shut down, and soft-start is reset. Thermal-overload protection can be triggered by power dissipation in the LDO regulator, by excessive driving losses, or by both. Therefore, carefully evaluate the total power dissipation (see the Power Dissipation section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

## Design Procedure

### Effective Input Voltage Range

Although the MAX15023 controllers can operate from input supplies up to 28V and regulate down to 0.6V, the minimum voltage conversion ratio ($V_{OUT}/V_{IN}$) might be limited by the minimum controllable on-time. For proper fixed-frequency PWM operation, the voltage conversion ratio should obey the following condition:

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 100ns (max) and $^{f}SW$ is the switching frequency in Hertz. If the desired voltage conversion does not meet the above condition, then pulse skipping occurs to decrease the effective duty cycle. To avoid this, decrease the switching frequency or lower the input voltage $V_{IN}$.

The maximum voltage conversion ratio is limited by the maximum duty cycle ($D_{max}$):

$$\frac{V_{OUT}}{V_{IN}} < D_{max} - \frac{D_{max} \times V_{DROP2} + (1 - D_{max}) \times V_{DROP1}}{V_{IN}}$$

where $V_{DROP1}$ is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances. $V_{DROP2}$ is the sum of the voltage drops in the charging path, including high-side switch, inductor, and PCB resistances. In practice, the above condition should be met with adequate margin for good load-transient response.

### Setting the Enable Input (EN_)

Each controller has an enable input referenced to an analog voltage (1.2V). When the voltage exceeds 1.2V, the regulator is enabled. To set a specific turn-on threshold that can act as a secondary UVLO, a resistive divider circuit can be used (see Figure 2)

Select $R_2$ (EN_ to SGND resistor) to a value lower than 200kΩ. Calculate $R_1$ ($V_{MON}$ to EN_ resistor) with the following equation:

$$R_1 = R_2 \left[ \left( \frac{V_{MON}}{V_{EN_H_}} \right) - 1 \right]$$

where $V_{EN_H_}$ = 1.2V (typical).

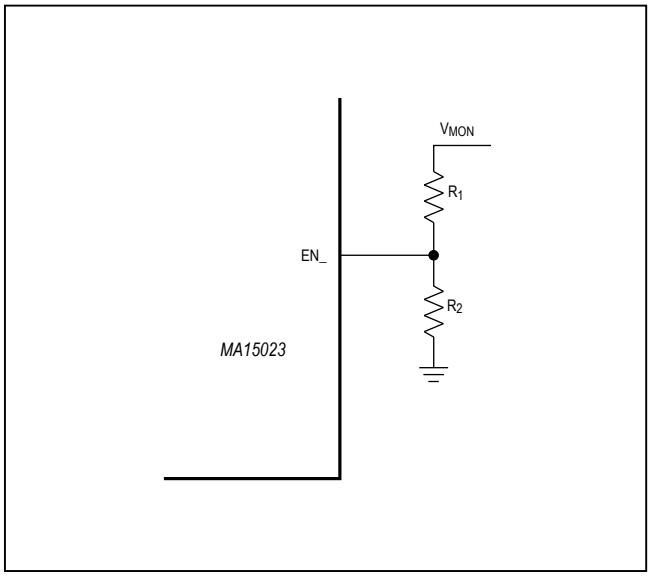



*Figure 2. Adjustable Enable Voltage*

## Setting the Output Voltage

Set the MAX15023 output voltage on each channel by connecting a resistive divider from the output to FB_ to SGND (Figure 3). Select $R_2$ (FB_ to SGND resistor) less than or equal to 16kΩ. Calculate $R_1$ (OUT_ to FB_ resistor) with the following equation:

$$R_1 = R_2\left[\left(\frac{V_{OUT_}}{V_{FB_}}\right) - 1\right]$$

where $V_{FB_}$ = 0.6V (typ) (see the *Electrical Characteristics* table) and $V_{OUT_}$ can range from 0.6V to (0.85 x $V_{IN}$).

Resistor $R_1$ also plays a role in the design of the Type III compensation network. If a Type III compensation network is used, make sure to review the values of $R_1$ and $R_2$ according to the *Type III Compensation Network (See Figure 5)* section.

## Setting the Switching Frequency

The switching frequency, $f_{SW}$, for each channel is set by a resistor ($R_T$) connected from RT to SGND. The relationship between $f_{SW}$ and RT is:

$$R_T = \frac{24806}{(f_{SW})^{1.0663}}$$

where $f_{SW}$ is in kHz, $R_T$ is in kΩ, and 24806 is in 1/farad. For example, a 600kHz switching frequency is set with RT = 27.05kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and $I^2R$ losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

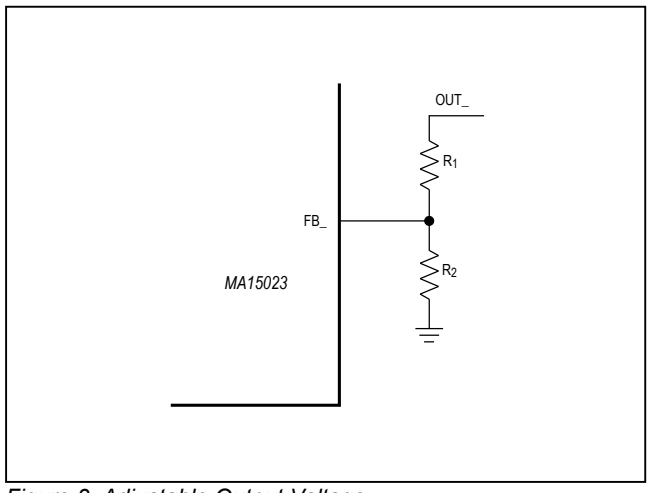



*Figure 3. Adjustable Output Voltage*

## Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15023: inductance value (L), inductor saturation current ($I_{SAT}$), and DC resistance ($R_{DC}$). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUT} LIR}$$

where $V_{IN}$, $V_{OUT}$, and $I_{OUT}$ are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by $R_T$ (see the *Setting the Switching Frequency* section). The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, efficiency, and transient response requirements. Lower inductor values minimize size and cost, but also improve transient response and reduce efficiency due to higher peak currents. On the other hand, higher inductance increases efficiency by reducing the RMS current, but requires more output capacitance to meet load-transient specifications.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor's saturation rating ($I_{SAT}$) must be high enough to ensure that saturation can occur only above the maximum current-limit value, given the tolerance of the low- side MOSFET's on-resistance and of the LIM_ reference current ($I_{LIM}$). On the other hand, these tolerances should not prevent the converter from delivering the rated load current ($I_{LOAD(MAX)}$). Combining these conditions, the inductor saturation current ($I_{SAT}$) should be such that:

$$I_{SAT} > \frac{R_{DS(ON,MAX)}}{R_{DS(ON,TYP)}} \times \left(1 + \frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

where $R_{DS(ON,MAX)}$ and $R_{DS(ON,TYP)}$ are the maximum and typical on-resistance of the low-side MOSFET. For a given inductor type and value, choose the LIR corresponding to the worst-case inductor tolerance.

For LIR = 0.4, and a +25% on the low-side MOSFET's $R_{DS(ON,MAX)}$, the inductor saturation current should be about 50% greater than the converter's maximum load current. A variety of inductors from different manufacturers can be chosen to meet this requirement (for example, Coilcraft MSS1278 series).

### Setting the Cycle-by-Cycle, Low-Side, Source Peak Current Limit

The minimum current-limit threshold must be high enough to support the maximum expected load current with the worst-case low-side MOSFET on-resistance value since the low-side MOSFET's on-resistance is used as the current-sense element. The inductor's cycle-by-cycle, low-side, source peak current occurs at $I_{LOAD(MAX)}$ minus half the ripple current. The ripple current is maximum when the inductor value is at the lower limit of its specified tolerance. The minimum value of the current-limit threshold voltage ($V_{ITH}$) should be greater than the voltage on the low-side MOSFET during the ripple-current valley:

$$V_{ITH} > R_{DS(ON,MAX)} \times I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right)$$

where $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET in ohms. Use the maximum value for $R_{DS(ON)}$ from the low-side MOSFET's data sheet.

To adjust the current-limit threshold, connect a resistor ($R_{LIM_}$) from LIM_ to SGND. The relationship between the current-limit threshold ($V_{ITH_}$) and $R_{LIM_}$ is:

$$LIM_ \quad \frac{10 \times V_{ITH_}}{50\ A}$$

where $R_{LIM_}$ is in kΩ and $V_{ITH_}$ is in mV.

An $R_{LIM_}$ resistance range of 6kΩ to 60kΩ corresponds to a current-limit threshold of 30mV to 300mV. When adjusting the current limit, use 1% tolerance resistors to minimize errors in the current-limit threshold setting.

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The two converters of the MAX15023 run 180° out-of-phase, thereby, effectively doubling the switching frequency at the input and lowering the input RMS current.

The input ripple waveform would be unsymmetrical due to the difference in load current and duty cycle between converter 1 and converter 2. In fact, the worst-case input RMS current occurs when only one controller is operating. The converter delivering the highest output power ($V_{OUT}$ x $I_{OUT}$) must be used in the formulas below:

The input capacitor RMS current requirement ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

$I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN}$ = 2$V_{OUT}$), so $I_{RMS(MAX)}$ = $I_{LOAD(MAX)/2}$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of ΔVQ (caused by the capacitor discharge) and ΔVESR (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge are equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$D = \frac{V_{OUT}}{V_{IN}}$$

All equations listed above are valid under the assumption that the input ports of both converters can be merged in the physical layout, so that only one input capacitor truly serves both converters. If this is not the case, additional low-ESR, low-ESL ceramic capacitors should be locally placed on each converter's input port, connected between the drain of the high-side MOSFET and the source of the low-side MOSFET.

### Output Capacitor

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output ripple voltage, and transient response. The output ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current flowing into and out of the capacitor:

$$\Delta V_{RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

The output voltage ripple as a consequence of the ESR and the output capacitance is:

$$\Delta V_{ESR} = \Delta I_L \times ESR$$

$$\Delta V_Q = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

where ΔIL is the peak-to-peak inductor current ripple (see the *Inductor Selection* section). These equations are suitable for initial capacitor selection, but final values should be verified by testing in a prototype or evaluation circuit.

As a general rule, a smaller inductor ripple current results in less output ripple voltage. The output capacitor must be also checked against load-transient response requirements. The allowable deviation of the output voltage during fast load transients also determines the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL ($\Delta V_{ESL}$), and the capacitor discharge causes a voltage droop during the load step.

Use a combination of low-ESR tantalum/aluminum electrolytic or polymer and ceramic capacitors for better transient load and voltage ripple performance. Non-leaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the load. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

$$t_{RESPONSE} \cong \frac{1}{3 \times f_O}$$

where $I_{STEP}$ is the load step, $t_{STEP}$ is the rise time of the load step, $t_{RESPONSE}$ is the response time of the controller, and $f_O$ is the closed-loop crossover frequency.

## Compensation

Each channel of the MAX15023 provides an internal transconductance amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use low-ESR aluminum electrolytic capacitors; for component-size sensitive applications, use low-ESR tantalum, polymer, or ceramic capacitors at the output. The high switching frequency of the MAX15023 allows use of ceramic capacitors at the output. Choose the small-signal components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin.

To choose the appropriate compensation network type, the power-supply poles and zeros, the zero crossover frequency, and the type of the output capacitor must be determined.

In a buck converter, the LC filter in the output stage introduces a pair of complex poles at the following frequency:

$$f_{PO} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The loop-gain crossover frequency ($f_O$, where the loop gain equals 1 (0dB)) should be set below 1/10 the switching frequency:

$$f_O \le \frac{f_{SW}}{10}$$

Choosing a lower crossover frequency might also help in reducing the effects of noise pickup into the feedback loop, such as jittery duty cycle.

In order to maintain a stable system, two stability criteria must be met:

1) The phase shift at the crossover frequency $f_O$, must be less than 180°. In other words, the phase margin of the loop must be greater than zero.
2) The gain at the frequency where the phase shift is -180° (gain margin) must be less than 1.

It is recommended to have a phase margin around +50° to +60° to maintain a robust loop stability and well-behaved transient response.

If an electrolytic or large-ESR tantalum output capacitor is used, the capacitor ESR zero $f_{ZO}$ typically occurs between the LC poles and the crossover frequency $f_O$ ($f_{PO} < f_{ZO} < f_O$). In this case, use a Type II (PI or proportional-integral) compensation network.

If a ceramic or low-ESR tantalum output capacitor is used, the capacitor ESR zero typically occurs above the desired crossover frequency $f_O$, that is $f_{PO} < f_O < f_{ZO}$. In this situation, choose a Type III (PID or proportional-integral-derivative) compensation network.

### Type II Compensation Network (See Figure 4)

If $f_{ZO}$ is lower than $f_O$ and close to $f_{PO}$, the phase lead of the capacitor ESR zero almost cancels the phase loss of one of the complex poles of the LC filter around the crossover frequency. Therefore, a Type II compensation network with a midband zero and a high-frequency pole can be used to stabilize the loop. In Figure 4, RF and CF introduce a midband zero ($f_{Z1}$). $R_F$ and $C_{CF}$ in the Type II compensation network also provide a high-frequency pole ($f_{P1}$), which mitigates the effects of the output high-frequency ripple.

To calculate the component values for Type II compensation network in Figure 4, follow the instruction below:

1) Calculate the gain of the modulator (GainMOD)—composed of the regulator's pulse-width modulator, LC filter, feedback divider, and associated circuitry at crossover frequency:

$$Gain_{MOD} = \frac{V_{IN}}{V_{OSC}} \times \frac{ESR}{(2\pi \times f_O \times L_{OUT})} \times \frac{V_{FB}}{V_{OUT}}$$

where $V_{IN}$ is the regulator's input voltage, $V_{OSC}$ is the amplitude of the ramp in the pulse-width modulator, $V_{FB}$ is the FB_ input voltage set-point (0.6V typically, see *Electrical Characteristics* table), and $V_{OUT}$ is the desired output voltage.

The gain of the error amplifier ($Gain_{EA}$) in midband frequencies is:

$$Gain_{EA} = g_m \times R_F$$

where $g_m$ is the transconductance of the error amplifier.

The total loop gain as the product of the modulator gain and the error amplifier gain at $f_O$ should equal 1. So:

$$Gain_{MOD} \times Gain_{EA} = 1$$

Therefore:

$$\frac{V_{IN}}{V_{OSC}} \times \frac{ESR}{(2\pi \times f_O \times L_{OUT})} \times \frac{V_{FB}}{V_{OUT}} \times g_m \times R_F = 1$$

Solving for $R_F$:

$$R_F = \frac{V_{OSC} \times (2\pi \times f_O \times L_{OUT}) \times V_{OUT}}{V_{FB} \times V_{IN} \times g_m \times ESR}$$

2) Set a midband zero ($f_{Z1}$) at 0.75 x $f_{PO}$ (to cancel one of the LC poles):

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F} = 0.75 \times f_{PO}$$

Solving for $C_F$:

$$C_F = \frac{1}{2\pi \times R_F \times f_{PO} \times 0.75}$$

3) Place a high-frequency pole at $f_{P1}$ = 0.5 x $f_{SW}$ (to attenuate the ripple at the switching frequency, $f_{SW}$) and calculate $C_{CF}$ using the following equation:

$$C_{CF} = \frac{1}{\pi \times R_F \times f_{SW} - \frac{1}{C_F}}$$

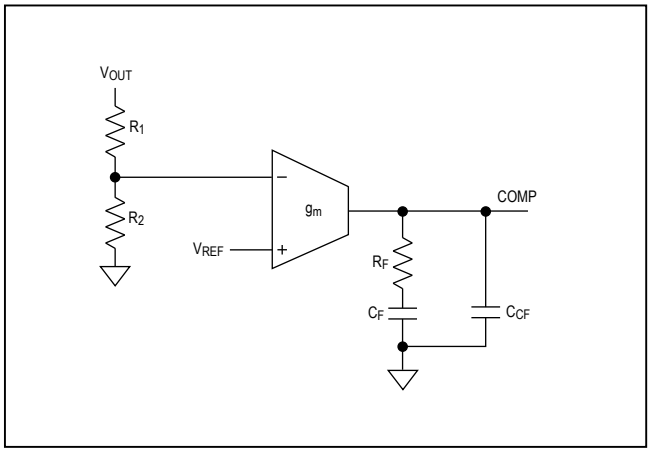



*Figure 4. Type II Compensation Network*

### Type III Compensation Network (See Figure 5)

If the output capacitor used is a low-ESR tantalum or ceramic type, the ESR-induced zero frequency is usually above the targeted zero crossover frequency ($f_O$). In this case, Type III compensation is recommended. Type III compensation provides three poles and two zeros at the following frequencies:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$$

$$f_{Z2} = \frac{1}{2\pi \times C_I \times (R_1 + R_I)}$$

Two midband zeros ($f_{Z1}$ and $f_{Z2}$) cancel the pair of complex poles introduced by the LC filter:

$$f_{P1} = 0$$

$f_{P1}$ introduces a pole at zero frequency (integrator) for nulling DC output voltage errors:

$$f_{P2} = \frac{1}{2\pi \times R_I \times C_I}$$

Depending on the location of the ESR zero ($f_{ZO}$), $f_{P2}$ can be used to cancel it, or to provide additional attenuation of the high-frequency output ripple:

$$f_{P3} = \frac{1}{2\pi \times R_F \times \frac{C_F \times C_{CF}}{C_F + C_{CF}}}$$

$f_{P3}$ attenuates the high-frequency output ripple.

The locations of the zeros and poles should be such that the phase margin peaks around $f_O$.

Ensure that $R_F >> 2/g_m$ ($1/g_m$(MIN) = 1/600µS = 1.67kΩ) and the parallel resistance of $R_1$, $R_2$, and $R_I$ is greater than $1/g_m$. Otherwise, a 180° phase shift is introduced to the response and will make it unstable.

The following procedure is recommended:

1) With $R_F \geq 10k\Omega$, place the first zero ($f_{Z1}$) at 0.5 x $f_{PO}$:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F} = 0.5 \times f_{PO}$$

so:

$$\frac{}{2\pi \times R_F \times 0.5 \times f_{PO}}$$

2) The gain of the modulator ($Gain_{MOD}$)—composed of the regulator's pulse-width modulator, LC filter, feedback divider, and associated circuitry at crossover frequency is:

$$Gain_{MOD} = \frac{V_{IN}}{V_{OSC}} \times \frac{1}{(2\pi \times f_O)^2 \times L_{OUT} \times C_{OUT}}$$

The gain of the error amplifier ($Gain_{EA}$) in midband frequencies is:

$$Gain_{EA} = 2\pi \times f_O \times C_I \times R_F$$

The total loop gain as the product of the modulator gain and the error amplifier gain at $f_O$ should be equal to 1. So:

$$Gain_{MOD} \times Gain_{EA} = 1$$

$$\frac{V_{IN}}{V_{OSC}} \times \frac{1}{(2\pi \times f_O)^2 \times C_{OUT} \times L_{OUT}} \times 2\pi \times f_O \times C_I \times R_F = 1$$

Solving for $C_I$:

$$C_I = \frac{V_{OSC} \times (2\pi \times f_O \times L_{OUT} \times C_{OUT})}{V_{IN} \times R_F}$$

3) If $f_{PO} < f_O < f_{ZO} < f_{SW/2}$, the second pole ($f_{P2}$) should be used to cancel $f_{ZO}$. This way, the Bode plot of the loop gain plot does not flatten out soon after the 0dB crossover, and maintains its -20dB/decade slope up to 1/2 the switching frequency. This is likely to occur if the output capacitor is a low-ESR tantalum or polymer. Then set:

$$f_{P2} = f_{ZO}$$

If a ceramic capacitor is used, then the capacitor ESR zero, $f_{ZO}$, is likely to be located even above 1/2 the switching frequency, that is, $f_{PO} < f_O < f_{SW/2} < f_{ZO}$. In this case, the frequency of the second pole ($f_{P2}$) should be placed high enough in order not to significantly erode the phase margin at the crossover frequency. For example, it can be set at 5 x $f_O$, so that its contribution to phase loss at the crossover frequency, $f_O$, is only about 11°:

$$f_{P2} = 5 \times f_O$$

Once $f_{P2}$ is known, calculate $R_I$:

$$R_I = \frac{1}{2\pi \times f_{P2} \times C_I}$$

4) Place the second zero ($f_{Z2}$) at 0.2 x $f_O$ or at $f_{PO}$, whichever is lower and calculate $R_1$ using the following equation:

$$R_1 = \frac{1}{2\pi \times f_{Z2} \times C_I} - R_I$$

5) Place the third pole ($f_{P3}$) at half the switching frequency and calculate $C_{CF}$:

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

6) Calculate $R_2$ as:

$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_1$$

## MOSFET Selection

The MAX15023's step-down controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include:

- On-resistance ($R_{DS(ON)}$ )
- Maximum drain-to-source voltage ($V_{DS(MAX)}$ )
- Minimum threshold voltage ($V_{TH(MIN)}$ )
- Total gate charge ($Q_g$)
- Reverse transfer capacitance ($C_{RSS}$)
- Power dissipation

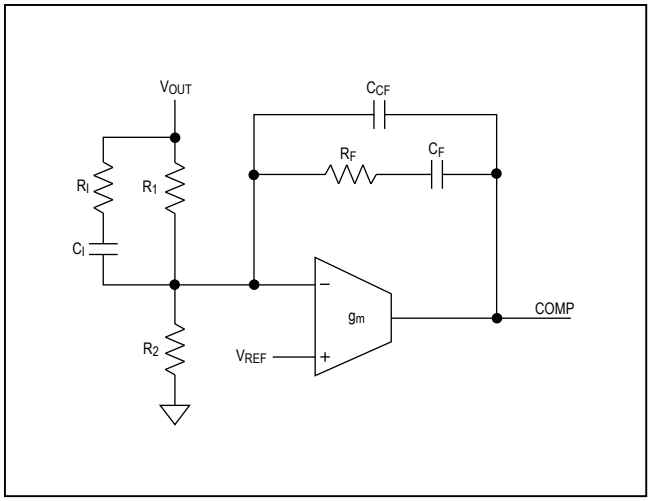



*Figure 5. Type III Compensation Network*

All four n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at VGS = 4.5V. For maximum efficiency, choose a high-side MOSFET (NH_) that has conduction losses equal to the switching losses at the typical input voltage. Ensure that the conduction losses at minimum input voltage do not exceed MOSFET package thermal limits, or violate the overall thermal budget. Also, ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget. Ensure that the MAX15023 DL_ gate drivers can drive a low-side MOSFET (NL_). In particular, check that the dV/dt caused by NH_ turning on does not pull up the NL_ gate through NL_'s drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, if the drive current is taken from the internal LDO regulator, the power dissipation due to drive losses must be checked. All MOSFETs must be selected so that their total gate charge is low enough; therefore, $V_{CC}$ can power all four drivers without overheating the IC:

$$P_{DRIVE} = V_{IN} \times Q_{G_TOTAL} \times f_{SW}$$

where $Q_{G_TOTAL}$ is the sum of the gate charges of all four MOSFETs.

## Power Dissipation

Device's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the device package, PCB copper area, other thermal mass, and airflow.

The power dissipated into the package ($P_T$) depends on the supply configuration (see the *Typical Application Circuits*). It can be calculated using the following equation:

$$P_T = V_{IN} \times I_{IN}$$

For the circuits of Figures 7 and 8:

$$P_T = V_{CC} \times (I_{IN} + I_{VCC})$$

where $V_{IN}$ and $V_{CC}$ are the voltages at the respective pins, $I_{IN}$ is the current at the input of the internal LDO ($I_{IN}$ is practically zero for the circuits of Figures 7 and 8), $I_{VCC}$ is the current consumed by the internal core and drivers when the internal regulator is unused for 5V supply operation (IN = $V_{CC}$). See the corresponding *Typical Operating Characteristics* for the typical curves of $I_{IN}$ and $I_{VCC}$ current consumption vs. operating frequency at various load capacitance values.

To estimate the temperature rise of the die, use the following equation:

$$T_J = T_A + (P_T \times \theta_{JA})$$

where $\theta_{JA}$ is the junction-to-ambient thermal resistance of the package, $P_T$ is power dissipated in the device, and TA is the ambient temperature. The $\theta_{JA}$ is 36°C/W for the 24-pin TQFN package on multilayer boards, with the conditions specified by the respective JEDEC standards (JESD51-5, JESD51-7). If actual operating conditions significantly deviate from those described in the JEDEC standards, then an accurate estimation of the junction temperature requires a direct measurement of the case temperature ($T_C$). Then, the junction temperature can be calculated using the following equation:

$$T_J = T_C + (P_T \times \theta_{JC})$$

Use 3°C/W as θJC thermal resistance for the 24-pin TQFN package. The case-to-ambient thermal resistance ($\theta_{CA}$) is dependent on how well the heat is transferred from the PCB to the ambient. Therefore, solder the exposed pad of the TQFN package to a large copper area to spread heat through the board surface, minimizing the case-to-ambient thermal resistance. Use large copper areas to keep the PCB temperature low.

### Boost Flying-Capacitor Selection

The MAX15023 uses a bootstrap circuit to generate the necessary gate-to-source voltage to turn on the high-side MOSFET. The selected n-channel high-side MOSFET determines the appropriate boost capacitance values ($C_{BST_}$ in *Typical Application Circuits*) according to the following equation:

$$C_{BST_} = \frac{Qg}{\Delta V_{BST_}}$$

where $Q_g$ is the total gate charge of the high-side MOSFET and $\Delta V_{BST_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $\Delta V_{BST_}$ such that the available gate drive voltage is not significantly degraded (e.g., $\Delta V_{BST_}$ = 100mV to 300mV) when determining $C_{BST_}$. The boost flying-capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF is recommended.

## Applications Information

### PCB Layout Guidelines

Make the controller ground connections as follows: create a small analog ground plane near the IC or use a dedicated internal plane. Connect this plane to SGND and use this plane for the ground connection for the IN bypass capacitor, compensation components, feedback dividers, RT resistor, and LIM_ resistors.

If possible, place all power components on the top side of the board, and run the power stage currents (especially the one having large high-frequency components) using traces or copper fills on the top side only, without adding vias.

On the top side, lay out a large PGND copper area for the output of channels 1 and 2, and connect the bottom terminals of the high-frequency input capacitors, output capacitors, and the source terminals of the low-side MOSFETs to that area.

Then, make a star connection of the SGND plane to the top copper PGND area with few vias in the vicinity of the source terminal sensing. Do not connect PGND and SGND anywhere else. Refer to the MAX15023 Evaluation Kit data sheet for guidance.

Keep the power traces and load connections short, especially at the ground terminals. This practice is essential for high efficiency and jitter-free operation. Use thick copper PCBs (2oz vs. 1oz) to enhance efficiency.

Place the controller IC adjacent to the synchronous rectifier MOSFETs (NL_) and keep the connections for LX_, PGND_, DH_, and DL_ short and wide. Use multiple small vias to route these signals from the top to the bottom side. The gate current traces must be short and wide, measuring 50 mils to 100 mils wide if the low-side MOSFET is 1in from the controller IC. Connect each PGND trace from the IC close to the source terminal of the respective low-side MOSFET.

Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from the sensitive analog areas (RT, COMP_, LIM_, and FB_). Group all SGND-referred and feedback components close to the IC. Keep the FB_ and compensation network nets as small as possible to prevent noise pickup.

## Typical Application Circuits

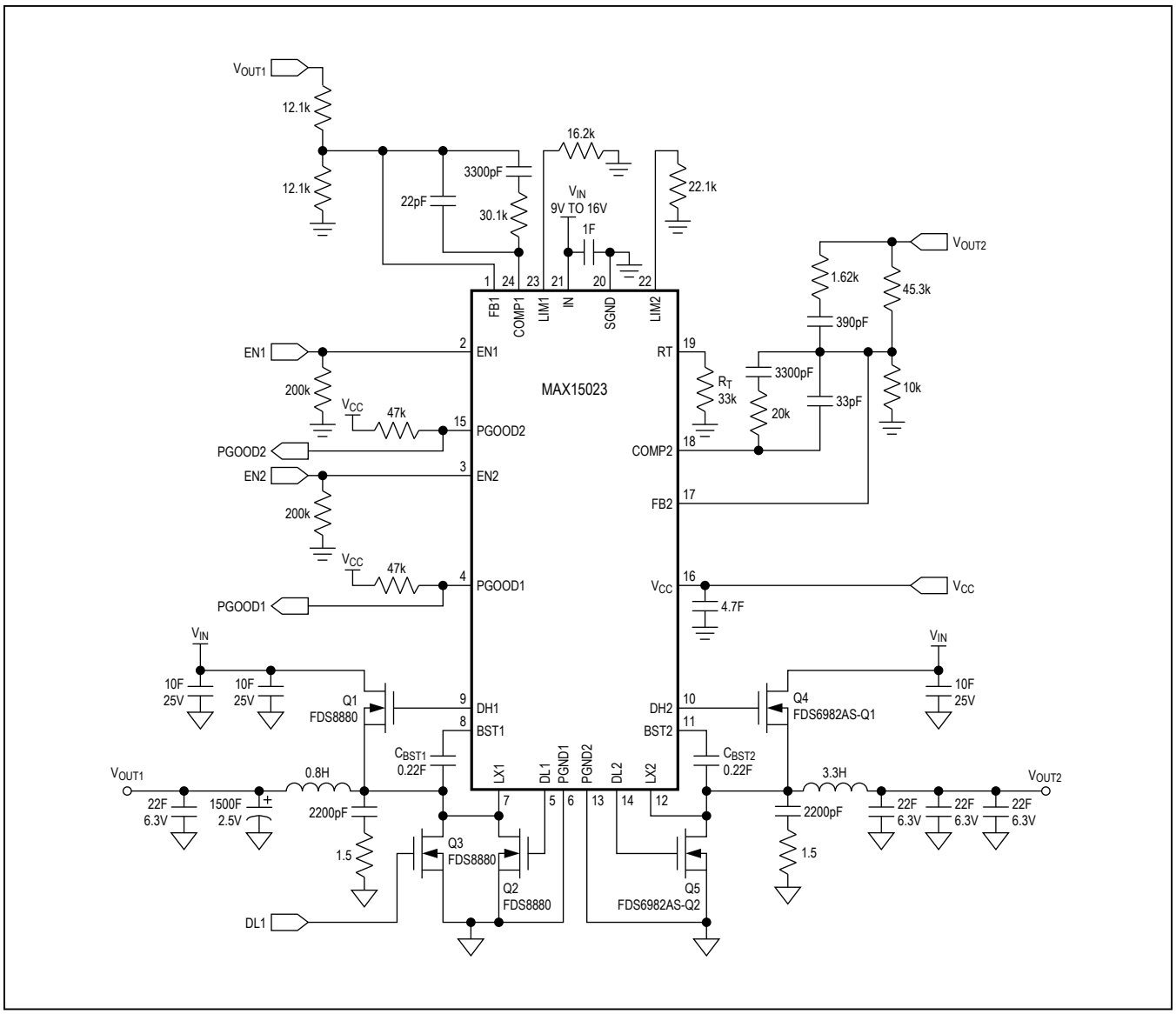



*Figure 6. Application Diagram (Operation from a Single-Supply Rail, $V_{IN}$ = 9V to 16V)*

## Typical Application Circuits (continued)

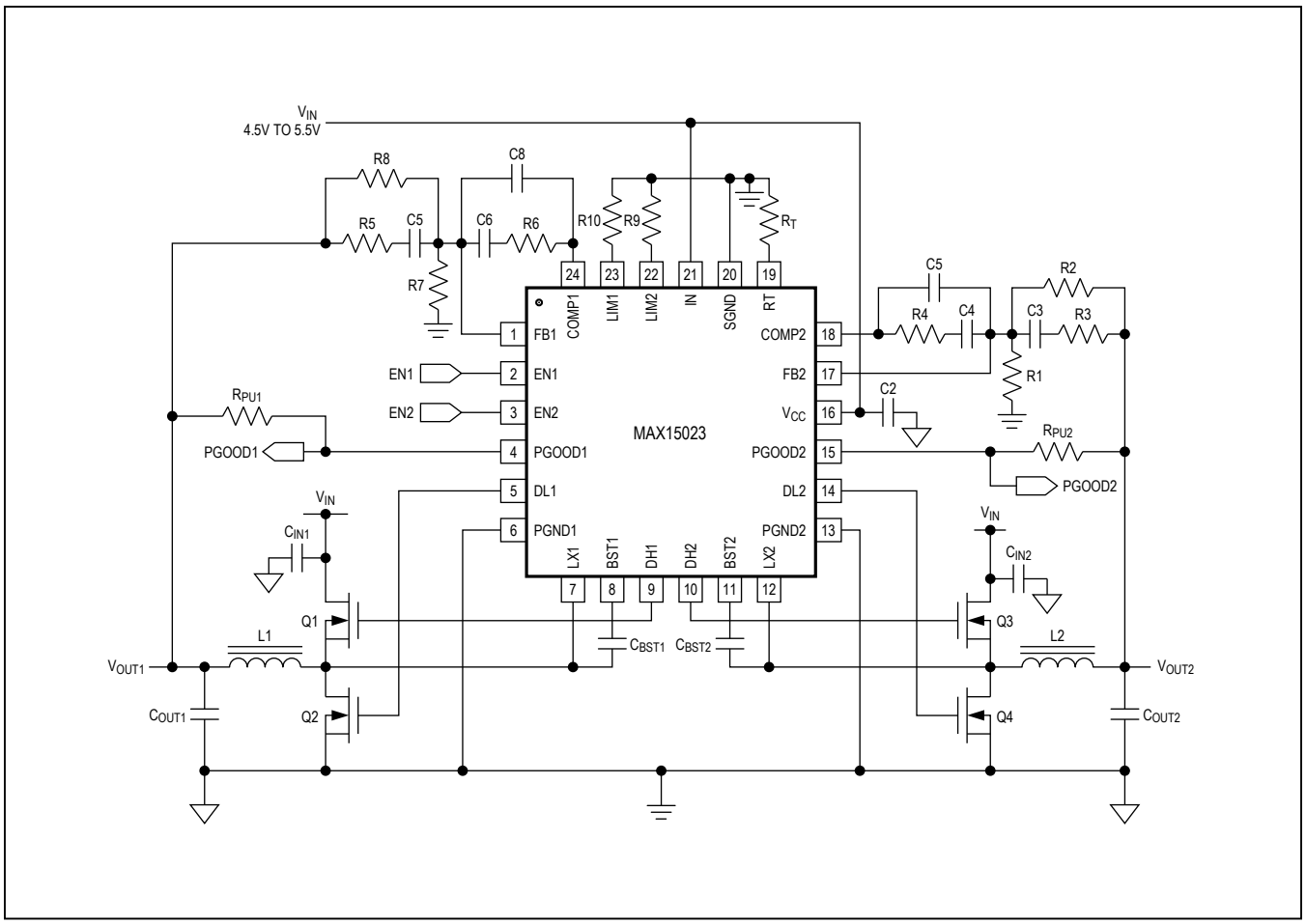



*Figure 7. Application Diagram (Operation with $V_{IN}$ = $V_{CC}$ = 5V ±10%)*

## Typical Application Circuits (continued)

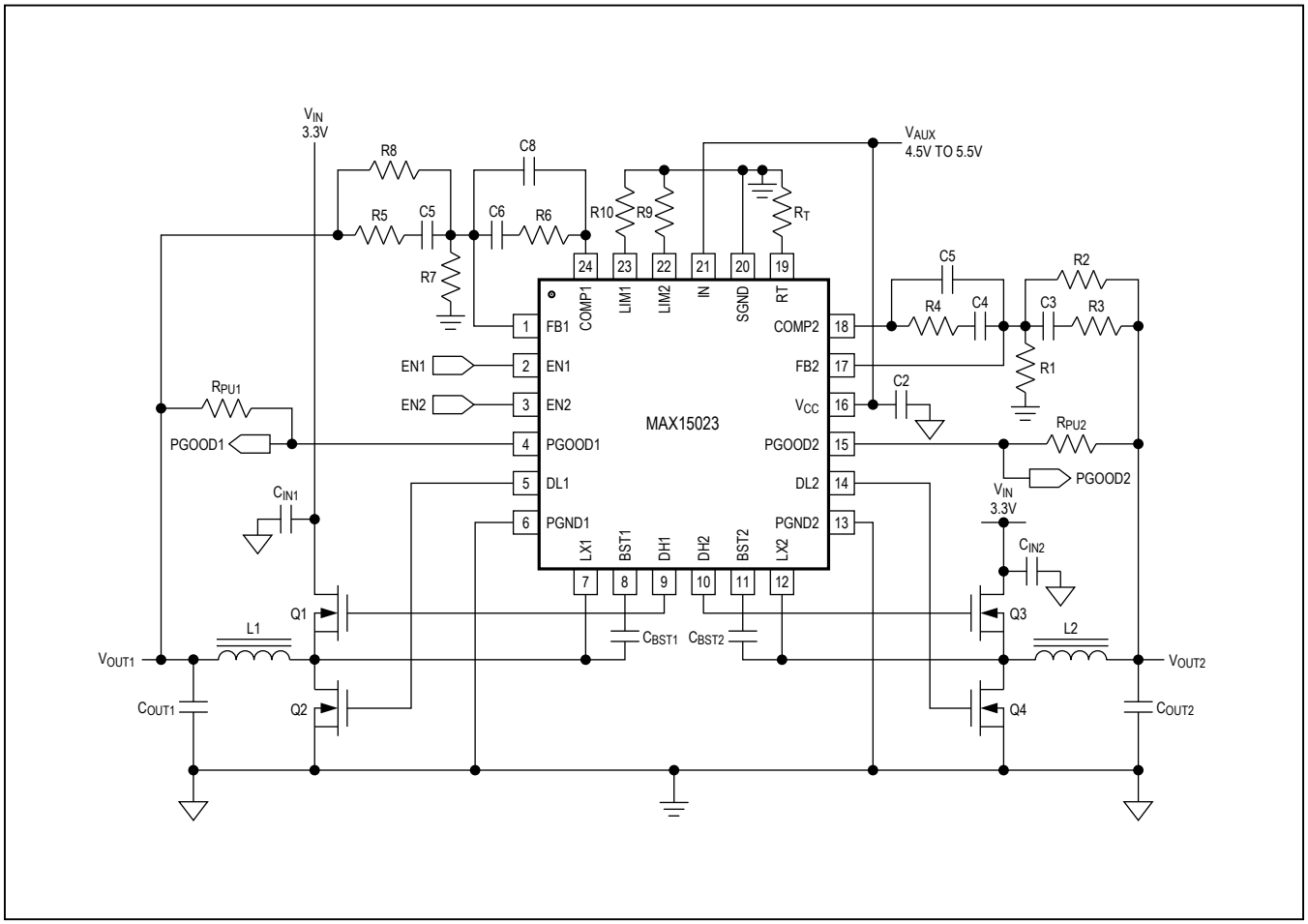



*Figure 8. Application Diagram (Operation with Auxiliary 5V Supply and 3.3V Bus)*

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 24 TQFN-EP | T2444+4 | 21-0139 | 90-0022 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 7/08 | Initial release | — |
| 1 | 2/09 | Updated *Electrical Characteristics*, *Current-Limit Circuit (LIM_)*, and *Setting the Enable Input (EN_)* sections. | 4, 15, 16 |
| 2 | 3/11 | Added automotive part MAX5023ETG/V+ | 1, 2, 13, 27 |
| 3 | 4/15 | Added automotive designation footnote | 1 |

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