Click here for production status of specific part numbers.

MAX15035 15A Step-Down Regulator with Internal Switches

General Description

The MAX15035 pulse-width modulation (PWM) controller provides high efficiency, excellent transient response, and high DC-output accuracy. Combined with the internal low on-resistance MOSFETs, the MAX15035 provides a highly efficient and compact solution for small form factor applications that need a high-power density.

Maxim's proprietary Quick-PWM™ quick-response, constant on-time PWM control scheme handles wide input/output voltage ratios (low-duty-cycle applications) with ease and provides 100ns instant-on response to load transients while maintaining a relatively constant switching frequency. The output voltage can be dynamically controlled using the dynamic REFIN, which supports input voltages between 0V to 2V. The REFIN adjustability combined with a resistive voltage-divider on the feedback input allows the MAX15035 to be configured for any output voltage between 0V to $0.9V_{IN}$.

The controller senses the current across the synchronous rectifier to achieve a low-cost and highly efficient valley current-limit protection. External current-limit control is provided to allow higher current-limit settings for applications with heatsinks and air flow, or for lower current applications that need lower current-limit settings to avoid overdesigning the application circuit. The adjustable current limit provides a high degree of flexibility, allowing thermally compensated protection or foldback current-limit protection using a voltage-divider partially derived from the output.

The MAX15035 includes a voltage-controlled soft-start and soft-shutdown to limit the input surge current, provide a monotonic power-up into a precharged output, and provide a predictable soft-start time. The controller also includes output fault protection—undervoltage and overvoltage protection—as well as thermal-fault protection.

The MAX15035 is available in a small 40-pin, 6mm x 6mm, TQFN package.

Features

- 4.5V to 26V Input Voltage Range
- Fast Transient Response
- Monotonic Power-Up with Precharged Output
- Supports Any Output Capacitor
  - No Compensation Required with Polymers/Tantalum
  - Stable with Ceramic Output Capacitors Using External Compensation
- Dynamically Adjustable Output Voltage
  - 0.5% V_{OUT} Accuracy Over Line and Load
- Adjustable Valley Current-Limit Protection
  - Thermal Compensation with NTC
  - Supports Foldback Current Limit
- Programmable Switching Frequency
- Overvoltage Protection
- Undervoltage Protection
- Voltage Soft-Start and Soft-Shutdown
- Power-Good Window Comparator

Applications

- Server Computers
- GPU Core Supplies
- DDR Memory—VDDQ or VTT
- Point-of-Load Applications
- Step-Down Power Supplies
- Storage Power Supplies

Ordering Information *appears at end of data sheet.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

19-4123; Rev 3; 4/18

maxim integrated™

Absolute Maximum Ratings

IN to PGND .....-0.3V to +28V
TON to GND .....-0.3V to +28V
V_{DD} to GND .....-0.3V to +6V
V_{CC} to GND .....-0.3V to (V_{DD} + 0.3V)
EN, $\overline{SKIP}$, PGOOD to GND.....-0.3V to +6V
REF, REFIN to GND.....-0.3V to (V_{CC} + 0.3V)
ILIM, FB to GND.....-0.3V to (V_{CC} + 0.3V)
GND to PGND .....-0.3V to +0.3V
LX to PGND.....-1V to +28V
BST to PGND .....(V_{DD} - 0.3V) to +34V
BST to LX .....-0.3V to +6V
BST to V_{DD} .....-0.3V to +28V
REF Short Circuit to GND .....Continuous
IN RMS Current Rating (continuous) 15A
PGND RMS Current Rating (continuous).....20A
Continuous Power Dissipation (T_A = +70°C)
40-Pin, 6mm x 6mm Thin QFN (T4066-MCM)
(derate 27mW/°C above +70°C) 2162mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 40-PIN TQFN	
Package Code	T4066M+1
Outline Number	21-0177
Land Pattern Number	90-0085

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics 1

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = ILIM = REF, $\overline{SKIP}$ = GND. **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{IN}			4.5		26.0	V
Quiescent Supply Current (V_{DD})	I_{DD} + I_{CC}	FB forced above REFIN			0.7	1.2	mA
Shutdown Supply Current (V_{DD})	I_{SHDN}	EN = GND, T_A = +25°C			0.1	2	µA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level; hysteresis = 100mV		3.95	4.2	4.45	V
V_{DD}-to-V_{CC} Resistance	R_{CC}				20		Ω
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.0V (Note 3)	R_{TON} = 97.5kΩ (600kHz)	123	164	205	ns
			R_{TON} = 200kΩ (300kHz)	275	303	331	
			R_{TON} = 302.5kΩ (200kHz)	379	442	505	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			225	350	ns
TON Shutdown Supply Current		EN = GND, V_{TON} = 26V, V_{CC} = 0V or 5V, T_A = +25°C			0.01	1	µA
REFIN Voltage Range	V_{REFIN}	(Note 2)		0		V_{REF}	V

Electrical Characteristics 1 (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = ILIM = REF, $\overline{SKIP}$ = GND. **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFIN Input Current	I_{REFIN}	T_A = +25°C, REFIN = 0.5V to 2V		-50		+50	nA
FB Voltage Range	V_{FB}	(Note 2)		0		V_{REF}	V
FB Voltage Accuracy	V_{FB}	V_{REFIN} = 0.5V, measured at FB, V_{IN} = 4.5V to 26V, $\overline{SKIP}$ = V_{DD}	T_A = +25°C	0.495	0.5	0.505	V
			T_A = 0°C to +85°C	0.493		0.507	
		V_{REFIN} = 1.0V	T_A = +25°C	0.995	1.0	1.005	
			T_A = 0°C to +85°C	0.993		1.007	
		V_{REFIN} = 2.0V	T_A = 0°C to +85°C	1.990	2.0	2.010	
FB Input Bias Current	I_{FB}	V_{FB} = 0.5V to 2.0V, T_A = +25°C		-0.1		+0.1	µA
FB Output Low Voltage		I_{SINK} = 3mA				0.4	V
Load-Regulation Error		$\overline{SKIP}$ = V_{DD}			0.1		%
Line-Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.2		%
Soft-Start/Soft-Stop Slew Rate	SS_{SR}	Rising/falling edge on EN		0.4	1.2	2.2	mV/µs
Dynamic REFIN Slew Rate	DYN_{SR}	Rising edge on REFIN		3	9.45	18	mV/µs
REFERENCE							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V	No load	1.990	2.00	2.010	V
			I_{REF} = -10µA to +50µA	1.98		2.02	
FAULT DETECTION							
Output Overvoltage-Protection Trip Threshold	OVP	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV		250	300	350	mV
		Dynamic transition			V_{REF} + 0.30		V
		Minimum OVP threshold			0.7		
Output Overvoltage Fault-Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold			5		µs
Output Undervoltage-Protection Trip Threshold	UVP	With respect to the internal target voltage (error comparator threshold) falling edge; hysteresis = 50mV		-240	-200	-160	mV
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold		100	200	350	µs
PGOOD Propagation Delay	t_{PGOOD}	UVP falling edge, 25mV overdrive			5		µs
		OVP rising edge, 25mV overdrive			5		
		Startup delay		100	200	350	
PGOOD Output-Low Voltage		I_{SINK} = 3mA				0.4	V
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN (PGOOD high impedance), PGOOD forced to 5V, T_A = +25°C				1	µA

Electrical Characteristics 1 (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = ILIM = REF, $\overline{SKIP}$ = GND. **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic REFIN Transition Fault Blanking Threshold		Fault blanking initiated; REFIN deviation from the internal target voltage (error comparator threshold); hysteresis = 10mV		±50		mV
Thermal-Shutdown Threshold	T_{SHDN}	Temperature rising, hysteresis = 15°C		160		°C
CURRENT LIMIT						
ILIM Input Range			0.4		V_{REF}	V
ILIM Input Bias Current		T_A = +25°C, ILIM = 0.4V to 2V	-0.1		+0.1	µA
Current-Limit Threshold	V_{ILIMIT}	V_{ILIM} = 0.4V, V_{GND} - V_{LX}	18	20	22	mV
		ILIM = REF (2.0V), V_{GND} - V_{LX}	92	100	108	
Current-Limit Threshold (Negative)	V_{INEG}	V_{ILIM} = 0.4V, V_{GND} - V_{LX}		-24		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{ILIM} = 0.4V, V_{GND} - V_{LX}, $\overline{SKIP}$ = GND or open		1		mV
Ultrasonic Frequency		$\overline{SKIP}$ = open (3.3V); V_{FB} = V_{REFIN} + 50mV	18	30		kHz
Ultrasonic Current-Limit Threshold		$\overline{SKIP}$ = open (3.3V); V_{FB} = V_{REFIN} + 50mV, V_{GND} - V_{LX}		-35		mV
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V		4	7	Ω
INPUTS AND OUTPUTS						
EN Logic-Input Threshold	V_{EN}	EN rising edge, hysteresis = 450mV (typ)	1.20	1.7	2.20	V
EN Logic-Input Current	I_{EN}	EN forced to GND or V_{DD}, T_A = +25°C	-0.5		+0.5	µA
$\overline{SKIP}$ Quad-Level Input Logic Levels	$V_{\overline{SKIP}}$	High (5V V_{DD})	V_{CC} - 0.4			V
		Open (3.3V)	3.0		3.6	
		Ref (2.0V)	1.7		2.3	
		Low (GND)			0.4	
$\overline{SKIP}$ Logic-Input Current	$I_{\overline{SKIP}}$	$\overline{SKIP}$ forced to GND or V_{DD}, T_A = +25°C	-2		+2	µA

Electrical Characteristics 2

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = ILIM = REF, $\overline{SKIP}$ = GND. **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V_{IN}			4.5	26	V
Quiescent Supply Current (V_{DD})	I_{DD} + I_{CC}	FB forced above REFIN			1.2	mA
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.0V (Note 3)	R_{TON} = 97.5kΩ (600kHz)	115	213	ns
			R_{TON} = 200kΩ (300kHz)	270	336	
			R_{TON} = 302.5kΩ (200kHz)	368	516	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			400	ns
REFIN Voltage Range	V_{REFIN}	(Note 2)		0	V_{REF}	V

Electrical Characteristics 2 (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = ILIM = REF, $\overline{SKIP}$ = GND. **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 1)

FB Voltage Range	V_{FB}	(Note 2)		0	V_{REF}	V
FB Voltage Accuracy	V_{FB}	Measured at FB, V_{IN} = 4.5V to 26V, $\overline{SKIP}$ = V_{DD}	V_{REFIN} = 0.5V	0.49	0.51	V
			V_{REFIN} = 1.0V	0.99	1.01	
			V_{REFIN} = 2.0V	1.985	2.015	
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**MAX**	**UNITS**
REFERENCE						
Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V		1.985	2.015	V
FAULT DETECTION						
Output Overvoltage-Protection Trip Threshold	OVP	With respect to the internal target voltage (error comparator threshold) rising edge; hysteresis = 50mV		250	350	mV
Output Undervoltage-Protection Trip Threshold	UVP	With respect to the internal target voltage (error comparator threshold); falling edge; hysteresis = 50mV		-240	-160	mV
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold		80	400	µs
PGOOD Output-Low Voltage		I_{SINK} = 3mA			0.4	V
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level, hysteresis = 100mV		3.95	4.45	V
CURRENT LIMIT						
ILIM Input Range				0.4	V_{REF}	V
Current-Limit Threshold	V_{ILIMIT}	V_{ILIM} = 0.4V, V_{GND} = V_{LX}		17	23	mV
		ILIM = REF (2.0V), V_{GND} - V_{LX}		90	110	
Ultrasonic Frequency		$\overline{SKIP}$ = open (3.3V), V_{FB} = V_{REFIN} + 50mV		17		kHz
INPUTS AND OUTPUTS						
EN Logic-Input Threshold	V_{EN}	EN rising edge hysteresis = 450mV (typ)		1.20	2.20	V
$\overline{SKIP}$ Quad-Level Input Logic Levels	$V_{\overline{SKIP}}$	High (5V V_{DD})		V_{CC} - 0.4		V
		Mid (3.3V)		3.0	3.6	
		Ref (2.0V)		1.7	2.3	
		Low (GND)			0.4	

Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

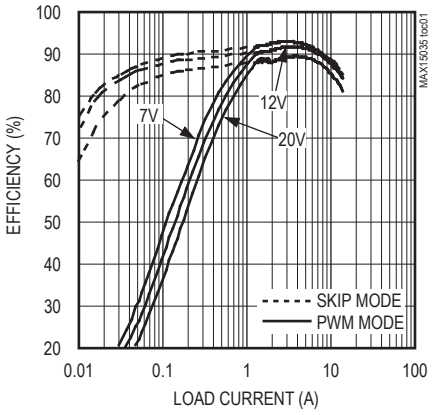
Note 2: The 0 to 0.5V range is guaranteed by design, not production tested.

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the unloaded LX node. The typical 25ns dead time that occurs between the high-side driver falling edge (high-side MOSFET turn-off) and the low-side MOSFET turnon) is included in the on-time measurement. Similarly, the typical 25ns dead time that occurs between the low-side driver falling edge (low-side MOSFET turn-off) and the high-side driver rising edge (high-side MOSFET turn-on) is included in the off-time measurement.

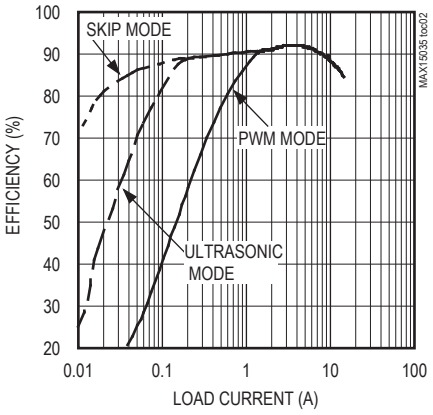
Typical Operating Characteristics

(MAX15035 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

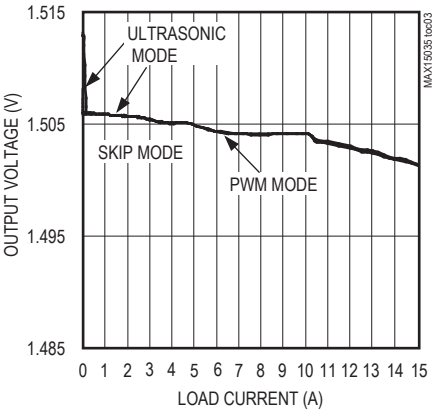
1.5V OUTPUT EFFICIENCY vs. LOAD CURRENT



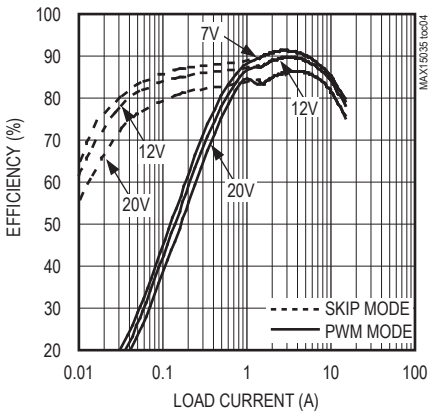
1.5V OUTPUT EFFICIENCY vs. LOAD CURRENT



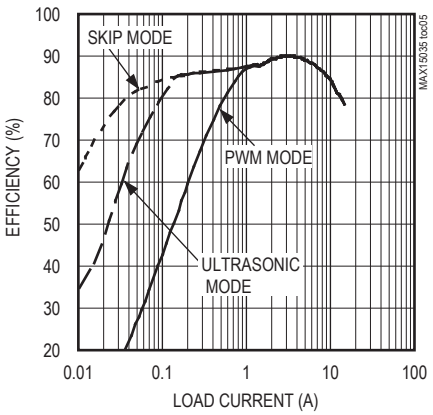
1.5V OUTPUT VOLTAGE vs. LOAD CURRENT



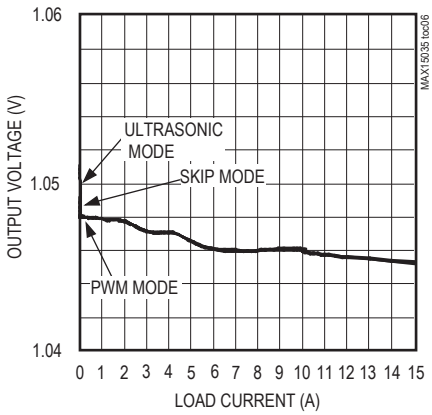
1.05V OUTPUT EFFICIENCY vs. LOAD CURRENT



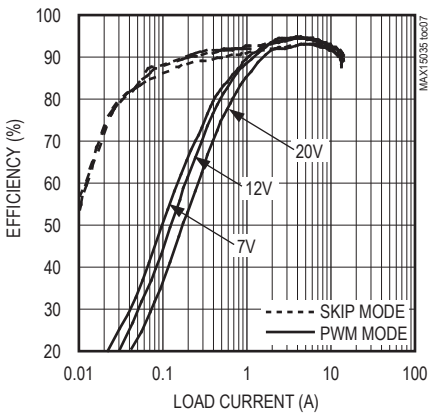
1.05V OUTPUT EFFICIENCY vs. LOAD CURRENT



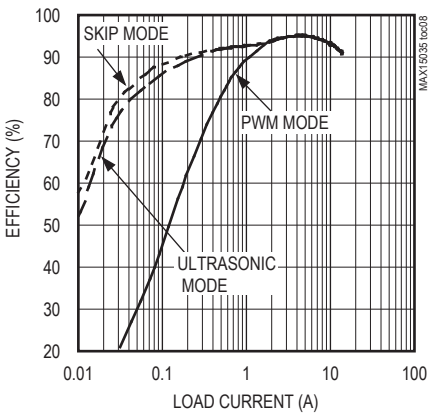
1.05V OUTPUT VOLTAGE vs. LOAD CURRENT



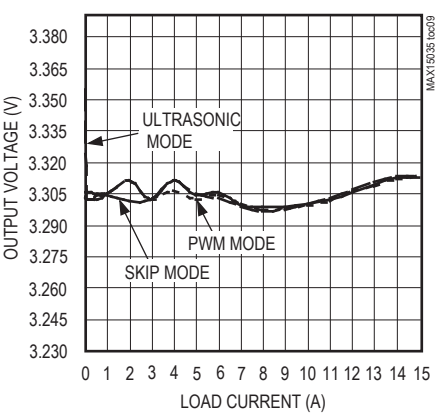
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



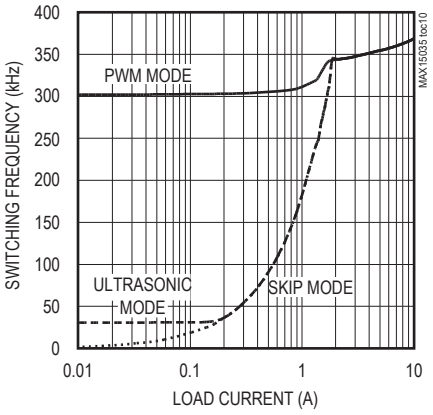
3.3V OUTPUT VOLTAGE vs. LOAD CURRENT



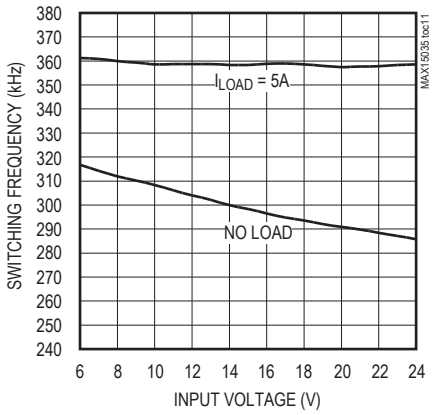
Typical Operating Characteristics (continued)

(MAX15035 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

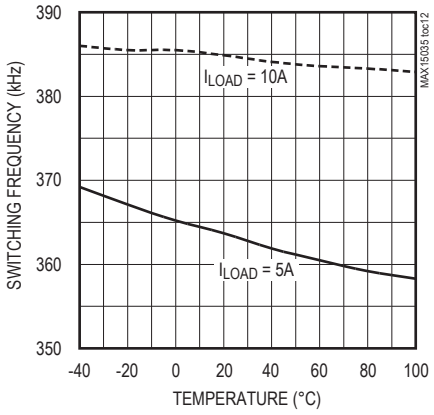
SWITCHING FREQUENCY vs. LOAD CURRENT



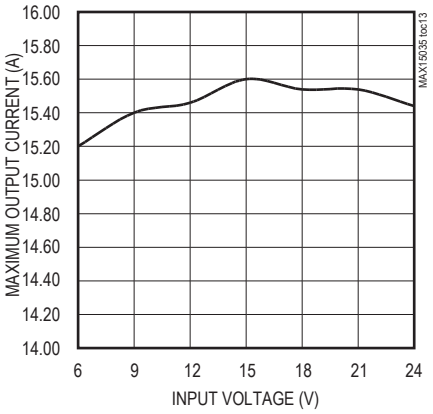
PWM MODE SWITCHING FREQUENCY vs. INPUT VOLTAGE



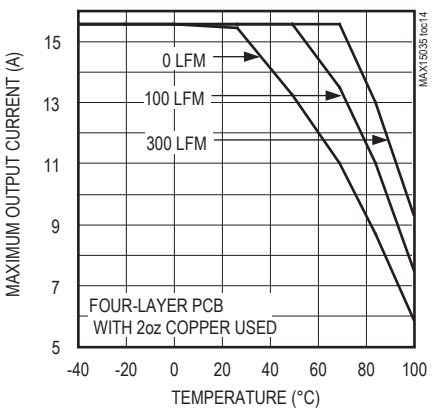
SWITCHING FREQUENCY vs. TEMPERATURE



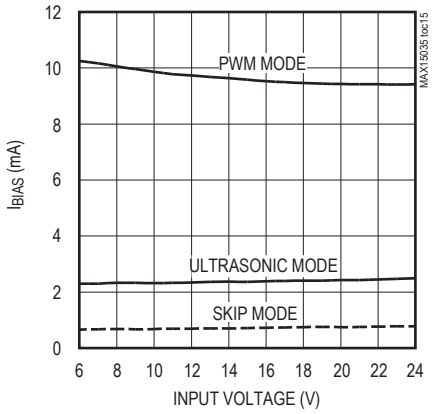
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



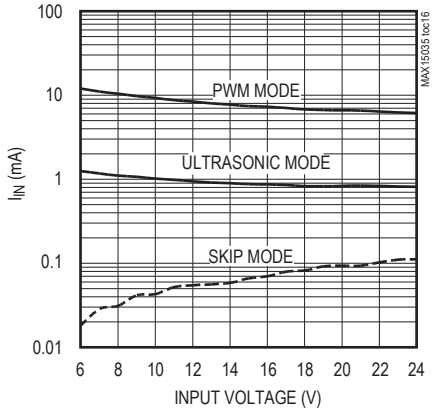
MAXIMUM OUTPUT CURRENT vs. AMBIENT TEMPERATURE



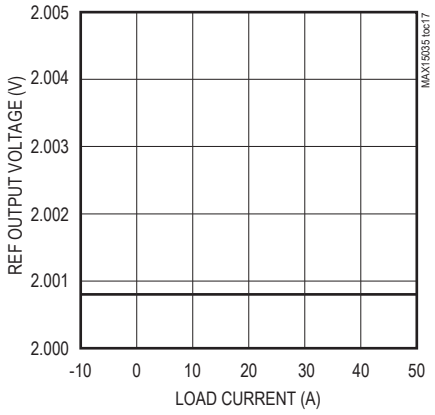
NO-LOAD SUPPLY CURRENT (I_{BIAS}) vs. INPUT VOLTAGE



NO-LOAD SUPPLY CURRENT (I_{IN}) vs. INPUT VOLTAGE



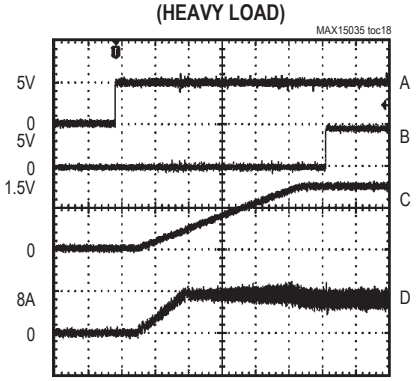
REF OUTPUT VOLTAGE vs. LOAD CURRENT



Typical Operating Characteristics (continued)

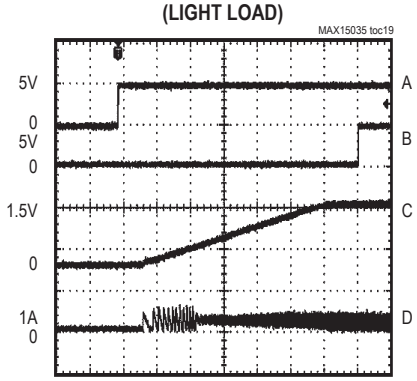
(MAX15035 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

SOFT-START WAVEFORM (HEAVY LOAD)



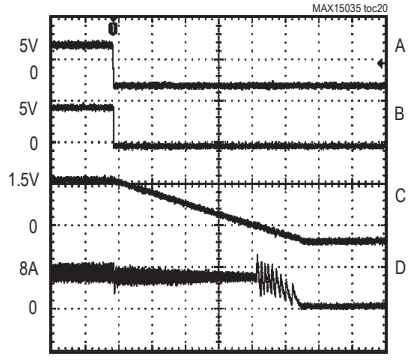
A. EN, 5V/div
B. PGOOD, 5V/div
I_{OUT} = 8A
C. V_{OUT}, 1V/div
B. INDUCTOR CURRENT, 10A/div

SOFT-START WAVEFORM (LIGHT LOAD)



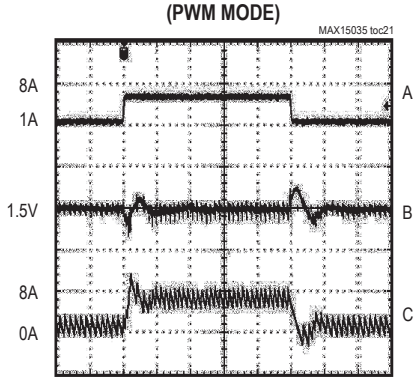
A. EN, 5V/div
B. PGOOD, 5V/div
I_{OUT} = 1A
C. V_{OUT}, 1V/div
B. INDUCTOR CURRENT, 10A/div

SHUTDOWN WAVEFORM



A. EN, 5V/div
B. PGOOD, 5V/div
I_{OUT} = 6A
C. V_{OUT}, 1V/div
B. INDUCTOR CURRENT, 5A/div

LOAD-TRANSIENT RESPONSE (PWM MODE)

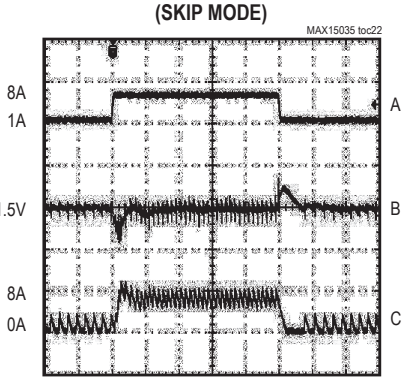


A. I_{OUT}, 10A/div
I_{OUT} = 1A TO 8A TO 1A
B. V_{OUT}, 20mV/div
C. INDUCTOR CURRENT, 5A/div

Typical Operating Characteristics (continued)

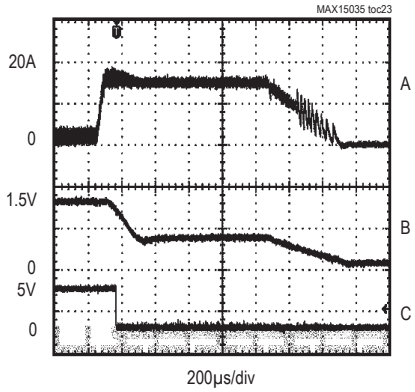
(MAX15035 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (SKIP MODE)



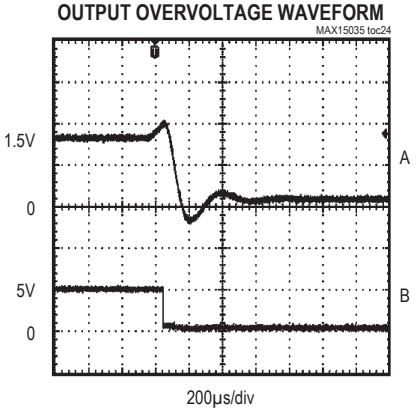
A. I_{OUT}, 10A/div
B. V_{OUT}, 20mV/div
C. INDUCTOR CURRENT, 5A/div
I_{OUT} = 1A TO 8A TO 1A

OUTPUT OVERCURRENT WAVEFORM



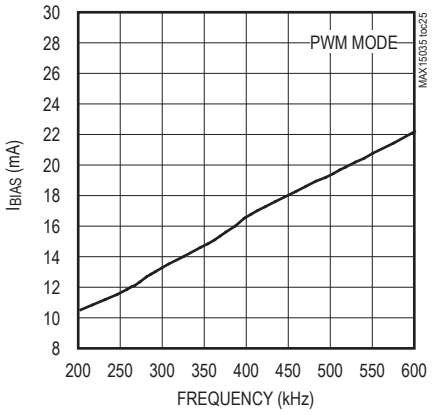
A. INDUCTOR CURRENT, 10A/div
B. V_{OUT}, 1V/div
C. PGOOD, 5V/div
I_{OUT} = 2A TO 20A

OUTPUT OVERVOLTAGE WAVEFORM

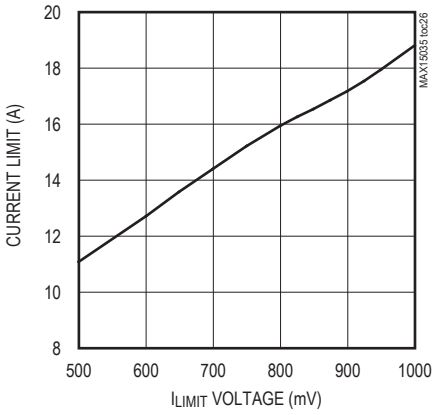


A. V_{OUT}, 1V/div
B. PGOOD, 5V/div
I_{OUT} = 2A TO 20A

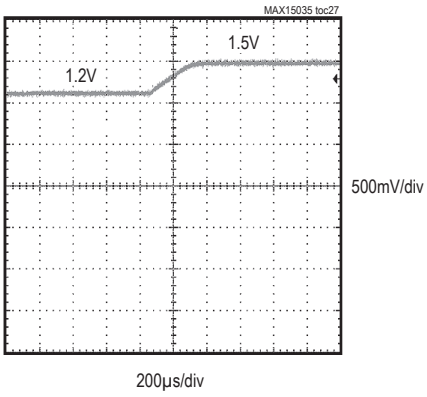
NO-LOAD BIAS CURRENT vs. FREQUENCY



OUTPUT CURRENT LIMIT vs. I_{LIMIT} VOLTAGE



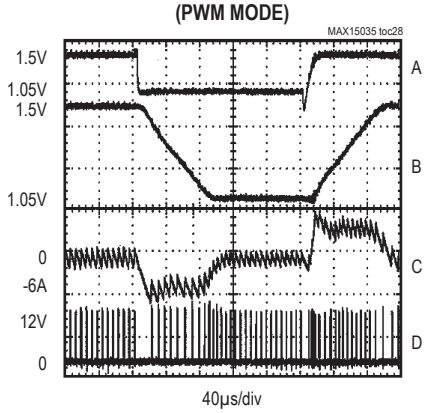
PREBIAS STARTUP-OUTPUT VOLTAGE



Typical Operating Characteristics (continued)

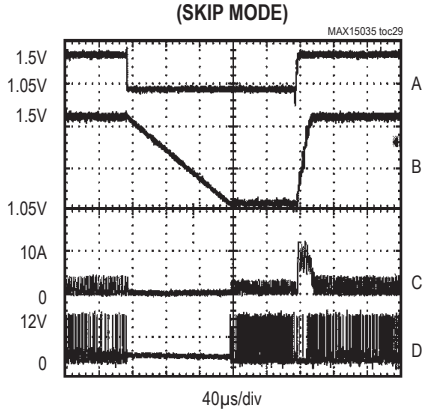
(MAX15035 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

DYNAMIC OUTPUT-VOLTAGE TRANSITION (PWM MODE)



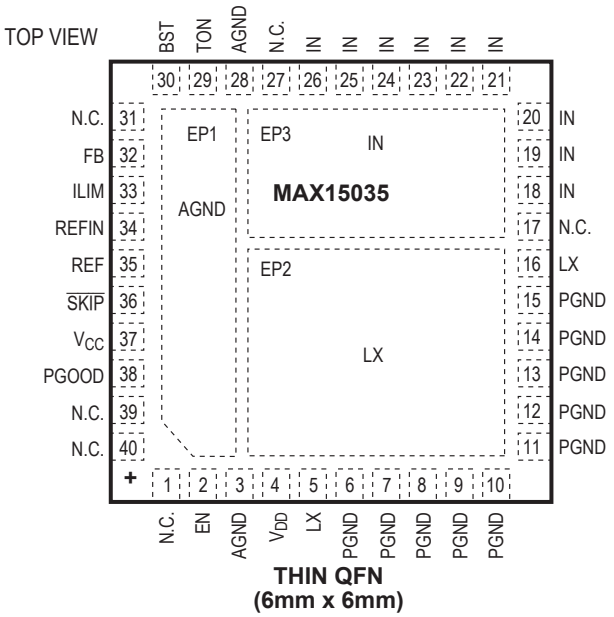
A. REFIN, 500mV/div
B. V_{OUT}, 200mV/div
I_{OUT} = 2A
C. INDUCTOR CURRENT, 10A/div
D. LX, 10V/div

DYNAMIC OUTPUT-VOLTAGE TRANSITION (SKIP MODE)



A. REFIN, 500mV/div
B. V_{OUT}, 200mV/div
I_{OUT} = 2A
C. INDUCTOR CURRENT, 10A/div
D. LX, 10V/div

Pin Configuration



THIN QFN
(6mm x 6mm)

Pin Description

PIN	NAME	FUNCTION
1, 17, 27, 31, 39, 40	N.C.	No Connection. Not internally connected.
2	EN	Shutdown Control Input. Connect to V_{DD} for normal operation. Pull EN low to put the controller into its 2µA (max) shutdown state. The MAX15035 slowly ramps down the target/output voltage to ground and after the target voltage reaches 0.1V, the controller forces LX into a high-impedance state and enters the low-power shutdown state. Toggle EN to clear the fault-protection latch.
3, 28	AGND	Analog Ground. Internally connected to EP1.
4	V_{DD}	Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to power ground with a 1µF or greater ceramic capacitor.
5, 16	LX	Inductor Connection. Internally connected to EP2. Connect LX to the switched side of the inductor as shown in Figure 1.
6–15	PGND	Power Ground
18–26	IN	Power MOSFET Input Power Source. Internally connected to EP3.
29	TON	Switching Frequency-Setting Input. An external resistor between the input power source and TON sets the switching period ($t_{SW} = 1/f_{SW}$) according to the following equation: $$t_{SW} = C_{TON}(R_{TON} + 6.5k\Omega)\left(\frac{V_{FB}}{V_{OUT}}\right)$$ where C_{TON} = 16.26pF and $V_{FB} = V_{REFIN}$ under normal operating conditions. If the TON current drops below 10µA, the MAX15035 shuts down and enters a high-impedance state. TON is high impedance in shutdown.
30	BST	Boost Flying Capacitor Connection. Connect to an external 0.1µF capacitor as shown in Figure 1. The MAX15035 contains an internal boost switch/diode (Figure 2).

Pin Description (continued)

PIN	NAME	FUNCTION
32	FB	Feedback Voltage Sense Connection. Connect directly to the positive terminal of the output capacitors for output voltages less than 2V as shown in Figure 1. For fixed-output voltages greater than 2V, connect REFIN to REF and use a resistive divider to set the output voltage (Figure 6). FB senses the output voltage to determine the on-time for the high-side switching MOSFET.
33	ILIM	Current-Limit Threshold Adjustment. The current-limit threshold is 0.05 times (1/20) the voltage at ILIM. Connect ILIM to a resistive divider (from REF) to set the current-limit threshold between 20mV and 100mV (with 0.4V to 2V at ILIM).
34	REFIN	External Reference Input. REFIN sets the feedback regulation voltage (V_{FB} = V_{REFIN}) of the MAX15035 using a resistor-divider connected between REF and AGND. The MAX15035 includes an internal window comparator to detect REFIN voltage transitions, allowing the controller to blank PGOOD and the fault protection.
35	REF	2V Reference Voltage. Bypass to analog ground using a 1nF ceramic capacitor. The reference can source up to 50µA for external loads.
36	$\overline{SKIP}$	Pulse-Skipping Control Input. This four-level input determines the mode of operation under normal steady-state conditions and dynamic output-voltage transitions: V_{DD} (5V) = Forced-PWM operation REF (2V) = Pulse-skipping mode (with forced-PWM during transitions) Open (3.3V) = Ultrasonic mode (without forced-PWM during transitions) GND = Pulse-skipping mode (without forced-PWM during transitions)
37	V_{CC}	5V Analog Supply Voltage. Internally connected to V_{DD} through an internal 20Ω resistor. Bypass V_{CC} to analog ground using a 1µF ceramic capacitor.
38	PGOOD	Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 200mV (typ) below or 300mV (typ) above the target voltage (V_{REFIN}), during soft-start, and soft-shutdown. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation. PGOOD is blanked—forced high-impedance state—when a dynamic REFIN transition is detected.
EP1 (41)	AGND	Exposed Pad 1/Analog Ground. Internally connected to the controller's ground plane and substrate. Connect directly to ground.
EP2 (42)	LX	Exposed Pad 2/Inductor Connection. Internally connected to drain of the low-side MOSFET and source of the high-side MOSFET (Figure 2). Connect LX to the switched side of the inductor as shown in Figure 1.
EP3 (43)	IN	Exposed Pad 3/Power MOSFET Input Power Source. Internally connected to drain of the high-side MOSFET (Figure 2).

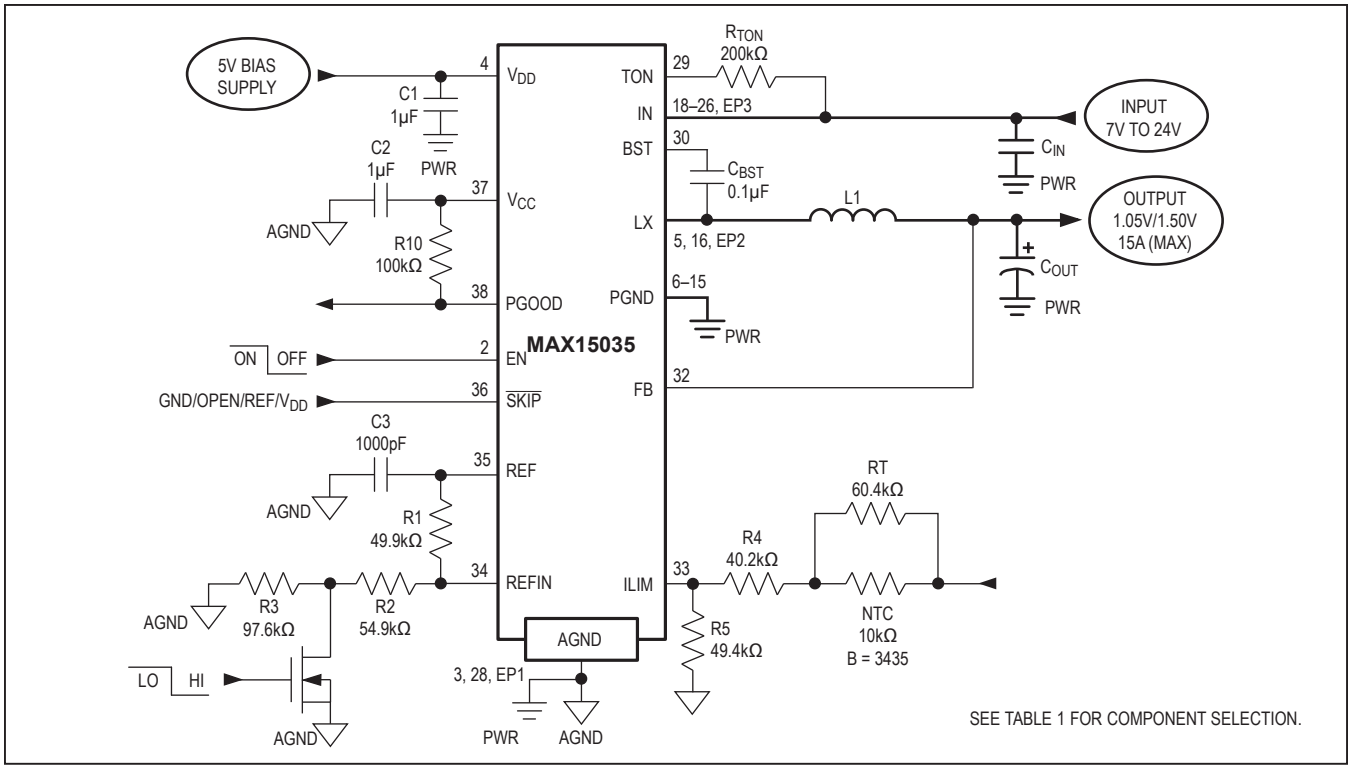


Figure 1. MAX15035 Standard Application Circuit

Table 1. Component Selection for Standard Applications

COMPONENT	V_{OUT} = 1.5V/1.05V AT 15A (Figure 1)	V_{OUT} = 3.3V AT 6A (Figure 6)	V_{OUT} = 1.5V/1.05V AT 10A (Figure 1)
	V_{IN} = 7V to 20V TON = 200kΩ (300kHz)	V_{IN} = 7V to 20V TON = 332kΩ (300kHz)	V_{IN} = 5V to 12V TON = 100kΩ (600kHz)
Input Capacitor	(3x) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2x) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(3x) 10µF, 25V Taiyo Yuden TMK432BJ106KM
Output Capacitor	(2x) 330µF, 6mΩ, 2V Panasonic EEFSX0D331XR	(1x) 330µF, 18mΩ, 4V SANYO 4TPE330MI	(1x) 470µF, 7mΩ, 2.5V SANYO 2R5TPLF470M7
Inductor	1.0µH, 5.3mΩ, 27.5A Vishay IHLP4040DZER1R0	1.5µH, 14mΩ, 9A NEC TOKIN MPLC1040L3R3	0.47µH, 3.7mΩ, 15A Cooper FP3-R47-R

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Cooper Bussmann	www.cooperet.com
KEMET Corp.	www.kemet.com
Murata Mfg. Co., Ltd.	www.murata.com
NEC TOKIN Corp.	www.nec-tokin.com
Panasonic Corp.	www.panasonic.com

SUPPLIER	WEBSITE
Pulse Engineering	www.pulseeng.com
SANYO NA Corp.	www.sanyo.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay	www.vishay.com
Würth Electronik GmbH & Co. KG	www.we-online.com

Standard Application Circuit

The MAX15035 standard application circuit (Figure 1) generates a 1.5V or 1.05V output rail for general-purpose use. See Table 1 for component selections. Table 2 lists the component suppliers.

Detailed Description

The MAX15035 step-down controller is ideal for low-duty-cycle (high-input voltage to low-output voltage) applications. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX15035 is specifically designed for handling fast-load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency, current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time (regardless of input voltage) pulse-frequency modulation (PFM) control schemes.

+5V Bias Supply (V_{CC}/V_{DD})

The MAX15035 requires an external 5V bias supply in addition to the input. See Figure 6 for an optional 5V bias generation circuit.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is determined by:

$$I_{BIAS} = I_Q + f_{SW}Q_G = 2mA \text{ to } 20mA \text{ (typ)}$$

The MAX15035 includes a 20Ω resistor between V_{DD} and V_{CC}, simplifying the PCB layout requirement.

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum offtime (200ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to input and output voltage. The high-side switch on-time is inversely proportional to the input voltage as sensed by the TON input, and proportional to the feedback voltage as sensed by the FB input:

$$\text{On-Time } (t_{ON}) = t_{SW} (V_{FB}/V_{IN})$$

where t_{SW} (switching period) is set by the resistance (R_{TON}) between TON and IN. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. Connect a resistor (R_{TON}) between TON and IN to set the switching period $t_{SW} = 1/f_{SW}$:

$$t_{SW} = C_{TON}(R_{TON} + 6.5k\Omega)\left(\frac{V_{FB}}{V_{OUT}}\right)$$

where C_{TON} = 16.26pF. When used with unity-gain feedback ($V_{OUT} = V_{FB}$), a 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{FB} + V_{DIS}}{t_{ON}(V_{IN} - V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the resistances in the charging path, including the highside switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the MAX15035.

Power-Up Sequence (POR, UVLO)

The MAX15035 is enabled when EN is driven high and the 5V bias supply (V_{DD}) is present. The reference powers up first. Once the reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 50µs one-shot delay in order to allow the bias circuitry and analog blocks enough time to settle to their proper

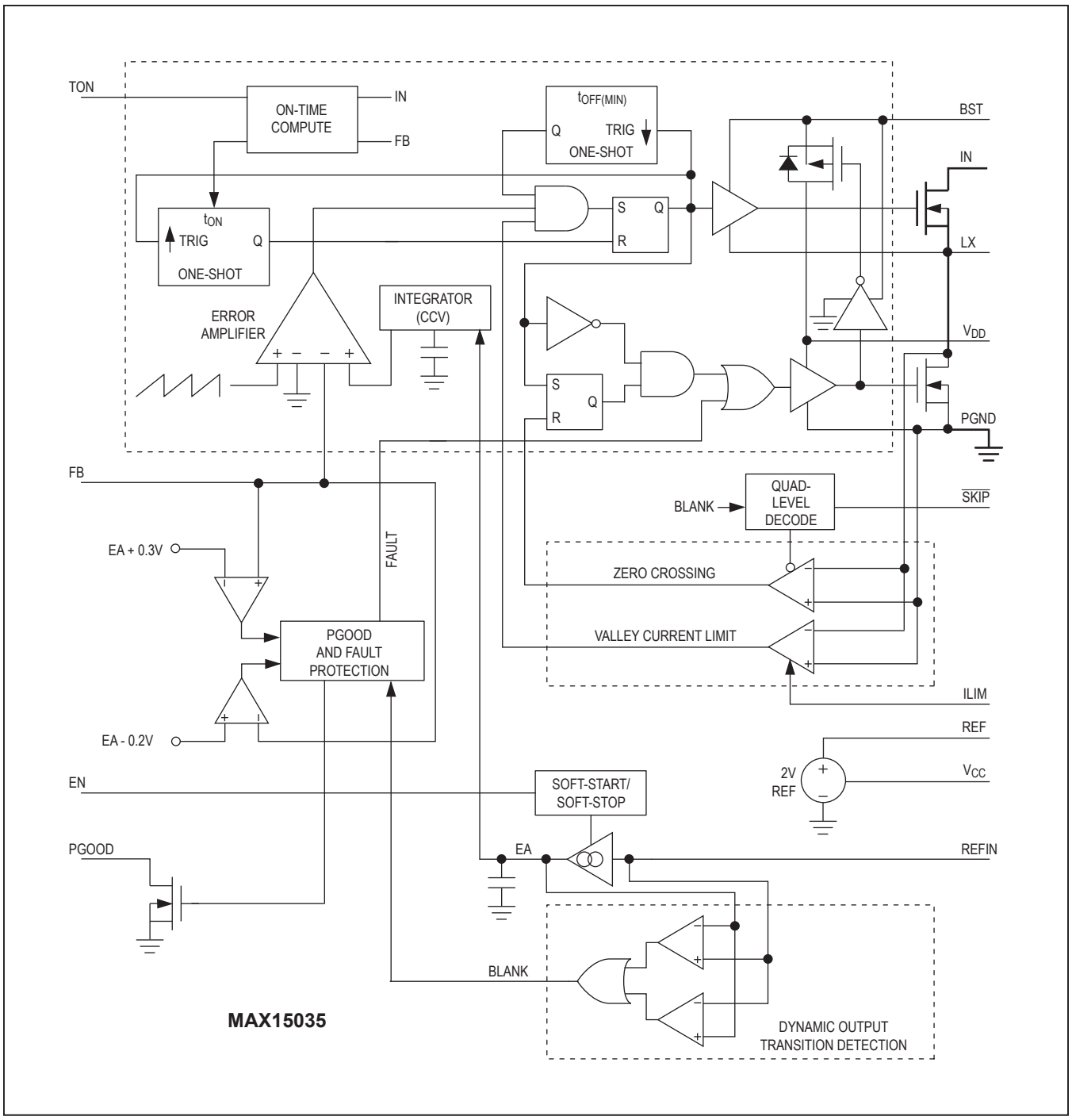


Figure 2. MAX15035 Block Diagram

states. With the control circuitry reliably powered up, the PWM controller may begin switching.

Power-on reset (POR) occurs when V_{CC} rises above approximately 3V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} exceeds 4.25V, and EN is driven high. With the reference in regulation, the controller ramps the output voltage to the target REFIN voltage with a 1.2mV/µs slew rate:

$$t_{START} = \frac{V_{FB}}{1.2mV/\mu s} = \frac{V_{FB}}{1.2V/ms}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PGOOD becomes high impedance approximately 200µs after the target REFIN voltage has been reached. The MAX15035 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown, regardless of the $\overline{SKIP}$ configuration.

For automatic startup, the input voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the input voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling EN or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high impedance on LX.

Shutdown

When the system pulls EN low, the MAX15035 enters low-power shutdown mode. PGOOD is pulled low immediately, and the output voltage ramps down with a 1.2mV/µs slew rate:

$$t_{SHDN} = \frac{V_{FB}}{1.2mV/\mu s} = \frac{V_{FB}}{1.2V/ms}$$

Slowly discharging the output capacitors by slewing the output over a long period of time (typically 0.5ms to 2ms) keeps the average negative inductor current low (damped response), thereby preventing the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX15035 shuts down completely—the drivers are disabled (high impedance on LX)—the reference turns off, and the supply currents drop to about 0.1µA (typ).

When a fault condition—output UVP or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle EN or cycle V_{CC} power below 0.5V.

The MAX15035 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown, regardless of the $\overline{SKIP}$ configuration.

Modes of Operation

Ultrasonic Mode ($\overline{SKIP}$ = Open = 3.3V)

Leaving $\overline{SKIP}$ unconnected activates a unique pulseskipping mode with a minimum switching frequency of 18kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(SKIP)}$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 33µs. Once triggered, the ultrasonic controller turns on the low-side MOSFET to induce a negative inductor current (Figure 3). After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET and triggers a constant on-time.

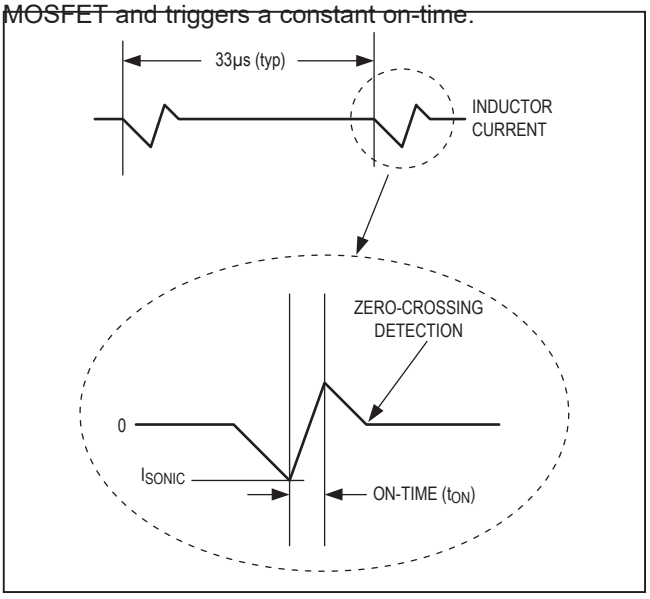


Figure 3. Ultrasonic Waveform

When the on-time expires, the controller re-enables the low-side MOSFET until the controller detects that the inductor current drops below the zero-crossing threshold. Starting with a negative inductor current pulse greatly reduces the peak output voltage when compared to starting with a positive inductor current pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equation:

$$V_{ISONIC} = I_L \times 0.006 = (V_{REFIN} - V_{FB}) \times 0.7$$

where $V_{FB} > V_{REFIN}$.

Forced-PWM Mode ($\overline{SKIP}$ = V_{DD})

The low-noise, forced-PWM mode ($\overline{SKIP}$ = V_{DD}) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while LX maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 10mA to 50mA, depending on the switching frequency.

The MAX15035 automatically always uses forced-PWM operation during shutdown, regardless of the $\overline{SKIP}$ configuration.

Automatic Pulse-Skipping Mode ($\overline{SKIP}$ = GND or REF)

In skip mode ($\overline{SKIP}$ = GND or 3.3V), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across LX to PGND.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX15035 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($\overline{SKIP}$ = GND and $I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

When $\overline{SKIP}$ is pulled to GND, the MAX15035 remains in pulse-skipping mode. Since the output is not able to sink current, the timing for negative dynamic output-voltage transitions depends on the load current and output capacitance. Letting the output voltage drift down is typically recommended to reduce the potential for audible noise since this eliminates the input current surge during negative output-voltage transitions. See Figures 4 and 5.

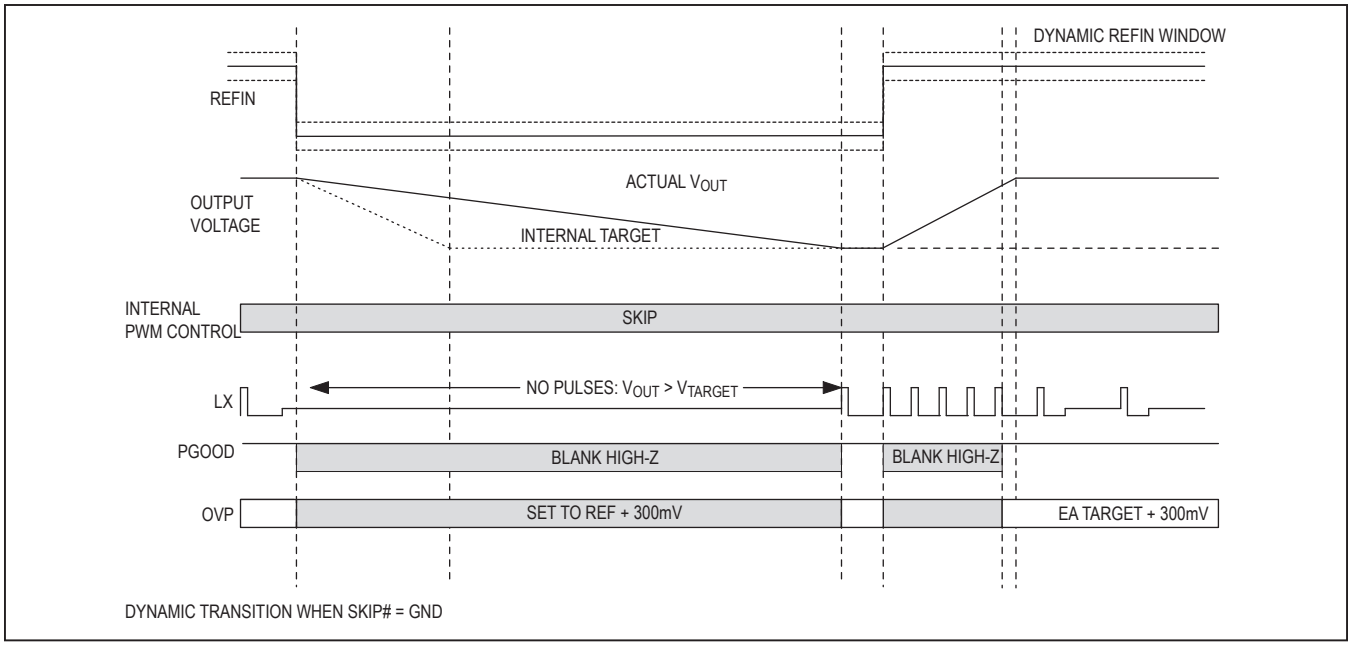


Figure 4. Dynamic Transition when $\overline{SKIP}$ = GND

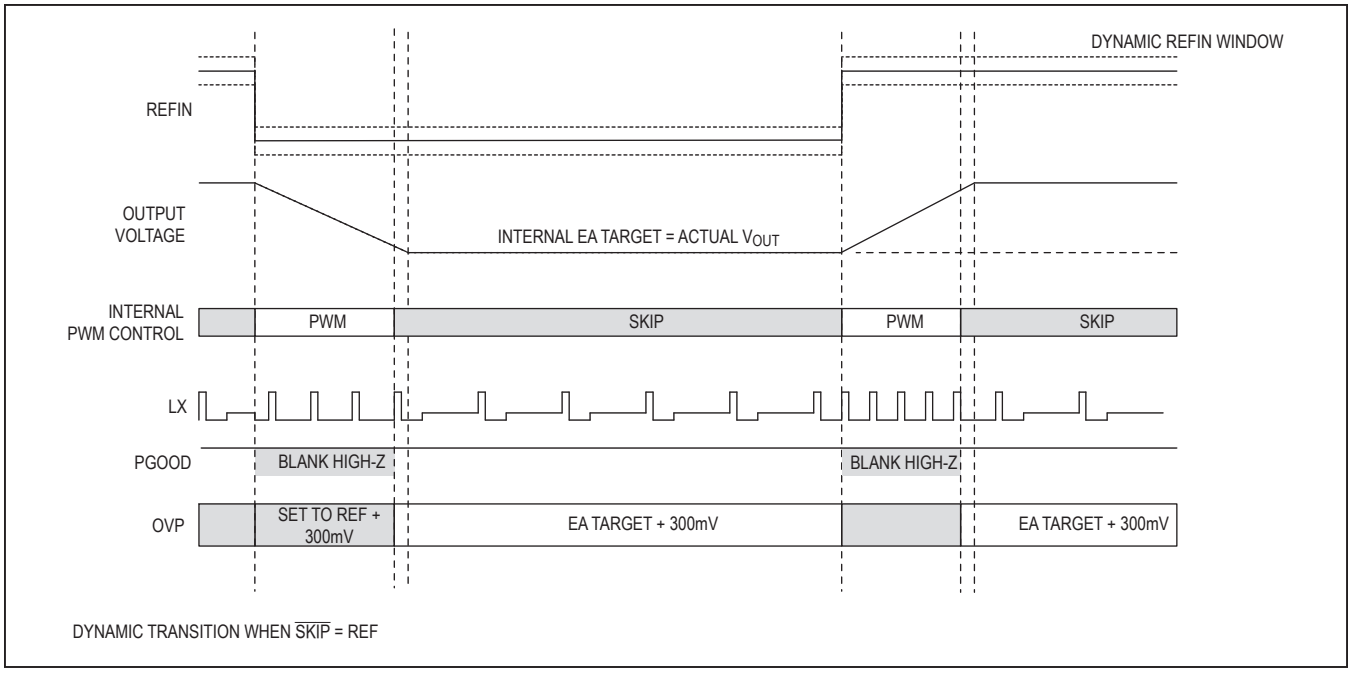


Figure 5. Dynamic Transition when $\overline{SKIP}$ = REF

Valley Current-Limit Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current through the low-side MOSFET. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX15035 also implements a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

Integrated Output Voltage

The MAX15035 regulates the valley of the output ripple, so the actual DC output voltage is higher than the slope-compensated target by 50% of the output ripple voltage. Under steady-state conditions, the MAX15035's internal integrator corrects for this 50% output ripple-voltage error, resulting in an output voltage that is dependent only on the offset voltage of the integrator amplifier provided in the *Electrical Characteristics* table.

Dynamic Output Voltages

The MAX15035 regulates FB to the voltage set at REFIN. By changing the voltage at REFIN (Figure 1), the MAX15035 can be used in applications that require dynamic output-voltage changes between two set points. For a step-voltage change at REFIN, the rate of change of the output voltage is limited either by the internal 9.45mV/µs slew-rate circuit or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is slower. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate. Additional load current may slow down the output voltage change during a positive REFIN voltage change, and may speed up the output voltage change during a negative REFIN voltage change.

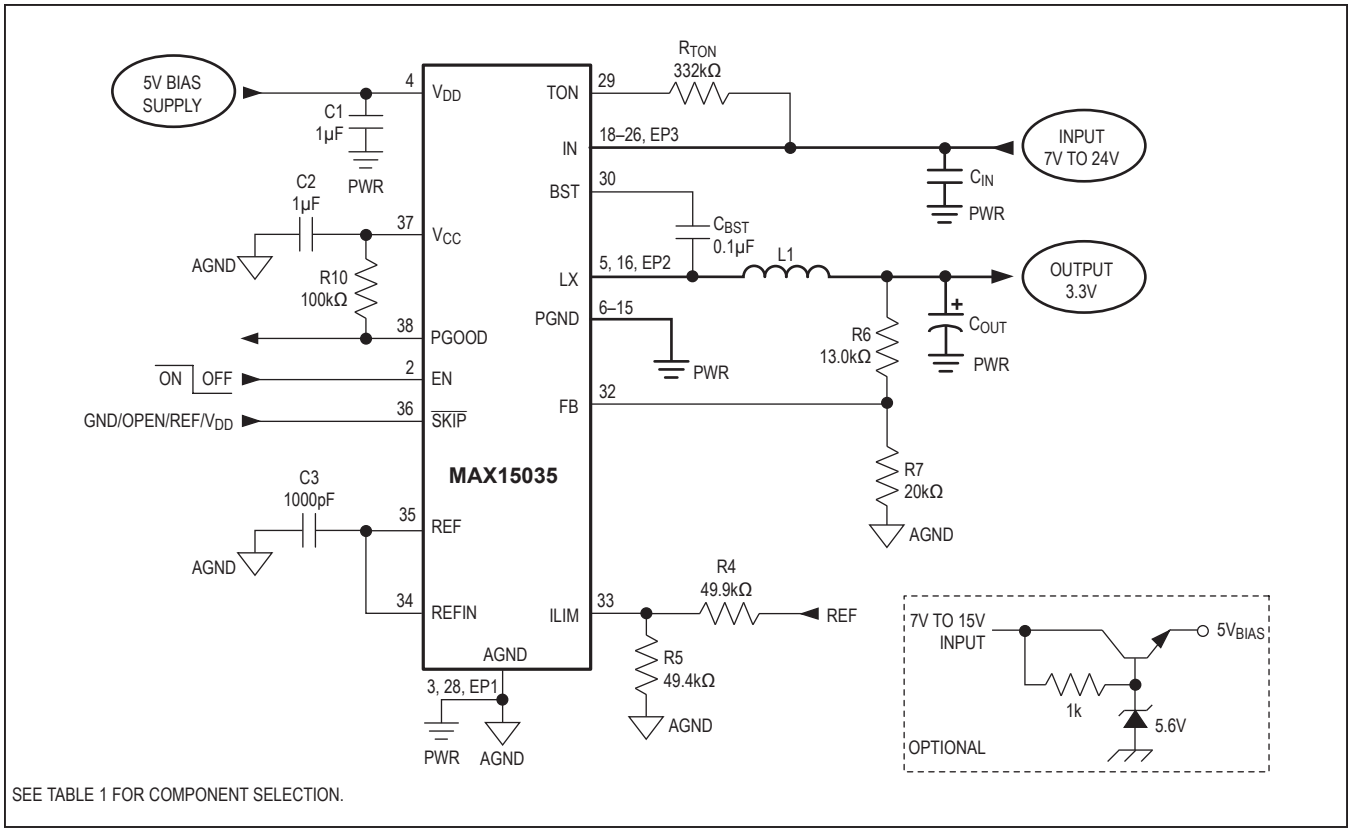


Figure 6. High Output-Voltage Application Using a Feedback Divider

Output Voltages Greater than 2V

Although REFIN is limited to a 0 to 2V range, the output-voltage range is unlimited since the MAX15035 utilizes a high-impedance feedback input (FB). By adding a resistive voltage-divider from the output to FB to analog ground (Figure 6), the MAX15035 supports output voltages above 2V. However, the controller also uses FB to determine the on-time, so the voltage-divider influences the actual switching frequency, as detailed in the *On-Time One-Shot* section.

Internal Integration

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This internal amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the compensated feedback ripple voltage and internal slope-compensation variation. The integrator amplifier has the ability to shift the output voltage by ±55mV (typ).

The MAX15035 disables the integrator by connecting the amplifier inputs together at the beginning of all downward REFIN transitions done in pulse-skipping mode. The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and over-voltage conditions. PGOOD is actively held low in shut-down (EN = GND), and during soft-start and soft-shutdown. Approximately 200µs (typ) after the soft-start terminates, PGOOD becomes high impedance as long as the feedback voltage is above the UVP threshold (REFIN - 200mV) and below the OVP threshold (REFIN + 300mV). PGOOD goes low if the feedback voltage drops 200mV below the target voltage (REFIN) or rises 300mV above the target voltage (REFIN), or the SMPS controller is shut down. For a logic-level PGOOD output voltage, connect an external

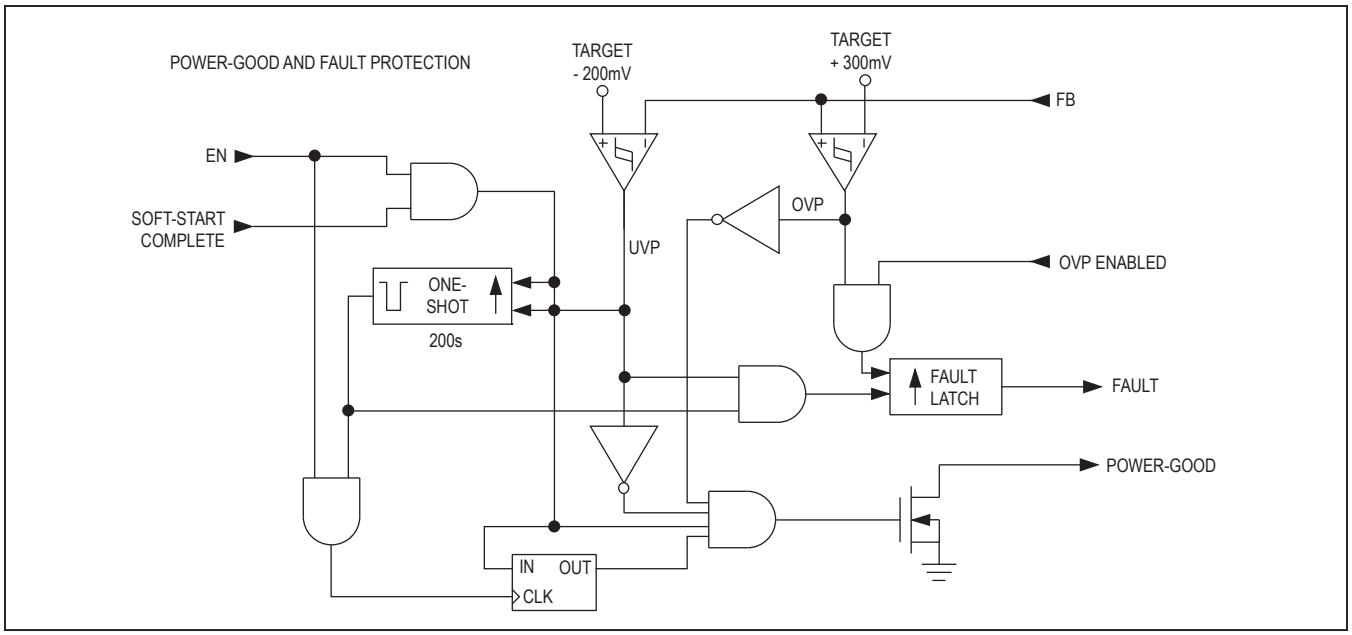


Figure 7. Power-Good and Fault Protection

pullup resistor between PGOOD and V_{DD}. A 100kΩ pullup resistor works well in most applications. Figure 7 shows the power-good and fault-protection circuitry.

Overvoltage Protection (OVP)

When the internal feedback voltage rises 300mV above the target voltage and OVP is enabled, the OVP comparator immediately forces LX low, pulls PGOOD low, sets the fault latch, and disables the SMPS controller. Toggle EN or cycle V_{CC} power below the V_{CC} POR to clear the fault latch and restart the controller.

Undervoltage Protection (UVP)

When the feedback voltage drops 200mV below the target voltage (REFIN), the controller immediately pulls PGOOD low and triggers a 200µs one-shot timer. If the feedback voltage remains below the undervoltage fault threshold for the entire 200µs, the undervoltage fault latch is set and the SMPS begins the shutdown sequence. When the internal target voltage drops below 0.1V, the MAX15035 forces a high impedance on LX. Toggle EN or cycle V_{CC} power below V_{CC} POR to clear the fault latch and restart the controller.

Thermal-Fault Protection (TSHDN)

The MAX15035 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, shuts down the controller, and forces a high impedance on LX. Toggle EN or cycle V_{CC} power below V_{CC} POR to reactivate the controller after the junction temperature cools by 15°C.

Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case input supply voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. The worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2\left[\left(\frac{V_{OUT} t_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})t_{SW}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the inductor ripple current (ΔI_L); therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - \frac{\Delta I_L}{2}$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by 0.006.

The valley current-limit threshold is precisely 1/20 the voltage seen at ILIM. Connect a resistive divider from REF to ILIM to analog ground (AGND) to set a fixed valley current-limit threshold. The external 400mV to 2V adjustment range corresponds to a 20mV to 100mV valley current-limit threshold. When adjusting the current-limit threshold, use 1% tolerance resistors and a divider current of approximately 5µA to 10µA to prevent significant inaccuracy in the valley current-limit tolerance.

The MAX15035 uses the low-side MOSFET's on-resistance as the current-sense element (R_{SENSE} = $R_{DS(ON)}$). A good general rule is to allow 0.5% additional resistance for each degree celsius of temperature rise, which must be included in the design margin unless the design includes an NTC thermistor in the ILIM resistive voltage-divider to thermally compensate the current-limit threshold.

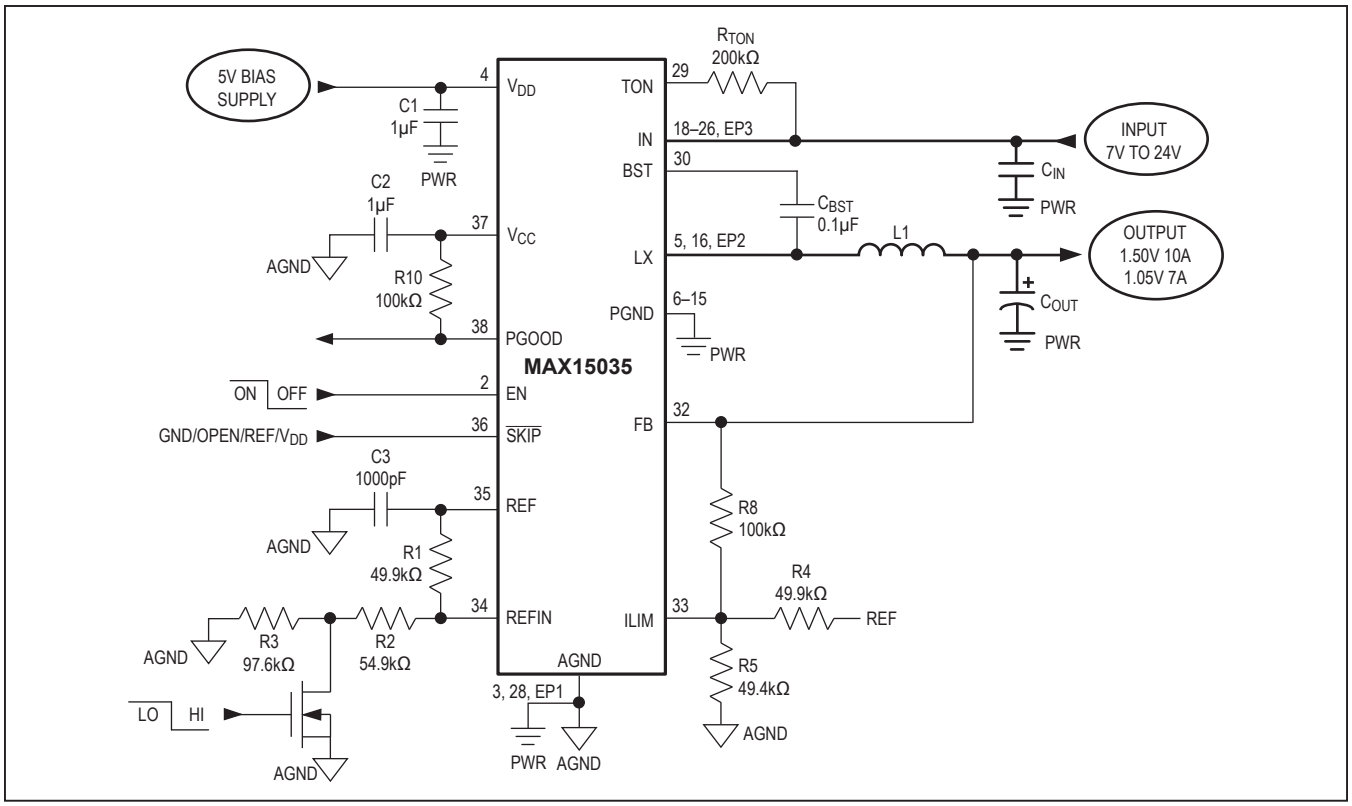


Figure 8. Standard Application with Foldback Current-Limit Protection

Foldback Current Limit

Including an additional resistor between ILIM and the output automatically creates a current-limit threshold that folds back as the output voltage drops (see Figure 8). The foldback current limit helps limit the inductor current under fault conditions, but must be carefully designed to provide reliable performance under normal conditions. The current-limit threshold must not be set too low, or the controller will not reliably power up. To ensure the controller powers up properly, the minimum current-limit threshold (when V_{OUT} = 0V) must always be greater than the maximum load during startup (which at least consists of leakage currents), plus the maximum current required to charge the output capacitors:

$$I_{START} = C_{OUT} \times 1mV/\mu s + I_{LOAD(START)}$$

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements. Additionally, the ESR impacts stability requirements. Capacitors with a high ESR value (polymers/tantalums) do not need additional external compensation components.

In core and chipset converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In low-power applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. The maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} \times f_{SW} \times L}{(V_{IN} - V_{OUT})V_{OUT}}\right] V_{RIPPLE}$$

where f_{SW} is the switching frequency.

With most chemistries (polymer, tantalum, aluminum electrolytic), the actual capacitance value required relates to the physical size needed to achieve low ESR and the chemistry limits of the selected capacitor technology. Ceramic capacitors provide low ESR, but the capacitance and voltage rating (after derating) are determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). Thus, the output capacitor selection requires carefully balancing capacitor chemistry limitations (capacitance vs. ESR vs. voltage rating) and cost. See Figure 9.

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the in-phase feedback ripple relative to the switching frequency, which is typically dominated by the output ESR. The boundary of instability is given by the following equation:

$$\frac{f_{SW}}{\pi} \geq \frac{1}{2\pi R_{EFF} C_{OUT}}$$

$$R_{EFF} = R_{ESR} + R_{PCB} + R_{COMP}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total ESR of the output capacitors, R_{PCB} is the parasitic board resistance between the output capacitors and feedback sense point, and R_{COMP} is the effective resistance of the DC- or AC-coupled current-sense compensation (see Figure 11).

For a standard 300kHz application, the effective zero frequency must be well below 95kHz, preferably below 50kHz. With these frequency requirements, standard tantalum and polymer capacitors already commonly used have typical ESR zero frequencies below 50kHz, allowing the stability requirements to be achieved without any additional current-sense compensation. In the standard application circuit (Figure 1), the ESR needed to support a $15mV_{P-P}$ ripple is 15mV/(10A x 0.3) = 5mΩ. Two 330µF, 9mΩ polymer capacitors in parallel provide 4.5mΩ (max) ESR and 1/(2π x 330µF x 9mΩ) = 53kHz ESR zero frequency. See Figure 10.

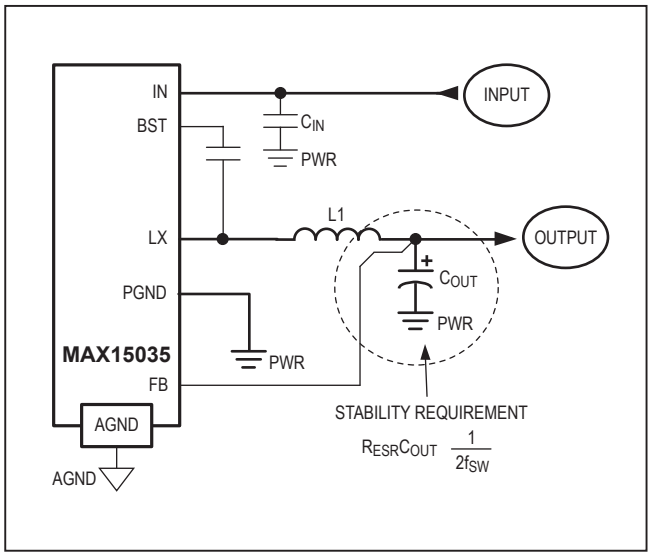


Figure 9. Standard Application with Output Polymer or Tantalum

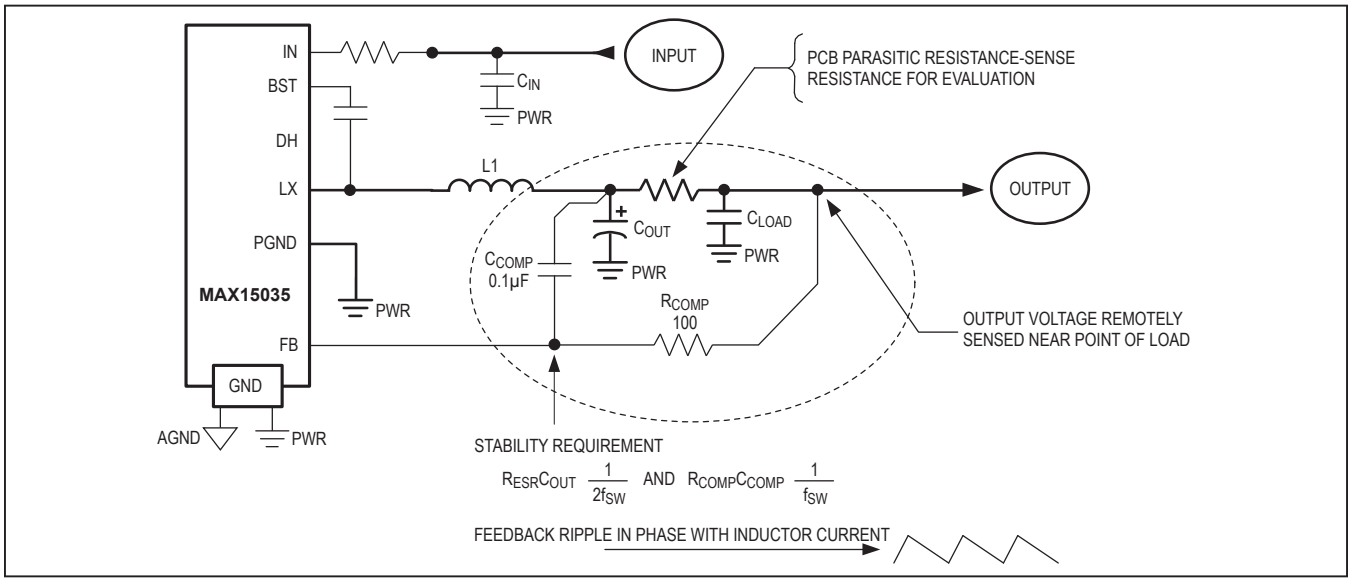
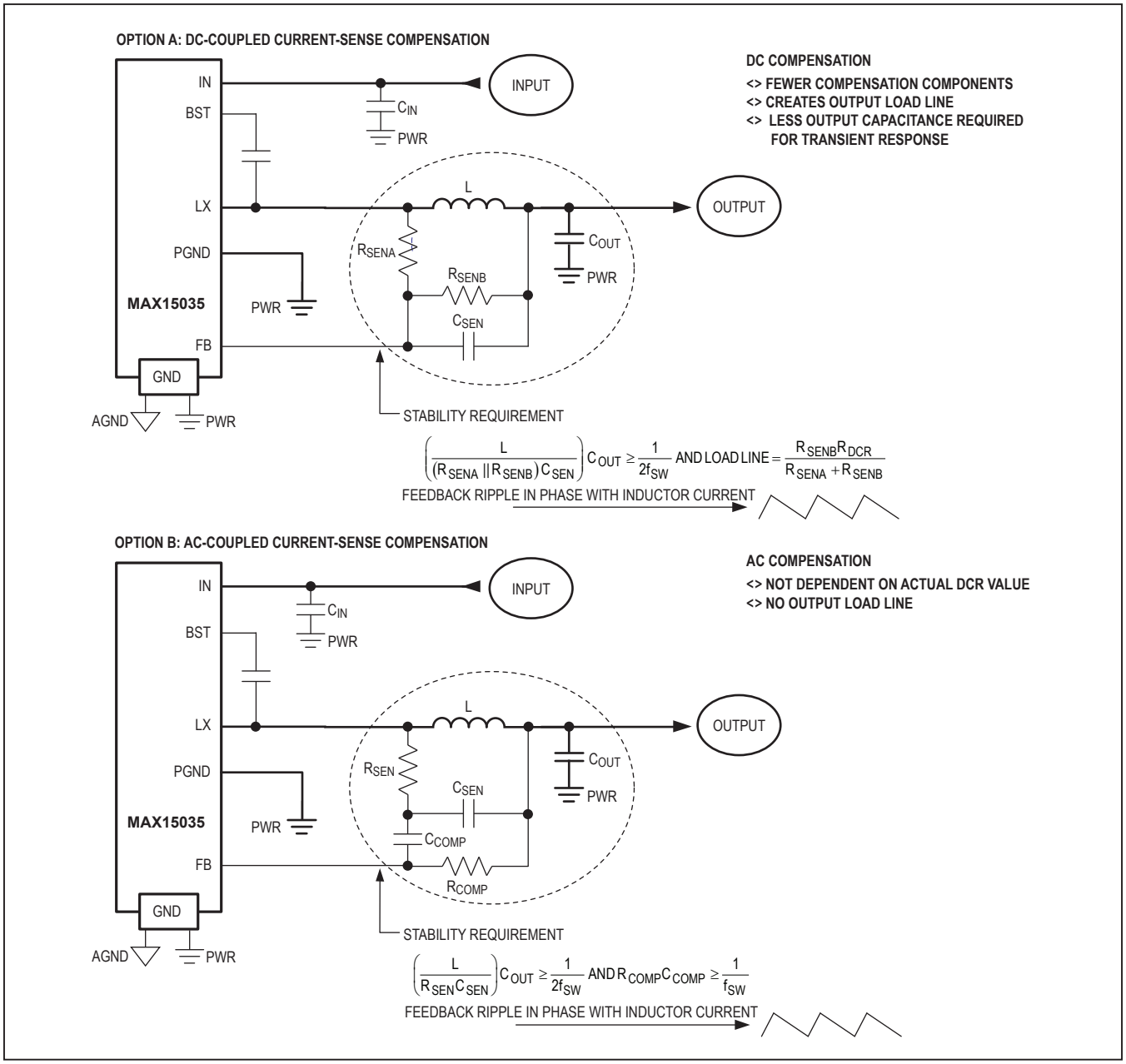


Figure 10. Remote-Sense Compensation for Stability and Noise Immunity

Ceramic capacitors have a high-ESR zero frequency, but applications with sufficient current-sense compensation may still take advantage of the small size, low ESR, and high reliability of the ceramic chemistry. Using the inductor DCR, applications using ceramic output capacitors may be compensated using either a DC compensation or AC compensation method (Figure 11).

The DC-coupling requires fewer external compensation capacitors, but this also creates an output load line that depends on the inductor's DCR (parasitic resistance). Alternatively, the current-sense information may be AC-coupled, allowing stability to be dependent only on the inductance value and compensation components and eliminating the DC load line.



$$\left(\frac{L}{(R_{SENA} \| R_{SENB}) C_{SEN}}\right) C_{OUT} \geq \frac{1}{2f_{SW}} \text{ AND LOAD LINE} = \frac{R_{SENB} R_{DCR}}{R_{SENA} + R_{SENB}}$$

$$\left(\frac{L}{R_{SEN} C_{SEN}}\right) C_{OUT} \geq \frac{1}{2f_{SW}} \text{ AND } R_{COMP} C_{COMP} \geq \frac{1}{f_{SW}}$$

Figure 11. Feedback Compensation for Ceramic Output Capacitors

When only using ceramic output capacitors, output over-shoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value may allow significant output over-shoot when stepping from full-load to no-load conditions, unless designed with a small inductance value and high switching frequency to minimize the energy transferred from the inductor to the capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback-loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage-ripple envelope for over-shoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements may be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{V_{IN}}\right)\sqrt{V_{OUT}(V_{IN} - V_{OUT})}$$

The worst-case RMS current requirement occurs when operating with $V_{IN} = 2V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Minimum Input-Voltage Requirements and Dropout Performance

The output voltage-adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low-input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the on-times. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Quick-PWM Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left(\frac{V_{OUT} - V_{DROOP} + V_{CHG}}{1 - \left(h \times t_{OFF(MIN)} f_{SW}\right)}\right)$$

where V_{DROOP} is the voltage-positioning droop, V_{CHG} is the parasitic voltage drop in the charge path, and $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout design example:

V_{OUT} = 3.3V

f_{SW} = 300kHz

$t_{OFF(MIN)}$ = 350ns

V_{DROOP} = 0V

V_{CHG} = 150mV (10A load)

h = 1.5

$$V_{IN(MIN)} = \left[\frac{3.3V - 0V + 150mV}{1 - (1.5 \times 350ns \times 300kHz)}\right] = 3.74V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \left[\frac{3.3V - 0V + 150mV}{1 - (1.0 \times 350ns \times 300kHz)}\right] = 3.52V$$

Therefore, V_{IN} must be greater than 3.52V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.74V.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the AGND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, REF bypass capacitors, REFIN components, and feedback compensation/dividers.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohms of excess trace resistance causes a measurable efficiency penalty.
4) Keep the power plane—especially LX—away from sensitive analog areas (REF, REFIN, FB, ILIM).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (C_{IN} and C_{OUT}). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; the controller's analog ground plane where sensitive analog components, the controller's AGND pin, and V_{CC} bypass capacitor go. The controller's AGND plane must meet the PGND plane only at a single point directly beneath the IC. This point must also be very close to the output capacitor ground terminal.
3) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15035ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

TRANSISTOR COUNT: 7169

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	7/08	Modified Figure 1, Tables 1 and 2.	12
2	10/08	Updated *Pin Description*, Figure 1, and *Detailed Description*.	11, 12, 13, 16, 18–21, 24
3	4/18	Updated *Package Information* table.	2

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