*Click **here** for production status of specific part numbers.*

MAX15158/MAX15158A High-Voltage Multiphase Boost Controller

General Description

MAX15158/MAX15158A is a high-voltage multiphase boost controller designed to support up to two MOSFET drivers and four external MOSFETs in single-phase or dual-phase boost/inverting-buck-boost configurations. Two devices can be stacked up for quad-phase operation. The output voltage of MAX15158 can be dynamically set through the 1V to 2.2V reference input (REFIN) for modular design support. For MAX15158A the REFIN pin is removed, and the internal 2.0V reference voltage is selected by default.

The switching frequency is controlled either through an external resistor setting the internal oscillator or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1MHz switching frequencies. The controller has a dedicated enable/input undervoltage-lockout (EN/UVLO) pin to configure for flexible power sequencing.

MAX15158/MAX15158A has a dedicated RAMP pin to adjust internal slope compensation. The device features adjustable overcurrent protection. The device incorporates current sense amplifiers to accurately measure the current of each phase across external sense resistors to implement accurate phase current sharing. The controller is also protected against output overvoltage, input undervoltage and thermal shutdown.

The device is available in 5mm x 5mm, 32-pin TQFN package and supports -40°C to 125°C junction temperature range.

Applications

- Communication
- Industrial
- Automotive
- Multiphase Boost

Benefits and Features

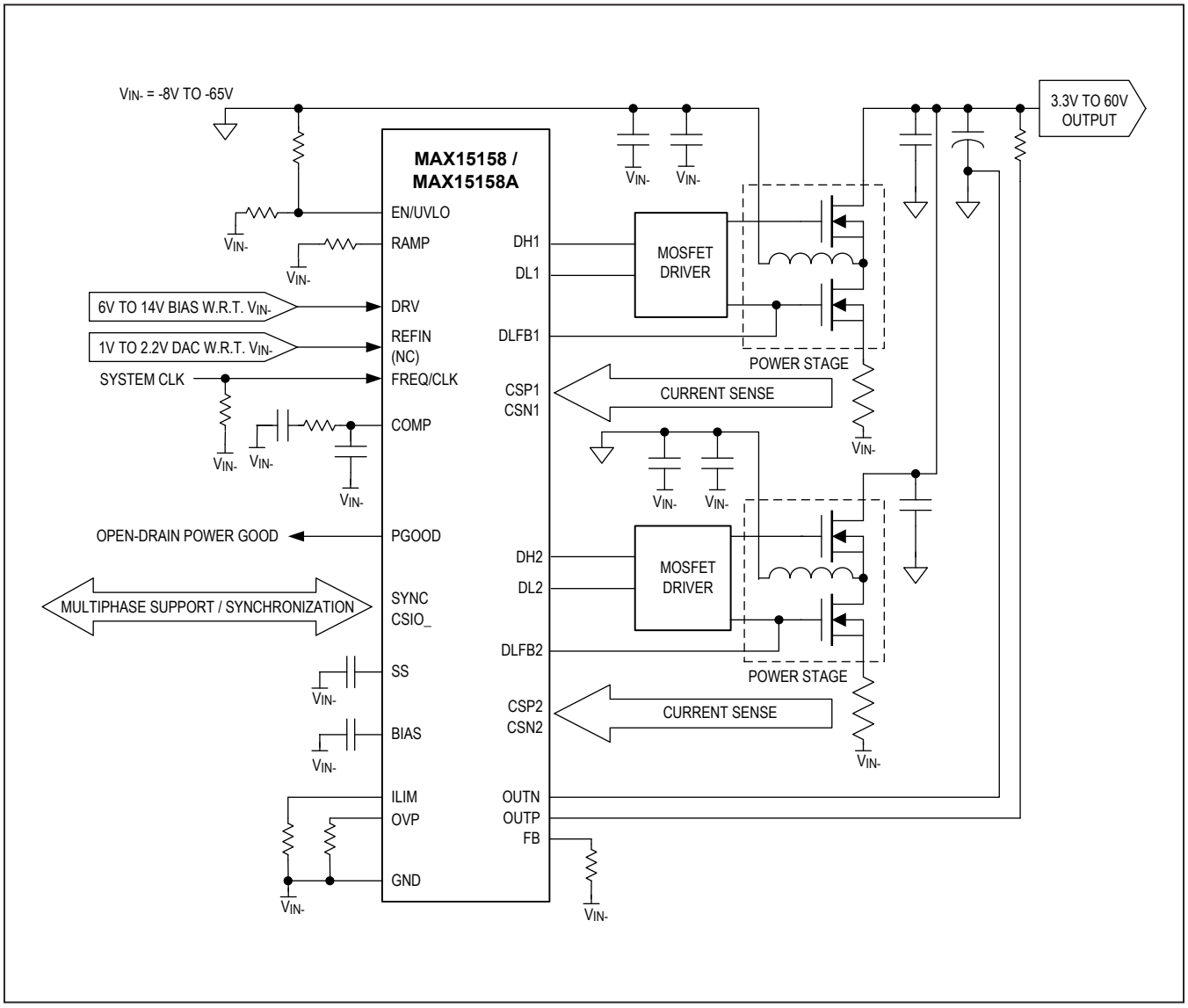
- Wide Operating Range
  - 8V to 76V Input Voltage Range for Booost Configuration and -8V to -76V Input Voltage Range for Inverting-Buck-Boost Configuration
  - 3.3V to 60V Output Voltage Range on the Top of Input Voltage
  - 120kHz to 1MHz Switching Frequency Range
  - -40°C to +125°C Temperature Range
  - Single/Dual/Quad-Phase Operation
  - Active Phase Current Balance Control
- Integration Reduces Design Footprint
  - Internal LDO for Bias Supply Generation
  - Multiphase Multiple Controller Synchronization and Interleave
  - Output Voltage Sense Level Shifter
- Robust Fault Protection Improves Quality and Reliability
  - Adjustable Input Undervoltage Lockout
  - Adjustable Cycle-by-Cycle Peak Current Limit and Fast Overcurrent Protection
  - Selectable Feedback Overvoltage Protection
  - Thermal Shutdown
- Flexible and Simple System Design
  - Adjustable Slope Compensation
  - Low-Side MOSFET Gate Monitoring for Accurate Current Sensing
  - Discontinuous-Conduction-Mode Operation is Supported when Using a Diode in Place of the High-Side MOSFET
- Small 5mm x 5mm TQFN package, 0.5mm pitch

***Ordering Information** appears at end of data sheet.*

19-100365; Rev 2; 11/19

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

OUTP, OUTN to GND.....-0.3V to +80V
CSP_, CSN_ to GND .....-0.3V to +0.3V
CSP_ to CSN_ .....-0.3V to +0.3V
DH_, DL_ to GND ..... -0.3V to (V_{BIAS} + 0.3V)
DLFB_ to GND ..... -0.3V to (V_{DRV}+ 0.3V)
DRV to GND.....-0.3V to +16V
BIAS to GND .....-0.3V to +6V
DRV to BIAS.....-0.3V to +16V
FB, PGOOD, REFIN to GND .....-0.3V to +6V
EN/UVLO, FREQ/CLK to GND .....-0.3V to +6V
COMP, SS, ILIM, OVP, RAMP,
SYNC to GND.....-0.3V to (V_{BIAS} + 0.3V)
CSION, CSIOP to GND.....-0.3V to (V_{BIAS} + 0.3V)
Maximum Current out of BIAS 100mA
Operating Temperature Range..... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C).....2.76W
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 32-PIN TQFN	
Package Code	T3255+6
Outline Number	**21-0140**
Land Pattern Number	**90-0603**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS (MAX15158), C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
DRV Operating Range	V_{DRV}		8.5		14	V
DRV Quiescent Current	I_{DRV}	Device Switching, 2 phases, 10pF load DH_ and DL_		10.0	15.4	mA
DRV Shutdown Current		EN = GND		10	19	µA
DRV Undervoltage-Lockout Threshold	$V_{DRV(UVLO)}$	V_{DRV} rising	8.00	8.27	8.41	V
		V_{DRV} falling	7.90	8.16	8.31	
BIAS LINEAR REGULATOR						
BIAS LDO Output Voltage	V_{BIAS}	I_{BIAS} = 5mA	4.66	4.75	4.81	V
BIAS LDO Current Limit			30	56	90	mA
BIAS Undervoltage-Lockout Threshold	$V_{BIAS(UVLO)}$	V_{BIAS} rising	4.10	4.24	4.40	V
		V_{BIAS} falling	4.00	4.19	4.32	
CONTROLLER ENABLE						
EN/UVLO Adjustable Undervoltage-Lockout Threshold	V_{UVLO}	V_{UVLO} rising	0.98	1.00	1.03	V
		V_{UVLO} falling	0.88	0.90	0.93	
EN/UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to V_{BIAS}	-1		+1	µA
FEEDBACK VOLTAGE LEVEL SHIFTER (OUTP, OUTN)						
OUTP Current Range	I_{OUTP}	OUTP = OUTN > 8V	0.05		3.000	mA
OUTN Bias Current	I_{OUTN}	OUTP = OUTN > 8V		220	375	µA
OUTP Leakage Current		OUTN = OUTP = BIAS		4	10	µA
OUTN Leakage Current		OUTN = OUTP = BIAS		3	10	µA
OUTN Undervoltage-Lockout Threshold	OUTN UVLO	Minimum OUTN voltage for HV FB operations	7.0	7.2	7.4	V
		OUTN UVLO hysteresis	6.8	7.0	7.2	
HV FB Voltage-Buffer Operating Range	V_{OUTP}, V_{OUTN}		8		76	V
CONTROL LOOP						
FB Regulation Threshold (Preset Mode)	V_{FB}	REFIN = BIAS (MAX15158)	1.97	2.00	2.02	V
FB-to-REFIN Offset Voltage (Tracking Mode)		V_{FB} – V_{REFIN} , V_{REFIN} = 1V to 2V	-9		+9	mV
REFIN Input Voltage Range	V_{REFIN}	(Note 2)	1		2.2	V

Electrical Characteristics (continued)

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS (MAX15158), C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Preset Mode REFIN Threshold Rising		100mV hysteresis (typ)	2.30	2.36		V
FB Input Leakage Current	I_{FB}	V_{FB} = 0V to 2V; OUTP = OUTN = BIAS	-1		+1	µA
REFIN Input Leakage Current	I_{REFIN}	V_{REFIN} = 0.4V to 2.2V	-1		+1	µA
CSP_-to-CSN_ Differential Voltage Range	$D_{VCS_}$	$V_{CSP_}$ - $V_{CSN_}$	-200		+200	mV
Current-Sense Common-Mode Voltage Range	$V_{CSP_}$, $V_{CSN_}$	With respect to GND (Note 3)	-300		+300	mV
CSP_, CSN_ Current-Sense Amplifier Gain	$A_{CS_}$			8.3		V/V
CSP_ , CSN_ Input Leakage Current	$I_{CSP_}$, $I_{CSN_}$	$V_{CSP_}$, $V_{CSN_}$ = ±200 mV with respect to AGND	-1		+1	µA
Error-Amplifier Transconductance	G_{MEA}			1.1		mS
Ramp Pin Amplitude Adjustable Range	V_{RAMP}		120		375	mV
Internal Slope Compensation Ramp Voltage to V_{RAMP} Ratio		V_{RAMP} = 0.3V		1.9		V/V
RAMP Bias Current	I_{RAMP}	V_{RAMP} = 0V	9.4	10.0	10.6	µA
SWITCHING FREQUENCY						
Preset PWM Switching Frequency	f_{SW}	$R_{FREQ/CLK}$ = OPEN	293	300	305	kHz
Adjustable PWM Switching Frequency	f_{SW}	R_{FREQ} = 20kΩ	105	115	125	kHz
		R_{FREQ} = 25kΩ	135	150	165	
		R_{FREQ} = 100kΩ (R_{FREQ} < 120 kΩ)	550	600	650	
PWM Switching frequency range	f_{SW}	FREQ/CLK externally applied	120		1000	kHz
FREQ/CLK Frequency Detection Range	f_{CLK}		0.48		4.00	MHz
FREQ/CLK Logic Level	V_{CLK}	Logic-high (rising)		1.80	1.85	V
		Logic-low (falling)	1.5	1.6		
FREQ/CLK Input Bias Current	I_{CLK}	$V_{FREQ/CLK}$ = GND	-10.7	-10.0	-9.3	µA
FREQ/CLK to PWM Switching Frequency Ratio	f_{CLK} / f_{SW}	1/2/4 Phases Operation		4		kHz/kHz

Electrical Characteristics (continued)

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS (MAX15158), C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
QUAD-PHASE CLOCK SYNC						
SYNC Logic Threshold	V_{SYNC}	Logic high (rising)		1.58	1.95	V
		Logic low (falling)	0.90	1.17		
SYNC Input Leakage Current	I_{SYNC}	V_{SYNC} = 0V to 4.6V, internal 5MΩ pulldown	-2		+2	µA
SYNC Frequency Range	f_{SYNC}		200		2000	kHz
SYNC Output Voltage Level	V_{SYNC}	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} - 0.4			V
		Logic-low, I_{SINK} = 10mA			0.4	
OUTPUT FAULT PROTECTION						
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} = 0V	17	20	23	mV
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} > 1.25V	94	100	106	mV
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Negative Overcurrent Protection		V_{ILIM} > 1.25V		-80		mV
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Negative Overcurrent Protection		V_{ILIM} = 0V		-16		mV
CSP_ to CSN_ Minimum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} = 0V	21	26	31	mV
CSP_ to CSN_ Maximum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} > 1.25V	121	133	145	mV
ILIM Source Current			9.4	10.0	10.6	µA
CSP_-to-CSN_ Cycle-by-Cycle Positive Peak Current Limit Threshold Accuracy		0.25V < V_{ILIM} < 0.95V	-15		+ 15	%
		V_{ILIM} = 500mV	-6		+6	%
CSP_-to-CSN_ Negative Overcurrent Protection Threshold Accuracy		V_{ILIM} = 500mV	-20		+20	%

Electrical Characteristics (continued)

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS (MAX15158), C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ILIM} to |CSP_ - CSN_| Cycle-by-Cycle Positive Peak Current Limit Threshold Ratio		V_{ILIM} = 500mV		10		V/V
Minimum REFIN and SS Voltage for Valid FB OV Fault		SS > 1V	1.00	1.02	1.04	V
FB Overvoltage Default Threshold (Preset Mode)	FB OV	Measured with respect to target voltage (REFIN = BIAS for MAX15158), V_{FB} falling, 3% hysteresis	8.5	10.0	12.0	%
FB Overvoltage Threshold (Tracking Mode)	FB OV	Measured with respect to target voltage (V_{REFIN} = 1V for MAX15158), V_{FB} falling, 3% hysteresis	8.5	10	11	%
OVP Selector Output Source Current		Resistor connected to GND	9.4	10.0	10.6	µA
Fault Propagation Delay		EN/UVLO falling to SS falling		12		µs
		Cumulative cycle-by-cycle peak current limit or negative overcurrent protection events for hiccup		32		Events
		FB OV		128		PWM CLK Cycles
Hiccup Timeout Duration				32,768		PWM CLK Cycles
PGOOD Threshold		PGOOD rising (REFIN = BIAS for MAX15158)	1.83	1.88	1.93	V
		PGOOD falling (REFIN = BIAS for MAX15158)	1.77	1.82	1.87	
PGOOD Falling and Rising Delay				64		PWM CLK Cycles
PGOOD Output Low Voltage	V_{PGOOD}	I_{SINK} = 3mA		20	40	mV
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN for MAX15158, V_{PGOOD} = 5V			1	µA
Thermal Shutdown	T_{SHDN}	15°C hysteresis		165		°C

Electrical Characteristics (continued)

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS (MAX15158), C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

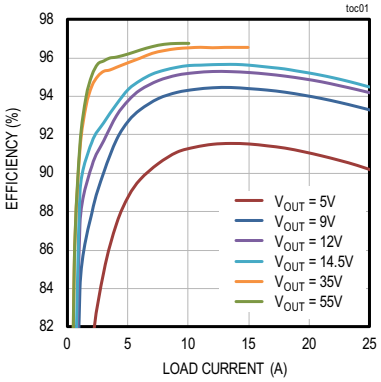
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START (SS)						
SS Amplifier Transconductance	$G_{M(SS)}$			0.2		mS
SS Current Capability	I_{SS}	Source	4.75	5.00	5.25	µA
		Sink	-5.8	-5.0	-4.2	
SS Pulldown Resistance	R_{SS}	Discharge		4.3		Ω
SS Undervoltage-Lockout Threshold	$V_{UVLO(SS)}$	SS rising		55		mV
		SS falling (drivers disabled)		45		
PWM Output						
DH_, DL_ Output Voltage Level	$V_{DH_}$, $V_{DL_}$	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} - 0.5			V
		Logic-low, I_{SINK} = 10mA			0.2	
DLFB_ Leakage Current	I_{LK}	$V_{DLFB_}$ = 9V	-1		+1	µA
DLFB_ Logic Threshold	V_{DLFB}	Logic high (rising)	0.75	0.80	0.85	V
		Logic low (falling)	0.45	0.50	0.55	
CURRENT SHARING (MULTIPHASE APPLICATIONS ONLY)						
CSIO_ Output Common-Mode Voltage	V_{CSION}	With respect to AGND		1.24		V
CSIO_ Differential Input Resistance	$R_{CSIO_}$			4.2		kΩ

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.
Note 2: For MAX15158, operating REFIN below 1V is not recommended due to disabled FB overvoltage-fault protection.
Note 3: Guaranteed by design, not production tested.

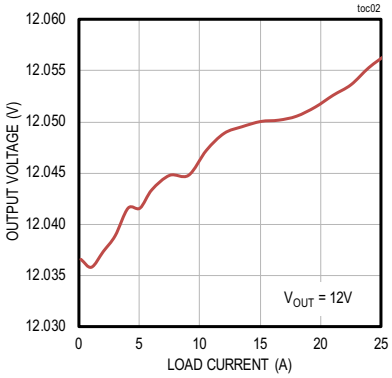
Typical Operating Characteristics

(T_A = -40°C to +125°C, V_{IN-} = -48V, unless otherwise noted. See the *Standard Application Circuits*.)

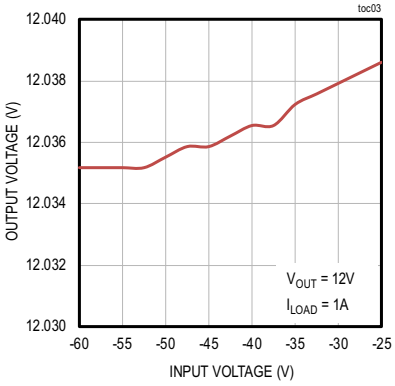
EFFICIENCY vs. LOAD CURRENT



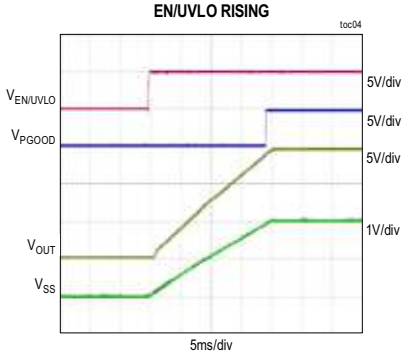
LOAD REGULATION



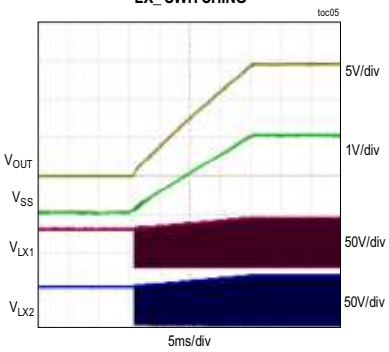
LINE REGULATION



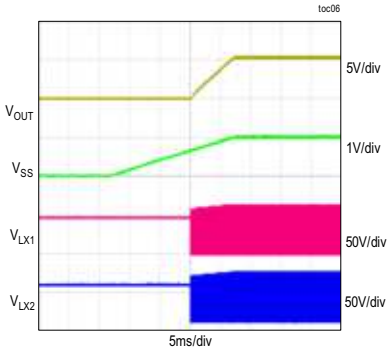
STARTUP WAVEFORM EN/UVLO RISING



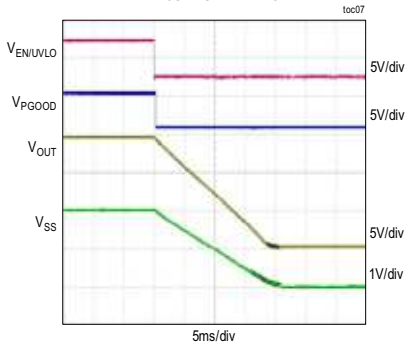
STARTUP WAVEFORM LX_ SWITCHING



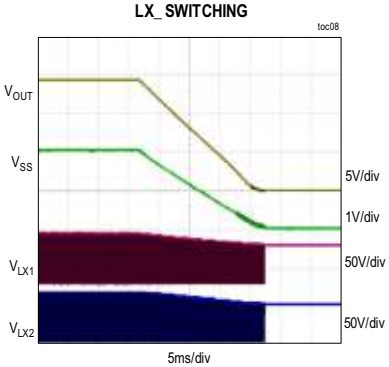
STARTUP WAVEFORM WITH PREBIASED OUTPUT VOLTAGE



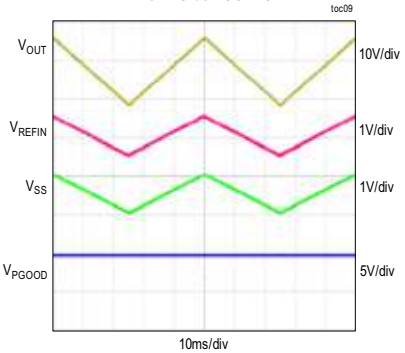
SHUT-DOWN WAVEFORM EN/UVLO FALLING



SHUT-DOWN WAVEFORM LX_ SWITCHING



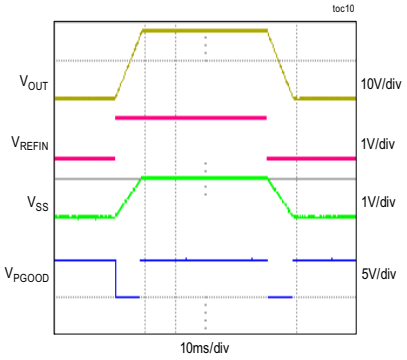
DYNAMIC REFIN RAMP RESPONSE 17.5V TO 35V OUTPUT



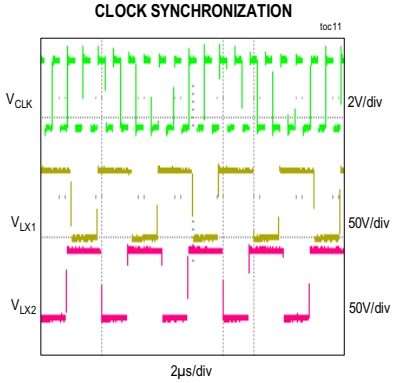
Typical Operating Characteristics (continued)

(T_A = -40°C to +125°C, V_{IN-} = -48V, unless otherwise noted. See the *Standard Application Circuits*.)

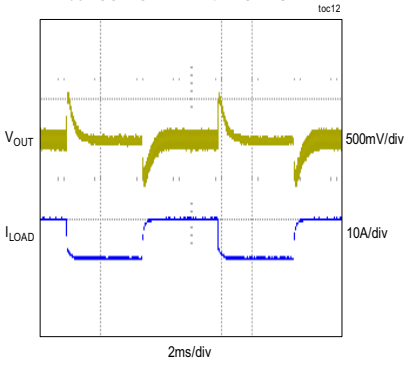
DYNAMIC REFIN STEP RESPONSE
17.5V TO 35V OUTPUT



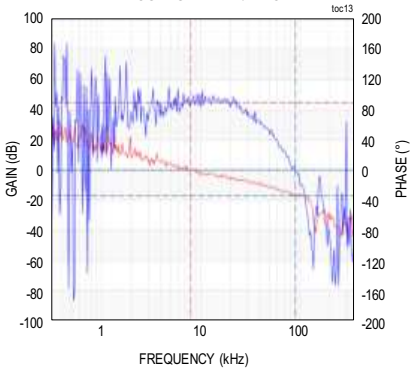
CLOCK SYNCHRONIZATION



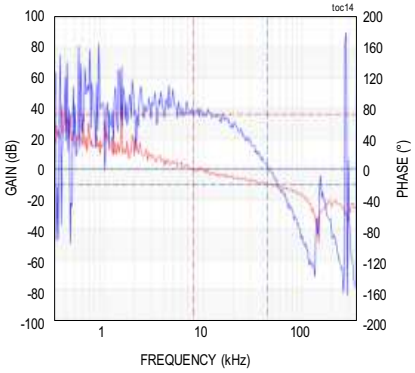
LOAD TRANSIENT WAVEFORM
35V OUTPUT WITH 10A LOAD STEP



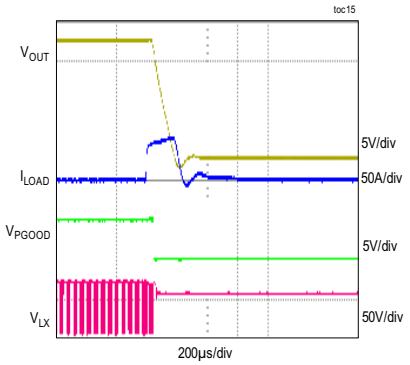
BODE PLOT
12V OUTPUT WITH 0A LOAD



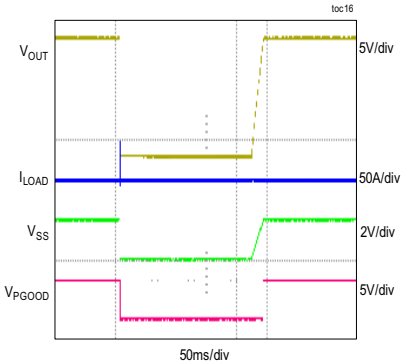
BODE PLOT
12V OUTPUT WITH 25A LOAD



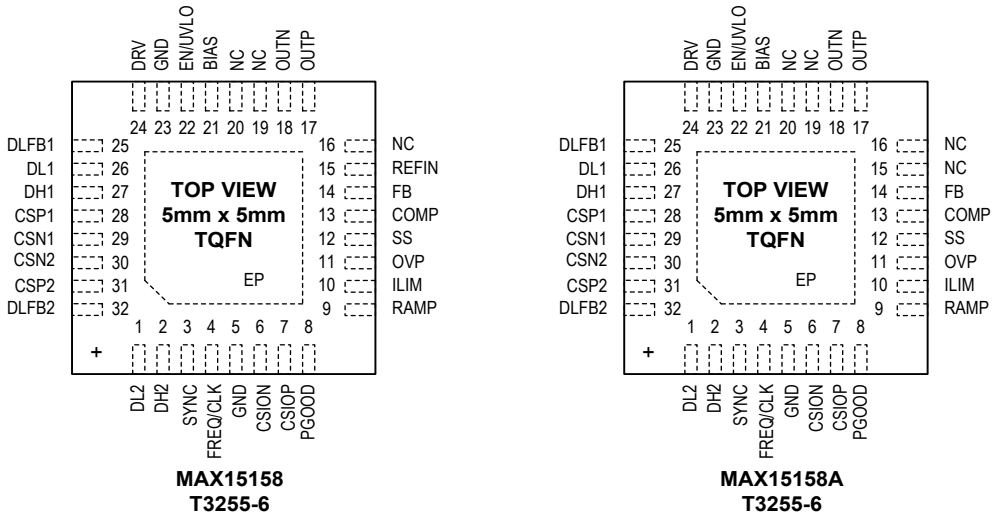
OUTPUT OVERCURRENT WAVEFORM



AUTO-RETRY AFTER
OVERCURRENT FAULT



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	DL2	Logic Output for Low-Side MOSFET Gate Driver for the Second Phase. Connect DL2 to the second phase external MOSFET driver low-side input pin.
2	DH2	Logic Output for High-Side MOSFET Gate Driver for the Second Phase. Connect DH2 to the second phase external MOSFET driver high-side input pin.
3	SYNC	Multiphase Synchronization Pin. For single IC operation, leave this pin unconnected. Tie this pin together when two MAX15158/MAX15158A ICs are stacked-up in master/slave operation mode.
4	FREQ/ CLK	Frequency Selection/Clock Synchronization Input. MAX15158/MAX15158A supports switching frequencies from 120kHz to 1MHz. Set the switching frequency by either selecting the appropriate external resistor to use the internal oscillator frequency, or by synchronizing the regulator to an external system clock (see Table 2). Leave the FREQ/CLK pin unconnected to select the preset 300kHz switching frequency or place a resistor between FREQ/CLK and GND to set the following: f_{SW} = (R_{FREQ}/100k) x 600kHz
5	GND	Analog Ground.
6	CSION	Negative Input of Master/Slave Current-Sense Signal. MAX15158/MAX15158A uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15158/ MAX15158A ICs are stacked up in master/slave operation mode.
7	CSIOP	Positive Input of Master/Slave Current-Sense Signal. MAX15158/MAX15158A uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15158/ MAX15158A ICs are stacked up in master/slave operation mode.
8	PGOOD	Open-Drain Power Good Output. MAX15158/MAX15158A pulls PGOOD low when the output voltage exceeds the OVP threshold, or drops below the output UVP threshold, during soft-start and shutdown (EN/UVLO pulled low). The PGOOD output goes high-impedance when the controller completes soft-start and remains in regulation.

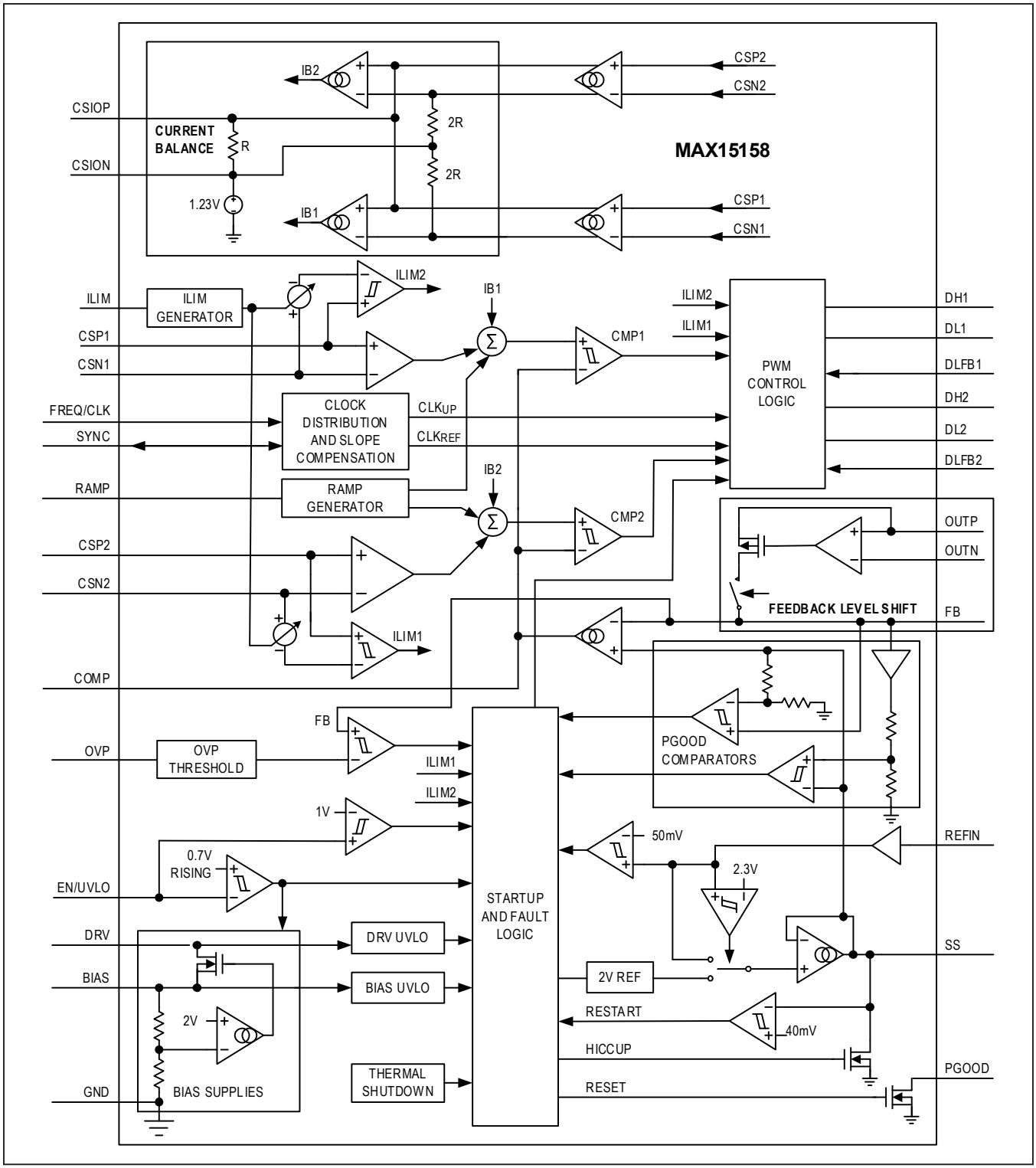
Pin Description (continued)

PIN	NAME	FUNCTION
9	RAMP	Slope Compensation Input. A resistor connected from RAMP to GND programs the amount of slope compensation. See the *Adjustable Slope Compensation (RAMP)* section.
10	ILIM	CSP_-CSN_ Cycle-by-Cycle/Hiccup Current Limit Threshold Selector. Connect a resistor from ILIM to GND to select the protection value.
11	OVP	Program Pin. Connect a resistor from OVP to GND to configure FB overvoltage protection, single-phase or dual-phase selection and FB level shifter selection (see Table 1).
12	SS	Soft-Start Control. The capacitance (C_{SS}) between SS to GND sets the startup period. An internal pulldown MOSFET holds SS low until the controller begins the startup sequence.
13	COMP	Compensation Amplifier Output. COMP is the output of the internal transconductance error amplifier. Connect a type II compensation network as shown in the Typical Application Circuit (See the *Compensation Design Guidelines* section).
14	FB	Feedback Input. When the FB level shifter is enabled, connect a resistor from FB to GND; when the FB level shifter is disabled, connect FB to the center of a resistive divider between the output and GND. For MAX15158A, FB regulates to the preset 2.0V reference voltage. For MAX15158, FB tracks the REFIN voltage (REFIN between 0.4V and 2.2V) or regulates to the preset 2.0V reference voltage by connecting REFIN to BIAS. Operation between 0.4V < REFIN < 1V is possible but the FB OVP is disabled. When two MAX15158/MAX15158A ICs are stacked-up in master/slave operation mode, connect FB of the slave to BIAS.
15	REFIN	External Reference Input of MAX15158. REFIN sets the feedback regulation voltage when supplied with a voltage between 0.4V and 2.2V. Connect REFIN pin to BIAS to select internal 2.0V reference voltage. Operation between 0.4V < REFIN < 1V is possible but the FB OV and UV fault functions are disabled.
	NC	Not Connected. For MAX15158A, this pin is NC (Not Connected), where the controller selects internal 2.0V reference voltage.
16, 19–20	NC	Not Connected
17	OUTP	Positive Differential Output Voltage Sense Input. MAX15158/MAX15158A can operate in inverting buck-boost mode and sense output voltage differentially using its internal FB level shifter. Connect a sense resistor between OUTP and positive node of output as shown in the *Typical Application Circuit*. OUTP must be shorted to OUTN and BIAS if the internal FB level shifter is disabled.
18	OUTN	Negative Differential Output Voltage Sense Input. MAX15158/MAX15158A can operate in inverting buck-boost mode and sense output voltage differentially using its internal FB level shifter. Connect OUTN to the negative node of output as shown in the *Typical Application Circuit*. Connect OUTN to OUTP and BIAS if the internal FB level shifter is disabled.
21	BIAS	4.75V Linear Regulator Output and Controller Bias Supply. Bypass to GND with a 2.2µF or greater ceramic capacitor.
22	EN/UVLO	Enable Control / Adjustable Undervoltage Lockout Input for Startup/Shutdown Power Sequencing. This pin has two voltage thresholds with hysteresis. The lower threshold (0.7V rising / 0.55V falling) determines whether the BIAS regulator is enabled/disabled. The higher threshold (1V rising / 0.9V falling) initiates soft-start / soft-shutdown and enables switching. Connect EN/UVLO to the center of a resistor divider between the input and GND to adjust the undervoltage lockout voltage level as shown in the *Typical Application Circuit*.
23	GND	Analog Ground.
24	DRV	Supply Voltage Input. Provide a 8.5V to 14V supply for internal bias generation.

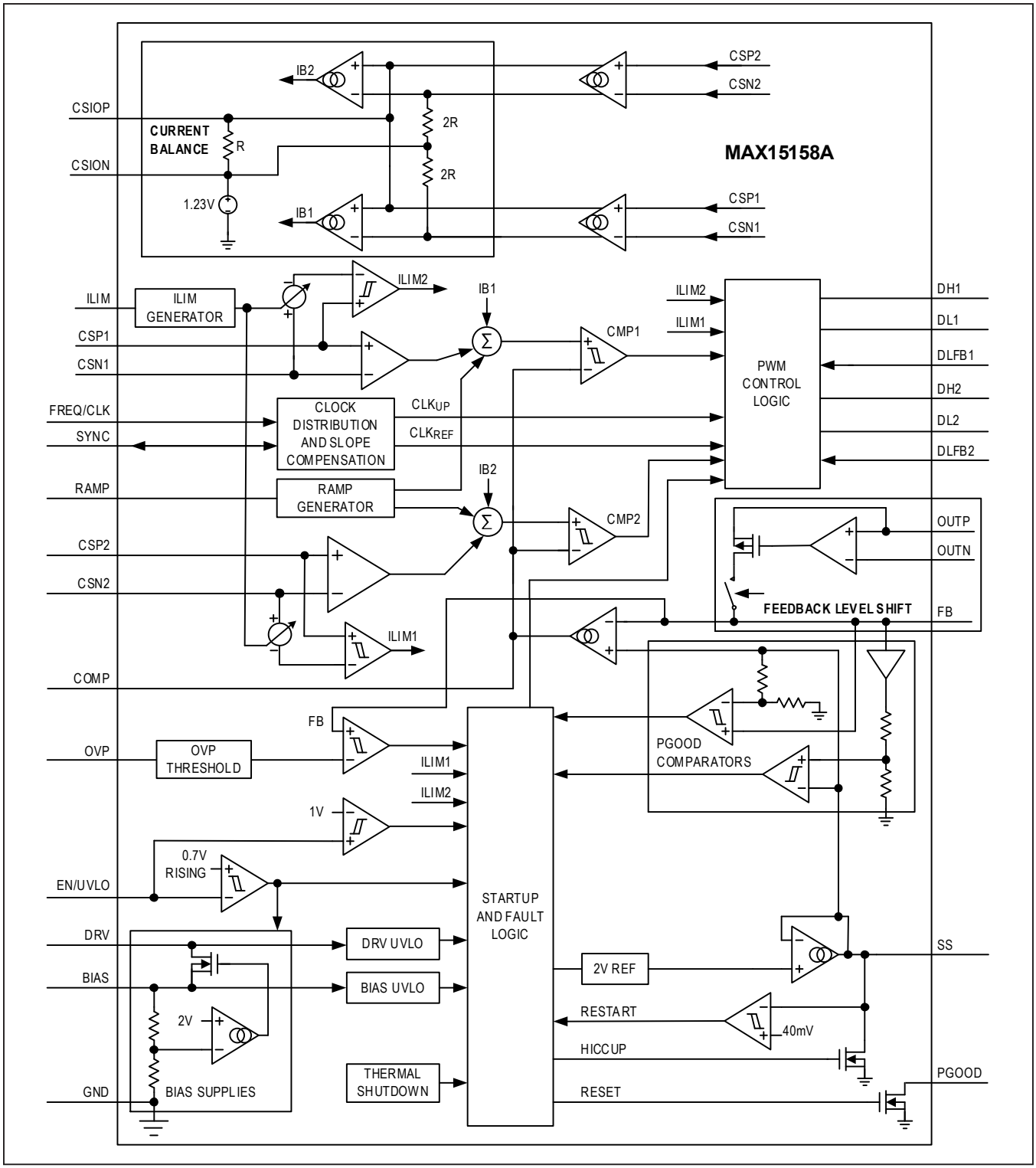
Pin Description (continued)

PIN	NAME	FUNCTION
25	DLFB1	External MOSFET Status Feedback Pin for the First Phase. Connect DLFB1 to the center of a resistor divider between the gate of the low-side MOSFET of the first phase and GND. See the *MOSFET Gate Control* section.
26	DL1	Logic Output for Low-Side MOSFET Gate Driver for the First Phase. Connect DL1 to the first phase external MOSFET driver low-side input pin.
27	DH1	Logic Output for High-Side MOSFET Gate Driver for the First Phase. Connect DH1 to the first phase external MOSFET driver high-side input pin.
28	CSP1	Positive Low-Side Differential Current-Sense Input for the First Phase. MAX15158/MAX15158A uses the differential current-sense signal in the current-mode control loop, and multiphase current sharing. Connect CSP1 to the "MOSFET side" of the current-sense resistor.
29	CSN1	Negative Low-Side Differential Current-Sense Input for the First Phase. MAX15158/MAX15158A uses the differential current-sense signal in the current-mode control loop, and multiphase current sharing. Connect CSN1 to the "ground side" of the current-sense resistor.
30	CSN2	Negative Low-Side Differential Current-Sense Input for the Second Phase. MAX15158/MAX15158A uses the differential current-sense signal in the current-mode control loop, and multiphase current sharing. Connect CSN2 to the "ground side" of the current-sense resistor.
31	CSP2	Positive Low-Side Differential Current-Sense Input for the Second Phase. MAX15158/MAX15158A uses the differential current-sense signal in the current-mode control loop, and multiphase current sharing. Connect CSP2 to the "MOSFET side" of the current-sense resistor.
32	DLFB2	External MOSFET Status Feedback Pin for the Second Phase. Connect DLFB2 to the center of a resistor divider between the gate of the low-side MOSFET of the second phase and GND. See the *MOSFET Gate Control* section.

Block Diagram



Block Diagram (continued)



Detailed Description

MAX15158/MAX15158A is a high-voltage multiphase boost controller designed to support up to two MOSFET drivers and four external MOSFETs in single-phase or dual-phase boost/inverting-buck-boost configurations. Two devices can be stacked up for quad-phase operation. When configured as inverting-buck-boost converter, the controller has an internal high-voltage FB level shifter to differentially sense the output voltage. The output voltage of MAX15158 can be dynamically set through the 1V to 2.2V reference input (REFIN) for modular design support. For MAX15158A the REFIN pin is removed, and the internal 2.0V reference voltage is selected by default.

The switching frequency is controlled either through an external resistor setting the internal oscillator or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1MHz switching frequencies. When two devices are stacked up as master-slave for quad-phase operation, the SYNC pin of two devices are connected to ensure the clock synchronization and phase interleaving. The controller has a dedicated enable/input undervoltage-lockout (EN/UVLO) pin to configure for flexible power sequencing.

MAX15158/MAX15158A has a dedicated RAMP pin to adjust internal slope compensation. The device features adjustable overcurrent protection. The device incorporates current sense amplifiers to accurately measure the current of each phase across external sense resistors to implement accurate phase current sharing. The controller is also protected against output overvoltage, input undervoltage and thermal shutdown.

High Voltage Internal FB Level Shifter

MAX15158/MAX15158A can support both boost and inverting-buck-boost applications. When configured in inverting-buck-boost operation, the GND pin of the device must be connected to the negative input voltage terminal (V_{IN-}), so that the ground of the IC is different than the ground of output capacitor and load. Output voltage cannot be controlled using a simple resistor divider. MAX15158/MAX15158A has a dedicated internal FB level shifter to differentially sense the output voltage. The internal FB level shifter can be enabled or disabled by connecting a resistor from the OVP pin to GND (See *Overvoltage Protection (OVP)* section). When the internal FB level shifter is enabled, connect OUTN to the ground node of the output capacitor and OUTP to the output terminal using a resistor R_{FB1}. FB is connected to GND (V_{IN-}) using a resistor R_{FB2}. The output voltage is set by these two resistors:

$$V_{OUT} = (R_{FB1}/R_{FB2}) \times V_{REF}$$

For MAX15158, V_{REF} can be externally supplied with a voltage between 1V and 2.2V on the REFIN pin. By connecting the REFIN pin to BIAS, the default internal 2.0V reference voltage is selected. For MAX15158A, V_{REF} = 2.0V and cannot be externally controlled. When the FB level shifter is enabled, the OUTN pin has a UVLO threshold that controls the power sequencing. If the voltage on OUTN falls below 7.0V (typ), the controller disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor through a 4.3Ω pulldown MOSFET.

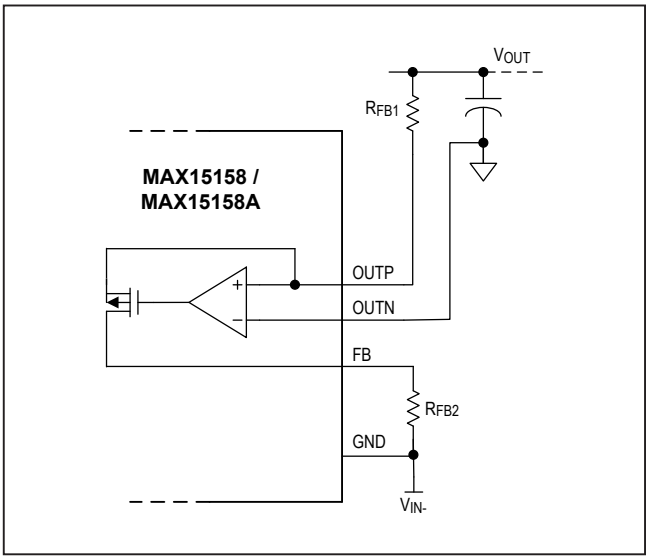


Figure 1. Using Internal FB Level Shifter

For inverting-buck-boost applications where V_{IN} is higher than 76V, MAX15158/MAX15158A can still be used but an external level shifter is required. The internal FB level shifter must be disabled. Pin OUTP and OUTN must be tied to BIAS. An example of using external FB level shifter is shown in Figure 2. Two matched PNP transistors are used. The output voltage is given by:

$$V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times V_{REF}$$

When operating in boost mode, the internal FB level shifter is disabled. Pin OUTP and OUTN must be tied to BIAS, and the FB pin must be connected to the center of a resistor divider from output to GND as shown in Figure 3. When the resistor divider is used, the output voltage is given by:

$$V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times V_{REF}$$

Peak-Current-Mode Control Loop

The controller relies on a fixed-frequency, peak-current-mode architecture to regulate the output. A detailed block diagram of the control loop is shown in Figure 4. A sense resistor is required between the source of the low-side MOSFET and GND for current sensing. The sense resistor should be selected so that the maximum differential voltage across CSP_ and CSN_ does not exceed the cycle-by-cycle peak current limit threshold (see the *Overcurrent Protection (OCP)* section). The differential voltage across CSP_ and CSN_ is amplified 8 times by a current sense amplifier. A high-frequency RC noise filter is suggested across the sense resistor. The RC time constant should not exceed 30ns.

The error between the output voltage feedback (V_{FB}) and reference voltage (V_{SS}) is fed to the input of an error amplifier. The output of the error amplifier (COMP) is required to connect to a type-II compensation network for control loop stability (see the *Compensation Design Guidelines* section). A slope compensation ramp generator is also used. The slope of the compensation ramp can be adjusted by connecting a resistor between RAMP and GND (see the *Adjustable Slope Compensation (RAMP)* section).

The controller drives on the low-side MOSFET (DL_ driven high) on each rising clock edge. When the PWM comparator detects that the sum of the current-sense amplifier output ($V_{CS_}$), the slope compensation ramp and the phase current imbalance signal exceeds the COMP voltage, the controller pulls DL_ low and drives DH_ high.

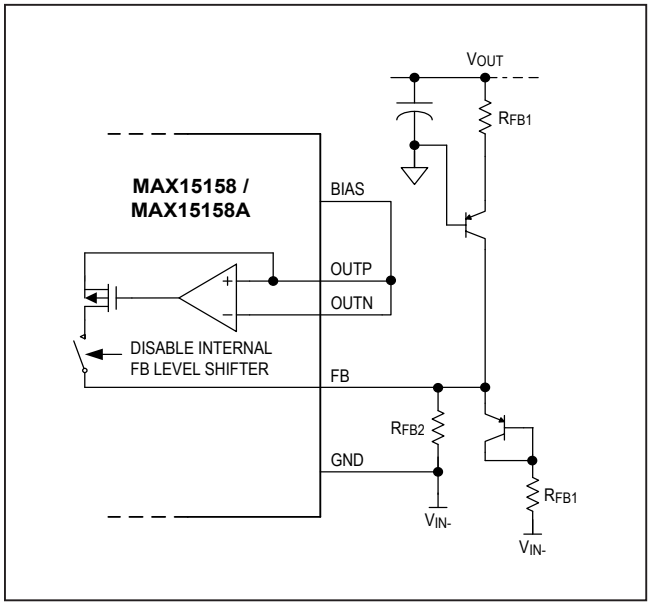


Figure 2. Using External FB Level Shifter

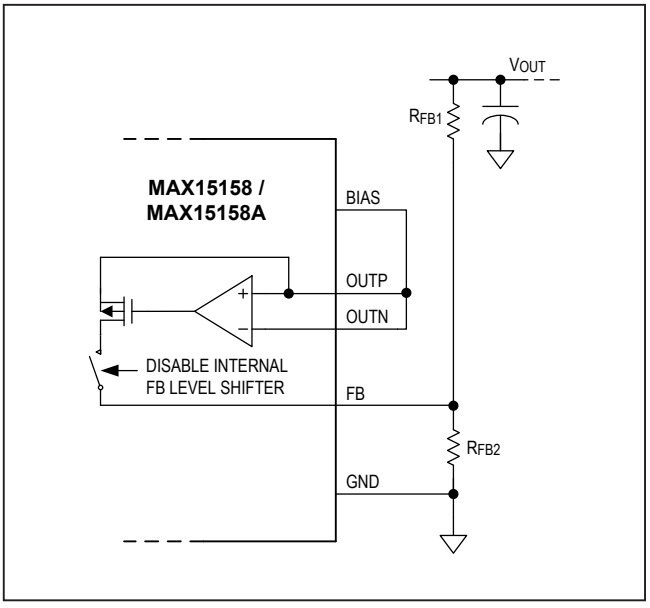


Figure 3. Using External FB Resistor Divider

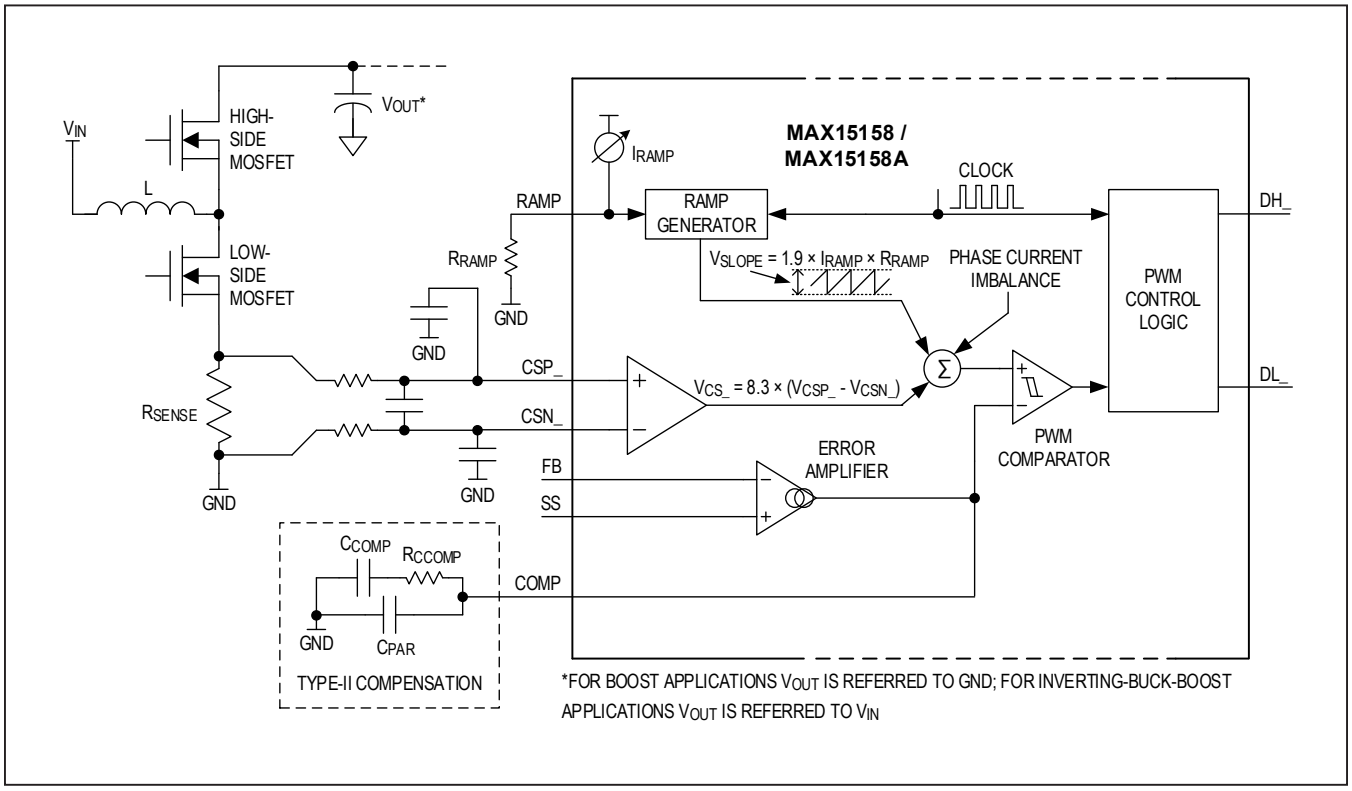


Figure 4. Peak-Current-Mode Control Loop

Compensation Design Guidelines

MAX15158/MAX15158A utilizes a fixed-frequency, peak current-mode control scheme to provide easy compensation and fast transient response. It is by nature for boost or inverting-buck-boost converters to have a right half plane (RHP) zero in their small signal control-to-output transfer function. For boost converters, the location of RHP zero is calculated by:

$$f_{RHP} = V_{OUT} \times (1 - D)^2 / (2 \times \pi \times I_{OUT(MAX)} \times L)$$

where:

$I_{OUT(MAX)}$ = Maximum load current per phase

D = Duty cycle = $1 - V_{IN}/V_{OUT}$

L = Value of the inductor

For inverting-buck-boost converters, the location of RHP zero is calculated by:

$$f_{RHP} = V_{OUT} \times (1 - D)^2 / (2 \times \pi \times I_{OUT(MAX)} \times L \times D)$$

where:

D = Duty cycle = $V_{OUT}/(|V_{IN}| + V_{OUT})$

For stable operation, it is required that the bandwidth of control loop (BW) is sufficiently lower than f_{RHP} and switching frequency (f_{SW}).

$$BW \le Minimum(f_{RHP}/7, f_{SW}/10)$$

A type-II compensation network is required to be connected between COMP and GND (R_{COMP}, C_{COMP} and C_{PAR} in Figure 4) to provide sufficient phase margin and gain margin to the control loop. The value of the compensation network can be selected by:

$$R_{COMP} = 16 \times \pi \times BW \times R_{SENSE} \times C_{OUT} \times V_{OUT} / [N \times (1 - D) \times G_{MEA} \times V_{REF}]$$

$$C_{COMP} = 5/(\pi \times R_{COMP} \times BW)$$

$$C_{PAR} = 1/(2 \times \pi \times R_{COMP} \times f_{SW})$$

where,

R_{SENSE} = Value of the sense resistor

C_{OUT} = Value of the output capacitor

N = Number of phases

G_{MEA} = Error Amplifier Transconductance (1.1mS, typ)

Adjustable Slope Compensation (RAMP)

When MAX15158/MAX15158A operates at a duty cycle greater than 50%, additional slope compensation is required to ensure stability and prevent subharmonic oscillations that occurs naturally in peak-current-mode controlled converters operating in continuous-conduction-mode (CCM). MAX15158/MAX15158A provides RAMP input to select the internal slope compensation ramp within a range of 230mV ~ 730mV. It is recommended that discontinuous-conduction-mode (DCM) designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

As shown in Figure 4, by connecting a resistor (R_{RAMP}) between RAMP and GND, the amplitude of the slope compensation ramp is calculated as:

$$V_{SLOPE} = 1.9 \times V_{RAMP} = 1.9 \times I_{RAMP} \times R_{RAMP}$$

where I_{RAMP} is the current sourced from RAMP to GND (10µA typ)

To guarantee stable and jitter-free operation, it is suggested to select the RAMP resistor that:

$$R_{RAMP} \geq 5 \times (V_{OUT(MAX)} - V_{IN(MIN)}) \times R_{SENSE}/(I_{RAMP} \times f_{SW} \times L)$$

where:

$V_{OUT(MAX)}$ = Maximum output voltage referred to GND

$V_{IN(MIN)}$ = Minimum input voltage referred to GND

R_{SENSE} = Value of the sense resistor

f_{SW} = Switching frequency

L = Value of the inductor

DRV Supply and Bias Regulator (BIAS)

The controller requires an external 8.5V to 14V DRV supply. The DRV supply powers the internal linear regulator that generates a regulated 4.75V bias supply to power the internal analog and digital control circuitry as shown in the *Block Diagram*. Bypass the BIAS pin with a 2.2µF or greater ceramic capacitor to maintain noise immunity and stability. The BIAS regulator provides up to 50mA of load current and the controller requires up to 5mA, so the remaining load capability can be used to support pullup resistors.

The controller has an undervoltage-lockout threshold on DRV. The undervoltage-protection circuits inhibit switching until DRV rises above 8.196V (typ).

If DRV drops below its undervoltage threshold, the controller determines that there is insufficient supply voltage to make valid control decisions. To protect the regulator and the output, the controller immediately pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 4.3Ω discharge MOSFET, placing the regulator into a high-impedance output state, so the output capacitance passively discharges through the load current.The BIAS linear regulator and internal reference power up only when DRV exceeds its undervoltage-lockout threshold and EN/UVLO is driven high.

EN/UVLO and Soft-Start/Shutdown

The EN/UVLO pin allows the input voltage operating range to be externally adjusted for power-sequence control. Connect EN/UVLO to the center of a resistor divider between the input and GND to adjust the undervoltage lockout voltage level as shown in the *Typical Application Circuit*. In the case where the DRV voltage threshold of the external MOSFET driver is higher than the undervoltage lockout threshold of the DRV pin, the EN/UVLO pin should also be pulled to GND before the external MOSFET driver is enabled. The EN/UVLO pin has two levels of thresholds with hysteresis. At power-up, once the voltage of the EN/UVLO pin is higher than 0.7V (typ) and DRV voltage is higher than its UVLO threshold, the internal 4.75V BIAS regulator is enabled. Once the voltage of EN/UVLO is higher than 1V (typ), and the internal reference stabilizes, the controller starts the initialization period where the OVP pin configuration is checked. During this initialization period, the controller pulls SS low through a 4.3Ω discharge MOSFET. As long as initialization is complete, the controller starts the soft-start sequence by charging the SS capacitor with a constant 5µA current source until the SS voltage reaches either the preset 2.0V target voltage (MAX15158A or MAX15158 with REFIN connected to BIAS), or the externally driven REFIN voltage (MAX15158, V_{REFIN} = 1V to 2.2V). The drivers start switching once SS exceeds 50mV and the controller detects that FB voltage is below the SS voltage. The controller enables the overvoltage fault-protection circuitry when SS exceeds 1V.

At power-down, once the voltage of EN/UVLO is below 0.9V (typ), the controller pulls PGOOD low and initiates the soft-shutdown sequence by discharging the SS capacitor with a constant 5µA current load. Since the output voltage tracks the SS voltage, the regulator actively discharges the output capacitors. Once the SS and FB voltage reaches 40mV, the controller stops switching and enters a low-power shutdown state. The device does not restart until the soft-shutdown sequence has completed. During the soft-shutdown cycle, the overvoltage fault protection remains active until the SS voltage falls below 1V. If the voltage of EN/UVLO is below 0.55V (typ) after soft-shutdown is complete, the 4.75V BIAS regulator is then disabled (see Figure 5).

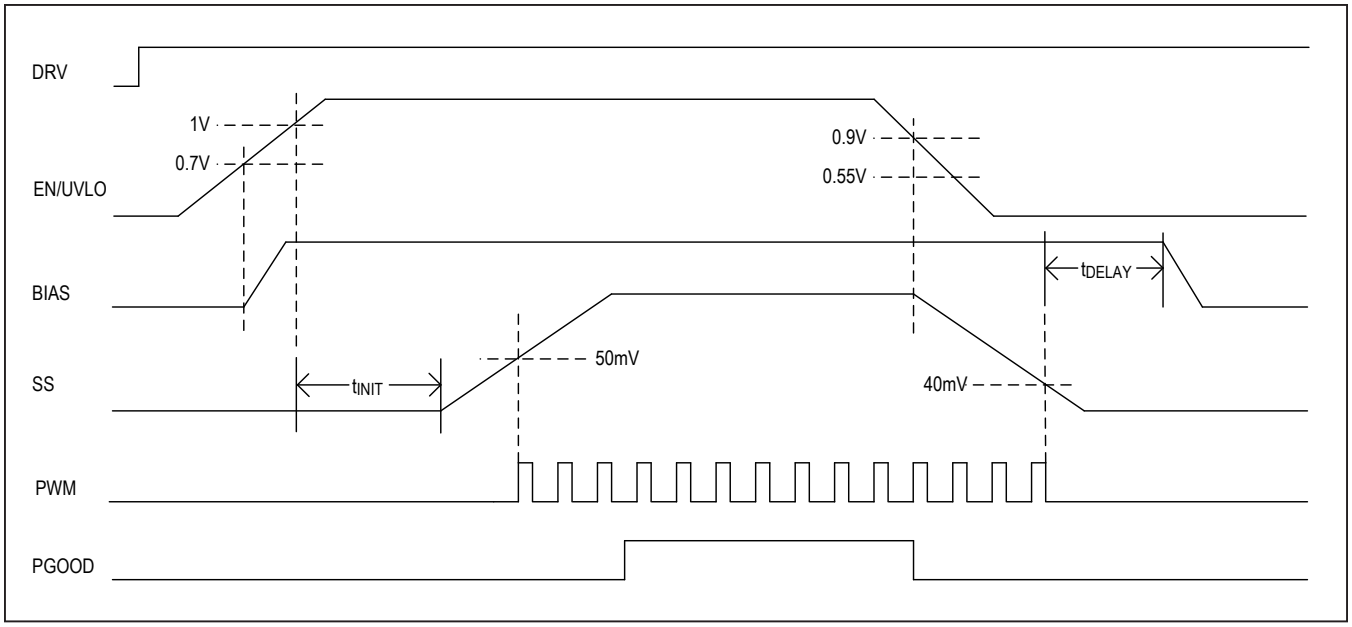


Figure 5. Soft-Start and Shutdown Sequence with EN/UVLO

Overcurrent Protection (OCP)

A current-sense resistor (R40 and R41 in the *Standard Application Circuits*) is connected between the source of the low-side MOSFET and GND. MAX15158/MAX15158A detects the current-sense signal (CSP_ to CSN_) and compares it with the cycle-by-cycle peak current limit threshold during low-side on-time. When the current exceeds the cycle-by-cycle peak current limit threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET to allow the inductor current to be discharged until the end of that switching cycle. Each phase has an independent up-down counter to accumulate the number of consecutive peak current limit events. If the counter exceeds 32, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

There is a secondary fast positive overcurrent protection (FPOCP) threshold, which is 33% higher than the cycle-by-cycle peak current limit threshold. If the inductor peak current exists the FPOCP threshold for two cycles, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

The cycle-by-cycle peak current limit threshold is set by a resistor at ILIM pin. A 10µA source current flows into the resistor and generates a voltage level. This voltage level is internally scaled by a factor of 0.10 to set cycle-by-cycle peak current limit threshold. The minimum and maximum settable current limit levels are 20mV and 100mV. The cycle-by-cycle peak current limit level is given by:

$$V_{OCP} = 0.10 \times 10\mu A \times R_{ILIM}$$

The maximum peak inductor current is set by both V_{OCP} and the current-sense resistor (R_{SENSE}).

$$I_{PEAK(MAX)} = V_{OCP}/R_{SENSE}$$

The device also has a negative overcurrent protection (NOCP) threshold which is -83% of the cycle-by-cycle peak current limit threshold. When the low-side MOSFET is turned on and the inductor current is below the NOCP threshold, the device will command to keep the low-side MOSFET on to allow the inductor current to be charged by the input voltage, until the inductor current is above the NOCP threshold. Each phase has an independent up-down counter to accumulate the number of consecutive NOCP events. If the counter exceeds 32, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

Overvoltage Protection (OVP)

MAX15158/MAX15158A has an OVP comparator to monitor the FB voltage. The device can be configured to disable OVP or select OVP threshold of 110% by connecting a resistor from the OVP pin to GND. FB OVP is also disabled when the voltage on the SS pin is below 1V. Once OVP is enabled, the drivers start switching, and voltage on the SS pin is higher than 1V, the FB overvoltage comparator trips if the feedback voltage exceeds the SS voltage by 110% for more than 128 PWM clock cycles. If the overvoltage comparator is triggered, the controller pulls PGOOD low, discharges the SS capacitor and disables the drivers. The controller immediately restarts once the fault condition has been removed. When OVP is disabled, the PGOOD will remain high when FB voltage is higher than the reference voltage.

The resistor from OVP pin to GND is also used to enable or disable the FB level shifter and select single or dual phase operation. Refer to the Table 1.

Thermal Shutdown (TSHDN)

The controller features a thermal fault-protection circuit. When the junction temperature rises above +165°C, the internal thermal sensor triggers the fault protection, disables the drivers, and discharges the SS capacitor. The controller remains disabled until the junction temperature cools by 15°C. Once the device has cooled down the controller automatically restarts using the soft-start sequence.

Switching Frequency (FREQ/CLK)

The controller supports 120kHz to 1MHz switching frequencies. Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. To adjust the switching frequency, either place an external resistor from FREQ/CLK to AGND, or drive FREQ/CLK with an external system clock (see Table 2). The resistively programmable switching frequency is determined by:

Table 1. FB OVP Settings, Phase and FB Level Shifter Configuration

OVP PIN VOLTAGE (V)	R_{OVP}	FB OVP THRESHOLD	FB LEVEL SHIFTER	PHASE CONFIGURATION
0.10 ± 0.05	GND	110%	DISABLED	Dual-phase or quad-phase operations
0.33 ± 0.05	33kΩ	DISABLED	ENABLED	
0.68 ± 0.05	68kΩ	110%	ENABLED	
1.00 ± 0.05	100kΩ	DISABLED	DISABLED	
1.33 ± 0.05	133kΩ	DISABLED	ENABLED	Single-phase operation
1.69 ± 0.05	169kΩ	110%	ENABLED	
2.05 ± 0.05	205kΩ	DISABLED	DISABLED	
2.53 ± 0.05	OPEN	110%	DISABLED	

Table 2. Phase and Master/Slave Configurations

NUMBER OF PHASES	NUMBER OF MAX15158/MAX15158A	FB OF SLAVE CONNECTED TO BIAS	CLK FREQUENCY
1	1	N/A	4 x f_{SW}
2	1	N/A	4 x f_{SW}
4	2	Yes	4 x f_{SW}

$$f_{SW} = (R_{FREQ}/100k\Omega) \times 600kHz$$

Phase and Master/Slave Configurations

MAX15158/MAX15158A can be configured in single-phase, dual-phase or quad-phase operation modes. When supporting quad-phase operation, two MAX15158/MAX15158A ICs are used as master and slave. The controller identifies the number of phases by the resistor at the OVP pin. This identification is used to determine how the controller responds to the multiphase clock signal generated by the primary phase.

For proper synchronization between two devices, connect the SYNC, SS, COMP, CSIOP and CSION of the master and slave devices. The FB, REFIN, OUTP and OUTN of the slave device are connected to its BIAS pin (see the *Standard Application Circuits*).

The two phases of the same device are interleaved 180°. When two MAX15158/MAX15158A ICs are stacked up, there is a 90° phase shift between master and slave (Figure 6).

Multiphase Current Balance

MAX15158/MAX15158A monitors the low side MOSFET current of each phase for active phase current balancing in multiphase operations. The current imbalance is applied to the cycle-by-cycle current sensing circuitry as a feedback, helping regulating so that load current is evenly shared between the two phases (see the *Block Diagram*).

In quad phase operation, the device uses the differential CSIO_ connections to communicate the average per-chip current between master and slave. The current-mode master and slave devices regulate their current so that all four phases share the load current equally.

MOSFET Gate Control

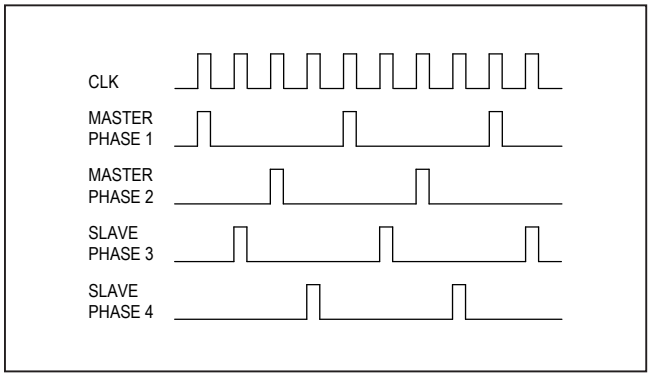


Figure 6. Quad Phase Synchronization (Master/Slave)

MAX15158/MAX15158A must be used with external MOSFET drivers to drive power MOSFETs for typical high-voltage applications. The device has dedicated DLFB_ pins to detect the gate voltage of the low-side MOSFETs to ensure no-shoot-through between the high- and low-side MOSFETs due to the mismatch delays caused by the external MOSFET driver. The DLFB_ pins have a rising threshold of 0.8V (typ) and falling threshold of 0.5V (typ). A resistor divider can be used from the gate of the low-side MOSFET to DLFB_ pins to match the MOSFET gate threshold voltage and the DLFB_ threshold (see the *Standard Application Circuits*), to allow robust operation with a wide range of MOSFETs while minimizing dead-time power losses.

Inductor Selection

A larger inductor value results in reduced inductor ripple current, leading to a reduced inductor core loss. However, a larger inductor value results in either a larger physical size or a higher series resistance (DCR) and a lower saturation current rating. Typically, inductor value is chosen to have current ripple (ΔI_L) around 50% of average inductor current. The average inductor current is can be calculated by:

$$I_{L(AVE)} = I_{LOAD(MAX)}/[(1 - D) \times N]$$

where:

N = Number of phases

The inductor can be chosen with the following formula:

$$L = D \times V_{IN}/(f_{SW} \times \Delta I_L)$$

Output Capacitor Selection

The output capacitors are selected to improve stability, output voltage ripple and load transient performance. To meet output voltage ripple (V_{RIPPLE}) requirement, the output capacitor can be selected by:

$$C_{OUT(RIPPLE)} = I_{LOAD(MAX)} \times D/(N \times f_{SW} \times V_{RIPPLE})$$

For some applications it is desired to limit output voltage overshoot and undershoot during load transient. To meet the load transient requirement, the output capacitor can be selected by:

$$C_{OUT(TRANSIENT)} = \Delta I_{LOAD}/(3 \times BW \times \Delta V_{OUT})$$

where:

ΔI_{LOAD} = Load current step,

BW = The control loop bandwidth (see *Compensation Design Guidelines*),

ΔV_{OUT} = The desired output voltage overshoot or undershoot.

The final output capacitance should be selected as:

$$C_{OUT} \geq \text{Maximum } (C_{OUT(RIPPLE)}, C_{OUT(TRANSIENT)})$$

Input Capacitor Selection

The input capacitors are selected to help reduce input voltage ripple (V_{IN_RIPPLE}). For boost converters, the input current is continuous. Neglecting ESR and ESL of the input capacitor, the input capacitor can be selected by:

$$C_{IN} = \Delta I_L/(8 \times N \times f_{SW} \times V_{IN_RIPPLE})$$

For inverting-buck-boost converters, the input current is discontinuous. The input capacitor can be selected by:

$$C_{IN} = I_{LOAD(MAX)} \times D/(N \times f_{SW} \times V_{IN_RIPPLE}).$$

PCB Layout Guidelines

PCB layout can dramatically affect the performance of the power converter. A poorly designed board can degrade efficiency, thermal performance, noise control, and even control-loop stability. At higher switching frequencies, layout issues are especially critical.

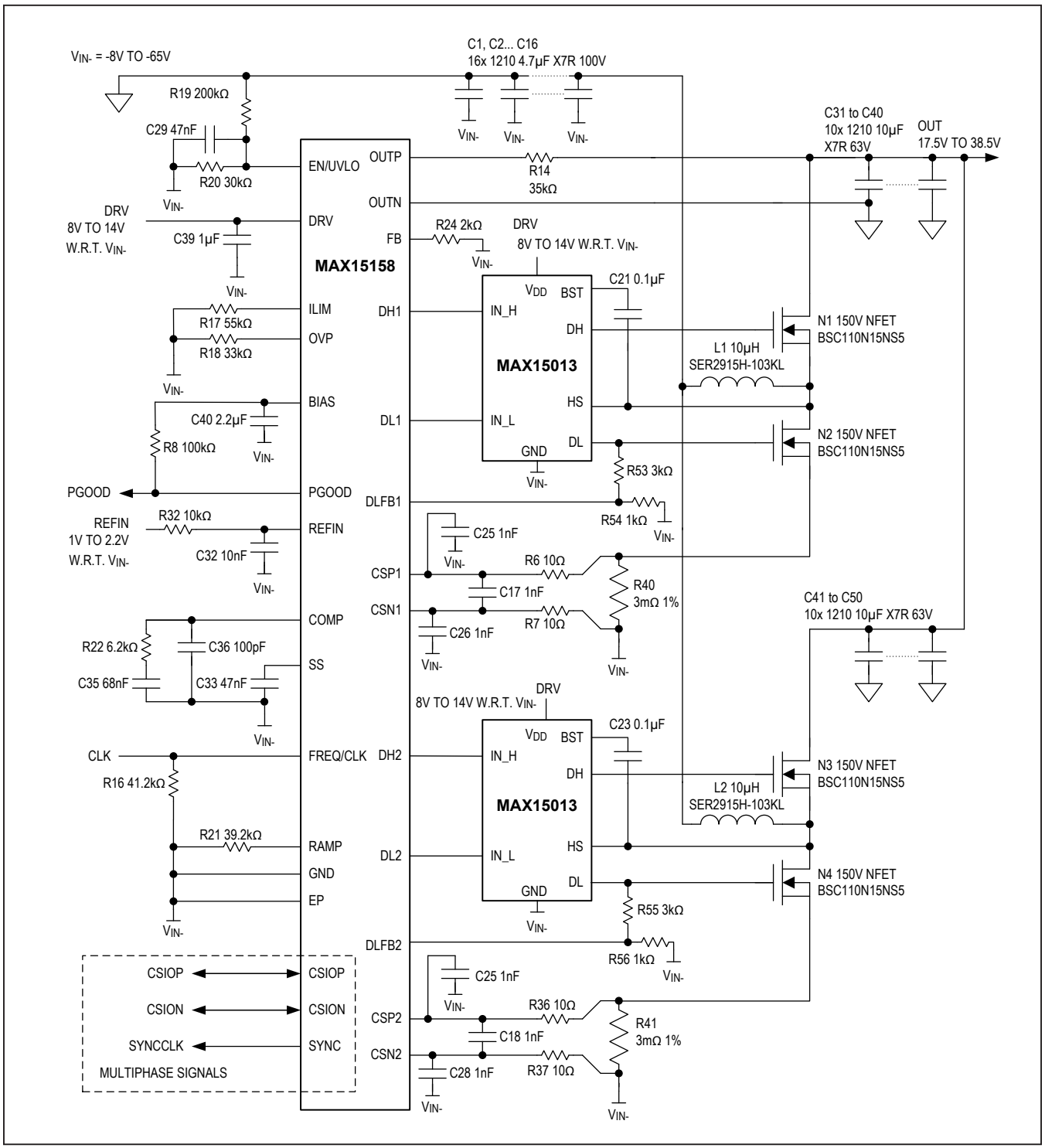
As a general guideline, the input capacitors, inductor, MOSFETs, sense resistor and output capacitors should be placed close together to minimize the high frequency current path. The MOSFET driver should be placed close to the MOSFETs and the switching node (SW) to keep the gate drive, BST and SW traces short. MAX15158/MAX15158A should keep some distance from the high dv/dt SW, BST, and gate drive traces. The peripheral RC components should be placed as close to the controller as possible. Priority should be given to the pins that are sensitive to noise (COMP, SS, REFIN, FB, etc.). It is suggested to place both differential-mode and common-mode filters between the CSP_ pin, CSN_ pin, and sense resistor (see the *Standard Application Circuits*).

For high power applications, it is suggested to use planes for the power traces V_{IN}, V_{OUT}, and GND. It is important to have enough vias connecting the power planes in different layers. The signal and power grounds must be seperated. All the power components, including input and output capacitors, MOSFETs, sense resistor and MOSFET driver should be connected to the power ground. MAX15158/MAX15158A and its peripheral RC components must be connected to the signal ground. It is suggested to have an island of signal ground in the closest internal layer underneath the controller. Multiple vias can be used to connect the signal ground island to the exposed pad of the controller and the ground nodes of the noise sensitive signal (COMP, SS, REFIN, FB, etc.). Signal ground should be tied to power ground through a short trace or 0Ω resistor, close to the power ground node of the sense resistor and input capacitors.

When the FB level shifter is used, the OUTP/OUTN sense lines must be routed differentially directly from the load points. The current sense lines from sense resistor to CSP_ and CSN_ should also be routed differentially. When the controller is configured to multiphase operation, the current sense lines of different phases should be kept apart to avoid signal coupling. Keep all sense lines and other noise sensitive signals (CSIO_, COMP, SS, REFIN, FB, etc.) away from the noisy traces (SW, BST, gate drives, FREQ/CLK, SYNC, etc.).

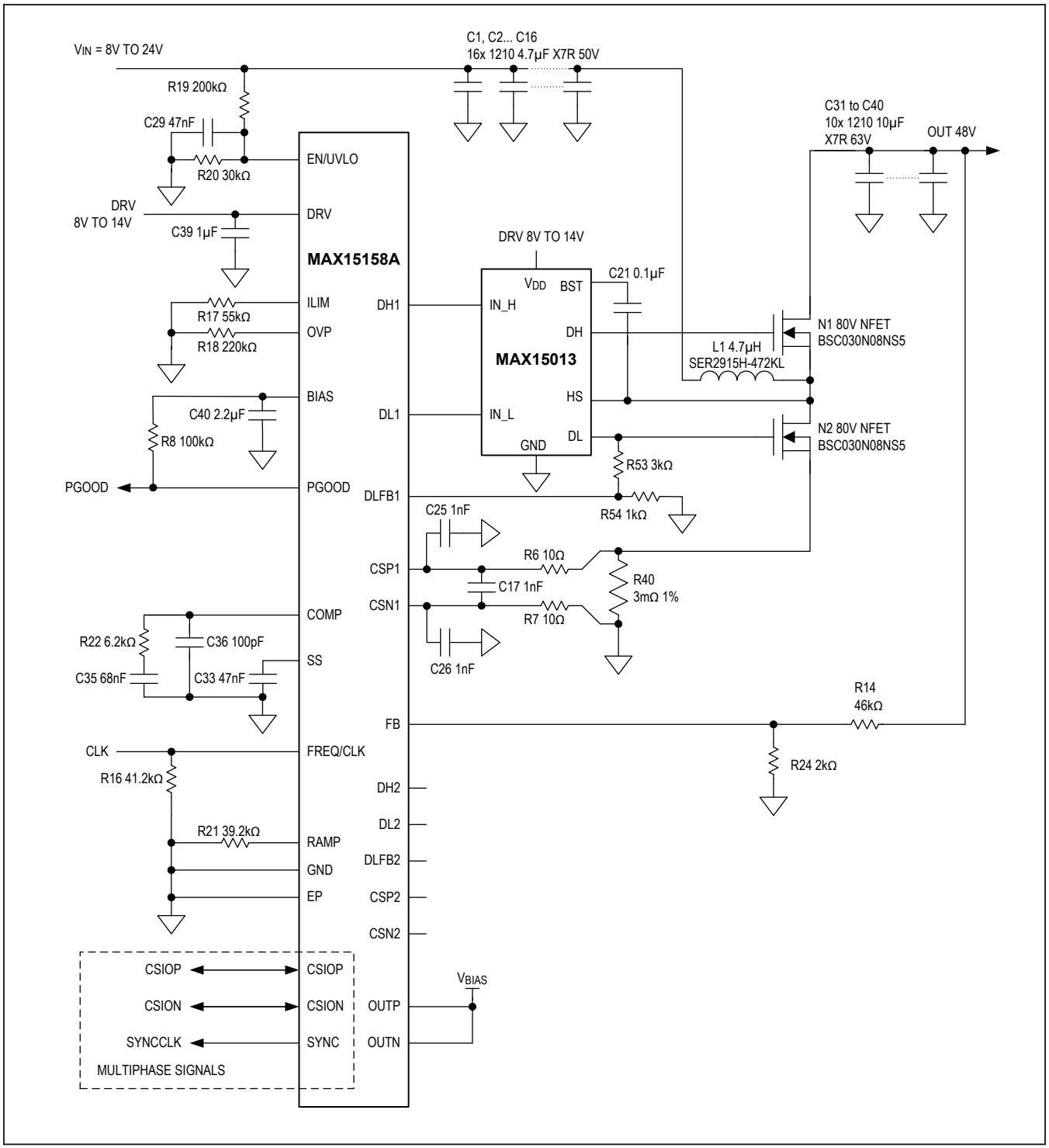
Standard Application Circuits

Dual-Phase Inverting Buck-Boost Converter



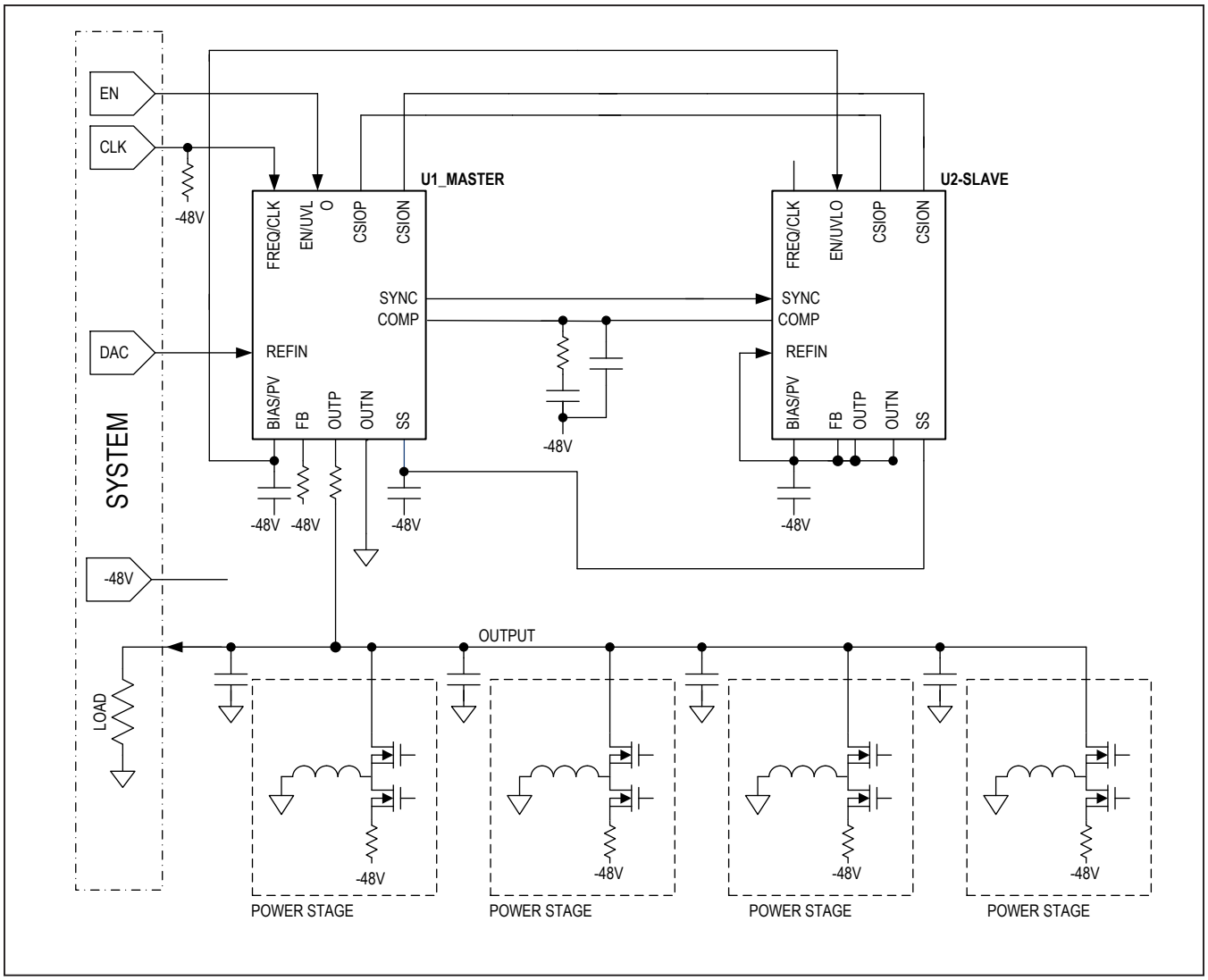
Standard Application Circuits (continued)

Single-Phase Boost Converter



Standard Application Circuits (continued)

Quad Phase Interconnects (Inverting Buck-Boost Converter)



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX15158ATJ+	-40°C to +125°C	32 TQFN-EP*
MAX15158ATJ+T	-40°C to +125°C	32 TQFN-EP*
MAX15158AATJ+	-40°C to +125°C	32 TQFN-EP*
MAX15158AATJ+T	-40°C to +125°C	32 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-complian package.
T = Tape and reel.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	9/18	Updated *Electrical Characteristics* table, *Block Diagrams*, *OVP* section, added *Inductor Selection* section, and update *Ordering Information* table	4, 6, 7, 13, 14, 16, 17, 19, 21, 25
2	11/19	Updated *General Description, Benefits and Features sections, Electrical Characteristics, Pin Description, Block Diagrams*, and *Detailed Description*	1, 4–7, 10, 11, 13–20

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