19-1976; Rev 1; 6/92

MAXIM

CMOS µP-Compatible, 5µs, 8-Bit ADCs

General Description

The MAX165/MAX166 are high-speed (5µs) microprocessor (µP)– compatible, 8-bit ADCs with track/hold (T/H). The T/H function allows full-scale signals up to 50kHz (386mV/µs slew rate) to be acquired and digitized accurately. Both ADCs use a successive approximation technique to achieve fast conversions and low power dissipation. The MAX165/MAX166 operate with a +5V supply and an internal or external +1.23V reference, and accept single-ended (MAX165) or differential (MAX166) voltages ranging from 0V to 2VREF.

The MAX165/MAX166 are easily interfaced to all popular 8-bit µPs through standard $\overline{CS}$ and $\overline{RD}$ control signals. These signals control the start of conversions and data access. A $\overline{BUSY}$ signal indicates the beginning and end of conversions. Since all the data outputs are latched and three-state buffered, the MAX165/MAX166 can be directly tied to a µP data bus or system input/output port.

The MAX165 is a plug-in replacement for the MX7575, with the addition of an internal 1.23V reference. For applications that require a differential analog input and an internal reference, the MAX166 is recommended.

Applications

Digital-Signal Processing
High-Speed Data Acquisition
Telecommunications
Audio Systems
High-Speed Servo Loops
Low-Power Data Loggers

Features

- ♦ 5µs Conversion Time
- ♦ Built-In Track/Hold
- ♦ ±1LSB Max Total Unadjusted Error
- ♦ 50kHz Signal Bandwidth
- ♦ Internal 1.23V Bandgap Reference and Buffer
- ♦ Single +5V Supply Operation
- ♦ 8-Bit µP Interface
- ♦ 100ns Data-Access Time
- ♦ 15mW Typ Power Consumption
- ♦ Small Footprint Packages
- ♦ Plug-In Upgrade to the MX7575 (MAX165)

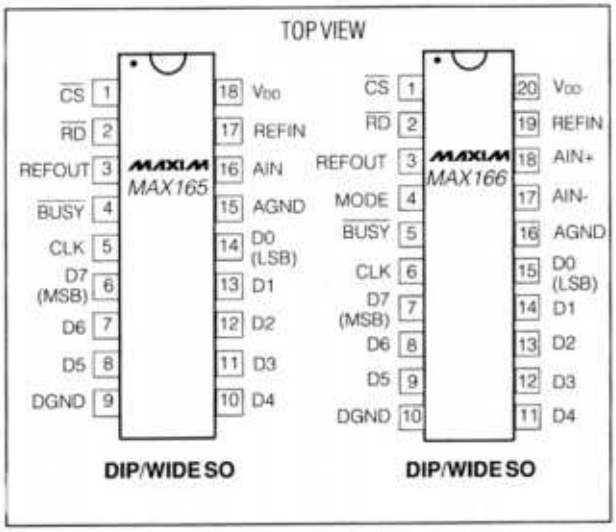
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX165ACPN	0°C to +70°C	18 Plastic DIP	±1/2
MAX165BCPN	0°C to +70°C	18 Plastic DIP	±1
MAX165ACWN	0°C to +70°C	18 Wide SO	±1/2
MAX165BCWN	0°C to +70°C	18 Wide SO	±1
MAX165BC/D	0°C to +70°C	Dice*	±1
MAX165AEPN	-40°C to +85°C	18 Plastic DIP	±1/2
MAX165BEPN	-40°C to +85°C	18 Plastic DIP	±1
MAX165AEWN	-40°C to +85°C	18 Wide SO	±1/2
MAX165BEWN	-40°C to +85°C	18 Wide SO	±1
MAX165AMJN	-55°C to +125°C	18 CERDIP**	±1/2
MAX165BMJN	-55°C to +125°C	18 CERDIP**	±1

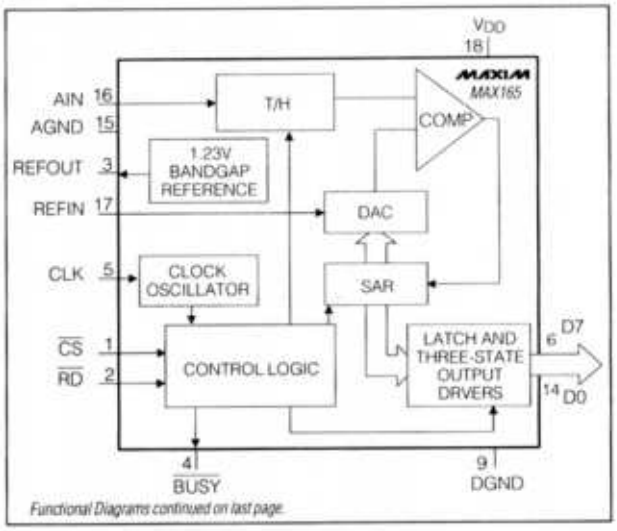
Ordering Information continued on last page.

* *Contact factory for dice specifications.*
***Contact factory for availability processing to MIL-STD-883.*

Pin Configurations



Functional Diagrams



Functional Diagrams continued on last page.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

CMOS µP-Compatible 5µs, 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND
(MAX165 Pins 1, 2) ..... -0.3V, V_{DD} +0.3V
(MAX166 Pins 1, 2, 4) ..... -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(MAX165 Pins 4, 6-8, 10-14) ..... -0.3V, V_{DD} +0.3V
(MAX166 Pins 5, 7-9, 11-15) ..... -0.3V, V_{DD} +0.3V
CLK Input Voltage (MAX165 Pin 5) to DGND ..... -0.3V, V_{DD} +0.3V
CLK Input Voltage (MAX166 Pin 6) to DGND ..... -0.3V, V_{DD} +0.3V
REFIN, REFOUT to AGND ..... -0.3V, V_{DD} +0.3V
MAX165 AIN to AGND ..... -0.3V, V_{DD} +0.3V
MAX166 AIN+, AIN- to AGND ..... -0.3V, V_{DD} +0.3V

Continuous Power Disipation (T_A = +70°C)
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above+70°C) 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX16_ _C_ _ ..... 0°C to +70°C
MAX16_ _E_ _ ..... -40°C to +85°C
MAX16_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, AIN- = 0V (MAX166), f_{CLK} = 4MHz external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE		MAX165A			±1	LSB
			MAX165B			±2	
			MAX166A/C			±1	
			MAX166B/D			±2	
Relative Accuracy			MAX165A			±1/2	LSB
			MAX165B			±1	
			MAX166A/C			±1/2	
			MAX166B/D			±1	
No-Missing-Codes Resolution				8			Bits
Full-Scale Error						±1	LSB
Full-Scale Tempco					±5		ppm/°C
Offset Error (Note 1)						±1/2	LSB
Offset Tempco					±5		ppm/°C
ANALOG INPUT							
Voltage Range		1LSB = 2VREF/256		0		2VREF	V
Voltage Range AIN+ (MAX166)				AIN-		V_{DD}	V
Voltage Range AIN- (MAX166)				0		AIN+	V
DC Input Impedance				10			MΩ
Slew Rate, Tracking				0.386			V/µs
SNR (Note 2)		V_{IN} = 2.46V_{p-p} at 10kHz (Figure 13)		45			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, AIN- = 0V (MAX166), f_{CLK} = 4MHz external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE (Note 2)							
REFIN Range (Note 3)	VREF	±5% variation for specified performance		1.16	1.23	1.29	V
REFIN Current	I_{REF}					500	µA
REFOUT Voltage	REFOUT	T_A = +25°C		1.18	1.21	1.23	V
REFOUT Load Regulation		T_A = +25°C, I_L = 0mA to 1.5mA				3	mV
REFOUT Supply Sensitivity		V_{DD} ±5%				±1.5	mV
Temperature Drift			MAX165AC/AE/BC/BE		40	70	ppm/°C
			MAX165AM/BM		60	100	
			MAX166AC/AE/BC/BE		40	70	
			MAX166AM/BM		60	100	
External Capacitive Load Requirement				4.7			µF
LOGIC INPUTS							
$\overline{CS}$, $\overline{RD}$, MODE (MAX166)							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C			±1	mA
			T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 3)	C_{IN}					10	pF
CLOCK							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Low Current	I_{INL}	V_{IN} = 0V	MAX16_ _C/E			700	µA
			MAX16_ _M			800	
Input High Current	I_{INH}	V_{IN} = V_{DD}	MAX16_ _C/E			700	µA
			MAX16_ _M			800	
LOGIC OUTPUTS							
$\overline{BUSY}$, D0 to D7							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 40µA		4.0			V
D0 to D7							
Floating State Leakage Current		V_{OUT} = 0V to V_{DD}	MAX16_ _C/E			±1	mA
			MAX16_ _M			±10	
Floating State Output Capacitance (Note 3)						10	pF
CONVERSION TIME (Note 4)							
With External Clock		f_{CLK} = 4MHz			5		µs
With Internal Clock		Using recommended clock components R_{CLK} = 100kΩ, C_{CLK} = 100pF, T_A = +25°C		5		15	µs
POWER REQUIREMENTS (Note 5)							
Supply Voltage	V_{DD}	±5% for specified performance			5		V
Supply Current	I_{DD}		MAX16_ _C/E		3	6	mA
			MAX16_ _M		3	7	
Power Dissipation					15		mW
Power-Supply Rejection		4.75V < V_{DD} < 5.25V				±1/4	LSB

CMOS µP-Compatible 5µs, 8-Bit ADCs

TIMING CHARACTERISTICS (Note 6)

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C		T_A = T_{MIN} to T_{MAX}				UNITS
			ALL		MAX16_ _C/E		MAX16_ _M		
			MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0		0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Time	t_2			100		100		120	ns
Data-Access Time after $\overline{RD}$	t_3	(Note 7)		100		100		120	ns
$\overline{RD}$ Pulse Width	t_4		100		100		120		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0		0		0		ns
Data-Access Time after $\overline{BUSY}$	t_6	(Note 7)		80		80		100	ns
Data-Hold Time after $\overline{RD}$	t_7	(Note 8)	10	80	10	80	10	100	ns
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_8		0		0		0		ns

Note 1: Offset Error is measured with respect to an ideal first code transition which occurs at 1/2LSB.
Note 2: REFOUT is not available for use in MAX166C/MAX166D. These parts must be used with an external reference.
Note 3: Guaranteed by design, not tested.
Note 4: Accuracy may degrade at conversion times other than those specified.
Note 5: Power-supply current is measured when MAX165/MAX166 are inactive, i.e.
for MAX165 $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = high;
for MAX166 CS = $\overline{RD}$ = $\overline{BUSY}$ = MODE = high.
Note 6: Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a 1.6V voltage level.
Note 7: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 8: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

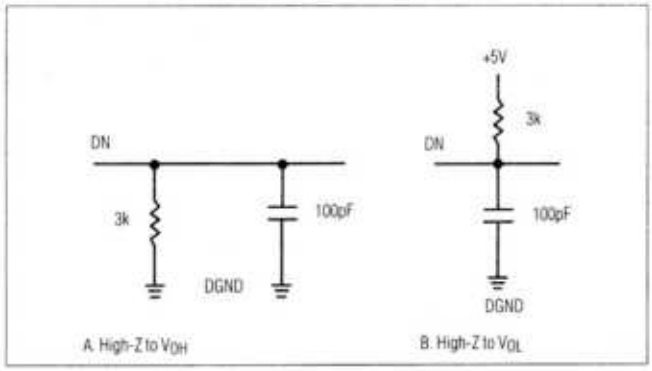


Figure 1. Load Circuits for Data-Access Time Test

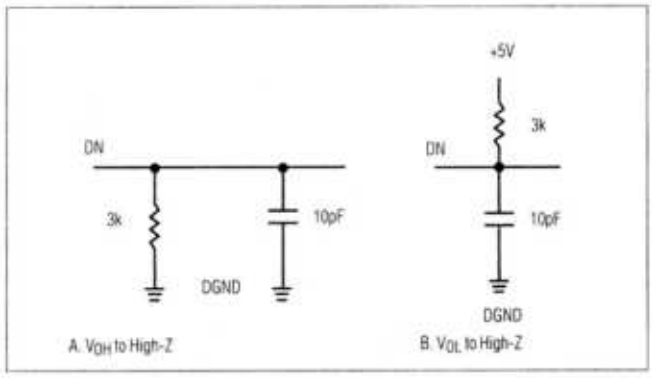


Figure 2. Load Circuits for Data-Hold Time Test

Detailed Description

Converter Operation

The MAX165/MAX166 use the successive approximation technique to convert an unknown analog input voltage to an 8-bit digital output code (see *Functional Diagrams*). The MAX165/MAX166 sample the input voltage on an internal capacitor once at the beginning of the conversion, (see *Track/Hold* section). The DAC is initially set to half scale, and the comparator determines whether the input signal is larger or smaller than half scale. If the input is larger, the DAC most significant bit (MSB) is kept; if it is smaller, the MSB is dropped. At the end of each comparison phase, the successive approximation register (SAR) stores the results of the previous decisions and determines the next trial bit. This information is loaded into the DAC after each decision. As the conversion proceeds, the analog input is approximated more closely as it is compared to the combined previous DAC bits and a new DAC trial bit. After 8 comparison cycles, the 8 bits stored in the SAR are latched into the output latches. At the end of the conversion, the $\overline{BUSY}$ signal goes high, and the data in the output latches is ready for µP access. Furthermore, the DAC is reset to half scale in preparation for the next conversion.

Microprocessor Interface

The $\overline{CS}$ and $\overline{RD}$ logic inputs are used to initiate conversions and to access data from the devices. The MAX165/

Pin Description

PIN		NAME	FUNCTION
MAX165	MAX166		
1	1	$\overline{CS}$	CHIP SELECT Input. $\overline{CS}$ must be low for the device to be selected, or to recognize the RD input.
2	2	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data. $\overline{RD}$ is also used to start conversions. See the *Digital Interface* section.
3	3	REFOUT	Output of the internal 1.23V bandgap reference
	4	MODE	MODE (MAX166). Mode = low puts the ADC into asynchronous-conversion mode. MODE has to be tied high for synchronous-conversion mode and ROM interface mode.
4	5	$\overline{BUSY}$	$\overline{BUSY}$ Output. $\overline{BUSY}$ going low indicates the start of a conversion. $\overline{BUSY}$ going high indicates the end of a conversion.
5	6	CLK	External Clock Input/Internal Oscillator Pin for frequency setting RC components.
6	7	D7 (MSB)	Three-State Data Output, bit 7 (MSB)
7	8	D6	Three-State Data Output, bit 6
8	9	D5	Three-State Data Output, bit 5
9	10	DGND	Digital Ground
10	11	D4	Three-State Data Output, bit 4
11	12	D3	Three-State Data Output, bit 3
12	13	D2	Three-State Data Output, bit 2
13	14	D1	Three-State Data Output, bit 1
14	15	D0 (LSB)	Three-State, Data Output, bit 0 (LSB)
15	16	AGND	Analog Ground
16		AIN	Analog Input – (single-ended with respect to AGND) 0V to 2VREF input range
	17	AIN–	Negative Analog Input – differential (MAX166)
	18	AIN+	Positive Analog Input – differential (MAX166)
17	19	REFIN	Reference Input +1.23V nominal
18	20	V_{DD}	Power-Supply Voltage +5V nominal

MAX166 have two common interface modes that will be referred to as slow-memory interface mode and ROM interface mode. In addition, the MAX166 has an asynchronous conversion mode (MODE pin = low) where continuous conversions are performed. In the slow-memory interface mode, $\overline{CS}$ and $\overline{RD}$ are taken low to start a conversion and remain low until the end of the conversion, at which time data is updated. This mode is designed for µPs that can be forced into a wait state. In ROM interface mode, however, the µP is not forced into a wait state. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low, and data from the previous conversion is read. At the end of the most recent conversion, the µP executes a READ instruction and starts another conversion.

Slow-Memory Interface Mode

Figure 3 shows the timing diagram for slow-memory interface mode. This mode is used with µPs that have a wait state capability of at least 5µs (such as the 8085A), where a READ instruction is extended to accommodate slow-memory devices. A conversion is started by executing a memory READ to the device (taking $\overline{CS}$ and $\overline{RD}$ low). The $\overline{BUSY}$ signal (which is connected to the µP READY input) then goes low and forces the µP into a wait state. The T/H, which has been tracking the analog input signal, holds the signal on the third falling clock edge after $\overline{RD}$ goes low (Figure 12). At the end of the conversion, $\overline{BUSY}$ returns high, the output latches, and buffers are updated with the new conversion results. The µP then completes the memory READ by acquiring this new data.

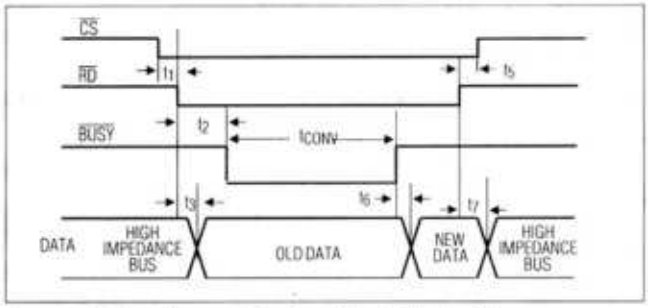


Figure 3. Slow-Memory Interface Mode Timing Diagram

CMOS µP-Compatible 5µs, 8-Bit ADCs

The MAX165/MAX166's fast conversion time ensures that the µP is not forced into a wait state for too long. Faster versions of many µPs, including the 8085A-2, test the status of the READY input right after the start of an instruction cycle. Therefore, for the MAX165/MAX166 to effectively place the µP in a wait state, their BUSY output should go low very early in the cycle. When using the 8085A-2, the earliest possible indication of an upcoming READ operation is provided by the S0 status signal. Thus, S0 (which is low for a READ cycle) should be connected to the RD input of the MAX165/MAX166. Figure 4 shows the connection diagram for the 8085A-2 to the MAX165/MAX166 in slow-memory interface mode.

ROM Interface Mode

Figure 5 shows the timing diagram for ROM interface mode. In this mode, the µP does not need to be placed in a wait state. A conversion is started with a READ instruction (RD and CS go low), and old data is accessed. The BUSY signal then goes low to indicate the start of a conversion. As before, the T/H acquires the signal on the third falling clock edge after RD goes low. At the end of conversion (BUSY going high), another READ instruction always accesses the new data and normally starts a second conversion. However, if RD and CS go low within one external clock period of BUSY going high, the second conversion is not started. For correct operation in this mode, RD and CS should not go low before BUSY returns high.

Figures 6 and 7 show the connection diagrams for interfacing the MAX165/MAX166 in ROM interface mode. Figure 6 shows the connection diagram to the 6502/6809 µPs, and Figure 7 shows interfacing to the Z-80.

Due to their fast interface timing, the MAX165/MAX166 will interface to the TMS32010 running at up to 18MHz. Figure 8 shows the connection diagram to the TMS32010. In this interface, the MAX165/MAX166 are mapped as a port address. A conversion is initiated by using an IN A and a PA instruction, and the conversion result is placed in the TMS32010 accumulator.

Asynchronous Conversion Mode (MAX166)

Tying the MODE pin low places the MAX166 into a continuous-conversion mode. The RD and CS inputs are only used for reading data from the converter. Figure 9 shows the timing diagram for this mode of operation, and Figure 10 shows the connection diagram of the converter to the 8085A. In this mode, the MAX166 appears like a ROM to the µP, in that data can be accessed independently of the clock. The output latches are normally

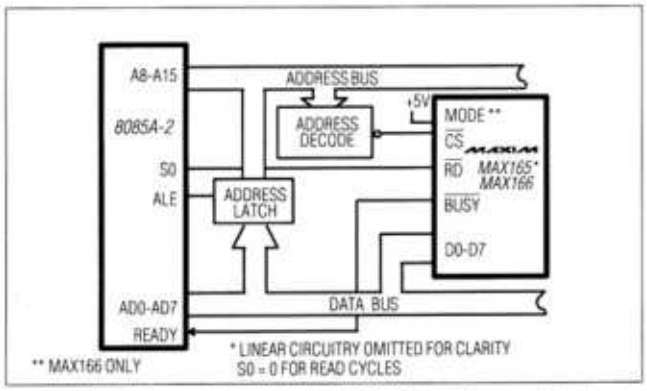


Figure 4. MAX165/MAX166 to 8085A-2 Slow-Memory Interface

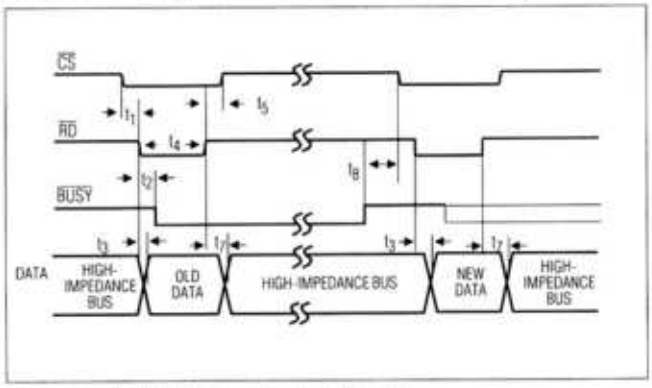


Figure 5. ROM Interface Timing Diagram

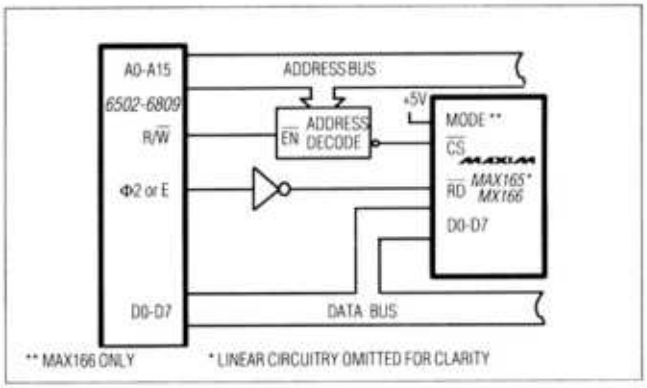


Figure 6. MAX165/MAX166 to 6502/6809 ROM Interface

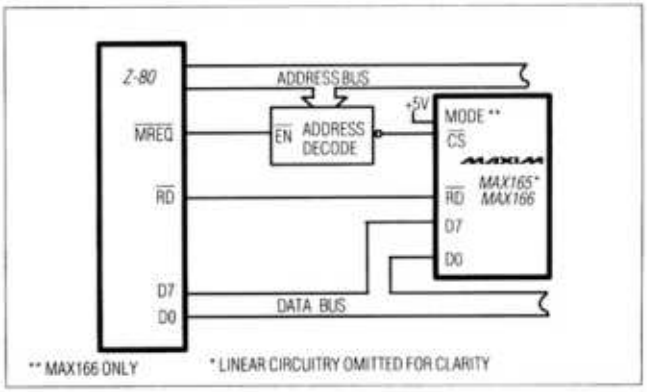


Figure 7. MAX165/MAX166 to Z-80 ROM Interface

updated on the rising edge of BUSY. But, if CS and RD are low when BUSY goes high, the data latches are not updated until one of these inputs returns high. Additionally, the MAX166 stops converting and BUSY stays high until RD or CS goes high. This mode of operation allows a simple µP interface.

Microprocessor Interface For Signal Acquisition

Many applications require sampling of the input signal at equal intervals to minimize errors caused by sampling uncertainty or jitter. To achieve this with the previously discussed interfaces, the user must match software delays or count the number of elapsed clock cycles. This becomes difficult in interrupt driven systems where the uncertainty in interrupt servicing delays is another complicating factor.

The solution is to use a real-time clock to control the start of a conversion. This should be synchronous with the clock input to the ADC (both should be derived from the same source) because the sampling instants occur three clock cycles after CS and RD go low. Therefore, the sampling instants occur at exactly equal intervals if the conversions are started at equal intervals. In this scheme, the output data is fed into a FIFO latch, which allows the µP to access data at its own rate. This guarantees that data is not read from the ADC in the middle of a conversion. If data is read from the ADC during a conversion, the conversion in progress may be disturbed, but the accessed data that belonged to the previous conversion will be correct.

The T/H starts holding the input on the third falling edge of the clock after CS and RD go low. If CS and RD go low within 20ns of a falling clock edge, the ADC may or may not consider this falling edge as the first of the three edges that determine the sampling instant. Therefore, the CS and RD should not be allowed to go low within this period when sampling accuracy is required.

Track/Hold

The T/H consists of a sampling capacitor and a switch to capture the input signal. The simplified diagram of this block is shown in Figure 11. At the beginning of the conversion, switch S1 is closed, and the input signal is tracked. The input signal is held (switch S1 opens) on the third falling edge of clock after CS and RD go low (Figure 12). This allows a minimum of two clock cycles for the input capacitor to be charged to the input voltage through the switch resistance. The time required for the hold capacitor to settle to ±1/4LSB is typically 7ns. Therefore, the input signal is allowed ample time to settle before it is acquired by the T/H. When a conversion ends, switch S1 closes, and the input signal is tracked.

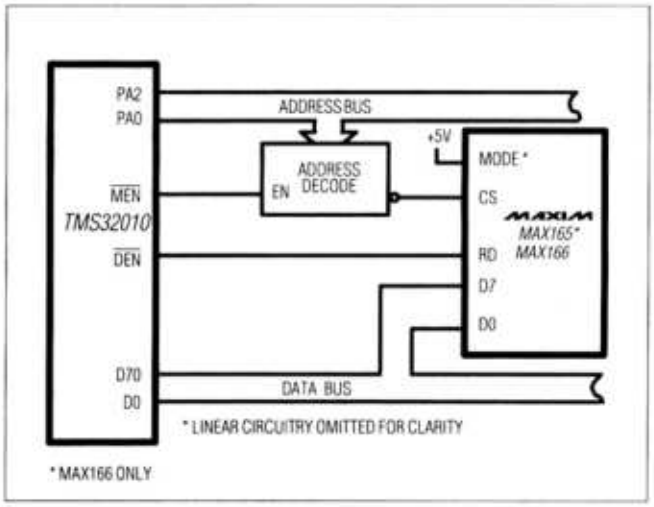


Figure 8. MAX165/MAX166 to TMS32010 ROM Interface

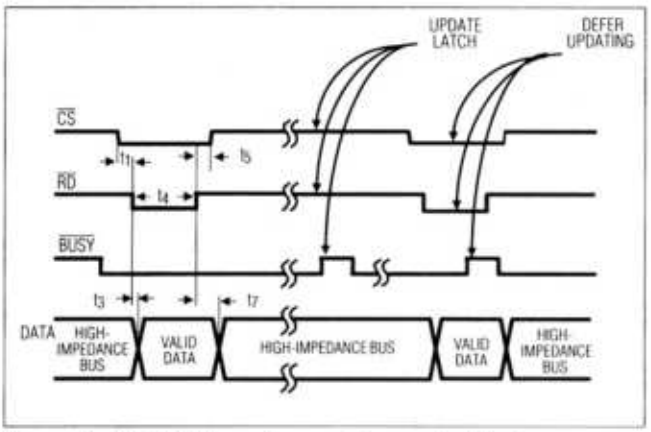


Figure 9. MAX166 Asynchronous-Conversion Mode Timing Diagram

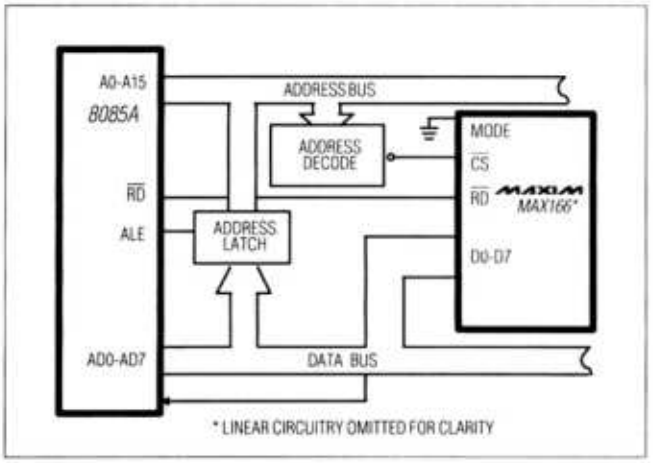


Figure 10. MAX166 to 8085A Asynchronous-Conversion Mode Interface

CMOS µP-Compatible 5µs, 8-Bit ADCs

The T/H can acquire signals with slew rates of up to 386mV/µs (or equivalently a 50kHz sine wave with $2.46V_{p-p}$ amplitude). Figure 13 shows the signal-to-noise ratio (SNR) versus input frequency for the ADC. The SNR plot is generated at a sampling rate of 200kHz using sinusoidal inputs with a $2.46V_{p-p}$ amplitude. The reconstructed sine wave is passed through a 50kHz, 8th-order Chebyshev filter. The improvement in SNR at high frequencies is due to the filter cutoff.

The switching nature of the analog input results in transient currents that charge the T/H's input capacitance. Keep the driving source impedance low (below 2kΩ) so the T/H's settling characteristics are not degraded. A low driving impedance also minimizes undesirable noise pick-up and reduces DC errors caused by transient currents at the analog input. As with any ADC, it is important to keep external noise sources to a minimum during a conversion. Keep the data bus as quiet as possible during a conversion, especially when the T/H is making a transition to hold mode.

Device accuracy may degrade slightly when conversion times are significantly longer than 5µs, as shown in Figure 14. This degradation is due to the charge that is lost from the hold capacacitor in the presence of small on-chip leakage currents.

Differential Input (MAX166)

The MAX166 converts differential inputs [(AIN+) - (AIN–)] in the 0V to 2VREF range. This can be especially useful in single-supply applications where the output swing requirements on the input amplifier are reduced. For example, if AIN- is tied to the reference output of the MAX166, the voltage swing on AIN+ must fall in the 1.23V to 3.69V range. Furthermore, the differential capability allows the converter to reject low-frequency common-mode signals.

The voltage at AIN+ is sampled at the beginning of the conversion and is referenced to AIN- during the conversion. Therefore, it is essential that the voltage on AIN- be relatively constant with respect to AGND during the conversion, otherwise conversion errors will result. If the AIN- input changes by a small voltage during the conversion, the conversion result can show an error in the same amount. For example, if the input has a 60Hz common-mode component of 0.5V with respect to AGND, an error of less than 0.1LSB is incurred during the 5µs conversion. Conversion errors increase with higher frequency or higher amplitude common-mode signals.

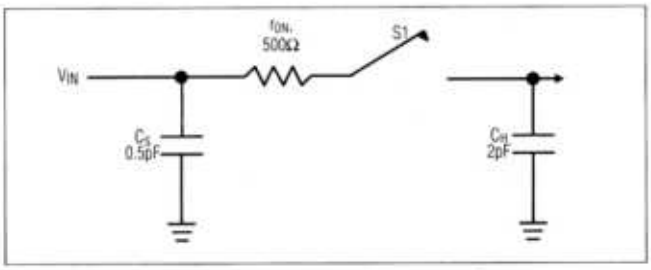


Figure 11. MAX165/MAX166 Equivalent Input Circuit

Reference Input

This ADC's high speed can be partially attributed to its DAC's "inverted-voltage output" topography. This topography provides low offset and gain errors and fast settling times. The input current to the DAC, however, is not constant. During a conversion, as different DAC codes are tried, the DAC's DC impedance can vary between 6kΩ and 18kΩ. Furthermore, when the DAC codes change, small amounts of transient current are drawn from the reference input. These characteristics require a low DC and AC driving impedance for the reference circuitry to minimize conversion errors.

Figure 15 shows the external reference circuitry recommended for driving the reference input of the MAX165/MAX166. The decoupling capacitors are necessary to provide a low AC source impedance.

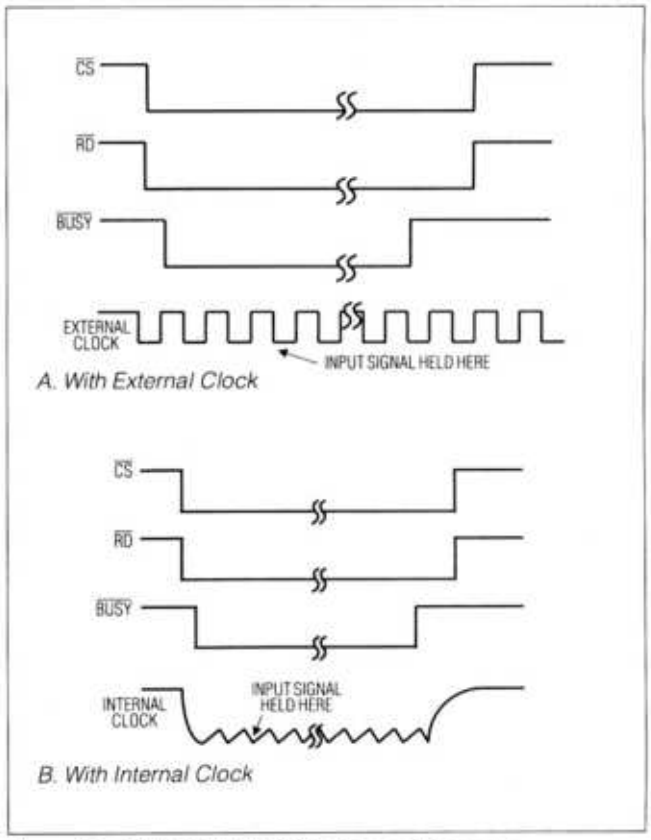


Figure 12. MAX165/MAX166 T/H Timing Diagrams (Slow-Memory Interface Mode)

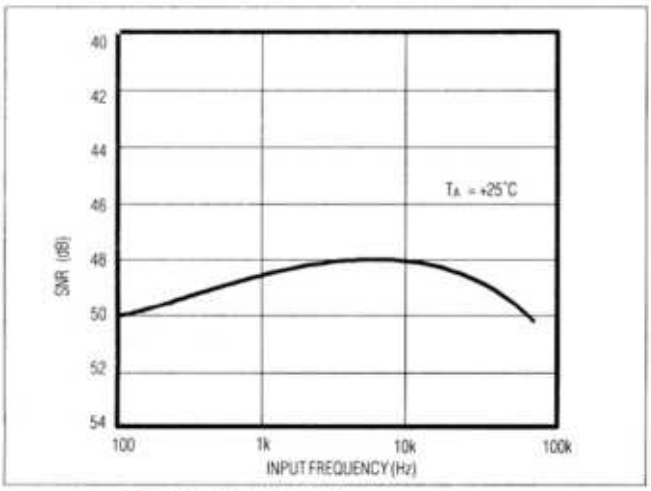


Figure 13. MAX165/MAX166 SNR vs. Input Frequency

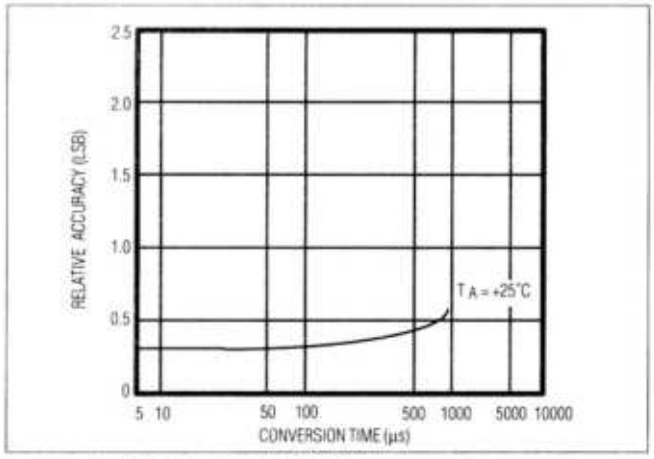


Figure 14. MAX165A/MAX166A Accuracy vs. Conversion Time

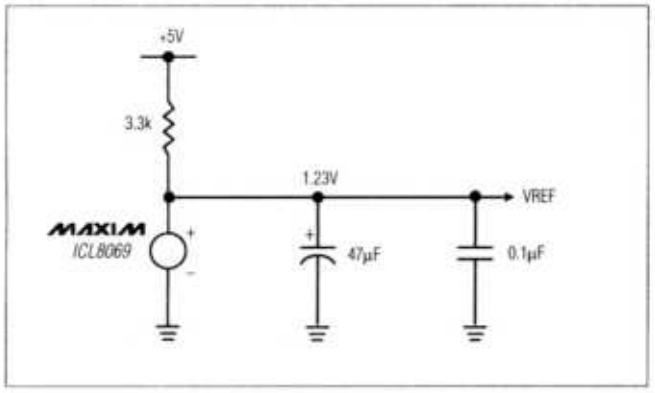


Figure 15. External Reference Circuit

Internal Reference

The MAX165/MAX166 have an internal 1.23V bandgap reference and buffer suitable for driving the reference input of the ADC. As discussed before, the reference input requires a low DC and AC driving impedance.

The reference buffer requires a 4.7µF low-ESR capacitor (tantalum or aluminum with additional 0.1µF ceramic) for compensation and to achieve low-AC impedance. If this capacitor is omitted, oscillations can occur on the REFOUT pin. If the user opts for an external reference, the REFOUT pin can be tied to V_{DD} to disable the internal reference.

Internal/External Clock

The MAX165/MAX166 can be run either with an externally applied clock or with their internal clock. In either case, the signal appearing at the clock pin is internally divided by two to provide an internal clock signal that is relatively insensitive to the input clock duty cycle. Therefore, a single conversion takes 20 input clock cycles, which corresponds to 10 internal clock cycles.

Internal Clock

The internal oscillator frequency is set by an external capacitor, C_{CLK}, and an external resistor, R_{CLK}, which are connected as shown in Figure 16a. During a conversion, a sawtooth waveform is generated on the CLK pin by charging C_{CLK} through R_{CLK} and discharging it through an internal switch. At the end of a conversion, the internal oscillator is shut down by clamping the CLK pin to V_{DD} through an internal switch. The circuit for the internal oscillator can be easily overdriven with an external clock source.

The internal oscillator provides a convenient clock source for the MAX165/MAX166. Typical conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 17. Due to process variations, the oscillation frequency for this R_{CLK}, C_{CLK} combination may vary by as much as ±50% from the nominal value shown in Figure 17. Therefore, an external clock should be used in the following situations:

1. Applications which require the conversion time to be within 50% of the minimum conversion time for the specified accuracy (5µs).
2. Applications in which time-related software constraints cannot accommodate conversion time differences, which may occur from unit to unit or over temperature for a given device.

External Clock

The CLK input of the MAX165/MAX166 may be driven directly by a 74HC or 4000B series buffer (e.g., 4049) or an LS TTL with a 5.6kΩ pullup resistor. At the end of a

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conversion, the device ignores the clock input and disables its internal clock signal. Therefore, the external clock may continue to run between conversions without being disabled. The duty cycle ratio of the external clock may vary from 70/30 to 30/70. As discussed previously, in order to maintain accuracy, clock rates significantly lower than the data sheet limits (4MHz) should not be used.

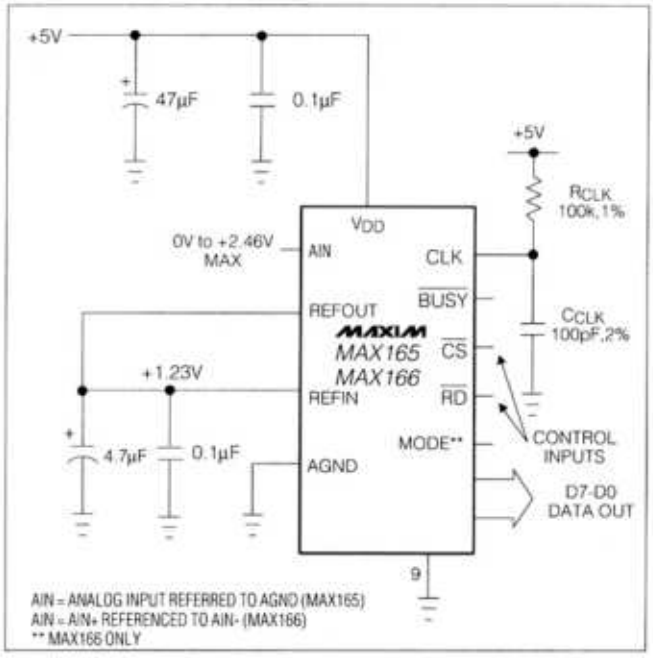


Figure 16a. MAX165/MAX166 Unipolar Configuration (Internal Reference)

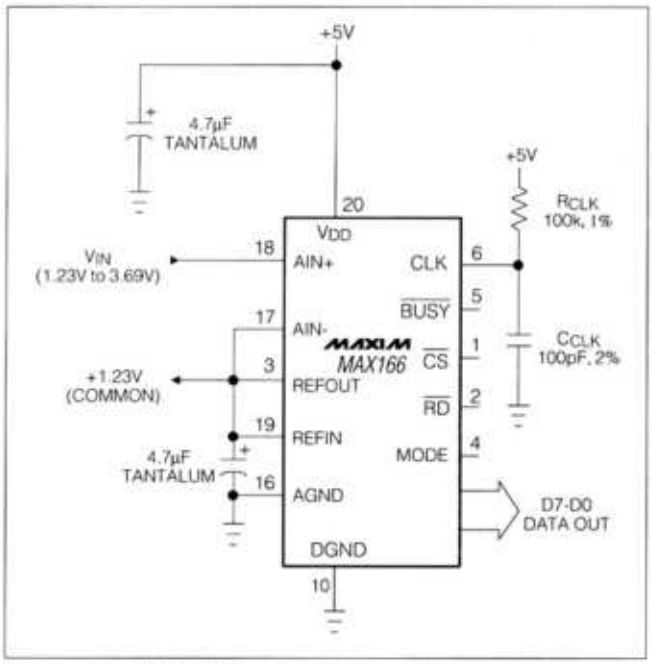


Figure 16b. MAX166 Unipolar Configuration

Applications Information

Unipolar Operation

Figures 16a and 16b show the analog circuit connections and nominal transfer characteristics (Figure 16c) for unipolar operation. Since the offset and full-scale errors of the MAX165/MAX166 are very small, it is not necessary to null these errors in most cases. If calibration is required, make adjustments as follows:

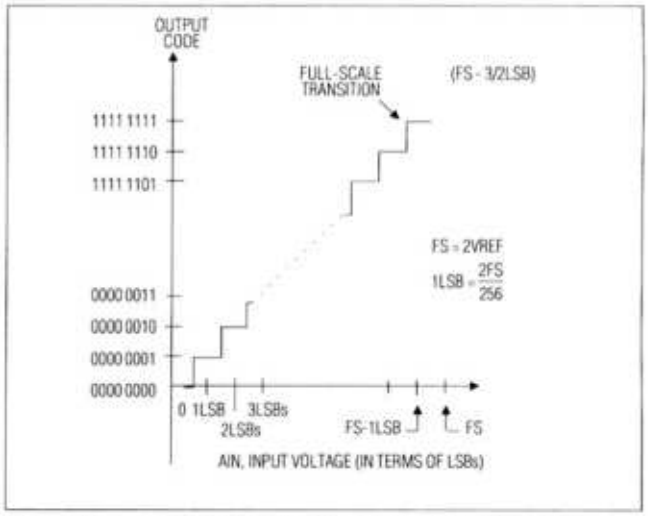


Figure 16c. Nominal Transfer Characteristic for Unipolar Operation

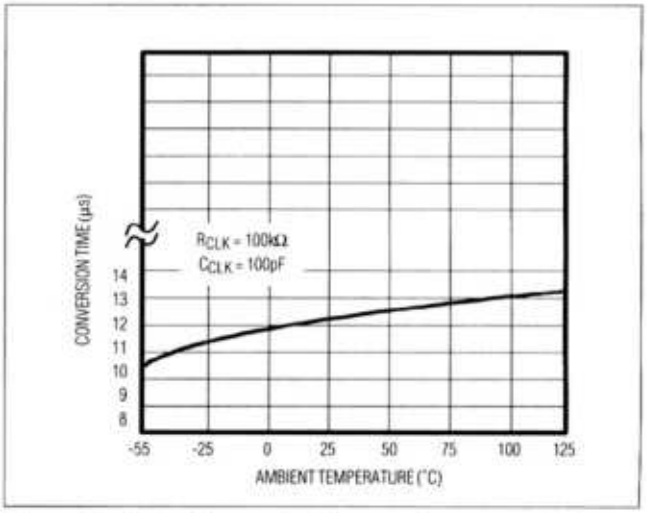


Figure 17. Typical Conversion Times vs. Temperature Using Internal Clock

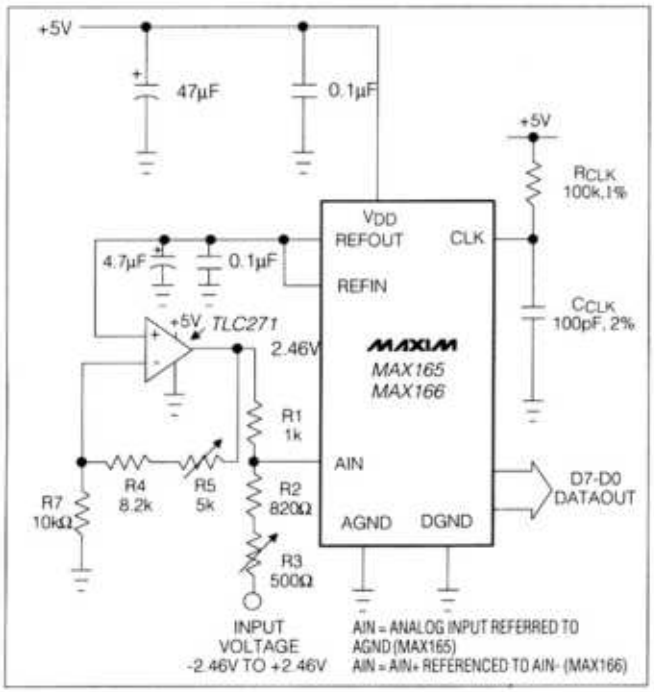


Figure 18a. MAX165/MAX166 Bipolar Configuration (Internal Reference)

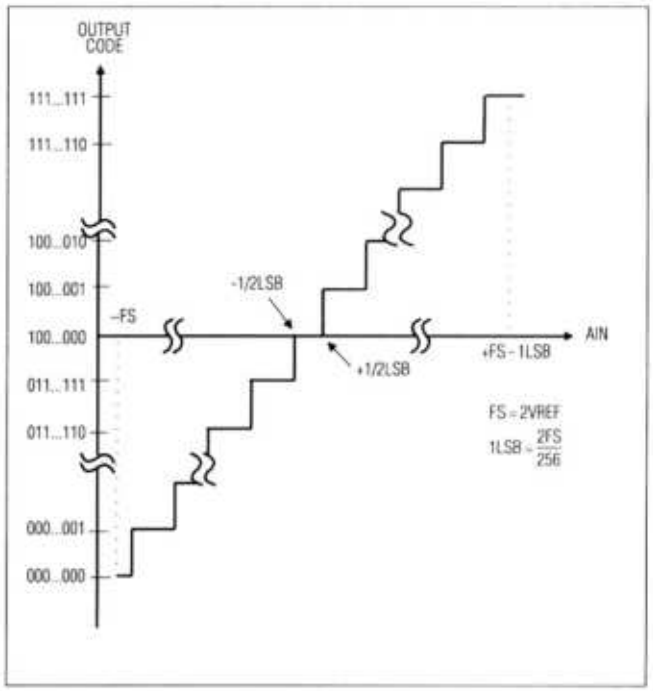


Figure 18b. Nominal Transfer Characteristic for Bipolar Operation

Offset Adjustment

The offset error can be easily adjusted using an op amp, as shown in Figure 18a. The op amp should have a common-mode input range that includes 0V. The op-amp input is initially set to +4.8mV (+1/2LSB), while its offset is varied until the ADC output code flickers between 0000 0000 and 0000 0001.

Full-Scale Adjustment

The full-scale adjustment is made by forcing the analog input, AIN, to +2.445V (FS - 3/2LSB). The reference input voltage is then varied until the ADC output code flickers between 1111 1110 and 1111 1111.

Bipolar Operation

Figure 18a shows an example of the circuit connections for bipolar operation and its nominal transfer characteristics (Figure 18B). The output code provided by the MAX165/MAX166 is offset binary. The analog input range for this circuit is ±2.46V (1LSB = 19.22mV), even though the voltage appearing at the AIN pin is in the 0V to +2.46V range. In most cases, the MAX165/MAX166's accuracy is high enough that calibration will not be neccesary. If calibration is not needed, resistors R1 through R7 should have a 0.1% tolerance, with R4 and R5 replaced by one 10kΩ resistor, and R2 and R3 with one 1kΩ resistor. If calibration is required, make adjustments as follows:

Offset Adjustment

Adjust the offset error by applying an analog input voltage of +2.43V (+FS - 3/2LSB). Resistor R5 is then adjusted until the output code flickers between 1111 1110 and 1111 1111.

Full-Scale Adjustment

The full-scale errors are nulled by applying an analog input voltage of -2.45V (-FS + 1/2LSB). Resistor R3 is then adjusted until the output code flickers between 0000 0000 and 0000 0001.

Noise

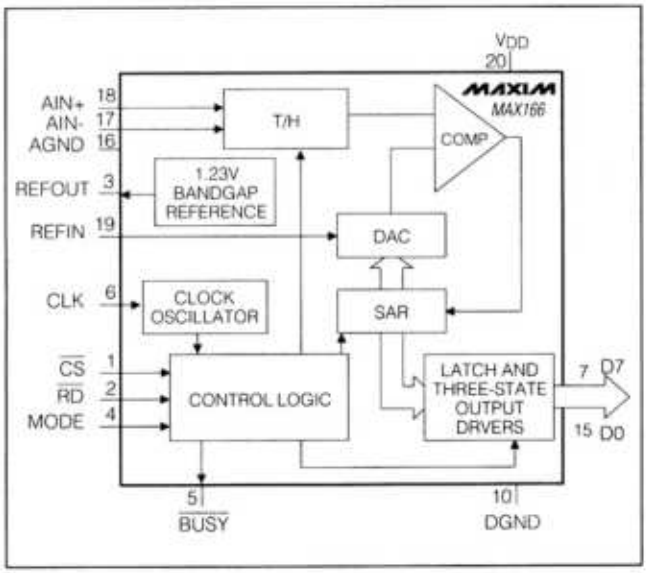
To minimize noise coupling, keep both the input signal lead to AIN and the signal return lead from AGND as short as possible. If this is not possible, a shielded cable or a twisted pair transmission line is recommended. Additionally, potential differences between the ADC ground and the signal source ground should be minimized since these voltage differences appear as errors super-imposed on the input signal. In order to minimize system noise pickup, the driving source resistance should be kept below 2kΩ.

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Proper Layout

For PC board layouts, take care to keep digital lines well separated from any analog lines. A single-point, analog ground, which is separate from the digital system ground, should be established near the MAX165/MAX166. Connect this analog ground point to the digital system ground through a single-track connection only. Any supply or reference bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point.

Functional Diagrams (continued)



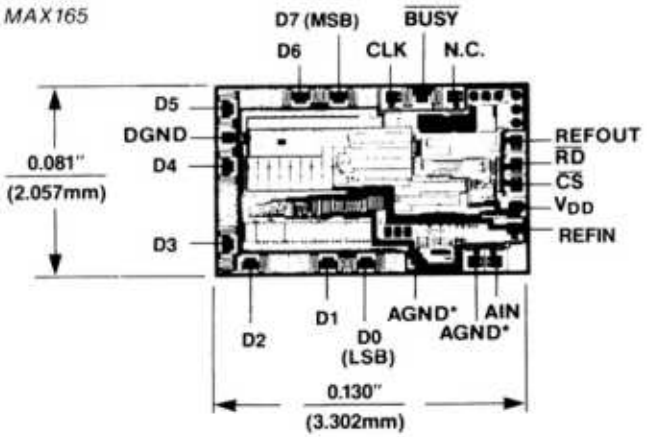
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX166ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX166BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX166CCPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX166DCPP	0°C to +70°C	20 Plastic DIP	±1
MAX166ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX166BCWP	0°C to +70°C	20 Wide SO	±1
MAX166CCWP	0°C to +70°C	20 Wide SO	±1/2
MAX166DCWP	0°C to +70°C	20 Wide SO	±1
MAX166BC/D	0°C to +70°C	Dice*	±1
MAX166DC/D	0°C to +70°C	Dice*	±1
MAX166AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX166BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX166CEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX166DEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX166AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX166BEWP	-40°C to +85°C	20 Wide SO	±1
MAX166CEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX166DEWP	-40°C to +85°C	20 Wide SO	±1
MAX166AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX166BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX166CMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX166DMJP	-55°C to +125°C	20 CERDIP**	±1

*Contact factory for dice specifications.
**Contact factory for availability processing to MIL-STD-883.

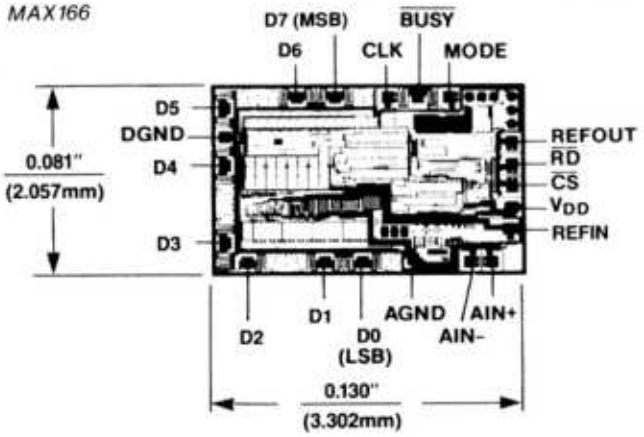
Chip Topographies

MAX165



*The two AGND pads must both be used (bonded together).

MAX166



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