EVALUATION KIT AVAILABLE

MAX16909

36V, 220kHz to 1MHz Step-Down Converter with Low Operating Current

General Description

The MAX16909 is a 3A, current-mode, step-down converter with an integrated high-side switch. The device is designed to operate with input voltages from 3.5V to 36V while using only 30µA quiescent current at no load. The switching frequency is adjustable from 220kHz to 1MHz by an external resistor and can be synchronized to an external clock. The output voltage is pin selectable to be 5V fixed or adjustable from 1V to 10V. The wide input voltage range along with its ability to operate at high duty cycle during undervoltage transients make the device ideal for automotive and industrial applications.

The device operates in skip mode for reduced current consumption in light-load applications. Protection features include overcurrent limit, overvoltage, and thermal shutdown with automatic recovery. The device also features a power-good monitor to ease power-supply sequencing.

The device operates over the -40°C to +125°C automotive temperature range, and is available in 16-pin TSSOP and TQFN (5mm x 5mm) packages with exposed pads.

Applications

Automotive

Industrial

High-Voltage Input DC-DC Converter

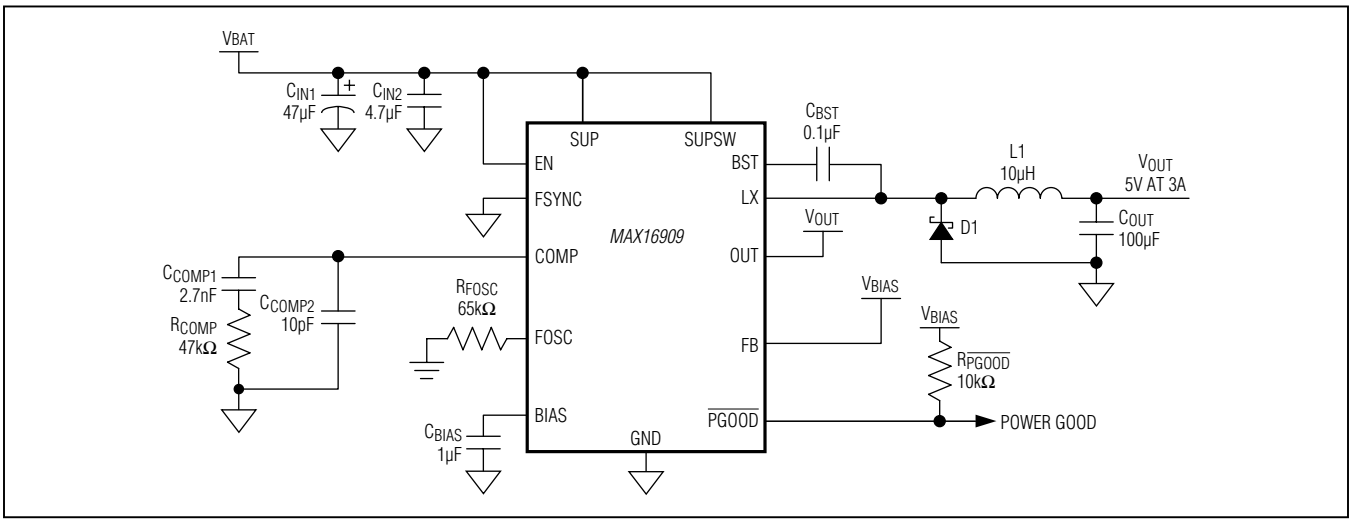
Point-of-Load Applications

Features

- **Wide 3.5V to 36V Input Voltage Range**
- **42V Input Transients Tolerance**
- **High Duty Cycle During Undervoltage Transients**
- **5V Fixed or 1V to 10V Adjustable Output Voltage**
- **Integrated 3A Internal High-Side (70mΩ typ) Switch**
- **Fast Load-Transient Response and Current-Mode Architecture**
- **Adjustable Switching Frequency (220kHz to 1MHz)**
- **Frequency Synchronization Input**
- **30µA Standby Mode Operating Current**
- **5µA Typical Shutdown Current**
- **Overvoltage, Undervoltage, Overtemperature, and Short-Circuit Protections**

Ordering Information appears at end of data sheet.

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5777; Rev 4; 1/17

ABSOLUTE MAXIMUM RATINGS

SUP, SUPSW, LX, EN to GND ..... -0.3V to +42V
SUP to SUPSW ..... -0.3V to +0.3V
BST to GND ..... -0.3V to +47V
BST to LX ..... -0.3V to +6V
OUT to GND ..... -0.3V to +12V
FOSC, COMP, BIAS, FSYNC, I.C., $\overline{PGOOD}$, FB to GND ..... -0.3V to +6V
LX Continuous RMS Current 4A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 26.1mW/°C above +70°C) 2088.8mW*
TQFN (derate 28.6mW/°C above +70°C) 2285.7mW*
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**As per the JEDEC 51 standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 35°C/W
Junction-to-Case Thermal Resistance(θ_{JC}) ..... 2.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, R_{FOSC} = 66.5kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}, V_{SUPSW}		3.5		36	V
Load-Dump Event Supply Voltage	V_{SUP_LD}	t_{LD} < 1s			42	V
Supply Current	I_{SUP}	I_{LOAD} = 1.5A		3.5		mA
	$I_{SUP_STANDBY}$	Standby mode, no load, V_{OUT} = 5V		30	60	µA
		Standby mode, no load, V_{OUT} = 5V, T_A = +25°C		30	45	
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		5	12	µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 36V	4.7	5	5.5	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.9	3.1	3.3	V
BIAS Undervoltage-Lockout Hysteresis				400		mV
Thermal-Shutdown Threshold				+175		°C
Thermal-Shutdown Threshold Hysteresis				15		°C
OUTPUT VOLTAGE (OUT)						
Output Voltage	V_{OUT}	V_{FB} = V_{BIAS}, normal operation	4.925	5	5.075	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, R_{FOSC} = 66.5kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Skip-Mode Output Voltage	V_{OUT_SKIP}	No load, V_{FB} = V_{BIAS}	4.925	5	5.15	V
Adjustable Output Voltage Range	V_{OUT_ADJ}	FB connected to external resistive divider	1		10	V
Load Regulation		V_{FB} = V_{BIAS}, 30mA < I_{LOAD} < 3A		0.5		%
Line Regulation		V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V		0.02		%/V
BST Input Current	I_{BST_ON}	High-side on, V_{BST} - V_{LX} = 5V		1.5	2.5	mA
LX Current Limit	I_{LX}	(Note 2)	3.4	4.1	6	A
Skip-Mode Threshold	I_{SKIP_TH}			300		mA
Power-Switch On-Resistance	R_{ON}	R_{ON} measured between SUPSW and LX, I_{LX} = 1A, V_{BIAS} = 5V		70	150	mΩ
High-Side Switch Leakage Current		V_{SUP} = 36V, V_{LX} = 0V, T_A = +25°C			1	µA
TRANSCONDUCTANCE AMPLIFIER (COMP)						
FB Input Current	I_{FB}			10		nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider; 0°C < T_A < +125°C	0.99	1.0	1.01	V
		-40°C < T_A < +125°C	0.985	1.0	1.015	
FB Line Regulation	ΔV_{LINE}	6V < V_{SUP} < 36V		0.02		%/V
Transconductance (from FB to COMP)	g_m	V_{FB} = 1V, V_{BIAS} = 5V (Note 2)		900		µS
Minimum On-Time	t_{ON_MIN}	(Note 2)		110		ns
Maximum Duty Cycle	DC_{MAX}	f_{SW} = 1MHz		98		%
		f_{SW} = 220kHz		99		
OSCILLATOR FREQUENCY						
Oscillator Frequency		R_{FOSC} = 66.5kΩ	360	400	444	kHz
EXTERNAL CLOCK INPUT (FSYNC)						
FSYNC Input Current		T_A = +25°C			1	µA
External Input Clock Acquisition Time	t_{FSYNC}			1		Cycles
External Input Clock Frequency		(Note 2)	f_{OSC} + 10%			Hz
External Input Clock High Threshold	V_{FSYNC_HI}	V_{FSYNC} rising	1.4			V
External Input Clock Low Threshold	V_{FSYNC_LO}	V_{FSYNC} falling			0.4	V
Soft-Start Time	t_{SS}			8.5		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, R_{FOSC} = 66.5kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

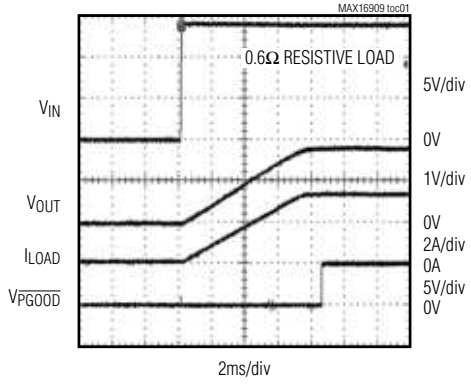
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUT (EN)						
Enable Input-High Threshold	V_{EN_HI}		2			V
Enable Input-Low Threshold	V_{EN_LO}				0.9	V
Enable Threshold Voltage Hysteresis	$V_{EN,HYS}$			0.2		V
Enable Input Current	I_{EN}	T_A = +25°C			1	µA
RESET						
Output Overvoltage Trip Threshold	V_{OUT_OV}		105	110	115	$\%V_{FB}$
$\overline{PGOOD}$ Switching Level	VTH_RISING	V_{FB} rising, $V_{\overline{PGOOD}}$ = high	93	95	97	$\%V_{FB}$
	$V_{TH_FALLING}$	V_{FB} falling, $V_{\overline{PGOOD}}$ = low	90	92.5	95	
$\overline{PGOOD}$ Debounce			10	35	60	µs
$\overline{PGOOD}$ Output Low Voltage		I_{SINK} = 5mA			0.4	V
$\overline{PGOOD}$ Leakage Current		V_{OUT} in regulation, T_A = +25°C			1	µA

Note 2: Guaranteed by design; not production tested.

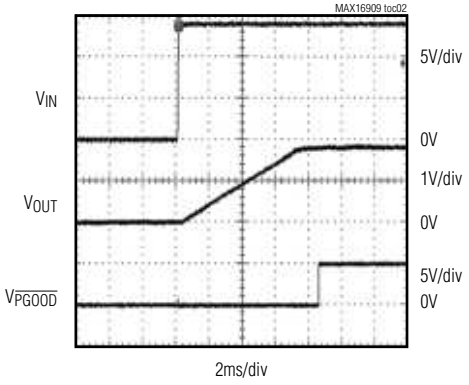
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, V_{OUT} = 1.8V, R1 = 80.6kΩ, R2 = 100kΩ, T_A = +25°C (Figure 4), unless otherwise noted.)

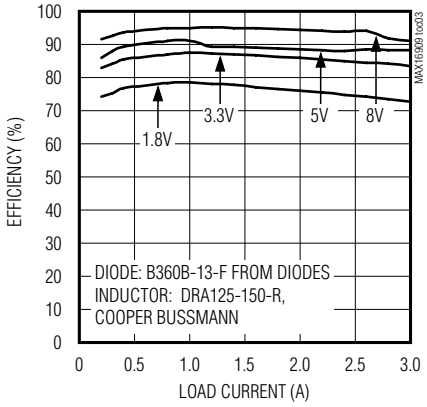
STARTUP INTO HEAVY LOAD (1.8V/400kHz)



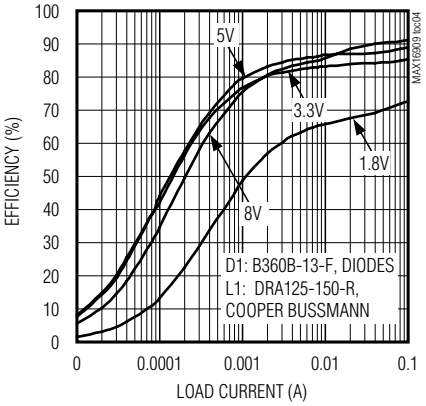
STARTUP INTO NO LOAD (1.8V/400kHz)



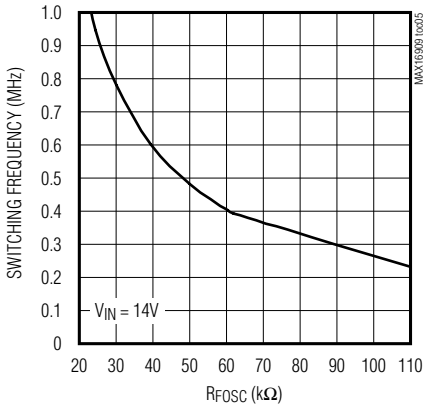
EFFICIENCY vs. LOAD CURRENT V_{IN} = 14V



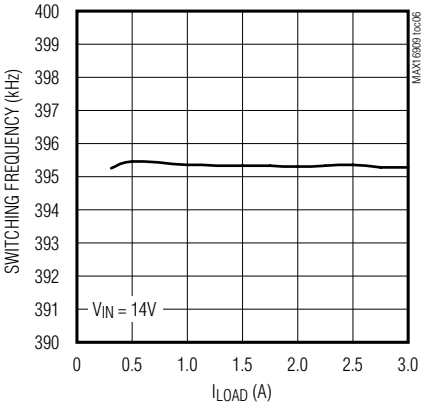
EFFICIENCY vs. LOAD CURRENT V_{IN} = 14V



SWITCHING FREQUENCY vs. R_{FOSC}



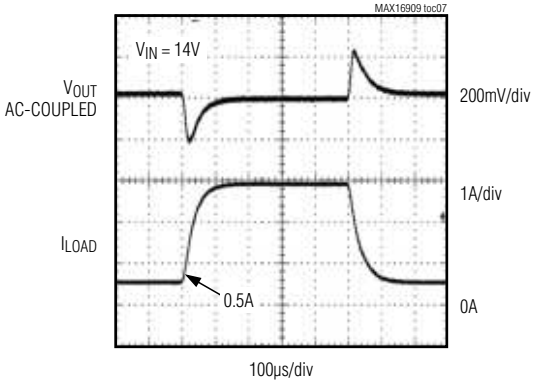
SWITCHING FREQUENCY vs. I_{LOAD} (1.8V/400kHz)



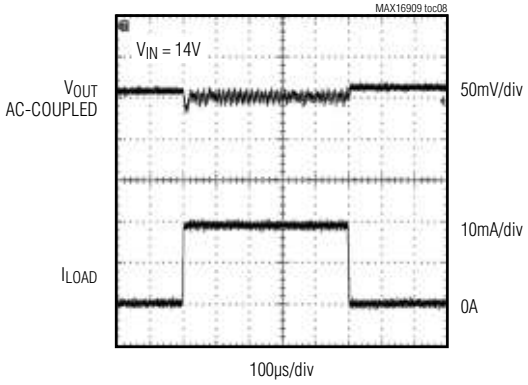
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, V_{OUT} = 1.8V, R1 = 80.6kΩ, R2 = 100kΩ, T_A = +25°C (Figure 4), unless otherwise noted.)

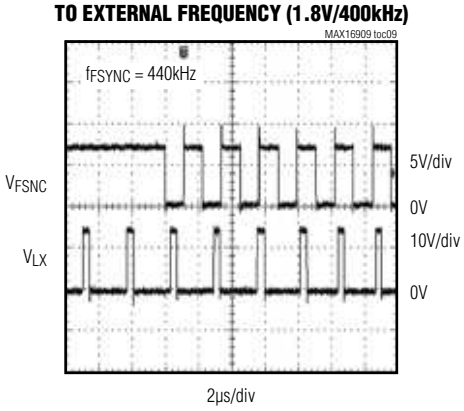
PWM MODE LOAD-TRANSIENT RESPONSE (1.8V/400kHz)



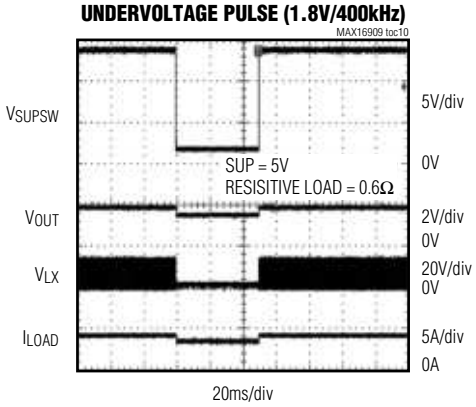
SKIP-MODE LOAD-TRANSIENT RESPONSE (1.8V/400kHz)



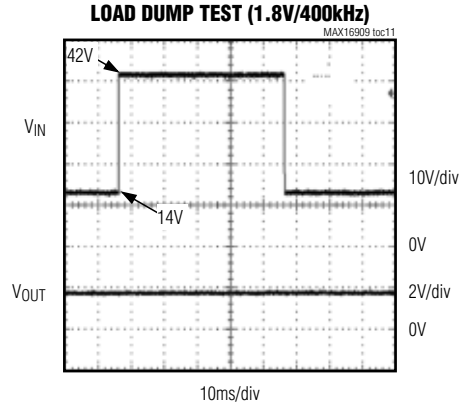
FSYNC TRANSITION FROM INTERNAL TO EXTERNAL FREQUENCY (1.8V/400kHz)



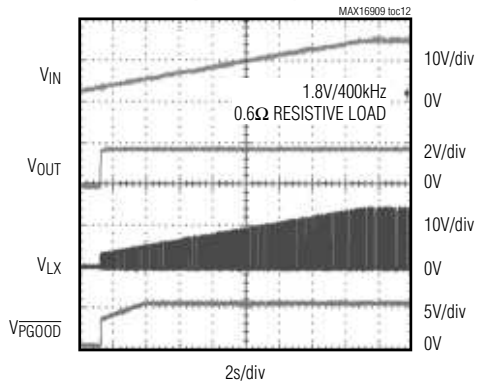
UNDERVOLTAGE PULSE (1.8V/400kHz)



LOAD DUMP TEST (1.8V/400kHz)



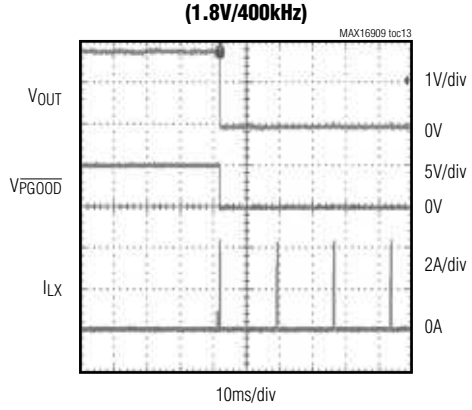
OUTPUT RESPONSE TO SLOW INPUT (ILOAD = 3A)



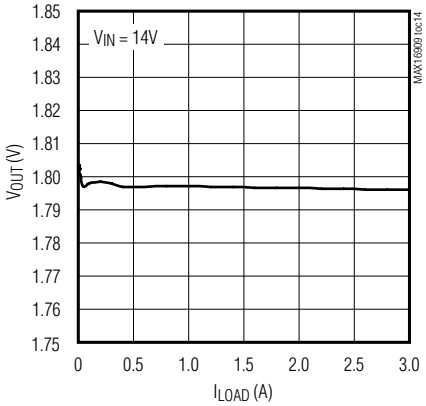
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, V_{OUT} = 1.8V, R1 = 80.6kΩ, R2 = 100kΩ, T_A = +25°C (Figure 4), unless otherwise noted.)

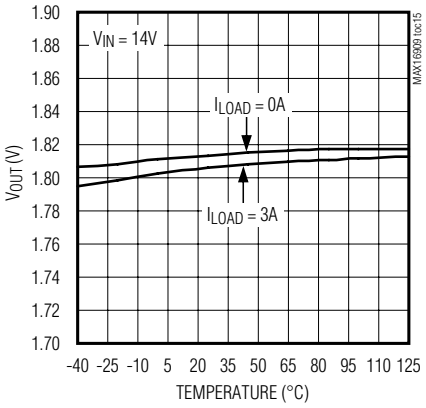
SHORT CIRCUIT TO GROUND TEST (1.8V/400kHz)



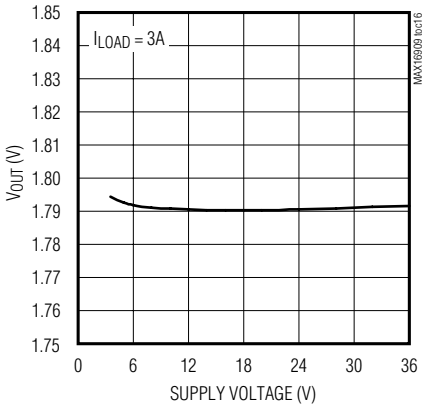
VOUT LOAD REGULATION (1.8V/400kHz)



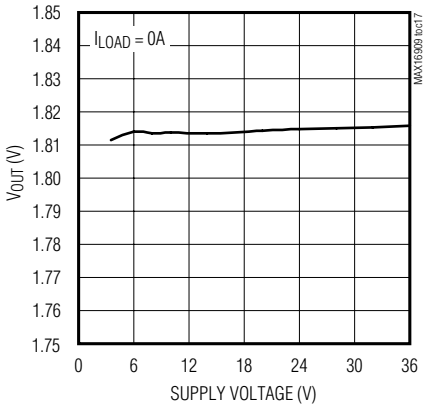
VOUT vs. TEMPERATURE (1.8V/400kHz)



VOUT vs. SUPPLY VOLTAGE (1.8V/400kHz)



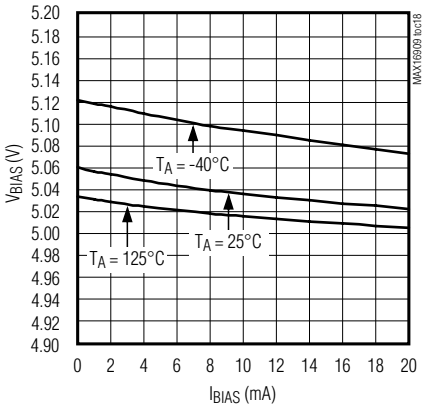
VOUT vs. SUPPLY VOLTAGE (1.8V/400kHz)



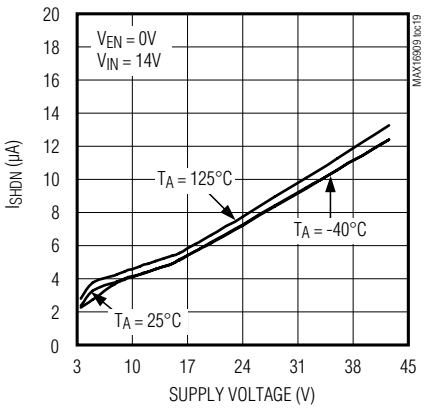
Typical Operating Characteristics (continued)

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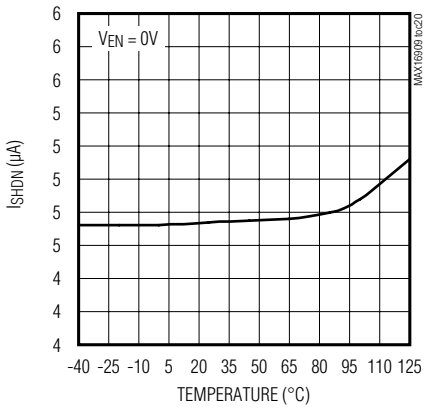
V_{BIAS} LOAD REGULATION (1.8V/400kHz)



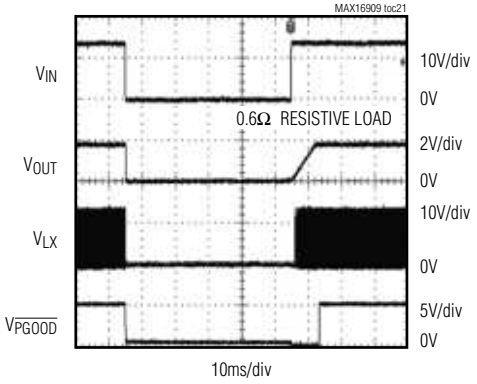
I_{SHDN} vs. SUPPLY VOLTAGE



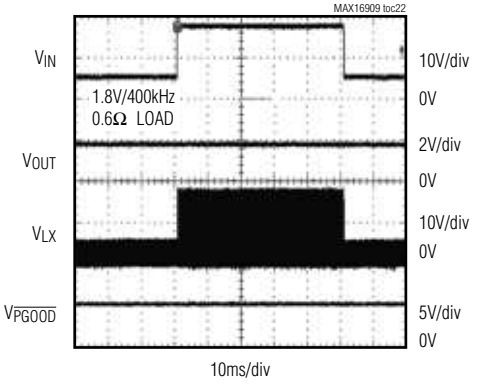
I_{SHDN} vs. TEMPERATURE



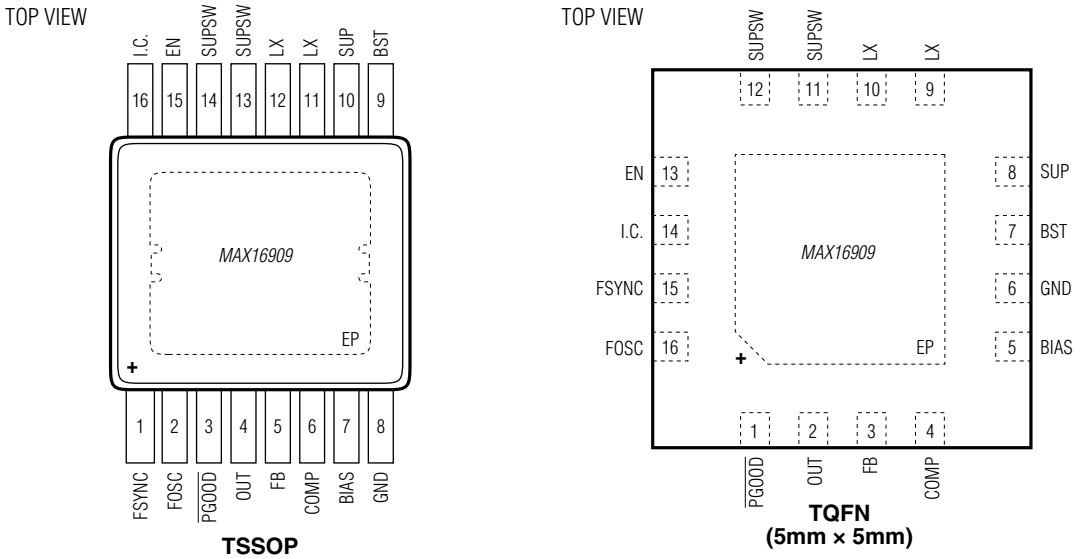
DIPS AND DROP TEST (1.8V/400kHz)



LINE TRANSIENT TEST (1.8V/400kHz)



Pin Configurations



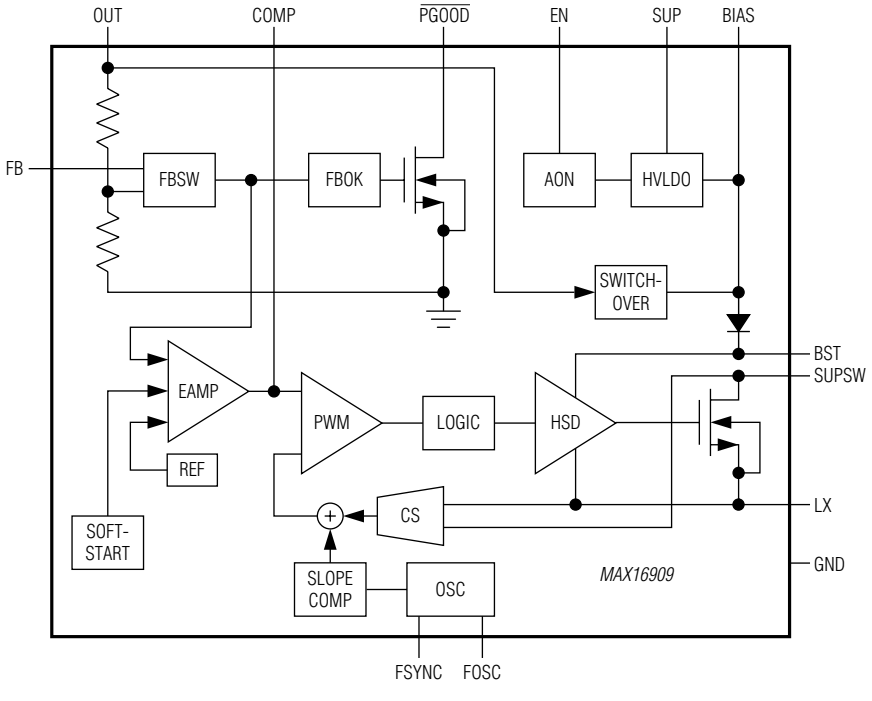
Pin Descriptions

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	15	FSYNC	Synchronization Input. The device synchronizes to an external signal applied to FSYNC. The external clock frequency must be 10% greater than the internal clock frequency for proper operation. Connect FSYNC to GND if the internal clock is used.
2	16	FOSC	Resistor-Programmable Switching-Frequency Setting Control Input. Connect a resistor from FOSC to GND to set the switching frequency.
3	1	$\overline{\text{PGOOD}}$	Open-Drain, Active-Low Output. $\overline{\text{PGOOD}}$ asserts when V_{OUT} is below the 92.5% regulation point. $\overline{\text{PGOOD}}$ deasserts when V_{OUT} is above the 95% regulation point.
4	2	OUT	Switch Regulator Output. OUT also provides power to the internal circuitry when the output voltage of the converter is set between 3V and 5V during standby mode.
5	3	FB	Feedback Input. Connect an external resistive divider from OUT to FB and GND to set the output voltage. Connect to BIAS to set the output voltage to 5V.
6	4	COMP	Error-Amplifier Output. Connect an RC network from COMP to GND for stable operation. See the *Compensation Network* section for more details.
7	5	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a 1µF capacitor to ground.
8	6	GND	Ground
9	7	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TSSOP	TQFN		
10	8	SUP	Voltage Supply Input. SUP powers up the internal linear regulator. Connect a minimum 4.7µF capacitor to ground.
11, 12	9, 10	LX	Inductor Switching Node. Connect a Schottky diode between LX and GND.
13, 14	11, 12	SUPSW	Internal High-Side Switch-Supply Input. SUPSW provides power to the internal switch. Connect a 0.1µF decoupling capacitor and a 4.7µF ceramic capacitor to ground.
15	13	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
16	14	I.C.	Internally Connected. Connect to ground for proper operation.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Internal Block Diagram



Detailed Description

The MAX16909 is a constant-frequency, current-mode, automotive buck converter with an integrated high-side switch. The device operates with input voltages from 3.5V to 36V and tolerates input transients from 3.5V up to 42V. During undervoltage events, such as cold-crank conditions, the internal pass device maintains 98% duty cycle.

The switching frequency is resistor programmable from 220kHz to 1MHz to allow optimization for efficiency, noise, and board space. A synchronization input FSYNC allows the device to synchronize to an external clock frequency.

During light-load conditions, the device enters skip mode for high efficiency. The 5V fixed output voltage eliminates the need for external resistors and reduces the supply current to 30µA. See the *Internal Block Diagram* for more information.

Wide Input Voltage Range (3.5V to 36V)

The device includes two separate supply inputs, SUP and SUPSW, specified for a wide 3.5V to 36V input voltage range. V_{SUP} provides power to the device and V_{SUPSW} provides power to the internal switch. When the device is operating with a 3.5V input supply, certain conditions such as cold crank can cause the voltage at SUPSW to drop below the programmed output voltage. As such, the device operates in a high duty-cycle mode to maintain output regulation.

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator, BIAS, that provides power to the internal circuitry. Connect a 1µF ceramic capacitor from BIAS to GND.

External Clock Input (FSYNC)

The device synchronizes to an external clock signal applied at FSYNC. The signal at FSYNC must have a 10% higher frequency than the internal clock frequency for proper synchronization.

Soft-Start

The device includes an 8.5ms fixed soft-start time for up to 500µF capacitive load with a 3A resistive load.

Minimum On-Time

The device features a 110ns minimum on-time that ensures proper operation at 1MHz switching frequency and high differential voltage between the input and the output. This feature is extremely beneficial in automotive applications where the board space is limited and the converter needs to maintain a well-regulated output voltage using an input voltage that varies from 9V to 18V. Additionally, the device incorporates an innovative design for fast-loop response that further ensures good output-voltage regulation during transients.

System Enable (EN)

An enable-control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.3V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the INH pin of a CAN transceiver.

EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout threshold, V_{UVL} = 3.15V (typ), the controller activates and the output voltage ramps up within 8.5ms.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5µA (typ). Drive EN high to bring the device out of shutdown.

Overvoltage Protection

The device includes overvoltage protection circuitry that protects the device when there is an overvoltage condition at the output. If the output voltage increases by more than 110% of its set voltage, the device stops switching. The device resumes regulation once the overvoltage condition is removed.

Fast Load-Transient Response

Current-mode buck converters include an integrator architecture and a load-line architecture. The integrator architecture has large loop gain but slow transient response. The load-line architecture has fast transient response but low loop gain. The device features an integrator architecture with innovative designs to improve transient response. Thus, the device delivers high output-voltage accuracy, plus the output can recover quickly from a transient overshoot, which could damage other on-board components during load transients.

Overload Protection

The overload protection circuitry is triggered when the device is in current limit and V_{OUT} is below the reset threshold. Under these conditions the device turns the high-side FET off for 16ms and re-enters soft-start. If the overload condition is still present, the device repeats the cycle.

Skip Mode/Standby Mode

During light-load operation the device enters skip mode operation. Skip mode turns off the majority of circuitry and allows the output to drop below regulation voltage before the switch is turned on again. The lower the load current, the longer it takes for the regulator to initiate a new cycle. Because the converter skips unnecessary cycles and turns off the majority of circuitry, the converter efficiency increases. When the high-side FET stops switching for more than 50µs, most of the internal circuitry, including LDO, draws power from V_{OUT} (V_{OUT} = 3V to 5.5V), allowing current consumption from the battery to drop to only 30µA.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +175°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down converter, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

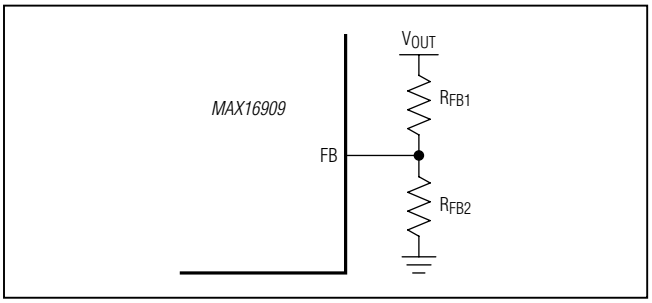


Figure 1. Adjustable Output-Voltage Setting

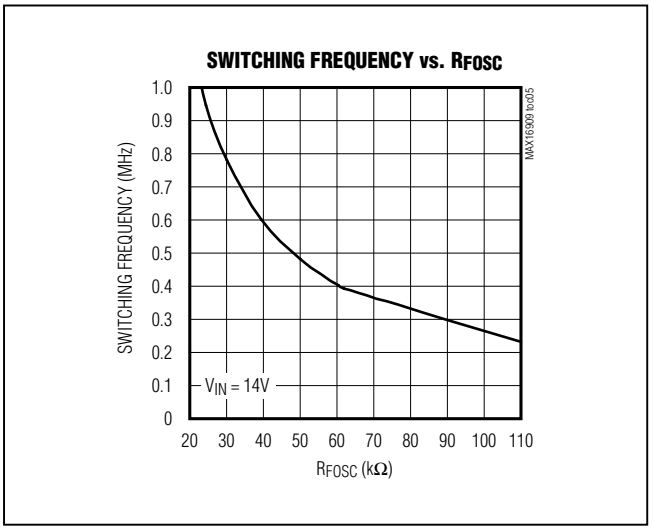


Figure 2. Switching Frequency vs. R_{FOSC}

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed 5V output voltage. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB to GND (Figure 1). Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1V (see the *Electrical Characteristics* table).

Internal Oscillator

The switching frequency, f_{SW}, is set by a resistor (R_{FOSC}) connected from FOSC to GND. See Figure 2 to select the correct R_{FOSC} value for the desired switching frequency. For example, a 400kHz switching frequency is set with R_{FOSC} = 65kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} f_{SW} I_{OUT} LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{FOSC} (see the *Internal Oscillator* section). The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient response requirements. Table 1 shows a comparison between small and large inductor sizes.

Table 1. Inductor Size Comparison

INDUCTOR SIZE	
SMALLER	**LARGER**
Lower price	Smaller ripple
Smaller form factor	Higher efficiency
Faster load response	Larger fixed-frequency range in skip mode

The inductor value must be chosen so that the maximum inductor current does not reach the device's minimum current limit. The optimum operating point is usually found between 25% and 35% ripple current. When pulse skipping (FSYNC low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in A, L is in H, and f_{SW} is in Hz.

Ferrite cores are often the best choices, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the equivalent series resistance (ESR) of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUPSW}}$$

where I_{OUT} is the maximum output current, and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple. So the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

Rectifier Selection

The device requires an external Schottky diode rectifier as a freewheeling diode. Connect this rectifier close to the device using short leads and short PCB traces. Choose a rectifier with a voltage rating greater than the maximum expected input voltage, V_{SUPSW}. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops.

Compensation Network

The device uses an internal transconductance error amplifier with its inverting input and its output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The device uses the voltage drop across the high-side MOSFET to sense inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. Only a simple single-series resistor (R_C) and capacitor (C_C) are required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (Figure 3). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to GND to cancel this ESR zero.

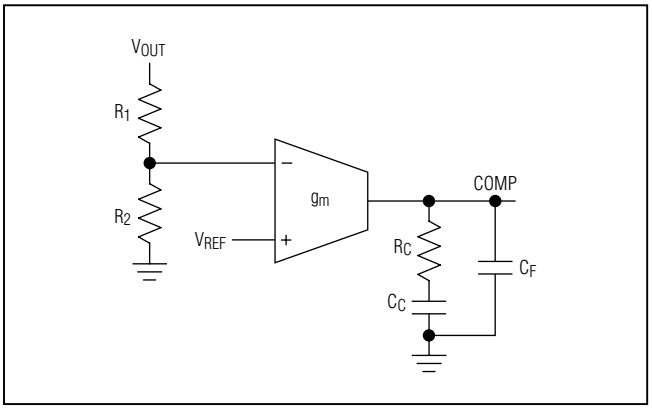


Figure 3. Compensation Network

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations allow to approximate the value for the gain of the power modulator ($GAIN_{MOD(DC)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the device.

$$GAIN_{MOD(DC)} = g_{mc} \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω, f_{SW} is the switching frequency in MHz, L is the output inductance in H, and g_{mc} = 3S.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times (R_{LOAD} + ESR)}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of “n” identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$ and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 900µS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)). Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}):

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(fC)} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} ($f_{zEA} = f_{pMOD}$) as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to GND. Set $f_{pEA} = f_{zMOD}$ and calculate C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

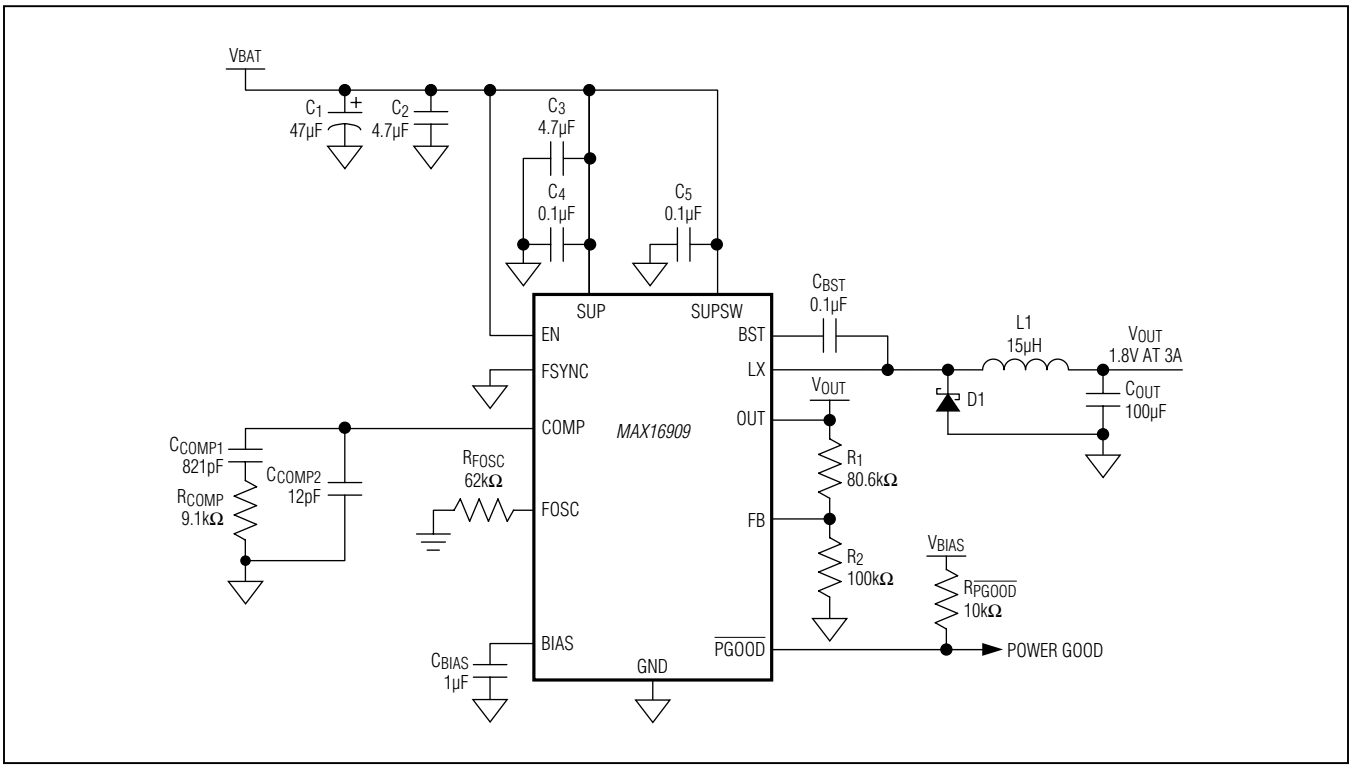


Figure 4. 1.8V/3A Configuration

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane for effective heat dissipation and for getting the full power out of the IC. Use multiple vias or a single large via in this plane for heat dissipation.
2) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path composed of input capacitor, high-side FET, inductor, and output capacitor should be as short as possible.
4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the IC.
6) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, enough isolation between analog return signals and high-power signals must be maintained.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16909RAUE+	-40°C to +125°C	16 TSSOP-EP*
MAX16909RAUE/V+	-40°C to +125°C	16 TSSOP-EP*
MAX16909RATE+	-40°C to +125°C	16 TQFN-EP*
MAX16909RATE/V+	-40°C to +125°C	16 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP-EP	U16E+3	21-0108	90-0120
16 TQFN-EP	T1655+4	21-0140	90-0121

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	9/11	Changed R_{FOSC} = 120kI to R_{FOSC} =66.5kI in the Electrical Characteristics globals and table; changed the min, typ, max values for R_{FOSC} from 190kHz (min), 220kHz (typ), 250kHz (max) to 360kHz (min), 400kHz (typ), 444kHz (max); changed the minimum on-time (t_{ON_MIN}) from 80ns (typ) to 110ns (typ); updated the $GAIN_{MOD(DC)}$ and f_{pMOD} equations; removed future status from the 16-pin TQFN package in the Ordering Information table	2, 3, 4, 11, 14, 17
2	8/12	Added two new OPNs in the Ordering Information table	17
3	10/14	Changed BIAS Regulator Voltage max limit in Electrical Characteristics	2
4	1/17	Changed Industrial/Military to Industrial in Applications section	1

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