MAX16961

3A, 2.2MHz, Synchronous Step-Down DC-DC Converter

General Description

The MAX16961 is a high-efficiency, synchronous step-down converter that operates with a 2.7V to 5.5V input voltage range and provides a 0.8V to 3.6V output voltage range. The wide input/output voltage range and the ability to provide up to 3A to load current make this device ideal for on-board point-of-load and post-regulation applications. The device achieves -3.7%/+2.6% output error over load, line, and temperature ranges.

The device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components. The optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions.

Integrated low R_{DSON} switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The device can be offered with factory-preset output voltages, or with an adjustable output voltage (contact factory for preset output-voltage options). Factory-preset output-voltage versions allow customers to achieve -3.7%/+2.6% output-voltage accuracy without using external resistors, while the adjustable output-voltage version provides the flexibility to set the output voltage to any desired value between 0.8V to 3.6V using an external resistive divider.

Additional features include 8ms soft-start, 16ms power-good output delay, overcurrent, and overtemperature protections.

The MAX16961 is available in thermally enhanced 16-pin TSSOP-EP and 16-pin (4mm x 4mm) TQFN-EP packages, and is specified for operation over the -40°C to +125°C automotive temperature range.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Small External Components**
  - ✧ **2.2MHz Operating Frequency**
- **Ideal for Point-of-Load Applications**
  - ✧ **3A Maximum Load Current**
  - ✧ **Adjustable Output Voltage: 0.8V to 3.6V**
  - ✧ **2.7V to 5.5V Operating Supply Voltage**
- **High Efficiency at Light Load**
  - ✧ **26µA Skip Mode Quiescent Current**
- **Minimizes Electromagnetic Interference**
  - ✧ **Programmable SYNC I/O Pin**
  - ✧ **Operates Above AM-Radio Band**
  - ✧ **Available Spread Spectrum**
- **Low Power Mode Saves Energy**
  - ✧ **1µA Shutdown Current**
- **Open-Drain Power-Good Output**
- **Limits Inrush Current During Startup**
  - ✧ **Soft-Start**
- **Overtemperature and Short-Circuit Protections**
- **16-Pin TSSOP-EP and 16-Pin (4mm x 4mm) TQFN-EP Packages**
- **-40°C to 125°C Operating Temperature Range**

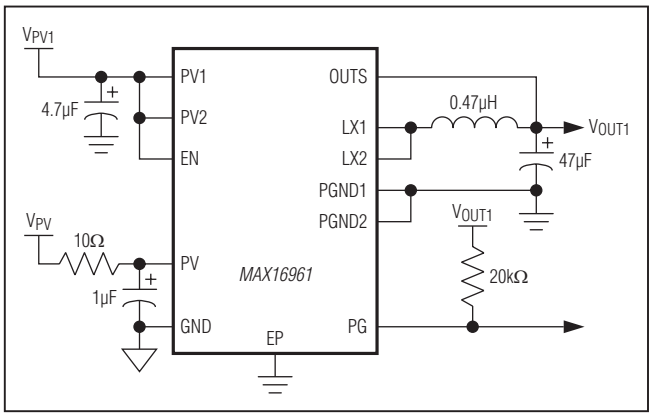
Applications

Automotive Infotainment

Point-of-Load Applications

Industrial/Military

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6520; Rev 5; 7/15

ABSOLUTE MAXIMUM RATINGS

PV, PV1, PV2 to GND .....-0.3V to +6V
EN, PG to GND .....-0.3V to +6V
PGND1 and PGND2 to GND .....-0.3V to +0.3V
LX1, LX2 Continuous RMS Current
(LX1 connected in Parallel with LX2).....4A
LX Current (LX1 connected in Parallel with LX2).....±6A (Note 5)
All Other Pins Voltages to GND .. (V_{PV} + 0.3V) to (V_{GND} - 0.3V)
Output Short-Circuit Duration.....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 25mW/°C above +70°C)..... 2000mW*
TSSOP (derate 26.1mW/°C above +70°C)..... 2088.8mW*
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**As per JEDEC51 Standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....6°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA})....38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{PV} = V_{PV1} = V_{PV2} = 5V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{PV}	Normal operation	2.7		5.5	V
Supply Current	I_{PV}	No load, V_{PWM} = 0V	12	26	45	µA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, T_A = +25°C		1	5	µA
Undervoltage-Lockout Threshold Low	V_{UVLO_L}		2.37			V
Undervoltage-Lockout Threshold High	V_{UVLO_H}				2.6	V
Undervoltage-Lockout Hysteresis				0.07		V
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
FB Regulation Voltage	V_{OUTS}			800		mV
Feedback Set-Point Accuracy	V_{OUTS}	I_{LOAD} = 4A	-3	0	+3	%
		I_{LOAD} = 0A	-0.5	+2	+3	
pMOS On-Resistance	R_{DSON_P}	V_{PV1} = 5V, $I_{LX_}$ = 0.4A, LX1 in parallel with LX2		34	55	mΩ
nMOS On-Resistance	R_{DSON_N}	V_{PV1} = 5V, $I_{LX_}$ = 0.8A, LX1 in parallel with LX2		25	45	mΩ
Maximum pMOS Current-Limit Threshold	I_{LIMP1}	LX1 and LX2 shorted together	3.9	5.1	6.3	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 5V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Current	I_{OUT}	(V_{OUT} + 0.5V ≤ V_{PV1} ≤ 5.5V) (Note 3)	3.3			A
OUTS Bias Current	I_{B_OUTS}	Fixed output voltage variants	1	2	5	µA
		Adjustable output version	-1		+1	
LX_ Leakage Current	I_{LX_LEAK}	$V_{PV_}$ = 5V, LX_ = PGND_ or PV_, T_A = +25°C	-1		+1	µA
Minimum On-Time	t_{ON_MIN}			60		ns
LX Discharge Resistance	R_{LX}	V_{EN} = 0V, through the OUTS pin	15	24	55	Ω
Maximum Short-Circuit Current					7.8	A
OSCILLATOR						
Oscillator Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Spread Spectrum	Δf/f	Spread spectrum enabled		+6		%
SYNC Input Frequency Range	f_{SYNC}	50% duty cycle (Note 4)	1.7		2.4	MHz
THERMAL OVERLOAD						
Thermal-Shutdown Threshold				+165		°C
Thermal-Shutdown Hysteresis				15		°C
POWER-GOOD OUTPUT (PG)						
PG Overvoltage Threshold	PG_{OVTH}	Percentage of nominal output	106	110	114	%
PG Undervoltage Threshold	PG_{UVTH}	Percentage of nominal output	90	92	94	%
PG Timeout Period				16		ms
Undervoltage-/Overvoltage-Propagation Delay				28		µs
Output High Leakage Current		T_A = +25°C			0.2	µA
PG Output Low Voltage		I_{SINK} = 3mA			0.4	V
		V_{PV} = 1.2V, I_{SINK} = 100µA			0.4	
ENABLE INPUTS (EN)						
Input Voltage High	V_{INH}	Input rising	2.4			V
Input Voltage Low	V_{INL}	Input falling			0.5	V
Input Hysteresis				0.85		V
Input Current		V_{EN} = high	0.1	1.0	2	µA
Pulldown Resistor		V_{EN} = low	50	100	200	kΩ
DIGITAL INPUTS (PWM, SYNC AS INPUT)						
Input Voltage High	V_{INH}		1.8			V
Input Voltage Low	V_{INL}				0.4	V
Input Voltage Hysteresis				50		mV
Pulldown Resistor			50	100	200	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 5V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

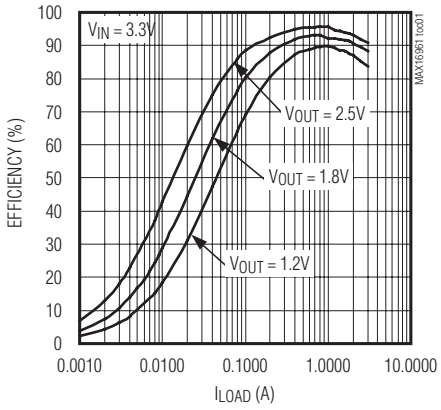
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (SYNC AS OUTPUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output-Voltage High	V_{OH}	V_{PV} = 5V, I_{SOURCE} = 3mA	4.2			V

Note 2: All limits are 100% production tested at +25°C. Limits over temperature are guaranteed by design.
Note 3: Calculated value based on an assumed inductor current ripple of 30%.
Note 4: For SYNC frequency outside (1.7, 2.4) MHz, contact factory.
Note 5: LX_ has internal clamp diodes to PGND_ and IN_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

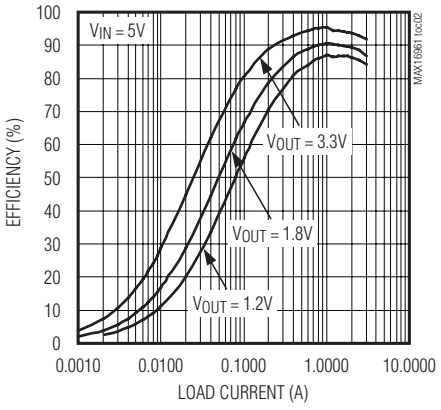
Typical Operating Characteristics

(V_{PV} = V_{PV1} = 5V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.)

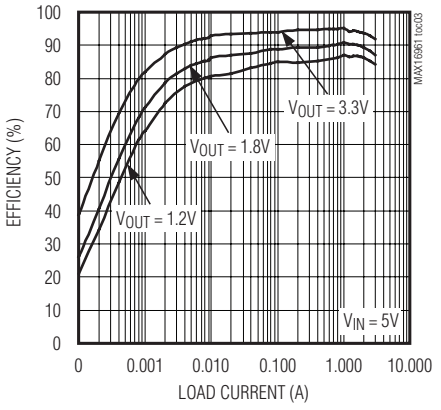
EFFICIENCY vs. LOAD CURRENT (PWM)



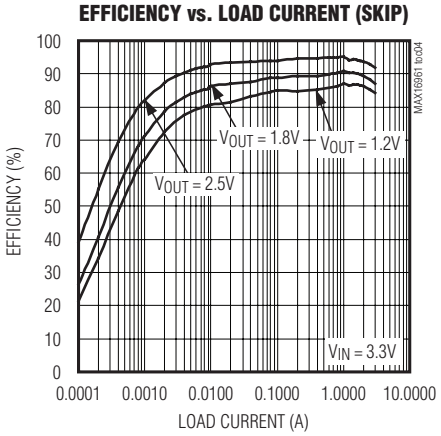
EFFICIENCY vs. LOAD CURRENT (PWM)



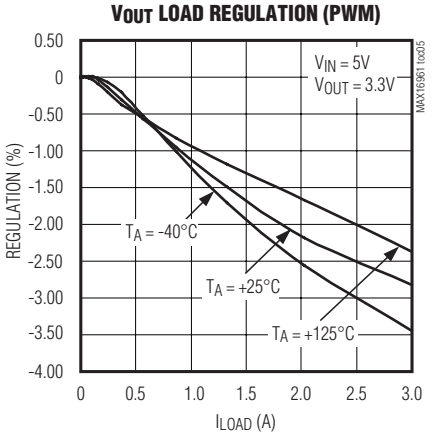
EFFICIENCY vs. LOAD CURRENT (SKIP)



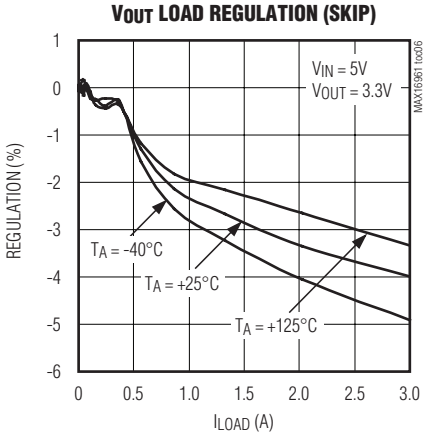
EFFICIENCY vs. LOAD CURRENT (SKIP)



VOUT LOAD REGULATION (PWM)



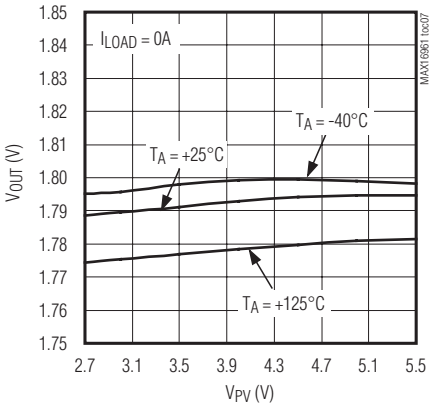
VOUT LOAD REGULATION (SKIP)



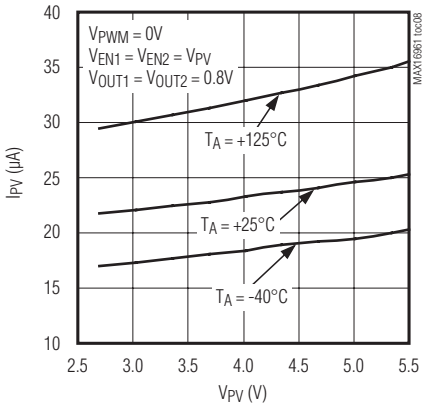
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

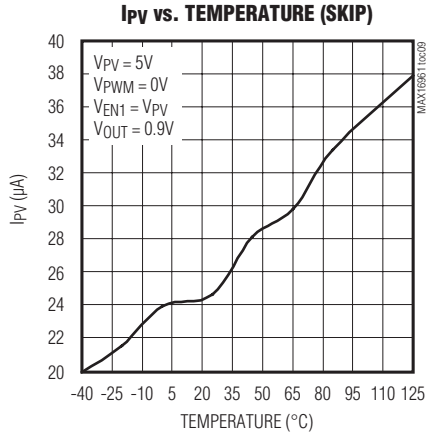
V_{OUT} vs. V_{PV} (PWM)



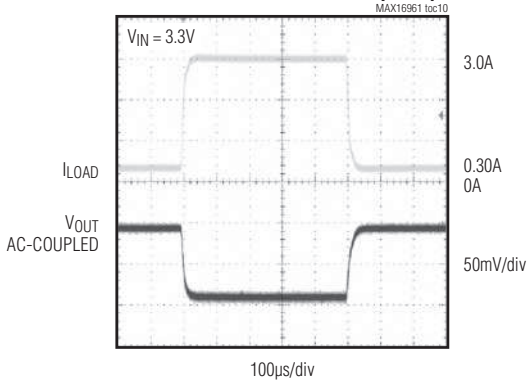
I_{PV} vs. V_{PV} (SKIP)



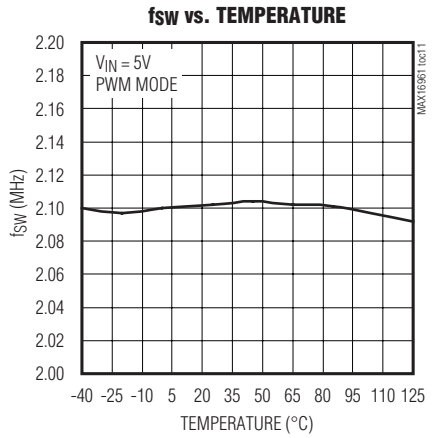
I_{PV} vs. TEMPERATURE (SKIP)



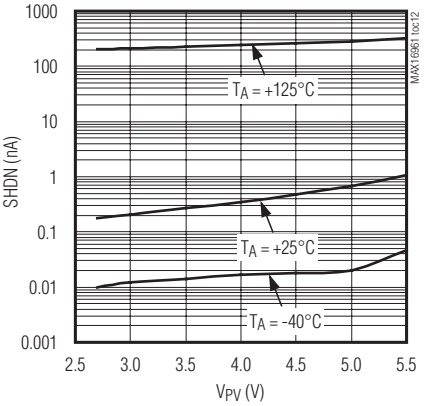
LOAD-TRANSIENT RESPONSE (PWM)



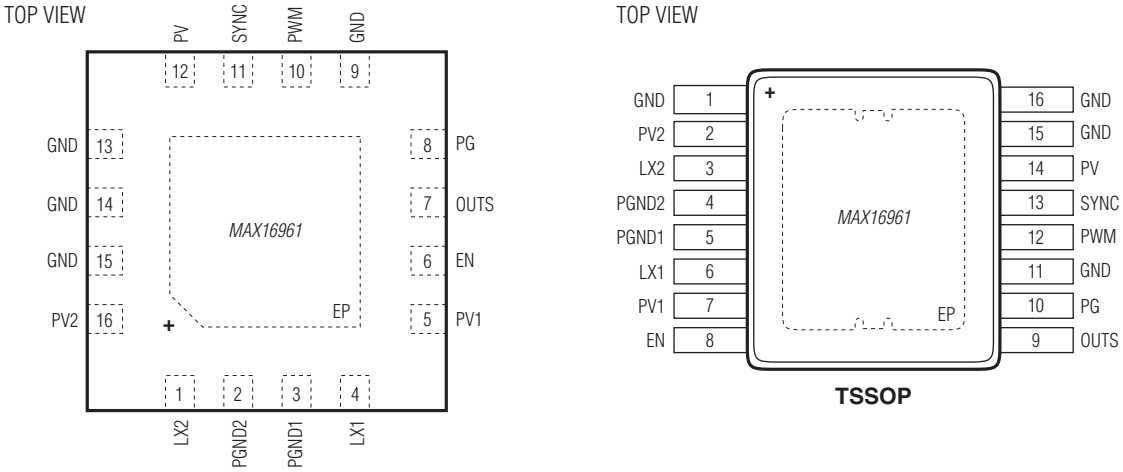
f_{SW} vs. TEMPERATURE



SHDN CURRENT vs. V_{PV}



Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	3	LX2	Switching Node 2. LX2 is high impedance when the converter is off.
2	4	PGND2	Power Ground 2
3	5	PGND1	Power Ground 1
4	6	LX1	Switching Node 1. LX1 is high impedance when the converter is off.
5	7	PV1	Input Supply 1. Bypass PV1 with at least a 4.7µF ceramic capacitor to PGND1. Connect PV1 to PV2 for normal operation.
6	8	EN	Enable Input. Drive EN high to enable the converter. Drive EN low to disable the converter.
7	9	OUTS	Feedback Input (Adjustable Output Option Only). Connect an external resistive divider from VOUT to OUTS and GND to set the output voltage. See Figure 2.
8	10	PG	Power-Good Output. Open-drain output. PG asserts when VOUT drops below 8% or rises above 10% of the nominal output voltage. Connect to a 20kΩ pullup resistor.
9, 13–15	1, 11, 15, 16	GND	Ground
10	12	PWM	PWM Control Input. Drive PWM high to put the converters in forced-PWM mode. Drive PWM low to put the converters in skip mode.
11	13	SYNC	Factory-Set Sync Input or Output. As an input, SYNC accepts a 1.7MHz to 2.4MHz external clock signal. As an output, SYNC outputs a 90° phase-shifted signal with respect to internal oscillator.

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
12	14	PV	Device Supply Voltage Input. Bypass with at least a 1µF ceramic capacitor to GND. In addition, connect a 10Ω decoupling resistor between PV and the bypass capacitor.
16	2	PV2	Input Supply 2. Bypass PV2 with at least a 4.7µF ceramic capacitor to PGND2. Connect PV2 to PV1 for normal operation.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use EP as the only IC ground connection. EP must be connected to GND.

Detailed Description

The MAX16961 is a high-efficiency, synchronous step-down converter that operates with a 2.7V to 5.5V input voltage range and provides a 0.8V to 3.6V output voltage range. The device delivers up to 3A of load current and achieves -3.7%/+2.6% output error over load, line, and temperature ranges.

The PWM input forces the device into either a fixed-frequency, 2.2MHz PWM mode or a low-power pulse-frequency modulation mode (skip). Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The factory-programmable synchronization I/O (SYNC) enables system synchronization.

Integrated low R_{DSON} switches help improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The device is offered with factory-preset output voltages that achieve -3.7%/+2.6% output-voltage accuracy without using external resistors. In addition, the output voltage can be set to any desired values between 0.8V to 3.6V using an external resistive divider with the adjustable option.

Additional features include 8ms soft-start, 16ms power-good delay output, overcurrent, and overtemperature protections. See Figure 1.

Power-Good Output (PG)

The device features an open-drain power-good output that asserts when the output voltage drops 8% below or rises 10% above the regulated voltage. PG remains asserted for a fixed 16ms timeout period after the output rises up to its regulated voltage. Connect PG to OUTS with a 20kΩ resistor.

Soft-Start

The device includes an 8ms fixed soft-start time. Soft-start time limits startup inrush current by forcing the output voltage to ramp up over time towards its regulation point.

Spread-Spectrum Option

The device featuring spread-spectrum (SS) operation varies the internal operating frequency up by SS = 6% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The internal oscillator is frequency modulated with a 6% frequency deviation. See the *Selector Guide* for available options.

Synchronization (SYNC)

SYNC is a factory-programmable I/O. See the *Selector Guide* for available options. When SYNC is configured as an input, a logic-high on PWM enables SYNC to accept signal frequency in the range of 1.7MHz < f_{SYNC} < 2.4MHz. When SYNC is configured as an output, a logic-high on PWM enables SYNC to output a 90° phase-shifted signal with respect to internal oscillator.

Current-Limit/Short-Circuit Protection

The device features current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET for minimum on-time period. This cycle repeats until the short or overload condition is removed.

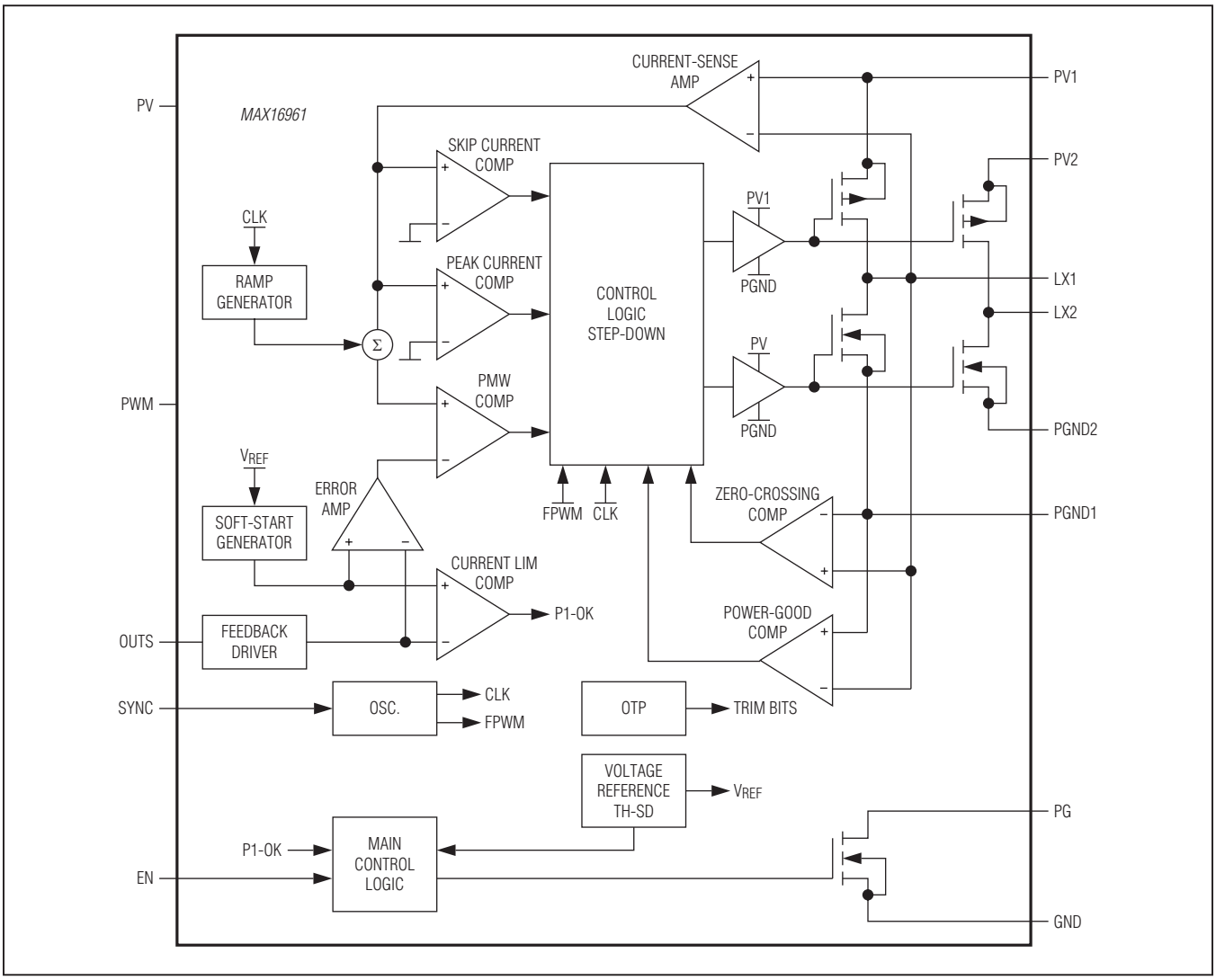


Figure 1. Internal Block Diagram

FPWM/Skip Modes

The device features an input (PWM) that puts the converter either in skip mode or forced-PWM (FPWM) mode of operation. See the *Pin Descriptions* section for mode details. In FPWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches the skip threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the FPWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converters to turn on the high-side switch only when needed to maintain regulation. As such, the converter does not switch MOSFETs on and off as often as is the case in the FPWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Table 1. Inductor Values vs. (V_{IN} - V_{OUT})

VIN - VOUT (V)	5.0 to 3.3	5.0 to 2.5	5.0 to 1.5	3.3 to 0.8
INDUCTOR (µH)	0.8	0.6	0.47	0.33

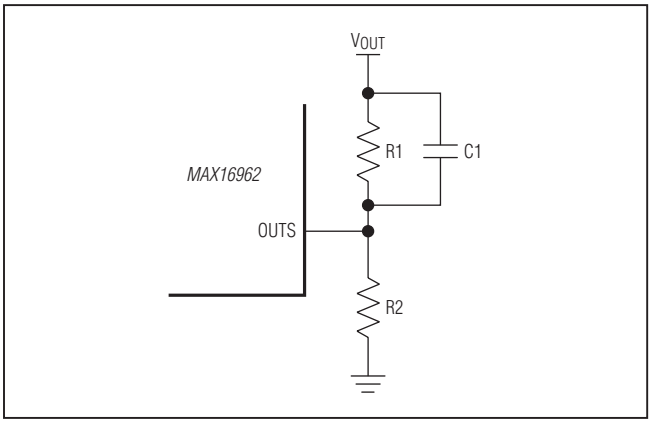


Figure 2. Adjustable Output Voltage Setting

Applications Information

Setting the Output Voltage

Connect OUTS to V_{OUT} for factory-programmed output voltage (see the *Selector Guide*). To set the output to other voltages between 0.8V and 3.6V, connect a resistive divider from output (V_{OUT}) to OUTS to GND (Figure 2). Select R2 (OUTS to GND resistor) less than or equal to 100kΩ. Calculate R1 (V_{OUT} to OUTS resistor) with the following equation:

$$R1 = R2\left[\left(\frac{V_{OUT}}{V_{OUTS}}\right) - 1\right]$$

$$\text{where } \frac{R1 \times R2}{R1 + R2} \le 7.5k\Omega$$

where V_{OUTS} = 800mV (see the *Electrical Characteristics* table).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across each resistor in the resistive-divider network. Use the following equation to determine the value of the capacitors:

$$C1 = 10pF\left(\frac{R2}{R1}\right)$$

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16961: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formulas to determine the minimum inductor value:

$$L_{MIN} = \left(V_{IN} - V_{OUT_}\right) \times \left(\frac{V_{OUT_}}{V_{IN}}\right) \times \frac{3}{f_{OP} \times 3A}$$

where f_{OP} is the operating frequency. This value is 2.2MHz unless externally synchronized to a different frequency.

The next equation ensures that the inductor current downslope is less than the internal slope compensation. For this to be the case, the following equation needs to be satisfied:

$$-m \ge \frac{m2}{2}$$

where m2 is the inductor current downslope:

$$\left[\frac{V_{OUT}}{L}\right]$$

and -m is the slope compensation:

$$\left[\frac{0.8 \times I_{MAX}}{\mu s}\right]$$

Solving for L:

$$L_{MIN2} = V_{OUT} \times \frac{\mu s}{1.6 \times 3A}$$

The equation that provides the bigger inductor value must be chosen for proper operation:

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is twice the chosen value from the above formula.

$$L_{MAX} = 2 \times L_{MIN}$$

The maximum inductor value must not exceed the calculated value from the above formula. This ensures that the current feedback loop receives the correct amount of current ripple for proper operation.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{PV1} - V_{OUT})}}{V_{PV1}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV1} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV1} - V_{OUT}) \times V_{OUT}}{V_{PV1} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{PV1}}$$

where I_{OUT} is the maximum output current, and D is the duty cycle.

It is strongly recommended that a 4.7µF small footprint be placed close to PV1 and PV2 and a minimum of 100nF small footprint be placed close to PV. Using a small footprint such as 0805 or smaller helps to reduce the total parasitic inductance.

Output Capacitor

The minimum capacitor required depends on output voltage, maximum device current capability, and the error-amplifier voltage gain. Use the following formula to determine the required output capacitor value:

$$C_{OUT(MIN)} = \frac{V_{REF} \times G_{EAMP}}{2\pi \times f_{CO} \times V_{OUT} \times R_{CS}}$$

$$= \frac{0.8V \times 31.7}{2\pi \times 210kHz \times V_{OUT} \times 167m\Omega}$$

where f_{CO}, the target crossover frequency, is 210kHz, G_{EAMP}, the error-amplifier voltage gain, is 31.7V/V, and R_{CS} is 167mΩ.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane for effective heat dissipation and maximizing the full power out of the device. Use multiple vias or a single large via in this plane for heat dissipation.
2) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Add small footprint blocking capacitors with low self-resonance frequency close to PV1, PV2, and PV.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path composed of input capacitors at PV1, PV2, inductor, and the output capacitor should be as short as possible.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.

6) OUTS is sensitive to noise for devices with external feedback option. The resistive network (R1 and R2) and the capacitive network (C1 and C2) must be placed close to OUTS and far away from the LX_ node and high switching current paths. The ground node of R2 and C2 must be close to GND.

7) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used enough isolation between analog return signals and high power signals must be maintained.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1644+4	21-0139	90-0070
16 TSSOP-EP	U16E+3	21-0108	90-0120

Selector Guide

ROOT PART	PACKAGE SUFFIX	OPTION SUFFIX	OUTPUT VOLTAGE	SPREAD SPECTRUM	SYNC IN/OUT
MAX16961	RAUE	A/V+	Ext. Adj.	Disabled	In
MAX16961	SAUE	A/V+	Ext. Adj.	Enabled	In
MAX16961	RATE	A/V+	Ext. Adj.	Disabled	In
MAX16961	SATE	A/V+	Ext. Adj.	Enabled	In

Note: *Contact the factory for variants with different output-voltage, spread-spectrum, and power-good delay time settings.*

Ordering Information

PART	TEMP RANGE	LOAD CURRENT CAPABILITY (A)	PIN-PACKAGE
MAX16961_ATE_/V+	-40°C to +125°C	4	16 TQFN-EP*
MAX16961_AUE_/V+	-40°C to +125°C	4	16 TSSOP-EP*

Note: *"_" is a package suffix placeholder for either "R" or "S", as shown in the Selector Guide. The 2nd "_" is in the option suffix.*
/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/12	Initial release	—
1	4/13	Added non-automotive parts to Selector Guide	11
2	9/13	Updated input voltage high min spec and input voltage low max spec, Figure 2, equation, step 6 in the *PCB Layout Guidelines* section, and the *Ordering Information*	3–5, 10, 11
3	5/14	Added FB regulation voltage specifications and updated V_{PV} condition in *Electrical Characteristics* table; corrected equations and updated Table 2 in the *Inductor Selection* and *Output Capacitor* sections; updated *Ordering Information*	2, 3, 9–11
4	6/15	Updated *General Description* section to make it clear that factory needs to be contacted for fixed output-voltage trim options	1
5	7/15	Added formula to equation in the *Setting the Output Voltage* section, replaced the *Output Capacitor* section, and deleted Table 2	9, 10
5.1		Corrected revision date	1

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