MAX16975

28V, 1.2A Automotive Step-Down Converter with Low Operating Current

General Description

The MAX16975 is a 1.2A current-mode step-down converter with an integrated high-side switch. The device operates with input voltages from 3.5V to 28V while using only 45µA quiescent current at no load. The switching frequency is adjustable from 220kHz to 1.0MHz by using an external resistor, and can be synchronized to an external clock. The device's output voltage is pin-selectable to a fixed 5V or adjustable from 1V to 10V using external resistors. The wide input voltage range makes the device ideal for automotive and industrial applications.

The device operates in skip mode for reduced current consumption in light-load conditions. An adjustable reset threshold helps keep microcontrollers alive down to the lowest specified input voltage. Protection features include cycle-by-cycle current limit, soft-start, overvoltage, and thermal shutdown with automatic recovery. The device also features a power-good monitor to ease power-supply sequencing.

The device is available in 16-pin QSOP and thermally enhanced QSOP-EP packages. It operates over the -40°C to +125°C automotive temperature range.

Ordering Information appears at end of data sheet.

Features

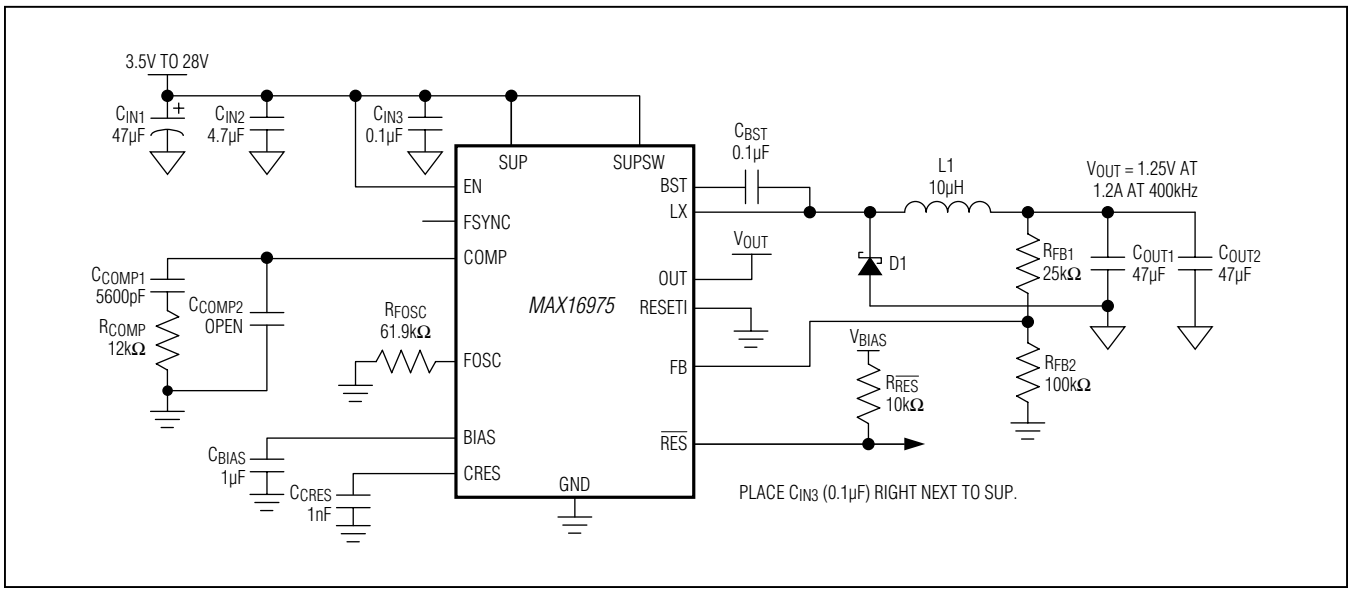
- **Wide 3.5V to 28V Input Voltage Range**
- **42V Input Transient Tolerance**
- **5V Fixed or 1V to 10V Adjustable Output Voltage**
- **Integrated 1.2A High-Side Switch**
- **220kHz to 1.0MHz Adjustable Switching Frequency**
- **Frequency Synchronization Input**
- **Internal Boost Diode**
- **45µA Skip-Mode Operating Current**
- **Less than 10µA Shutdown Current**
- **Adjustable Power-Good Output Level and Timing**
- **3.3V Logic Level to 42V Compatible Enable Input**
- **Current-Limit, Thermal Shutdown, and Overvoltage Protection**
- **-40°C to +125°C Automotive Temperature Range**

Applications

Automotive

Industrial

Typical Application Circuit



For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX16975.related**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5673; Rev 1; 10/13

ABSOLUTE MAXIMUM RATINGS

SUP, SUPSW, LX, EN to GND ..... -0.3V to +45V
BST to GND ..... -0.3V to +47V
BST to LX ..... -0.3V to +6V
OUT to GND ..... -0.3V to +12V
SUP to SUPSW ..... -0.3V to +0.3V
RESETI, FOSC, COMP, BIAS, FSYNC, CRES, $\overline{RES}$, FB to GND ..... -0.3V to +6V
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.6mW/°C above +70°C) 771.5mW
QSOP-EP (derate 22.7mW/°C above +70°C) 1818.20mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 103.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 37°C/W

QSOP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 44°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS*

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 22µH, C_{IN} = 4.7µF, C_{OUT} = 100µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}, V_{SUPSW}	Normal operation	3.5		28	V
Supply Current	I_{SUP}	Normal operation, no switching		2.9		mA
		Skip mode, no load, V_{OUT} = 5V		45		µA
Shutdown Supply Current		V_{EN} = 0V		9		µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 42V, V_{OUT} < 3V or V_{OUT} > 5.5V, I_{LOAD} = 0A (Note 2)	4.7	5.0	5.3	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.95	3.15	3.35	V
BIAS Undervoltage Hysteresis				550		mV
Thermal-Shutdown Threshold				+175		°C
Thermal-Shutdown Threshold Hysteresis				+15		°C
OUTPUT VOLTAGE (OUT)						
Output Voltage	V_{OUT}	Normal operation, V_{FB} = V_{BIAS}, I_{LOAD} = 1A, T_A = +25°C	4.95	5	5.05	V
		Normal operation, V_{FB} = V_{BIAS}, I_{LOAD} = 1A, -40°C ≤ T_A ≤ +125°C	4.9	5	5.1	
Skip-Mode Output Voltage	V_{OUT_SKIP}	No load, V_{FB} = V_{BIAS} (Note 3)	4.9	5.05	5.2	V
Load Regulation		V_{OUT} = 5V, V_{FB} = V_{BIAS}, 30mA < I_{LOAD} < 1A		0.3		%
Line Regulation		6V < V_{SUP} < 28V		0.02		%/V

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

ELECTRICAL CHARACTERISTICS* (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 22µH, C_{IN} = 4.7µF, C_{OUT} = 100µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BST Input Current	I_{BST}	V_{BST} - V_{LX} = 5V		1.7	2.5	mA
LX Current Limit	I_{LX}	V_{SUP} = 4.5V to 28V, V_{SUPSW} = 14V, T_A = +25°C	1.5	1.8	2.0	A
		V_{SUP} = 4.5V to 28V, V_{SUPSW} = 14V	1.5	1.8		
Skip-Mode Current Threshold	I_{SKIP_TH}			200		mA
Power-Switch On-Resistance	R_{ON}	R_{ON} measured between SUPSW and LX, I_{LX} = 1A, V_{SUP} = 4.5V to 28V, V_{BST} - V_{LX} = 4.5V		300	550	mΩ
LX Leakage Current	$I_{LX,LEAK}$	V_{SUPSW} = 28V, V_{LX} = 0V, T_A = +25°C		0.01	1	µA
TRANSCONDUCTANCE AMPLIFIER (COMP)						
FB Input Current	I_{FB}			20		nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider, T_A = +25°C	0.99	1.0	1.01	V
		FB connected to an external resistive divider, -40°C ≤ T_A ≤ +125°C	0.985	1.0	1.015	
FB Line Regulation	ΔV_{LINE}	4.5V < V_{SUP} < 28V		0.02		%/V
Transconductance (from FB to COMP)	g_m	V_{FB} = 1V, V_{BIAS} = 5V		1000		µS
Minimum On-Time	t_{ON}			110		ns
Cold-Crank Event Duty Cycle	DC_{CC}			94		%
OSCILLATOR FREQUENCY						
Oscillator Frequency		R_{FOSC} = 25.5kΩ, V_{SUP} = 4.5V to 28V		1.0		MHz
		R_{FOSC} = 61.9kΩ, V_{SUP} = 4.5V to 28V	348	400	452	kHz
		R_{FOSC} = 120kΩ, V_{SUP} = 4.5V to 28V (Note 3)	191	220	249	kHz
Oscillator Frequency Range	f_{OSC}	(Note 3)	220		1000	kHz
EXTERNAL CLOCK INPUT (FSYNC)						
External Input Clock Acquisition Time	t_{FSYNC}			1		Cycles
External Input Clock Frequency		(Note 3)	f_{OSC} + 10%			Hz
External Input Clock High Threshold	V_{FSYNC_HI}	V_{FSYNC} rising	1.4			V
External Input Clock Low Threshold	V_{FSYNC_LO}	V_{FSYNC} falling			0.4	V
FSYNC Pulldown Resistance	R_{FSYNC}			500		kΩ
Soft-Start Time	t_{SS}	f_{SW} = 400kHz		4		ms
		f_{SW} = 1.0MHz		1.6		ms
ENABLE INPUT (EN)						
Enable On Threshold Voltage Low	V_{EN_LO}				0.8	V

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

ELECTRICAL CHARACTERISTICS* (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 22µH, C_{IN} = 4.7µF, C_{OUT} = 100µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Enable On Threshold Voltage High	V_{EN_HI}			2.2			V
Enable Threshold Voltage Hysteresis	$V_{EN,HYS}$				0.2		V
Enable Input Current	I_{EN}				10		nA
RESET							
Reset Internal Switching Level	V_{TH_RISING}	V_{FB} rising, V_{RESETI} = 0V		93	95	96.5	%V_{FB}
	$V_{TH_FALLING}$	V_{FB} falling, V_{RESETI} = 0V		91	93	95	
RESETI Threshold Voltage	V_{RESETI_HI}	V_{RESETI} falling		1.05	1.25	1.4	V
CRES Threshold Voltage	V_{CRES_HI}	V_{CRES} rising		1.07	1.13	1.19	V
CRES Threshold Hysteresis	V_{CRES_HYS}				0.05		V
RESETI Input Current	I_{RESET}	V_{RESETI} = 0V			0.02		µA
CRES Source Current	I_{CRES}	V_{OUT} in regulation		9.5	10	10.5	µA
CRES Pulldown Current	I_{CRES_PD}	V_{OUT} out of regulation		1			mA
$\overline{RES}$ Output Low Voltage		I_{SINK} = 5mA				0.4	V
$\overline{RES}$ Leakage Current (Open-Drain Output)		V_{OUT} in regulation	T_A = +25°C			1	µA
			T_A = +125°C		20		nA
Reset Debounce Time	t_{RES_DEB}	V_{RESETI} falling			25		µs

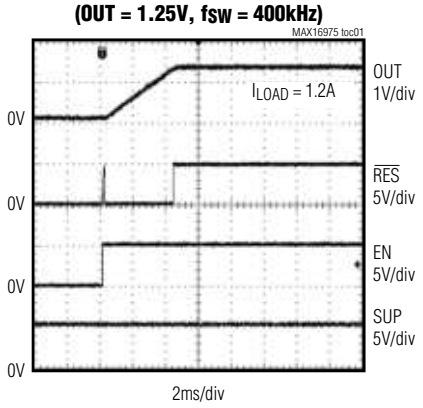
Note 2: When 3V < V_{OUT} < 5.5V, the bias regulator is connected to the output to save quiescent current, V_{BIAS} = V_{OUT}.
Note 3: Guaranteed by design; not production tested.

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

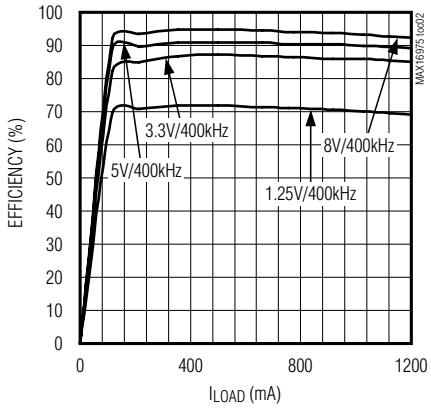
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 4.7µH, C_{IN} = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = +25°C, unless otherwise noted.)

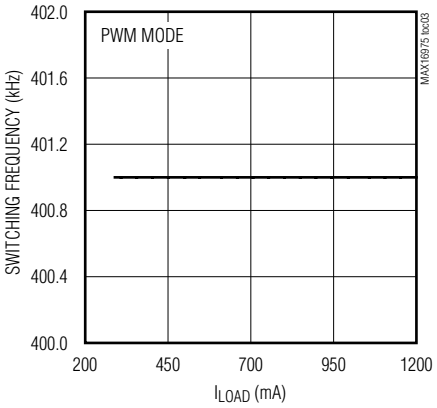
STARTUP WITH FULL LOAD (OUT = 1.25V, f_{SW} = 400kHz)



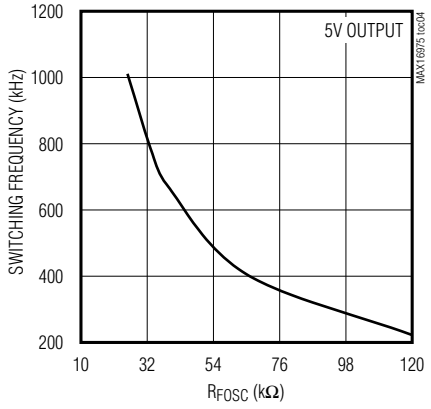
EFFICIENCY vs. LOAD CURRENT



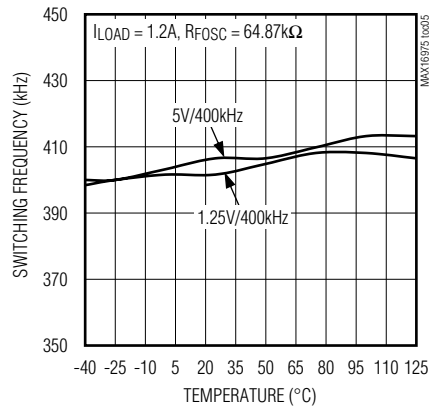
SWITCHING FREQUENCY vs. LOAD CURRENT (1.25V/400kHz)



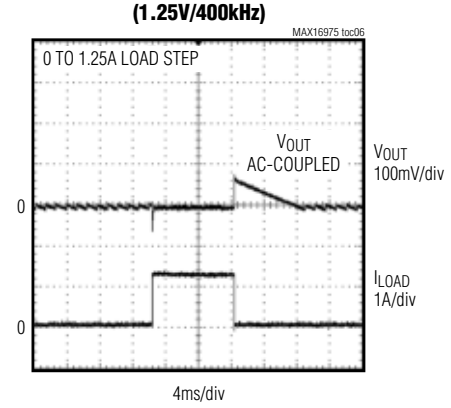
SWITCHING FREQUENCY vs. R_{FOSC}



SWITCHING FREQUENCY vs. TEMPERATURE (1.25V/400kHz, 5V/400kHz)



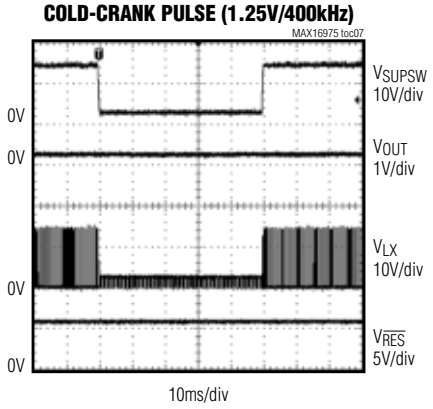
LOAD-STEP RESPONSE (1.25V/400kHz)



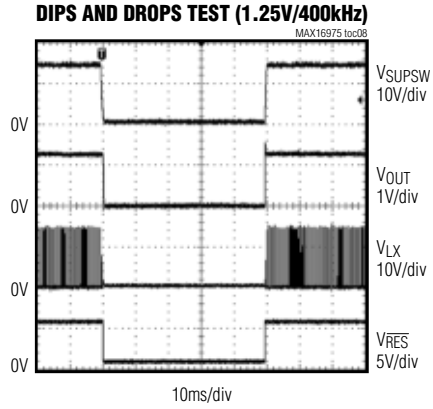
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 4.7µH, C_{IN} = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = +25°C, unless otherwise noted.)

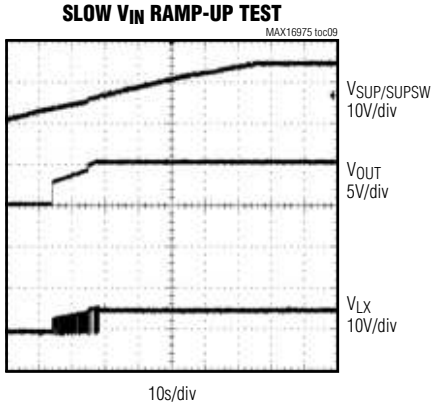
COLD-CRANK PULSE (1.25V/400kHz)



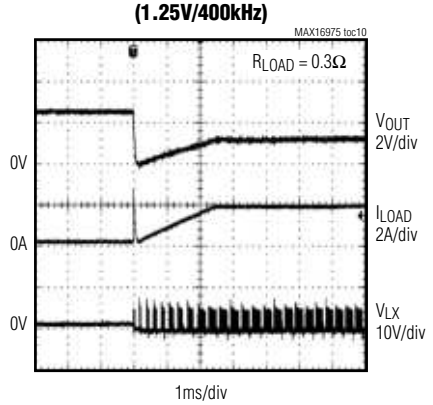
DIPS AND DROPS TEST (1.25V/400kHz)



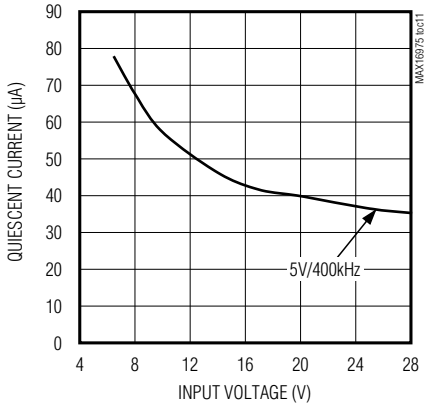
SLOW V_{IN} RAMP-UP TEST



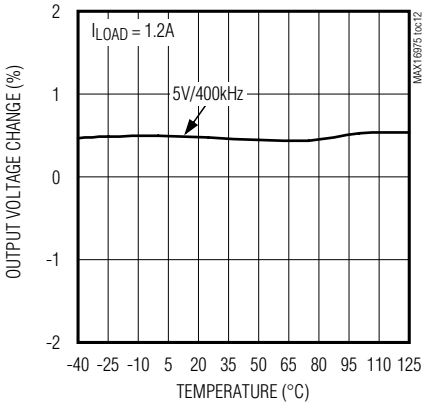
OUTPUT SHORT-CIRCUIT TEST (1.25V/400kHz)



QUIESCENT CURRENT vs. INPUT VOLTAGE



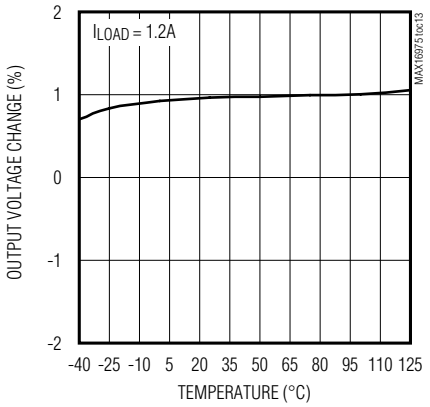
V_{OUT} vs. TEMPERATURE IN PWM MODE (5V/400kHz)



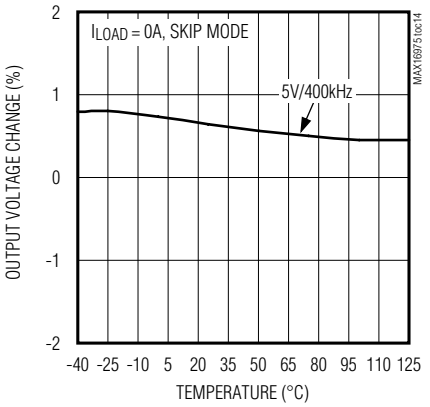
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 4.7µH, C_{IN} = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 61.9kΩ, T_A = +25°C, unless otherwise noted.)

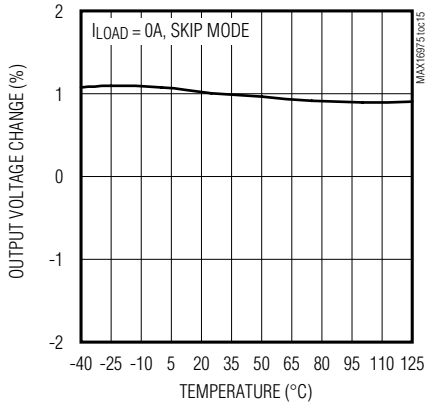
V_{OUT} vs. TEMPERATURE IN PWM MODE (1.25V/400kHz)



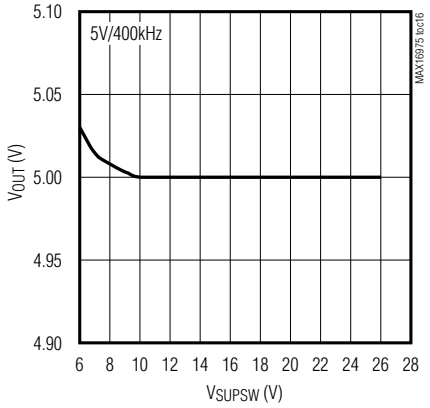
V_{OUT} vs. TEMPERATURE IN SKIP MODE (5V/400kHz)



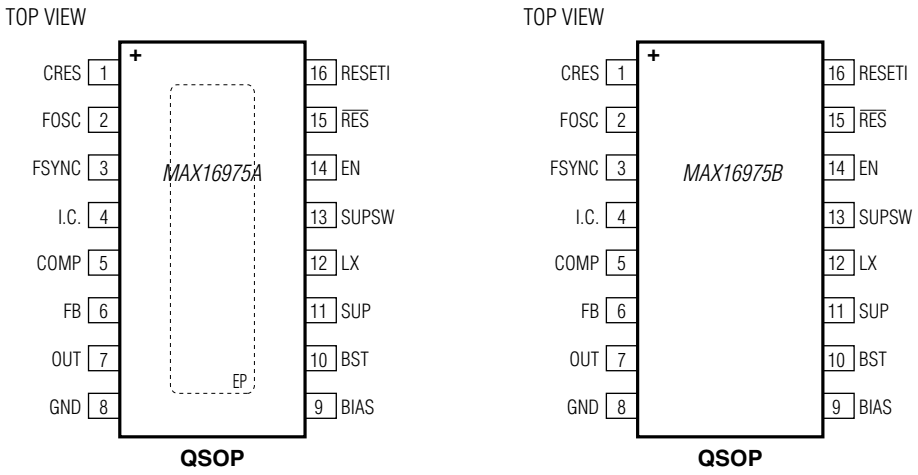
V_{OUT} vs. TEMPERATURE IN SKIP MODE (1.25V/400kHz)



LINE REGULATION



Pin Configurations



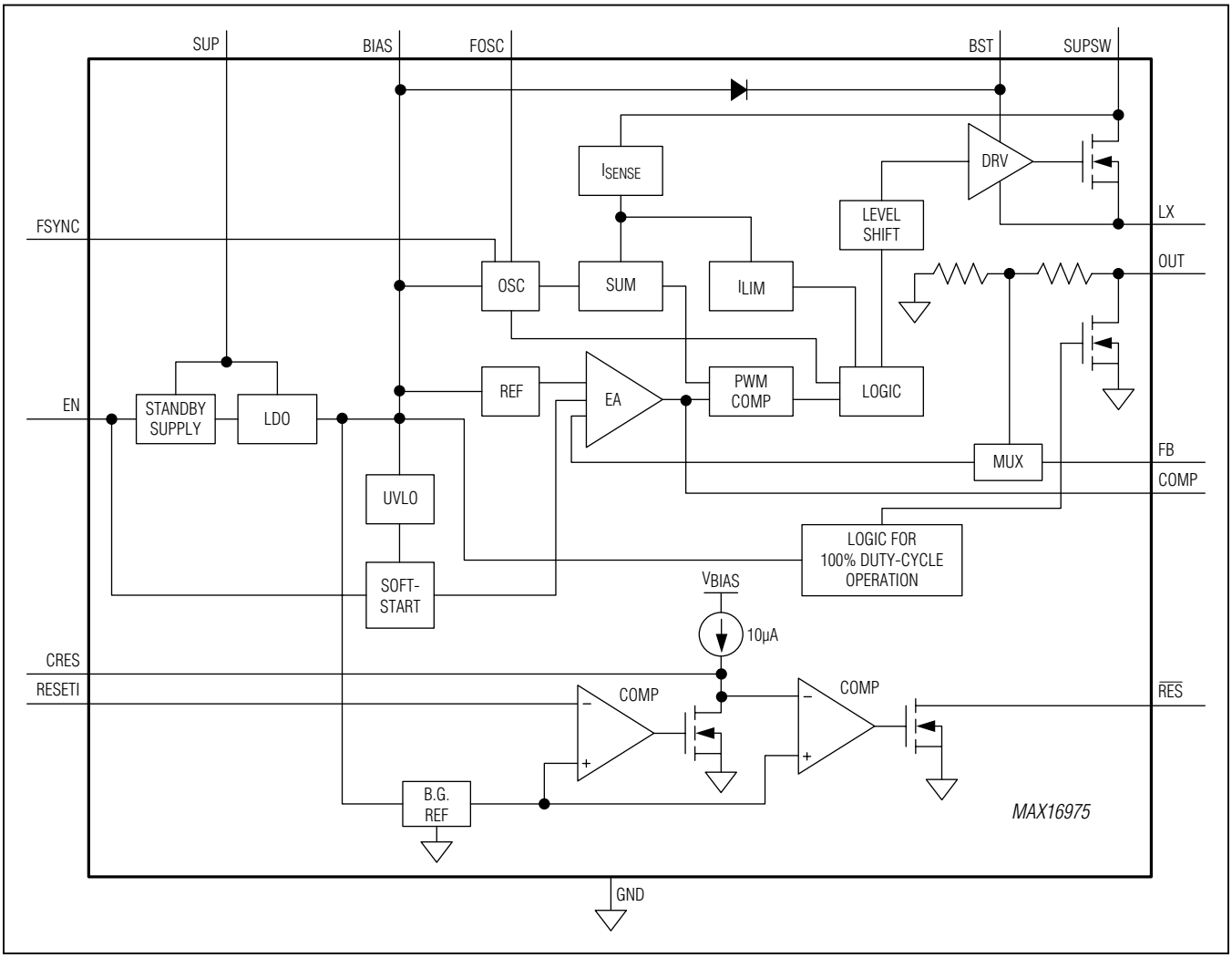
Pin Description

PIN	NAME	FUNCTION
1	CRES	Analog Reset Timer. CRES sources 10µA (typ) of current into an external capacitor to set the reset timeout period. Reset timeout period is defined as the time between the start of output regulation and $\overline{RES}$ switching to high impedance. Leave CRES unconnected for minimum delay time.
2	FOSC	Resistor-Programmable Switching Frequency Control Input. Connect a resistor from FOSC to GND to set the switching frequency (see the *Internal Oscillator* section).
3	FSYNC	Synchronization Input. The device synchronizes to an external signal applied to FSYNC. The external signal period must be 10% shorter than the internal clock period for proper operation.
4	I.C.	Internally Connected. Connect to GND.
5	COMP	Error-Amplifier Output. Connect a compensation network from COMP to GND for stable operation. See the *Compensation Network* section.
6	FB	Feedback Input. Connect an external resistive divider from FB to OUT and GND to set the output voltage between 1V and 10V. Connect FB directly to BIAS to set the output voltage to 5V. See the *Applications Information* section.
7	OUT	Connect OUT to the output of the converter. OUT provides power to the internal circuitry when the output voltage of the converter is set between 3V and 5.6V. During shutdown, OUT is pulled to GND with a 50Ω resistor.
8	GND	Ground
9	BIAS	Linear Regulator Output. BIAS powers the internal circuitry. Bypass BIAS with a 1µF capacitor to ground as close as possible to the device. During shutdown, BIAS is actively discharged through a 32kΩ resistor.
10	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
11	SUP	Voltage Supply Input. SUP powers the internal linear regulator. Connect a 4.7µF capacitor from SUP to ground. Connect SUP to SUPSW.
12	LX	Inductor Connection. Connect a rectifying Schottky diode between LX and GND. Connect an inductor from LX to the output.

Pin Description (continued)

PIN	NAME	FUNCTION
13	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. Connect a 4.7µF capacitor from SUPSW to ground. Connect SUP to SUPSW. See the *Input Capacitor* section.
14	EN	Battery-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
15	$\overline{RES}$	Open-Drain Active-Low Reset Output. $\overline{RES}$ asserts when V_{OUT} is below the reset threshold set by RESETI.
16	RESETI	Reset Threshold Level Input. Connect to a resistive divider to set the reset threshold for $\overline{RES}$. Connect RESETI to GND to enable the internal reset threshold.
—	EP	Exposed Pad (MAX16975A Only). Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Functional Diagram



Detailed Description

The MAX16975 is a constant-frequency, current-mode automotive buck converter with an integrated high-side switch. The device operates with input voltages from 3.5V to 28V and tolerates input transients up to 42V. During undervoltage events, such as cold-crank conditions, the internal pass device maintains 94% duty cycle for a short time.

An open-drain, active-low reset output helps to monitor the output voltage. The device offers an adjustable reset threshold that helps to keep microcontrollers alive down to the lowest specified input voltage and a capacitor-programmable reset timeout to ensure proper startup.

The switching frequency is resistor-programmable from 220kHz to 1.0MHz to allow optimization for efficiency, noise, and board space. A clock input, FSYNC, allows the device to synchronize to an external clock.

During light-load conditions, the device enters skip mode that reduces the quiescent current down to 45µA and increases light-load efficiency. The 5V fixed output voltage eliminates the need for external resistors and reduces the supply current by up to 50µA.

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator, V_{BIAS}, that provides power to the internal circuitry. Connect a 1µF ceramic capacitor from BIAS to GND. When the output voltage is set between 3V and 5.5V, the internal linear regulator only provides power until the output is in regulation. The internal linear regulator turns off once the output is in regulation and allows OUT to provide power to the device. The internal regulator turns back on once the external load on the output of the device is higher than 100mA. In addition, the linear regulator turns on anytime the output voltage is outside the 3V to 5.5V range.

External Clock Input (FSYNC)

The device synchronizes to an external clock signal applied at FSYNC. The signal at FSYNC must have a frequency of 10% higher than the internal clock frequency for proper synchronization.

Adjustable Reset Level

The device features a programmable reset threshold using a resistive divider between OUT, RESETI, and GND. Connect RESETI to GND for the internal threshold. $\overline{RES}$ asserts low when the output voltage falls to 93% of the programmed level. $\overline{RES}$ deasserts when the output voltage goes above 95% of the set voltage.

Some microprocessors accept a wide input voltage range (3.3V to 5V, for example) and can operate during dropout of the device. Use a resistive divider at RESETI to adjust the reset activation level ($\overline{RES}$ goes low) to lower levels. The reference voltage at RESETI is 1.25V (typ).

The device also offers a capacitor-programmable reset timeout period. Connect a capacitor from CRES to GND to adjust the reset timeout period. When the output voltage goes out of regulation, $\overline{RES}$ asserts low and the reset timing capacitor discharges with a 1mA pulldown current. Once the output is back in regulation the reset timing capacitor recharges with 10µA (typ) current. $\overline{RES}$ stays low until the voltage at CRES reaches 1.13V (typ).

Dropout Operation

The device features an effective maximum duty cycle to help refresh the BST capacitor when continuously operated in dropout. When the high-side switch is on for three consecutive clock cycles, the device forces the high-side switch off during the final 35% of the fourth clock cycle. When the high-side switch is off, the LX node is pulled low by the current flowing through the inductor. This increases the voltage across the BST capacitor. To ensure that the inductor has enough current to pull LX to ground, an internal load sinks current from V_{OUT} when the device is close to dropout and external load is small. Once the input voltage is increased above the dropout region, the device continues to regulate at the set output voltage.

The device operates with no load and no external clock at an effective maximum duty cycle of 94% in deep dropout. This effective maximum duty cycle is influenced by the external load and by the optional external synchronized clock.

System Enable (EN)

An enable-control input (EN) activates the device from the low-power shutdown mode. EN is compatible with inputs from the automotive battery level down to 3.3V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the INH inputs of a CAN transceiver.

EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout level, V_{UVL} = 3.15V (typ), the controller activates and the output voltage ramps up within 2048 cycles of the switching frequency.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown mode reduces the quiescent current to 9µA (typ). Drive EN high to turn on the device.

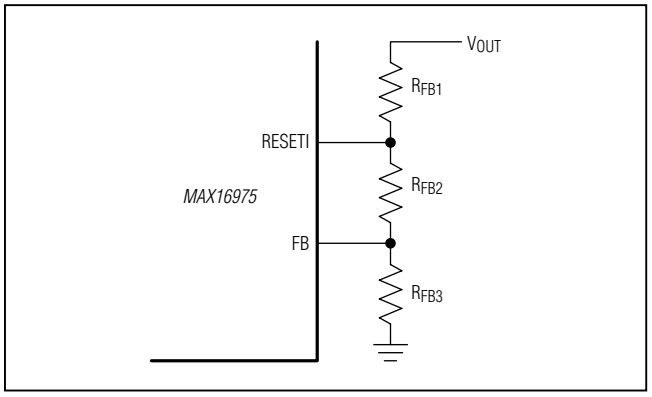


Figure 1. Output Voltage/Reset Threshold Resistive Divider Network

Overvoltage Protection

The device includes overvoltage protection circuitry that protects the device when there is an overvoltage condition at the output. If the output voltage increases by more than 12% of its set voltage, the device stops switching. The device resumes regulation once the overvoltage condition is removed.

Overload Protection

The overload protection circuitry is activated when the device is in current limit and V_{OUT} is below the reset threshold. Under these conditions, the device enters a soft-start mode. When the overcurrent condition is removed before the soft-start mode is over, the device regulates the output voltage to the set value. Otherwise, the soft-start cycle repeats until the overcurrent condition is removed.

Skip Mode

During light-load operation, $I_{INDUCTOR} \leq 200mA$, the device enters skip-mode operation. Skip mode turns off the internal switch and allows the output to drop below regulation voltage before the switch is turned on again. The lower the load current, the longer it takes for the regulator to initiate a new cycle effectively increasing light-load efficiency. During skip mode, the device quiescent current drops to as low as 45µA.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +175°C (typ), an internal thermal sensor shuts down the step-down controller, allowing the device to cool. The thermal sensor turns on the device again after the junction temperature cools by +15°C.

Applications Information

Output Voltage/Reset Threshold Resistive Divider Network

Although the device's output voltage and reset threshold can be set individually, Figure 1 shows a combined resistive divider network to set the desired output voltage and the reset threshold using three resistors. Use the following formula to determine the R_{FB3} of the resistive divider network:

$$R_{FB3} = \frac{R_{TOTAL} \times V_{REF}}{V_{OUT}}$$

where V_{REF} = 1V, R_{TOTAL} = selected total resistance of R_{FB1}, R_{FB2}, and R_{FB3} in ohms, and V_{OUT} is the desired output voltage in volts.

Use the following formula to calculate the value of R_{FB2} of the resistive divider network:

$$R_{FB2} = \frac{R_{TOTAL} \times V_{REF_RES}}{V_{RES}} - R_{FB3}$$

where V_{REF_RES} is 1.25V (see the *Electrical Characteristics* table) and V_{RES} is the desired reset threshold in volts.

The precision of the reset threshold function is dependent on the tolerance of the resistors used for the divider.

BST Capacitor Selection for Dropout Operation

The device includes an internal boost capacitor refresh algorithm for dropout operation. This is required to ensure proper boost capacitor voltage that delivers power to the gate-drive circuitry. When the HSFET is on consecutively for 3.65 clock cycles, the internal counter detects this and turns off the HSFET for 0.35 clock cycles. This is of particular concern when V_{IN} is falling and approaching V_{OUT} at the minimum switching frequency (220kHz).

The worst-case condition for boost capacitor refresh time is with no load on the output. For the boost capacitor to recharge completely, the LX node must be pulled to ground. If there is no current through the inductor then the LX node does not go to ground. To solve this issue, an internal load of about 100mA turns on at the sixth clock cycle, which is determined by a separate counter.

In the worst-case condition with no load, the LX node does not go below ground during the first detect of the

3.65 clock cycles. The device waits for the next 3.65 clock cycles to finish. As a result, the soonest the LX node can go below ground is 4 + 3.65 = 7.65 clock cycles. This time does not factor in the size of the inductor and the time it takes for the inductor current to build up to 100mA (internal load).

No load minimum time before refresh is:

ΔT (no load) = 7.65 clock cycles = 7.65 x 4.54µs (at 220kHz) = 34.73µs

Assuming a full 100mA is needed to refresh the BST capacitor and depending on the size of the inductor, the time it takes to build up full 100mA in the inductor is given by:

ΔT (inductor) = L x $\Delta I/\Delta V$ (current build-up starts from the sixth clock cycle)

L = inductor value chosen in the design guide.

ΔI is the required current = 100mA.

ΔV = voltage across the inductor (assume this to be 0.5V), which means V_{IN} is greater than V_{OUT} by 0.5V.

If ΔT (inductor) < 7.65 – 6 (clock cycles) then the BST capacitor is sized as follows:

BST_CAP ≥ I_BST(dropout) x ΔT (no load)/ΔV (BST capacitor)

ΔT (no load) = 7.65 clock cycles = 34.73µs.

ΔV (BST capacitor), for (3.3V to 5V) output = V_{OUT} – 2.7V (2.7V is the minimum voltage allowed on the BST capacitor).

If ΔT (inductor) > 7.65 - 6 clock cycles then we need to wait for the next count of 3.65 clock cycles making ΔT (no load) = 11.65 clock cycles.

Assume ΔT (no load) to be 16 clock cycles when designing the BST capacitor with a typical inductor value for 220kHz operation.

The final BST_CAP equation is:

BST_CAP = I_BST (dropout) x ΔT (no load)/ΔV (BST capacitor)

where:

I_BST (dropout) = 2.5mA (worst case)

ΔT (no load) = 16 clock cycles

ΔV (BST capacitor) = V_{OUT} - 2.7V

Reset Timeout Period

The device offers a capacitor-adjustable reset timeout period. CRES can source 10µA of current. Use the following formula to set the timeout period.

$$\text{RESET_TIMEOUT} = \frac{1.13V \times C}{10\mu A} (s)$$

where C is the capacitor from CRES to GND in Farads.

Internal Oscillator

The device's internal oscillator is programmable from 220kHz to 1.0MHz using a single resistor at FOSC. Use the following formula to calculate the switching frequency:

$$f_{OSC} (Hz) \approx \frac{26.4 \times 10^9 (\Omega \times Hz)}{R}$$

where R is the resistor from FOSC to GND in ohms.

For example, a 220kHz switching frequency is set with R_{FOSC} = 120kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{SUPSW} - V_{OUT})}{V_{SUPSW} f_{SW} I_{OUT} LIR}$$

where V_{SUPSW}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{FOSC}. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient response requirements. Table 1 shows a comparison between small and large inductor sizes.

Table 1. Inductor Size Comparison

INDUCTOR SIZE	
SMALLER	**LARGER**
Lower price	Smaller ripple
Smaller form-factor	Higher efficiency
Faster load response	Larger fixed-frequency range in skip mode

The inductor value must be chosen so that the maximum inductor current does not reach the minimum current limit of the device. The optimum operating point is usually found between 15% and 35% ripple current. When pulse skipping (light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{SUPSW} - V_{OUT})}{V_{SUPSW} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in A, L is in H, and f_{SW} is in Hz.

Ferrite cores are often the best choices, although powdered iron is inexpensive and can work well at 220kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{SUPSW} - V_{OUT})}}{V_{SUPSW}}$$

I_{RMS} is at a maximum value when the input voltage equals twice the output voltage ($V_{SUPSW} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from ΔV_Q and ΔV_{ESR} to be 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUPSW} - V_{OUT}) \times V_{OUT}}{V_{SUPSW} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

and

$$D = \frac{V_{OUT}}{V_{SUPSW}}$$

I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. So the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

Rectifier Selection

The device requires an external Schottky diode rectifier as a freewheeling diode. Connect this rectifier close to the device using short leads and short PCB traces. Choose a rectifier with a continuous current rating higher than the highest output current-limit threshold (1.5A) and with a voltage rating higher than the maximum expected input voltage, V_{SUPSW}. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops.

Compensation Network

The device uses an internal transconductance error amplifier with its inverting input and its output available for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, so the device uses the voltage drop across the high-side MOSFET. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. A simple single series resistor (R_C) and capacitor (C_C) are all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (Figure 2). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_{MC} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations allow to approximate the value for the gain of the power modulator ($GAIN_{MOD(DC)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the device.

$$GAIN_{MOD(dc)} = g_{MC} \times \frac{R_{LOAD} \times f_{SW} \times L}{R_{LOAD} + (f_{SW} \times L)}$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω, f_{SW} is the switching frequency in MHz, L is the output inductance in µH, and g_{MC} = 3S.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_{SW} \times L}{R_{LOAD} + (f_{SW} \times L)} + ESR \right)}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$ and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

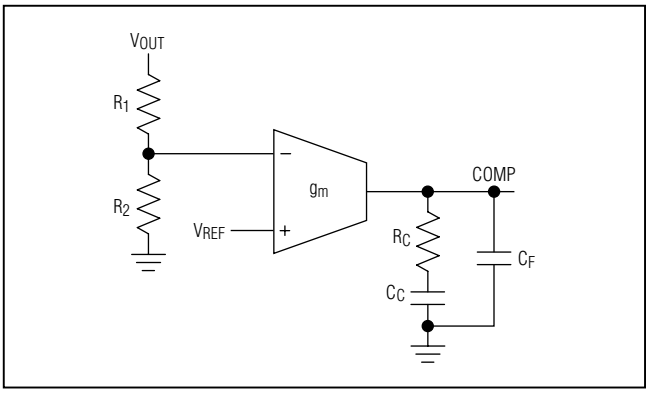


Figure 2. Compensation Network

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ). The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 1000µS (typ), and $R_{OUT,EA}$ is the output resistance of the 50MΩ error amplifier.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)).

Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) is set below 1/5th the switching frequency and much higher than the power-modulator pole (f_{pMOD}):

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C is equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is lower than 5 x f_C, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same. For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(f_C)} = g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} ($f_{zEA} = f_{pMOD}$):

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to GND. Set $f_{pEA} = f_{zMOD}$ and calculate C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Make the high-current path comprising of an input capacitor, high-side FET, inductor, and the output capacitor as short as possible.
4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) Route the analog signal lines away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the device.
6) Make the ground connection for the analog and power section close to the device. This keeps the ground current loops to a minimum. In cases where only one ground is used, enough isolation between analog return signals and high power signals must be maintained.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16975AAEE/V+	-40°C to +125°C	16 QSOP-EP*
MAX16975BAEE/V+	-40°C to +125°C	16 QSOP

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167
16 QSOP-EP	E16E+10	21-0112	90-0239

28V, 1.2A Automotive Step-Down Converter with Low Operating Current

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	10/13	Updated the *General Description* section and added thermal characteristics of the QSOP-EP package	1, 2

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