MAX16993

Step-Down Controller with Dual 2.1MHz Step-Down DC-DC Converters

General Description

The MAX16993 power-management integrated circuit (PMIC) is a 2.1MHz, multichannel, DC-DC converter designed for automotive applications. The device integrates three supplies in a small footprint. The device includes one high-voltage step-down controller (OUT1) designed to run directly from a car battery and two low-voltage step-down converters (OUT2/OUT3) cascaded from OUT1. Under no-load conditions, the MAX16993 consumes only 30µA of quiescent current, making it ideal for automotive applications.

The high-voltage synchronous step-down DC-DC controller (OUT1) operates from a voltage up to 36V continuous and is protected from load-dump transients up to 42V. There is a pin-selectable frequency option of either 2.1MHz or a factory-set frequency for 1.05MHz, 525kHz, 420kHz, or 350kHz. The low-voltage, synchronous step-down DC-DC converters run directly from OUT1 and can supply output currents up to 3A.

The device provides a spread-spectrum enable input (SSEN) to provide quick improvement in electromagnetic interference when needed. There is also a SYNC input for providing an input to synchronize to an external clock source (see the *Selector Guide*). The device includes overtemperature shutdown and overcurrent limiting. The device also includes individual $\overline{\text{RESET}}_$ outputs and individual enable inputs. The individual $\overline{\text{RESET}}_$ outputs provide voltage monitoring for all output channels.

The MAX16993 is available in a 32-pin TQFN/side-wettable QFND-EP package and is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive
- Industrial

Benefits and Features

- High-Efficiency Voltage DC-DC Controller Saves Power
  - 3.5V to 36V Operating Supply Voltage
  - Output Voltage: Pin Selectable, Fixed, or Resistor-Divider Adjustable
    - 350kHz to 2.1MHz Operation
    - 30µA Quiescent Current with DC-DC Controller Enabled
- Dual 2.1MHz DC-DC Converters with Integrated FETs Save Space
  - OUT2 and OUT3 are Cascaded from OUT1, Improving Efficiency
  - 3A Integrated FETs
  - 0.8V to 3.95V Output Voltage
  - Fixed or Resistor-Divider-Adjustable Output Voltage
  - 180° Out-of-Phase Operation
  - Robust for the Automotive Environment
- Current-Mode Architecture with Forced-PWM and Skip Modes of Operation
  - Frequency Synchronization Input/Output Reduces System Noise
  - Individual Enable Inputs and $\overline{\text{RESET}}_$ Outputs
  - Overtemperature and Short-Circuit Protection
  - AECQ-100 Qualified
  - 32-Pin TQFN-EP (5mm x 5mm x 0.75mm) and Side-Wettable QFND-EP (5mm x 5mm x 0.8mm)
  - -40°C to +125°C Operating Temperature Range

***Ordering Information* and *Selector Guide* appear at end of data sheet.**

19-6684; Rev 14; 12/16

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Absolute Maximum Ratings

V_{SUP}, EN1 to GND .....-0.3V to +45V
PV_ to GND.....-0.3V to +6.0V
PV_ to GND.....-0.3V to +6.0V
PV2 to GND, PV2 to PGND2.....-0.3V to +6.0V
PV3 to GND, PV3 to PGND3.....-0.3V to +6.0V
PGND2–PGND3 to GND.....-0.3V to +0.3V
LX1 to GND.....-6.0V to V_{SUP} + 6.0V
BST1 to LX1 (Note 1).....-0.3V to +6.0V
DH1 to LX1 (Note 1).....-0.3V to BST1 + 0.3V
BIAS to GND.....-0.3V to +6.0V
DL1 to GND (Note 1).....-0.3V to PV1 + 0.3V
LX2 to PGND2.....-0.3V to PV2 + 0.3V
LX3 to PGND3.....-0.3V to PV3 + 0.3V
OUT1, CS1, OUT2, OUT3 to GND .....-0.3V to +6.0V
SYNC to GND .....-0.3V to PV_ + 0.3V
FB1, EN2, EN3 to GND.....-0.3V to +6.0V
$\overline{RESET_}$, $\overline{ERR}$ to GND.....-0.3V to +6.0V
CS1 to OUT1.....-0.3V to +0.3V
CSEL1, SSEN to GND .....-0.3V to +6.0V
COMP1 to GND.....-0.3V to PV + 0.3V
LX2, LX3 Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70ºC)
Side-Wettable QFND (derate 27mW/ºC above +70ºC).....2160mW
TQFN (derate 34.5mW/ºC above +70ºC).....2758.6mW
Operating Temperature Range.....-40ºC to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65ºC to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Side-Wettable QFND
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2.8°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... 1.7°C/W

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = 14V, V_{PV1} = V_{BIAS}, V_{PV2} = V_{PV3} = V_{OUT1}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Startup Threshold	$V_{SUP,STARTUP}$	V_{SUP} rising	4.25	4.5	4.75	V
Supply Voltage Range	V_{SUP}	Normal operation, after Buck 1 startup	3.5		36	V
Supply Current	I_{SUP}	V_{EN1} = V_{EN2} = V_{EN3} = 0V		4	15	µA
		V_{EN1} = 5V, V_{EN2} = V_{EN3} = 0V (no load)		20	40	
Oscillator Frequency	f_{SW}		2.0	2.1	2.2	MHz
SYNC Input Frequency Range			1.7		2.4	MHz
Spread-Spectrum Range		V_{SSEN} = V_{GND}		0		%
		V_{SSEN} = V_{BIAS}		+6		
BIAS Regulator Voltage	V_{BIAS}	6V ≤ V_{SUP} ≤ 42V, no switchover	4.6	5.0	5.4	V
PV_ POR		V_{BIAS} falling	2.5	2.7	2.9	V
		Hysteresis		0.45		

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{PV1} = V_{BIAS}, V_{PV2} = V_{PV3} = V_{OUT1}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT1: HIGH-VOLTAGE SYNCHRONOUS STEP-DOWN DC-DC CONTROLLER							
OUT1 Switching Frequency	f_{SW1}	Internally generated (see the *Selector Guide*)	V_{CSEL1} = V_{GND}		2100		kHz
			V_{CSEL1} = V_{BIAS} (factory option)		1050		
			V_{CSEL1} = V_{BIAS} (factory option)		525		
			V_{CSEL1} = V_{BIAS} (factory option)		420		
			V_{CSEL1} = V_{BIAS} (factory option)		350		
Voltage	V_{OUT1}	Fixed option (see the *Selector Guide*)	V_{FB1} = V_{GND}		3.3		V
			V_{FB1} = V_{BIAS} (factory option)		5.0		
			V_{FB1} = V_{BIAS} (factory option)		3.15		
FB1 Regulation Voltage		Adjustable option (see the *Selector Guide*)		0.985	1.0	1.019	V
Error Amplifier Transconductance	g_{MEA}			300	700	1200	µS
Voltage Accuracy	V_{OUT1}	5.5V ≤ V_{SUP} ≤ 18V, 0 < V_{LIM1} < 75mV, PWM mode		-2.0		+2.5	%
DC Load Regulation		PWM mode			0.02		%/A
DC Line Regulation		PWM mode			0.03		%/V
OUT1 Discharge Resistance		V_{EN1} = V_{GND} or V_{SUP}			100	200	Ω
High-Side Output Drive Resistance		V_{DH1} rising, I_{DH1} = 100mA			2	4	Ω
		V_{DH1} falling, I_{DH1} = 100mA			1	4	
Low-Side Output Drive Resistance		V_{DL1} rising, I_{DL1} = 100mA			2.5	5	Ω
		V_{DL1} falling, I_{DL1} = 100mA			1.5	3	
Output Current-Limit Threshold	V_{LIM1}	CSI – OUT1		100	120	150	mV
Skip Current Threshold	I_{SKIP}	CS1 – OUT1, no load		10	35	60	mV
Soft-Start Ramp Time					4		ms
LX_ Leakage Current		V_{LX1} = V_{SUP}			0.01		µA
Duty-Cycle Range		PWM mode				97.2	%
Minimum On-Time					60	75	ns
OUT1 OV Threshold				107	110	113	%

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{PV1} = V_{BIAS}, V_{PV2} = V_{PV3} = V_{OUT1}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT2 AND OUT3: LOW-VOLTAGE SYNCHRONOUS STEP-DOWN DC-DC CONVERTERS						
Supply Voltage Range	V_{SUP}		2.7		5.5	V
Supply Current	$I_{PV_}$	$V_{EN_}$ = 5V, no load		0.1	5	µA
Skip Mode Peak Current				0.2 x I_{LMAX}		mA
Voltage Accuracy	V_{OUT}	0A ≤ I_{LOAD} ≤ I_{MAX}, PWM mode	-3.0		+3.0	%
Feedback-Voltage Accuracy		Adjustable mode, I_{OUT2} = 0mA	0.806	0.815	0.824	V
Load Regulation		0A ≤ I_{LOAD} ≤ I_{MAX} (PWM mode)	-1.5	-1.0		%
		0A ≤ I_{LOAD} ≤ I_{MAX} (PWM mode, low gain, see the *Selector Guide*)	-2.5	-1.7		
LX_ On-Resistance High		$I_{LX_}$ = -800mA		70	110	mΩ
LX_ On-Resistance Low		$I_{LX_}$ = 800mA		50	90	mΩ
Current-Limit Threshold	I_{LMAX}	I_{MAX} = 3.0A option (see the *Selector Guide*)	5.0	5.6		A
		I_{MAX} = 1.5A option (see the *Selector Guide*)	2.5	3.0		
LX_ Rise/Fall Time		PV2 = PV3 = 3.3V, $I_{OUT_}$ = 2A		4		ns
Soft-Start Ramp Time				2.5		ms
LX_ Leakage Current				0.01		µA
Duty-Cycle Range		PWM mode	15		100	%
LX_ Discharge Resistance				22	48	Ω
$\overline{\text{RESET}}$_						
Reset Threshold		Rising (relative to nominal output voltage)	92	95	98	%
		Falling (relative to nominal output voltage)	90	92	95	
OUT1 Active Timeout Period		See the *Selector Guide* (16,384 clocks)		7.8		ms
		See the *Selector Guide* (8192 clocks)		3.9		
		See the *Selector Guide* (4096 clocks)		1.9		
		See the *Selector Guide* (256 clocks)		0.1		
OUT2, OUT3 Active Timeout Period		See the *Selector Guide* (16,384 clocks)		7.8		ms
		See the *Selector Guide* (8192 clocks)		3.9		
		See the *Selector Guide* (4096 clocks)		1.9		
		See the *Selector Guide* (256 clocks)		0.1		

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{PV1} = V_{BIAS}, V_{PV2} = V_{PV3} = V_{OUT1}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

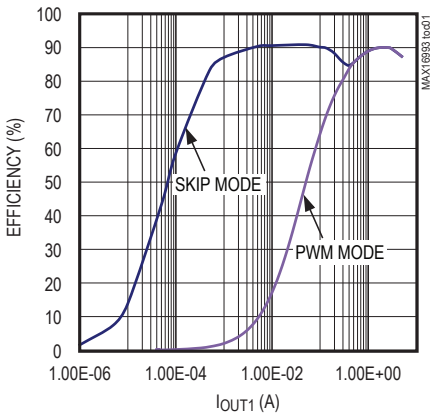
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Level		I_{SINK} = 3mA		0.1	0.2	V
Propagation Time		OUT1, 5% below threshold	5	10	20	µs
		OUT2/OUT3, 5% below threshold	2	4	8	µs
$\overline{ERR}$						
Output Low Level		I_{SINK} = 3mA		0.1	0.2	V
THERMAL OVERLOAD						
Thermal-Warning Temperature				+150		°C
Thermal-Shutdown Temperature				+170		°C
Thermal-Shutdown Hysteresis				15		°C
ENABLE INPUTS (EN_)						
Input High		$V_{EN_}$ rising	1.6	1.8	2.0	V
Hysteresis				0.2		V
EN Input Current		$V_{EN_}$ = 5V	0.5	1.0	2.0	µA
SYNCHRONIZATION I/O (SYNC)						
Input High		SYNC input option (see the *Selector Guide*)	1.8			V
Input Low		SYNC input option (see the *Selector Guide*)			0.8	V
Input Current		SYNC input option (see the *Selector Guide*); V_{SYNC} = 5V		50	80	µA
Pulldown Resistance				100		kΩ
LOGIC INPUTS (CSEL1, SSEN)						
Input High			1.4			V
Input Low					0.5	V
Input Current		T_A = +25°C			2	µA

Note 3: All units are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

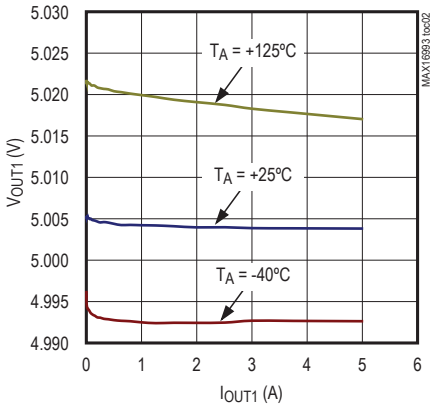
Typical Operating Characteristics

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted)

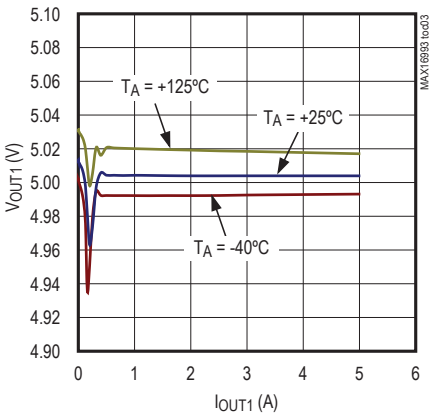
BUCK 1 EFFICIENCY



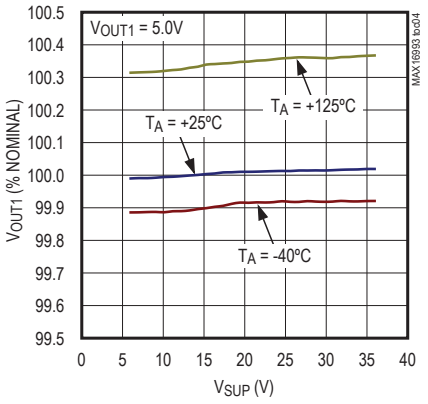
BUCK 1 LOAD REGULATION (PWM)



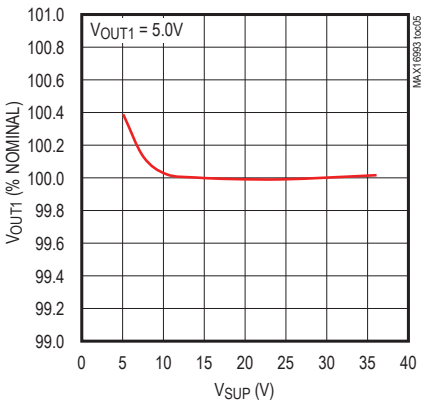
BUCK 1 LOAD REGULATION (SKIP)



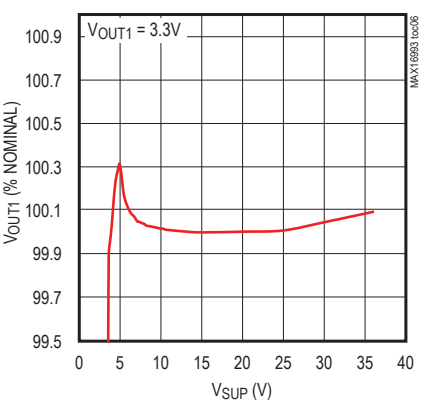
BUCK 1 LINE REGULATION (PWM MODE)



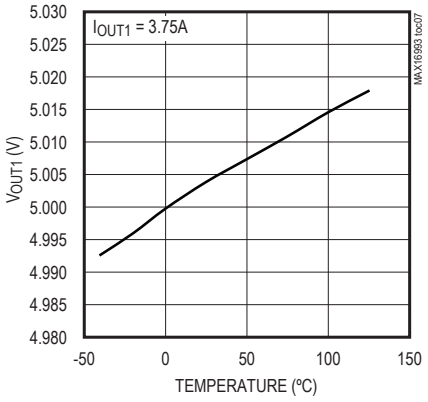
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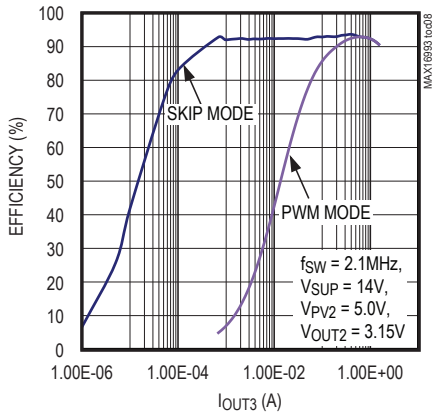
BUCK 1 LINE REGULATION (SKIP MODE)



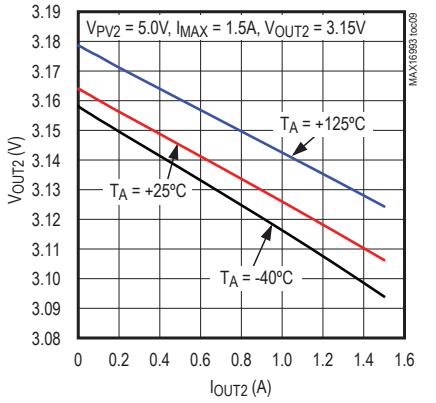
VOUT1 vs. TEMPERATURE



BUCK 2 EFFICIENCY



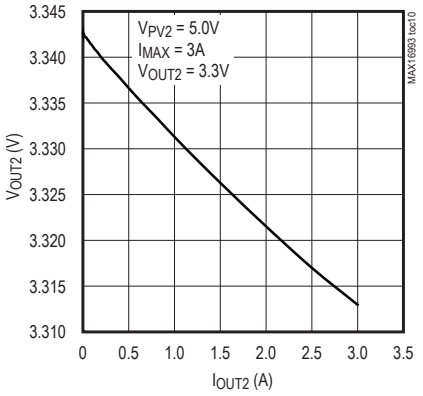
BUCK 2 LOAD REGULATION (PWM MODE)



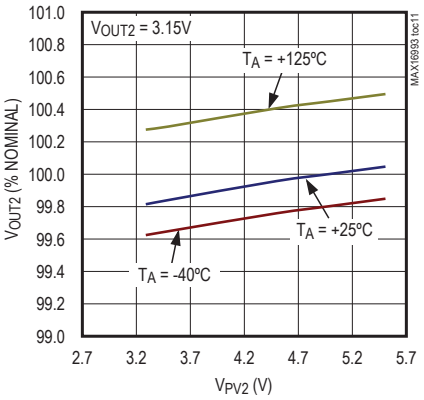
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted)

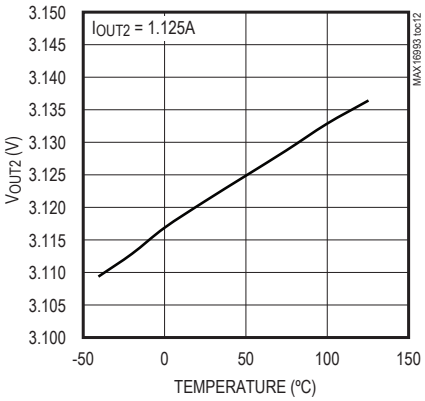
BUCK 2 LOAD REGULATION (PWM MODE)



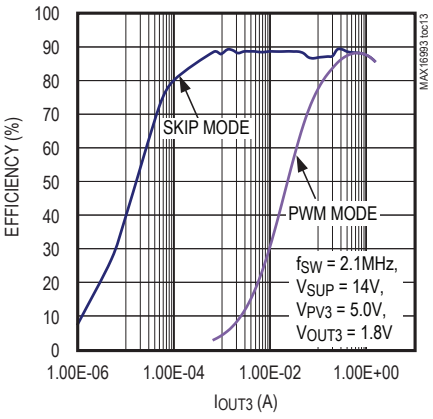
BUCK 2 LINE REGULATION (PWM MODE)



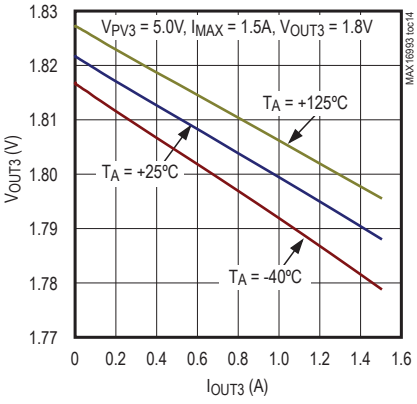
VOUT2 vs. TEMPERATURE



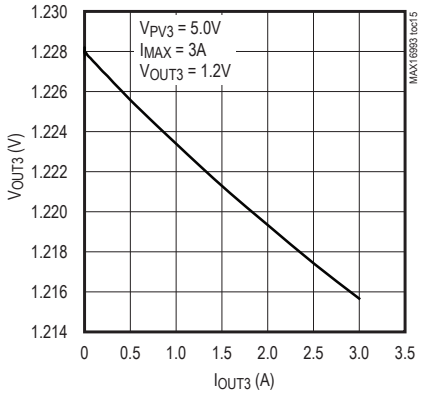
BUCK 3 EFFICIENCY



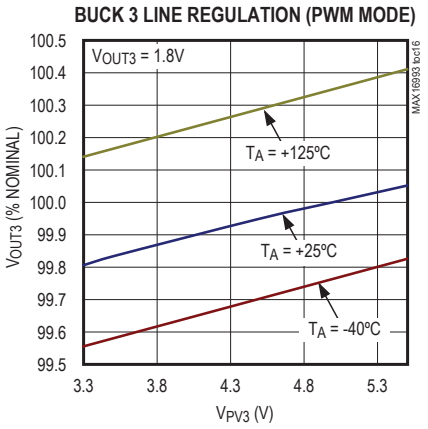
BUCK 3 LOAD REGULATION (PWM MODE)



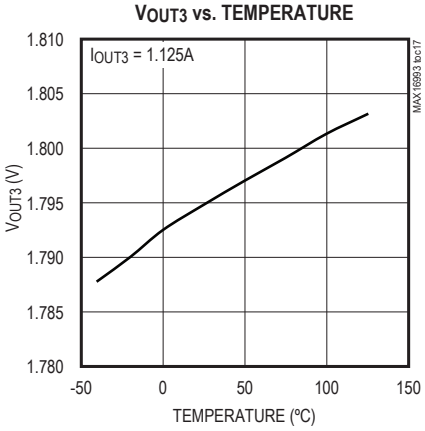
BUCK 3 LOAD REGULATION (PWM MODE)



BUCK 3 LINE REGULATION (PWM MODE)



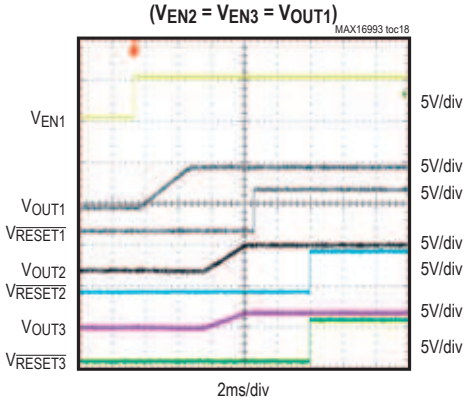
VOUT3 vs. TEMPERATURE



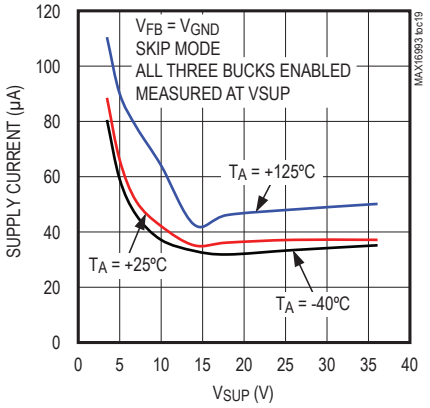
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted)

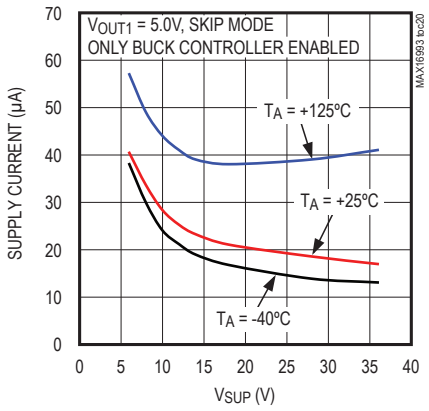
STARTUP SEQUENCE
(V_{EN2} = V_{EN3} = V_{OUT1})



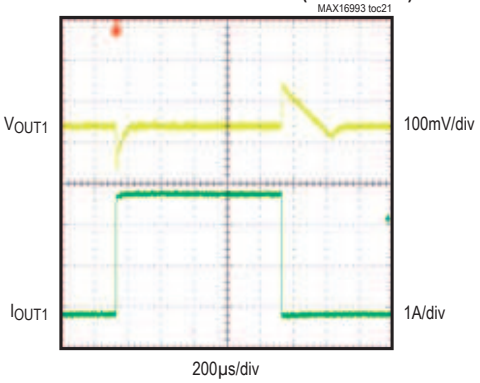
SUPPLY CURRENT vs. SUPPLY VOLTAGE



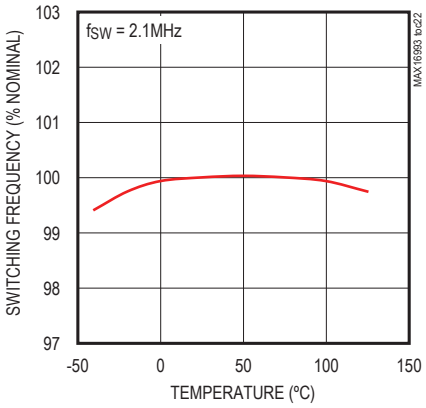
SUPPLY CURRENT vs. SUPPLY VOLTAGE



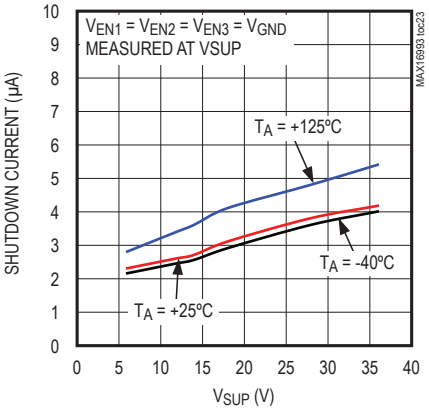
LOAD TRANSIENT RESPONSE (PWM MODE)



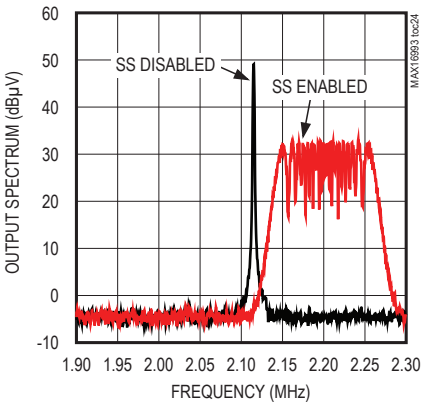
f_{SW} vs. TEMPERATURE



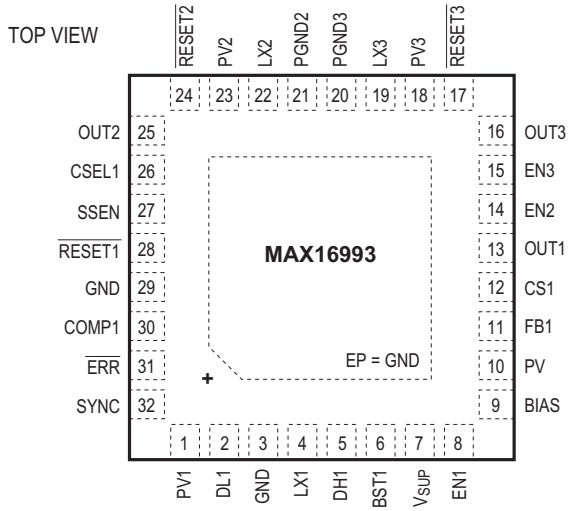
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



SPECTRAL ENERGY DENSITY



Pin Configuration



TQFN/SIDE-WETTABLE QFND

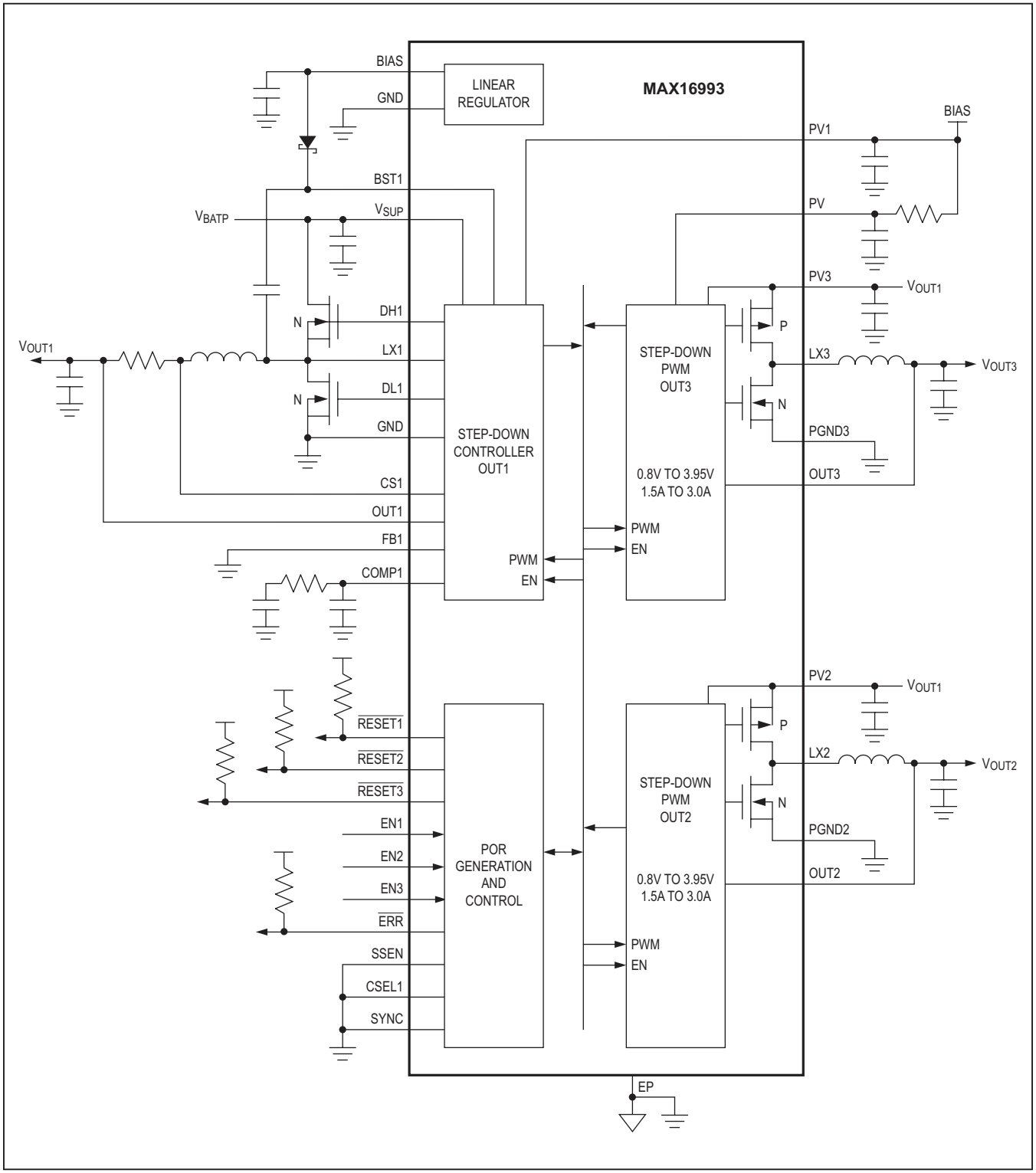
Pin Description

PIN	NAME	FUNCTION
1	PV1	Supply Input for Buck 1 Low-Side Gate Drive. Connect a ceramic bypass capacitor of at least 0.1µF from PV1 to GND.
2	DL1	Low-Side Gate-Drive Output for Buck 1. DL1 output voltage swings from V_{GND} to V_{PV1}.
3	GND	Power Ground for Buck 1
4	LX1	Inductor Connection for Buck 1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate drive.
5	DH1	High-Side Gate-Drive Output for Buck 1. DH1 output voltage swings from V_{LX1} to V_{BST1}.
6	BST1	Bootstrap Capacitor Connection for High-Side Gate Drive of Buck 1. Connect a high-voltage diode between BIAS and BST1. Connect a ceramic capacitor between BST1 and LX1. See the *High-Side Gate-Drive Supply (BST1)* section.
7	V_{SUP}	Supply Input. Bypass V_{SUP} with a minimum 0.1µF capacitor as close as possible to the device.
8	EN1	High-Voltage Tolerant, Active-High Digital Enable Input for Buck 1. Driving EN1 high enables Buck 1.
9	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 2.2µF minimum value. BIAS provides the power to the internal circuitry. See the *Linear Regulator (BIAS)* section.
10	PV	Analog Supply. Connect PV to BIAS through a 10Ω resistor and connect a 1µF ceramic capacitor from PV to ground.
11	FB1	Feedback Input for Buck 1. For the fixed output-voltage option, connect FB1 to BIAS for the factory-trimmed (3.0V to 3.75V or 4.6V to 5.35V) fixed output. Connect FB1 to GND for the 3.3V fixed output. For the resistor-divider adjustable output-voltage option, connect FB1 to a resistive divider between OUT1 and GND to adjust the output voltage between 3.0V and 5.5V. In adjustable mode, FB1 regulates to 1.0V (typ). See the *OUT1 Adjustable Output-Voltage Option* section.

Pin Description (continued)

PIN	NAME	FUNCTION
12	CS1	Positive Current-Sense Input for Buck 1. Connect CS1 to the positive terminal of the current-sense resistor. See the *Current-Limit/Short-Circuit Protection* and *Current-Sense Measurement* sections.
13	OUT1	Output Sense and Negative Current-Sense Input for Buck 1. The buck uses OUT1 to sense the output voltage. Connect OUT1 to the negative terminal of the current-sense resistor. See the *Current-Limit/Short-Circuit Protection* and *Current-Sense Measurement* sections.
14	EN2	Active-High Digital Enable Input for Buck 2. Driving EN2 high enables Buck 2.
15	EN3	Active-High Digital Enable Input for Buck 3. Driving EN3 high enables Buck 3.
16	OUT3	Buck Converter 3 Voltage-Sense Input. Connect OUT3 to the output of Buck 3. Connect OUT3 to an external feedback divider when setting DC-DC3 voltage externally. See the *OUT2/OUT3 Adjustable Output-Voltage Option* section.
17	$\overline{\text{RESET3}}$	Open-Drain Buck 3 Reset Output. $\overline{\text{RESET3}}$ remains low for a fixed time after the output of Buck 3 has reached its regulation level (see the *Selector Guide*). To obtain a logic signal, pull up $\overline{\text{RESET3}}$ with an external resistor connected to a positive voltage lower than 5V.
18	PV3	Buck 3 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV3 to PGND3. Connect PV3 to OUT1.
19	LX3	Buck 3 Switching Node. LX3 is high impedance when the device is off.
20	PGND3	Power Ground for Buck 3
21	PGND2	Power Ground for Buck 2
22	LX2	Buck 2 Switching Node. LX2 is high impedance when the device is off.
23	PV2	Buck 2 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV2 to PGND2. Connect PV2 to OUT1.
24	$\overline{\text{RESET2}}$	Open-Drain Buck 2 Reset Output. This output remains low for a fixed time after the output of Buck 2 has reached its regulation level (see the *Selector Guide*). To obtain a logic signal, pull up $\overline{\text{RESET2}}$ with an external resistor connected to a positive voltage lower than 5V.
25	OUT2	Buck Converter 2 Voltage-Sense Input. Connect OUT2 to the output of Buck 2. Connect OUT2 to an external feedback divider when setting DC-DC2 voltage externally. See the *OUT2/OUT3 Adjustable Output-Voltage Option* section.
26	CSEL1	Buck 1 Clock Select. Connect CSEL1 to GND for 2.1MHz operation. Connect CSEL1 to BIAS for an OTP-programmable divide-down operation. See the *Selector Guide* for the f_{SW1} divide ratio.
27	SSEN	Spread-Spectrum Enable. Connect SSEN to GND for standard oscillator operation. Connect SSEN to BIAS to enable the spread-spectrum oscillator.
28	$\overline{\text{RESET1}}$	Open-Drain Buck 1 Reset Output. $\overline{\text{RESET1}}$ remains low for a fixed time after the output of Buck 1 has reached its regulation level (see the *Selector Guide*). To obtain a logic signal, pull up $\overline{\text{RESET1}}$ with an external resistor connected to a positive voltage lower than 5V.
29	GND	Analog Ground
30	COMP1	Compensation for Buck 1. See the *Compensation Network* section.
31	$\overline{\text{ERR}}$	Open-Drain Error-Status Output. $\overline{\text{ERR}}$ signals a thermal-warning/shutdown condition. To obtain a logic signal, pull up $\overline{\text{ERR}}$ with an external resistor connected to a positive voltage lower than 5V.
32	SYNC	Synchronization Input. SYNC allows the device to synchronize to other supplies. Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to BIAS or an external clock to enable fixed-frequency forced-PWM-mode operation.
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND2–PGND3 and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Typical Operating Circuit



Detailed Description

The MAX16993 power-management integrated circuit (PMIC) is a 2.1MHz, multichannel, DC-DC converter designed for automotive applications. The device includes one high-voltage step-down controller (OUT1) designed to run directly from a car battery and two low-voltage step-down converters (OUT2/OUT3) cascaded from OUT1.

The 2.1MHz, high-voltage buck controller operates with a 3.5V to 36V input voltage range and is protected from load-dump transients up to 42V. The high-frequency operation eliminates AM band interference and reduces the solution footprint. It can provide an output voltage between 3.0V and 5.5V set at the factory or with external resistors. Each device has two frequency options that are pin selectable: 2.1MHz or a lower frequency based on factory setting. Available factory-set frequencies are 1.05MHz, 525kHz, 420kHz, or 350kHz. Under no-load conditions, the device consumes only 30µA of quiescent current with OUT1 enabled.

The dual buck converters can deliver 1.5A or 3.0A of load current per output. They operate directly from OUT1 and provide 0.8V to 3.95V output voltage range. Factory trimmed output voltages achieve ±3% output error over load, line, and temperature without using expensive ±0.1% resistors. In addition, adjustable output-voltage versions can be set to any desired values between 0.8V and 3.6V using an external resistive divider. On-board low $R_{DS(ON)}$ switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs (see the *PCB Layout Guidelines* section).

The device features a SYNC input (see the *Synchronization (SYNC)* section and the *Selector Guide*). An optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency, and a factory-programmable synchronization I/O (SYNC) allows better noise immunity. Additional features include a 4ms fixed soft-start for OUT1 and 2.5ms for OUT2/OUT3, individual $\overline{\text{RESET}}$_ outputs, overcurrent, and overtemperature protections. See the *Selector Guide* for the available options.

Enable Inputs (EN_)

All three regulators have their own enable input. When EN1 exceeds the EN1 high threshold, the internal linear regulator is switched on. When V_{SUP} exceeds the $V_{SUP,STARTUP}$ threshold, Buck 1 is enabled and OUT1 starts to ramp up with a 4ms soft-start. Once the Buck 1 soft-start is complete, Buck 2 and Buck 3 can be enabled. When either Buck 2 or Buck 3 is enabled, the corresponding output ramps up with a 2.5ms soft-start. When an enable input is pulled low, the converter is switched off and the corresponding OUT_ and $\overline{\text{RESET}}$_ are driven low. If EN1 is low, all regulators are disabled.

Reset Outputs ($\overline{\text{RESET}}$_)

The device features individual open-drain $\overline{\text{RESET}}$_ outputs for each buck output that asserts when the buck output voltage drops 6% below the regulated voltage. $\overline{\text{RESET}}$_ remains asserted for a fixed timeout period after the buck output rises up to its regulated voltage. The fixed timeout period is programmable between 0.1ms and 7.4ms (see the *Selector Guide*). To obtain a logic signal, pull up $\overline{\text{RESET}}$_ with an external resistor connected to a positive voltage lower than 5V.

Linear Regulator (BIAS)

The device features a 5V internal linear regulator (BIAS). Connect BIAS to PV, which acts as a supply for internal circuitry. Also connect BIAS to PV1, which acts as a supply for the low-side gate driver of Buck 1. Bypass BIAS as close as possible to the device with a 2.2µF or larger ceramic capacitor. BIAS can provide up to 100mA (max), but is not designed to supply external loads. After OUT1 completes soft-start, BIAS LDO is turned off and the BIAS pin is shorted to the OUT1 pin internally to power the internal circuits (e.g., if OUT1 is set to 3.3V, BIAS transitions from 5V to 3.3V after soft-start).

Internal Oscillator

Buck 1 Clock Select (CSEL1)

The device offers a Buck 1 clock-select input. Connect CSEL1 to GND for 2.1MHz operation. Connect CSEL1 to BIAS to divide down the Buck 1 clock frequency by 2, 4, 5, or 6 (see the *Selector Guide*). Buck 2 and Buck 3 switch at 2.1MHz (typ) and are not controlled by CSEL1.

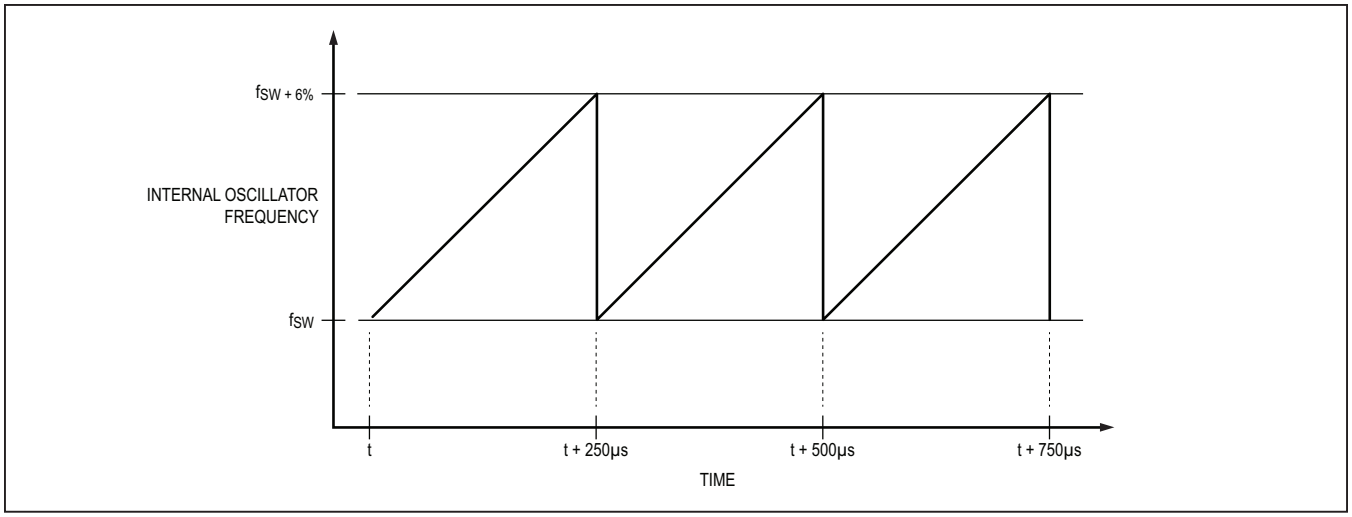


Figure 1. Effect of Spread Spectrum on Internal Oscillator

Spread-Spectrum Enable (SSEN)

The device features a spread-spectrum enable (SSEN) input that can quickly enable spread-spectrum operation to reduce radiated emissions. Connect SSEN to BIAS to enable the spread-spectrum oscillator. Connect SSEN to GND for standard oscillator operation. When spread spectrum is enabled, the internal oscillator frequency is varied between f_{SW} and (f_{SW} + 6%). The change in frequency has a sawtooth shape and a frequency of 4kHz (see Figure 1). This function does not apply to externally applied oscillation frequency. See the *Selector Guide* for available options.

Synchronization (SYNC)

SYNC is factory-programmable I/O. See the *Selector Guide* for available options. When SYNC is configured as an input, a logic-high on SYNC enables fixed-frequency, forced-PWM mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts signal frequencies in the range of 1.7MHz < f_{SYNC} < 2.4MHz. The external clock should have a duty cycle of 50%. A logic-low at the SYNC input enables the device to enter a low-power skip mode under light-load conditions.

Common Protection Features

Undervoltage Lockout

The device offers an undervoltage-lockout feature. Undervoltage detection is performed on the PV input. If V_{SUP} decreases to the point where Buck 1 is in drop-out, PV begins to decrease. If PV falls below the UVLO threshold (2.7V, typ), all three converters switch off and the $\overline{RESET_}$ outputs assert low. Once the device has been switched off, V_{SUP} must exceed the $V_{SUP,STARTUP}$ threshold before Buck 1 turns back on.

Output Overvoltage Protection

The device features overvoltage protection on the buck converter outputs. If the FB1 input exceeds the output overvoltage threshold, a discharge current is switched on at OUT1 and $\overline{RESET1}$ asserts low.

Soft-Start

The device includes a 4ms fixed soft-start time on OUT1 and 2.5ms fixed soft-start time on OUT2/OUT3. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. If OUT1 is prebiased above 1.25V, all three buck converters do not start up until the prebias has been removed. Once the prebias has been removed, OUT1 self-discharges to GND and then goes into soft-start.

Thermal Warning and Overtemperature Protection

The device features an open-drain, thermal-warning indicator ($\overline{ERR}$). $\overline{ERR}$ asserts low when the junction temperature exceeds +150°C (typ). The hysteresis on the thermal warning is 15°C (typ). For a logic signal, connect a pullup resistor from $\overline{ERR}$ to a supply less than or equal to 5V. When the junction temperature exceeds +170°C (typ), an internal thermal sensor shuts down the buck converters, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C (typ).

Buck 1 (OUT1)

Buck controller 1 uses a PWM current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope-compensation ramp, which are summed into the main PWM comparator to preserve inner-loop stability and eliminate inductor staircasing. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached, or the peak current limit is reached. During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier and pushes the output LC filter pole normally found in a voltage-mode PWM to a higher frequency.

During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit (see the *Current-Limit/Short-Circuit Protection* section), the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle.

PWM/Skip Modes

The device features a synchronization input that puts all the buck regulators either in skip mode or forced-PWM mode of operation (see the *Synchronization (SYNC)* section). In the PWM mode of operation, the regulator switches at a constant frequency with variable on-time. In the skip mode of operation, the regulator's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the regulator to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the regulator does not switch MOSFETs on and off as often as is the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Minimum On-Time and Duty Cycle

The high-side gate driver for Buck 1 has a minimum on-time of 75ns (max). This helps ensure no skipped pulses when operating the device in PWM mode at 2.1MHz with supply voltage up to 18V and output voltage down to 3.3V. Pulse skipping can occur if the on-time falls below the minimum allowed (see the *Electrical Characteristics*).

Current-Limit/Short-Circuit Protection

OUT1 offers a current-limit feature that protects Buck 1 against short-circuit and overload conditions on the buck controller. Buck 1 offers a current-limit sense input (CS1). Place a sense resistor in the path of the channel 1 current flow. Connect CS1 to the high side of the sense resistor and OUT1 to the low side of the sense resistor. Current-limit protection activates once the voltage across the sense resistor increases above the 120mV (typ) current-limit threshold. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down. The converter allows the high-side MOSFET to turn on only when the voltage across the current-sense resistor ramps down to below 120mV (typ). This cycle repeats until the short or overload condition is removed.

Current-Sense Measurement

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output, as shown in Figure 2. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement.

High-Side Gate-Drive Supply (BST1)

The high-side MOSFET is turned on by closing an internal switch between BST1 and DH1 and transferring the bootstrap capacitor's (at BST1) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX1 voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor. The selected n-channel high-side MOSFET determines the appropriate boost capacitance values (C_{BST1} in the *Typical Operating Circuit*) according to the following equation:

$$C_{BST1} = \frac{Q_G}{\Delta V_{BST1}}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST1} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST1} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST1} = 100mV to 300mV) when determining C_{BST1}. Use a Schottky diode when efficiency is most important, as this maximizes the gate-drive voltage. If the quiescent current at high temperature is important, it may be necessary to use a low-leakage switching diode.

The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases. A minimum value of 470nF is recommended when using a Schottky diode.

Dropout

When OUT1 input voltage is lower than the desired output voltage, the converter is in dropout mode. Buck 1 continuously draws current from the bootstrap capacitor when the high-side switch is on. Therefore, the bootstrap capacitor needs to be refreshed periodically. When in dropout, the Buck 1 high-side gate drive shuts off every 8µs, at which point the low-side gate drive turns on for 120ns.

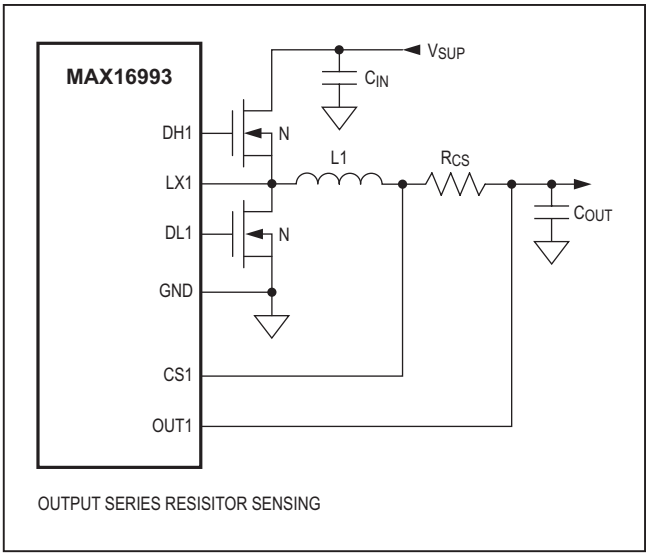


Figure 2. Current-Sense Configuration

Buck 2 and Buck 3 (OUT2 and OUT3)

Buck converters 2 and 3 are high-efficiency, low-voltage converters with integrated FETs. They use a PWM current-mode control scheme that is operated at 2.1MHz to optimize component size and efficiency, while eliminating AM band interference. The buck converters can be configured to deliver 1.5A or 3.0A per channel. They operate directly from OUT1 and have either fixed or resistor-programmable (see the *Selector Guide*) output voltages that range from 0.8V to 3.95V. Buck 2 and Buck 3 feature low on-resistance internal FETs that contribute to high efficiency and smaller system cost and board space. Integration of the p-channel high-side FET enables both channels to operate with 100% duty cycle when the input voltage falls to near the output voltage. They feature a programmable active timeout period (see the *Selector Guide*) that adds a fixed delay before the corresponding $\overline{\text{RESET_}}$ can go high.

FPWM/Skip Modes

The MAX16993 features an input (SYNC) that puts the converter either in skip mode or forced PWM (FPWM) mode of operation. See the *Internal Oscillator* section. In FPWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the FPWM mode.

Skip mode helps improve efficiency in light-load applications by allowing the converters to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in the FPWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Current-Limit/Short-Circuit Protection

Buck converters 2 and 3 feature current limit that protects the device against short-circuit and overload conditions at their outputs. The current limit value is dependent on the version selected, 1.5A or 3.0A maximum DC current. See the *Selector Guide* for the current limit value of the chosen option and the *Electrical Characteristics* table for the corresponding current limit. In the event of a short-circuit or overload condition at an output, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down.

The converter allows the low-side MOSFET to turn off only when the inductor current ramps down to the low-side MOSFET's current threshold. This cycle repeats until the short or overload condition is removed.

Applications Information

OUT1 Adjustable Output-Voltage Option

The device's adjustable output-voltage version (see the *Selector Guide* for details) allows the customer to set OUT1 voltage between 3.0V and 5.5V. Connect a resistive divider from OUT1 to FB1 to GND to set the output voltage (Figure 3). Select R2 (FB1 to GND resistor) less than or equal to 100kΩ. Calculate R1 (V_{OUT1} to FB1 resistor) with the following equation:

$$R_1 = R_2 \left[\left(\frac{V_{OUT1}}{V_{FB1}} \right) - 1 \right]$$

where V_{FB1} = 1.0V (see the *Electrical Characteristics*).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R1 in the resistive divider network. Use the following equation to determine the value of the capacitor:

if R2/R1 > 1, C1 = C(R2/R1)

else, C1 = C, where C = 10pF.

For fixed output options, connect FB1 to BIAS for the factory-programmed, fixed output voltage. Connect FB1 to GND for a fixed 3.3V output voltage.

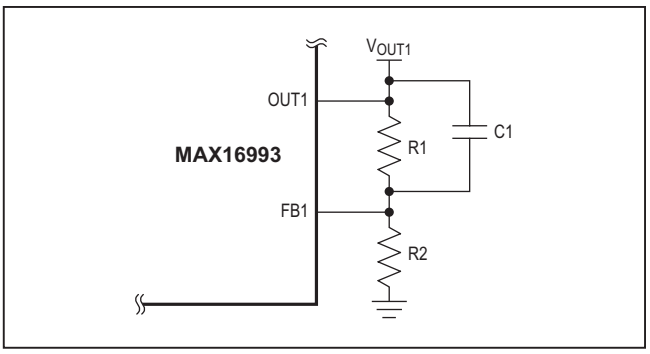


Figure 3. Adjustable OUT1 Voltage Configuration

OUT1 Current-Sense Resistor Selection

Choose the current-sense resistor based on the maximum inductor current ripple (K_{INDMAX}) and minimum current-limit threshold across current-sense resistor ($V_{LIM1MIN}$ = 0.1V).

The formula for calculating the current-sense resistor is:

$$Rcs_{MAX} = \frac{V_{LIM1MIN}}{I_{OUTMAX} \times \left(1 + \frac{K_{INDMAX}}{2}\right)}$$

where I_{OUTMAX} is the maximum load current for Buck 1 and K_{INDMAX} is the maximum inductor current ripple. The maximum inductor current ripple is a function of the inductor chosen, as well as the operating conditions, and is typically chosen between 0.3 and 0.4:

$$K_{INDMAX} = \frac{(V_{SUP} - V_{OUT}) \times D}{I_{OUTMAX} \times f_{SW1}[MHz] \times L[\mu H]}$$

where D is the duty cycle. Below is a numerical example to calculate the current-sense resistor in Figure 2. The maximum inductor current ripple is chosen at the maximum supply voltage (36V) to be 0.4:

$$Rcs_{MAX} = \frac{0.1}{I_{OUTMAX} \times \left(1 + \frac{K_{INDMAX}}{2}\right)}$$

$$= \frac{0.1}{5 \times \left(1 + \frac{0.4}{2}\right)} = 0.0166\,\Omega$$

OUT1 Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use

the following formulas to determine the minimum inductor value:

$$L_{MIN1}[H] = 1.3 \times \left[(V_{SUPMAX} - V_{OUT1}) \times \left(\frac{V_{OUT1}}{V_{SUPMAX}} \right) \times \left(\frac{1}{f_{SW1} \times I_{OUTMAX} \times K_{INDMAX}} \right) \right]$$

where f_{SW1} is the operating frequency and 1.3 is a coefficient that accounts for inductance initial precision.

or:

$$L_{MIN2}[H] = 1.3 \times \frac{V_{OUT1}}{0.8\,V} \times R_{CS} \times A_{V_CS} \times \frac{2.1 \times 10^6}{f_{SW1}}$$

where A_{V_CS} is current-sense amplifier gain (8V/V, typ).

For proper operation, the chosen inductor value must be greater than or equal to L_{MIN1} and L_{MIN2}. The maximum inductor value recommended is twice the chosen value from the above formulas.

Table 1 lists some of the inductor values for 5A output current and several switching frequencies and output voltages.

Buck 1 Input Capacitor

The device is designed to operate with a single 0.1µF capacitor on the V_{SUP} input and a single 0.1µF capacitor on the PV1 input. Place these capacitors as close as possible to their corresponding inputs to ensure the best EMI and jitter performance.

OUT1 Output Capacitor

The primary purpose of the OUT1 output capacitor is to reduce the change in V_{OUT1} during load transient conditions. The minimum capacitor depends on the output voltage, maximum current, and load regulation accuracy.

Use the following formula to determine the minimum output capacitor for Buck 1:

$$C_{OUT} \geq \frac{I_{OUT1(MAX)}}{2\pi \times f_{CO} \times \frac{\Delta V_{OUT1}}{V_{OUT1}} \times V_{OUT1}}$$

where f_{CO} is the crossover frequency set by R_C and C_C, and ΔV_{OUT1} is the allowable change in voltage during a load transient condition.

For proper functionality, ceramic capacitors must be used. Make sure that the self-resonance of the ceramic capacitors is above 1MHz to avoid instability.

Buck 1 MOSFET Selection

Buck 1 drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs are:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Minimum threshold voltage ($V_{TH(MIN)}$)
- Total gate charge (Q_G)
- Reverse transfer capacitance (C_{RSS})
- Power dissipation

Both n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V when V_{OUT1} is set to 5V or V_{GS} = 3V when V_{OUT1} is set to 3.3V. The conduction losses at minimum input voltage should not exceed MOSFET package thermal limits or violate the overall thermal budget. Also, ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget. In particular, check that the dV/dt caused by DH1 turning on does not pull up the DL1 gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, the power dissipation in the device due to drive losses must be checked. Both MOSFETs must be selected so that their total gate charge

Table 1. Inductor Values vs. (V_{SUPMAX}, V_{OUT1})

V_{SUPMAX} to V_{OUT1} (V)	V_{SUPMAX} = 36V, V_{OUT1} = 5V					V_{SUPMAX} = 36V, V_{OUT1} = 3.3V				
f_{SW1} (MHz)	2.1	1.05	0.525	0.420	0.350	2.1	1.05	0.525	0.420	0.350
INDUCTOR (µH), I_{LOAD} = 5A	1.5	3.3	5.6	6.8	8.2	1.0	2.2	4.7	4.7	6.8

is low enough; therefore, $PV1/V_{OUT1}$ can power both drivers without overheating the device:

$$P_{DRIVE} = V_{OUT1} \times (Q_{GTOTH} + Q_{GTOTL}) \times f_{SW1}$$

where Q_{GTOTL} is the low-side MOSFET total gate charge and Q_{GTOTH} is the high-side MOSFET total gate charge. Select MOSFETs with a $Q_{G_}$ total of less than 10nC. The selected MOSFET must have an input capacitance (C_{ISS}) less than 900pF (typ) to prevent possible damage to the device.

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the DH1 path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Compensation Network

The device uses a current-mode-control scheme that regulates the output voltage by forcing the required current through the external inductor, so the controller uses the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. A single series resistor (R_C) and capacitor (C_C) is all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 4). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP1 to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier (see Figure 4). The power modulator has a DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equation:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω and $g_{mc} = 1/(A_{V_CS} \times R_{DC})$ in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 8V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The unity-gain frequency of the power stage is set by C_{OUT} and g_{mc}:

$$f_{UGAINpMOD} = \frac{g_{mc}}{2\pi \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of like-value capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 660µS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 30MΩ (typ).

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output

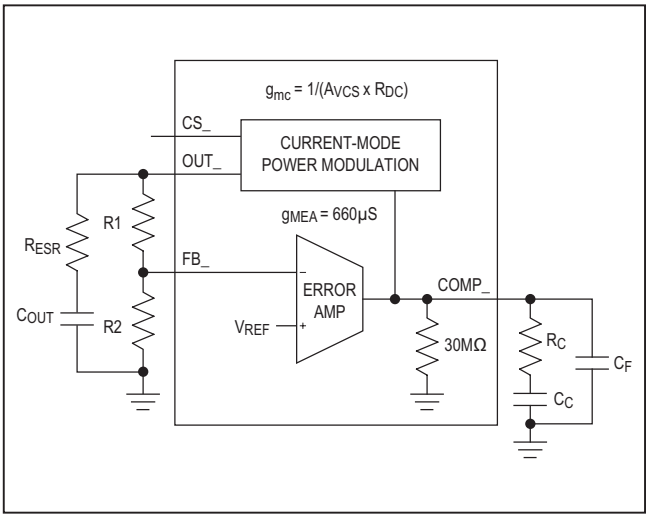


Figure 4. Compensation Network

capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)).

Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5 of the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_{CO} in the range:

$$f_{pMOD} << f_{CO} \le \frac{f_{SW}}{5}$$

At the crossover frequency, the total loop gain must be equal to 1.

Thus:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(R_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,EA} \times f_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP1 to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

Below is a numerical example to calculate the compensation network component values of Figure 4:

A_{V_CS} = 8V/V

R_{DCR} = 22mΩ

$g_{mc} = 1/(A_{V_CS} \times R_{DC}) = 1/(8 \times 0.022) = 5.68$

V_{OUT} = 5V

$I_{OUT(MAX)}$ = 5A

$R_{LOAD} = V_{OUT}/I_{OUT(MAX)} = 5V/6A = 0.833\Omega$

$C_{OUT} = 4 \times 47\mu F = 188\mu F$

ESR = 9mΩ/4 = 2.25mΩ

f_{SW} = 0.420MHz

$GAIN_{MOD(dc)} = 5.68 \times 0.833 = 4.73$

$$f_{pMOD} = \frac{1}{2\pi \times 188\,\mu F \times 0.833} \approx 1kHz$$

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

$1kHz << f_C \le 80.6\,kHz$, Select $f_C = 20\,kHz$

$$f_{zMOD} = \frac{1}{2\pi \times 2.25\,m\Omega \times 188\,\mu F} \approx 376\,kHz$$

Since $f_{zMOD} > f_C$:

$R_C \approx 33k\Omega$

$C_C \approx 4.7nF$

$C_F \approx 12pF$

OUT2/OUT3 Adjustable Output-Voltage Option

The device's adjustable output-voltage version (see the *Selector Guide* for details) allows the customer to set the outputs to any voltage between 0.8V and 3.95V. Connect a resistive divider from the buck converter output ($V_{OUT_(BUCK)}$) to OUT_ to GND to set the output voltage (Figure 5). Select R4 (OUT_ to GND resistor) less than

or equal to 100kΩ. Calculate R3 ($V_{OUT_(BUCK)}$ to OUT_ resistor) with the following equation:

$$R3 = R4\left[\left(\frac{V_{OUT_(BUCK)}}{V_{OUT_}}\right) - 1\right]$$

where $V_{OUT_}$ = 800mV (see the *Electrical Characteristics*).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor in parallel to R3 in the resistive divider network. Use the following equation to determine the value of the capacitor:

if R4/R3 > 1, C2 = C(R4/R3)

else, C2 = C, where C = 10pF.

For fixed output-voltage options, connect OUT_ to $V_{OUT_}$ for the factory-programmed, fixed-output voltage between 0.8V and 3.95V.

OUT2/OUT3 Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16993: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formulas to determine the minimum inductor value.

$$L_{MIN1} = \frac{\left(V_{IN} - V_{OUT_}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 35\%}$$

R_{CS}	0.378Ω for 1.5A channel 0.167Ω for 3.0A channel
I_{MAX}	3.0A or 1.5A depending on part number. Use the maximum output capability of the output channel for the part number being used.
f_{SW}	Operating frequency. This value is 2.1MHz unless externally synchronized to a different frequency.

The next equation ensures that the inductor current down slope is less than the internal slope compensation. For this to be the case the following equation needs to be satisfied:

-m ≥ m2/2

m2	The inductor current downslope. [V_{OUT}/L x R_{CS}]
-m	Slope Compensation [0.47 x V/µs]

Solving for L and adding a 1.5 multiplier to account for tolerances in the system:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.5$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two.

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 1.6 times the chosen value from the above formula.

$$L_{MAX} = 1.6 \times L_{MIN}$$

Select a nominal inductor value based on the following formula:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

OUT2/OUT3 Input Capacitor

Place a single 4.7µF ceramic bypass capacitor on the PV2 and PV3 inputs. Phase interleaving of the two low-voltage buck converters contributes to a lower required input capacitance by cancelling input ripple currents. Place the bypass capacitors as close as possible to their corresponding PV_ input to ensure the best EMI and jitter performance.

OUT2/OUT3 Output Capacitor

The minimum capacitor required depends on output voltage, maximum device current capability, and the error-amplifier voltage gain. Use the following formula to determine the required output capacitor value:

$$C_{OUT(MIN)} = \frac{V_{REF} \times G_{EAMP}}{2\pi \times f_{CO} \times V_{OUT} \times R_{CS}}$$

V_{REF}	Reference voltage, V_{REF} = 0.8V.
R_{CS}	Internal current-sense resistance. See the *Selector Guide* for the value for each specific part number. R_{CS} = 0.378Ω; for 1.5A output channels R_{CS} = 0.167Ω; for 3.0A output channels
f_{CO}	Target crossover frequency, which is 210kHz.
G_{EAMP}	Error-amplifier voltage gain. See the Selector Guide for the setting for each channel. 44.7V/V = Normal gain setting 31.7V/V = Low gain setting

The low gain setting trades off increased load-regulation error for a smaller output capacitor requirement. This allows optimization of system cost when system requirements allow for the increase in load regulation.

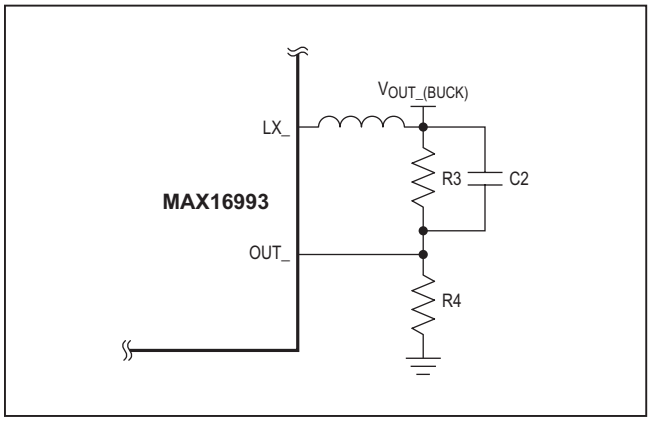


Figure 5. Adjustable OUT2/OUT3 Voltage Configuration

For proper functionality, ceramic capacitors must be used. Make sure that the self-resonance of the ceramic capacitors is above 1MHz to avoid instability.

Thermal Considerations

How much power the package can dissipate strongly depends on the mounting method of the IC to the PCB and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed is 2160mW in the side-wettable QFND package. More power dissipation can be handled by the package if great attention is given during PCB layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some MAX16993 applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JC} + \theta_{CA}}$$

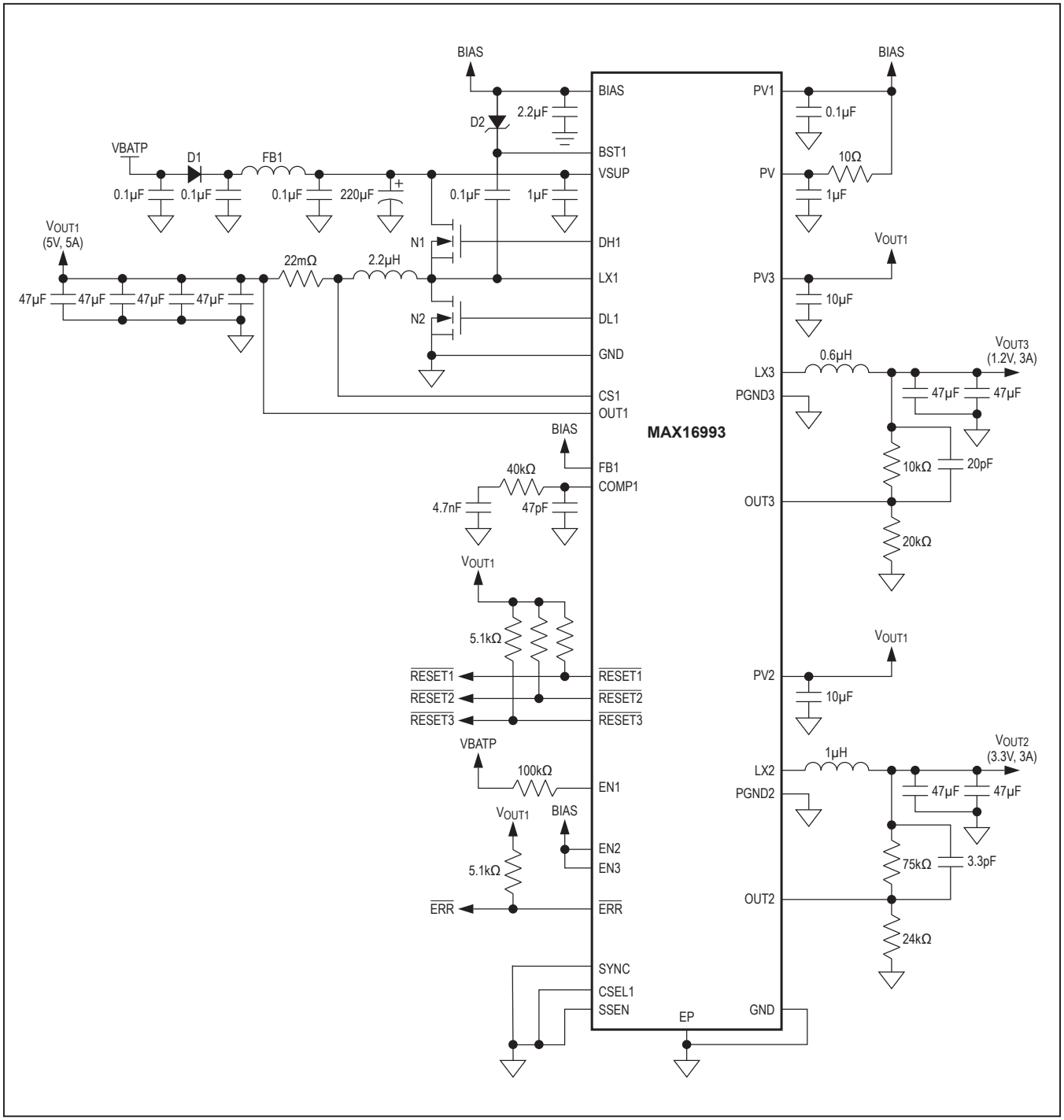
where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient air temperature, θ_{JC} (2.8°C/W for the side-wettable QFND) is the thermal resistance from the junction to the case, and θ_{CA} is the thermal resistance from the case to the surrounding air through the PCB, copper traces, and the package materials. θ_{CA} is directly related to system-level variables and can be modified to increase the maximum power dissipation. The QFND package has an exposed thermal pad on its underside. This pad provides a low thermal-resistance path for heat transfer into the PCB. This low thermally resistive path carries a majority of the heat away from the IC. The PCB is effectively a heatsink for the IC. The exposed pad should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed pad should be soldered to a thermal landing, which is connected to the ground plane by thermal vias. The thermal landing should be at least as large as the exposed pad and can be made larger depending on the amount of free space from the exposed pad to the other pin landings. A sample layout is available on the MAX16993 Evaluation Kit to speed designs.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible.
4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the device.
6) Use a single ground plane to reduce the chance of ground-potential differences. With a single ground plane, enough isolation between analog return signals and high-power signals must be maintained.

Typical Application Circuit



Selector Guide

OPTION	BUCK 1			BUCK 2			BUCK 3			SYNC
	FIXED OUTPUT VOLTAGE (V)	f_{SW1} DIVIDE RATIO FROM f_{SW}	ACTIVE TIMEOUT PERIOD (ms)	FIXED OUTPUT VOLTAGE (V)	MAX OUTPUT CURRENT (A)	ACTIVE TIMEOUT PERIOD (ms)	FIXED OUTPUT VOLTAGE (V)	MAX OUTPUT CURRENT (A)	ACTIVE TIMEOUT PERIOD (SAME AS BUCK 2) (ms)	
A	3.3/5.0	÷5	3.9	ADJ	3.0	3.9	ADJ	3.0	3.9	Input
B	3.3/5.0	÷5	3.9	3.15	1.5	3.9	1.8 (L)	1.5	3.9	Input
C	3.3/5.0	÷5	1.9	ADJ	1.5	1.9	ADJ	1.5	1.9	Input
D	3.3/5.0	÷5	3.9	1.05	3.0	3.9	3.3	1.5	3.9	Input
E	3.3/5.0	÷5	3.9	3.30	1.5	3.9	1.5	1.5	3.9	Input
F	3.3/5.0	÷5	3.9	3.3	1.5	3.9	1.2	1.5	3.9	Input
G	3.3/5.0	÷5	3.9	3.3	1.5	3.9	1.8	1.5	3.9	Input
H	3.3/5.2	÷5	3.9	3.3	3.0	3.9	1.8	1.5	3.9	Input
I	ADJ	÷5	1.9	ADJ	1.5	1.9	ADJ	1.5	1.9	Input
J*	3.3/5.0	÷4	3.9	ADJ	3.0	3.9	ADJ	3.0	3.9	Input
K	3.3/5.0	÷5	3.9	1.05	3.0	3.9	3.3	3.0	3.9	Input
L	3.3/4.9	÷5	3.9	3.3	1.5	3.9	1.25	1.5	3.9	Input

(L) = Low gain setting.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16993AGJ_/VY+	-40°C to +125°C	32 QFND-EP**
MAX16993ATJ_+	-40°C to +125°C	32 TQFN-EP†
MAX16993ATJ_/V+	-40°C to +125°C	32 TQFN-EP†

Note: *Insert the desired suffix letter (from the Selector Guide) into the blank to indicate buck switching frequency, active time-out period, fixed or adjustable output voltages, and maximum output current.*

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

***EP = Exposed pad/side-wettable flanked package.*

†EP = Exposed pad.

Contact factory for options that are not included. Factory-selectable features include:

- *f_{SW1} divide ratio with respect to master clock*
- *DC-DC output voltage*
- *Number of cycles in active timeout period*
- *Independent current limit for each channel up to 3A*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 QFND-EP	G3255Y+1	21-0563	90-0361
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/13	Initial release	—
1	8/13	Corrected package type (from TQFN to QFND)	1, 2, 9, 22, 24
2	10/13	Added TQFN package, and updated SYNC pin function, limit/short-circuit information, *Package Thermal Characteristics*, *Typical Application Circuit, Selector Guide*, *Ordering Information*, and *Package Information* sections	1, 2, 9, 10, 16, 23, 24
3	12/13	Updated bypass capacitor on PV pin in *Pin Description* and added /V TQFN package to *Ordering Information*	9, 24
4	2/14	Removed lossless DCR sensing from data sheet, updated *Typical Operating Circuit*, and updated G_{CS} values in *OUT2/OUT3 Output Capacitor* section	11, 15, 21
5	3/14	Corrected the G_{CS} equation and -m equation in the *OUT2/OUT3 Inductor Selection* tables; updated the TQFN package code in the *Package Information* table	20, 24
6	6/14	Removed references to SYNC output functionality: updated *General Description*, *Electrical Characteristics*, *Pin Description*, *General Description*, *Synchronization (SYNC)*, *OUT2/OUT3 Inductor Selection* sections, and *Typical Application Circuit* and *Ordering Information*	1, 5, 10, 12, 13, 20, 23, 24
7	7/14	Removed future product references from option F, G, H, and I variants in *Selector Guide*	24
8	7/14	Corrected equation for slope compensation	20
9	10/14	Removed future product reference and updated Option D in *Selector Guide,* corrected land pattern number for TQFN in *Package Information*	24
10	1/15	Added option J variant in *Selector Guide*	24
11	3/15	Updated *Benefits and Features*, added new Note 1 to *Absolute Maximum Ratings* and renumbered remaining notes in *Package Thermal Characteristics* and *Electrical Characteristics*, *added missing units in Electrical Characteristics*, clarified equations in *OUT1 Inductor* Selection, *Compensation Network,* and *OUT2/OUT3 Adjustable Output-Voltage Option* sections, updated *OUT2/OUT3 Inductor Selection* and *OUT2/OUT3 Output Capacitor* section, deleted Table 2 and Table 3, and added future product designation to option J variant in *Selector Guide*	1–5, 16, 19–21, 24
12	9/15	Miscellaneous updates	4, 14, 18, 20, 23
13	7/16	Updated *Absolute Maximum Ratings* and *Linear Regulator (BIAS)* sections; removed future product reference from Option K and added Option L in *Selector Guide*	2, 12, 23
14	12/16	Removed future product reference from Option L in *Selector Guide* and changed fixed output voltage from 3.3/5.0 to 3.3/4.9	23

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