19-4305; Rev 0; 10/08

EVALUATION KIT AVAILABLE

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

MAX17031

General Description

The MAX17031 is a dual Quick-PWM™ step-down power-supply (SMPS) controller with synchronous rectification, intended for main 5V/3.3V power generation in battery-powered systems. Low-side MOSFET sensing provides a simple low-cost, highly efficient current sense for valley current-limit protection. Combined with the output overvoltage and undervoltage protection features, this current limit ensures robust output supplies.

The 5V/3.3V SMPS outputs can save power by operating in pulse-skipping mode or in ultrasonic mode to avoid audible noise. Ultrasonic mode forces the controller to maintain switching frequencies greater than 20kHz at light loads. The SKIP input also has an accurate logic threshold, allowing it to be used as a secondary feedback input to refresh an external charge pump or secondary winding without overcharging the output voltages.

An internal 100mA linear regulator generates the 5V bias needed for power-up or other low-power "always-on" suspend supplies. An internal bypass circuitry allows automatic bypassing of the linear regulator when the 5V SMPS is active.

The device includes independent shutdown controls with well-defined logic thresholds to simplify power-up and power-down sequencing. To prevent current surges at startup, the internal voltage target is slowly ramped up from zero to the final target over a 1ms period. To prevent the output from ringing below ground in shutdown, the internal voltage target is ramped down from its previous value to zero over a 1ms period. A combined power-good (PGOOD) output simplifies the interface with external controllers. The MAX17031 is available in a 24-pin thin QFN (4mm x 4mm) package.

Applications

Notebook Computers

Ultra-Mobile PC

Main System Supply (5V and 3.3V Supplies)

2 to 4 Li+ Cells Battery-Powered Devices

Telecommunication

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Dual Quick-PWM**
- **Preset 5V and 3.3V Outputs**
- **Internal 100mA, 5V Linear Regulator**
- **Internal OUT1 LDO5 Bypass Switch**
- **Secondary Feedback (SKIP Input) Maintains Charge Pump**
- **3.3V, 5mA Real-Time Clock (RTC) Power (Always On)**
- **2V ±1% 50µA Reference**
- **6V to 24V Input Range**
- **Pulse-Skipping/Forced-PWM/Ultrasonic Mode Control**
- **Independent SMPS and LDO5 Enable Controls**
- **Combined SMPS PGOOD Outputs**
- **Minimal Component Count**

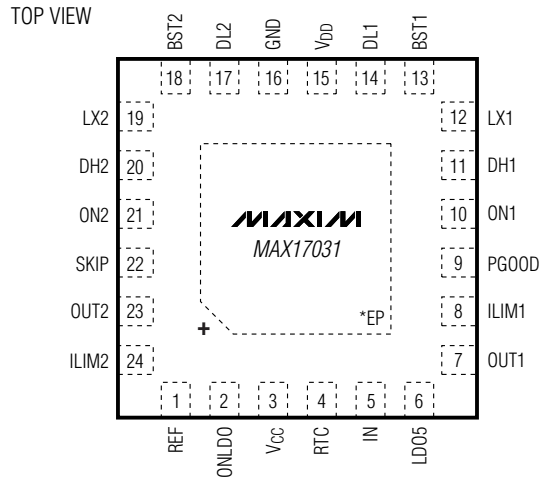
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17031ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



THIN QFN
4mm × 4mm

*EXPOSED PAD.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +28V
V_{DD}, V_{CC} to GND .....-0.3V to +6V
RTC, LDO5, ONLDO to GND .....-0.3V to +6V
OUT2 to GND .....-0.3V to +6V
ON1, ON2, PGOOD to GND.....-0.3V to +6V
OUT1 to GND.....-0.3V to (V_{LDO5} + 0.3V)
SKIP to GND.....-0.3V to (V_{CC} + 0.3V)
REF, ILIM1, ILIM2 to GND.....-0.3V to (V_{CC} + 0.3V)
DL_ to GND .....-0.3V to (V_{DD} + 0.3V)
BST_ to GND .....-0.3V to +36V
BST_ to V_{DD}.....-0.3V to +30V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
BST1 to LX1.....-0.3V to +6V
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
BST2 to LX2.....-0.3V to +6V
LDO5, RTC, REF Short Circuit to GND.....Momentary
RTC Current Continuous.....+5mA
LDO5 Current (Internal Regulator) Continuous .....+100mA
LDO5 Current (Switched Over) Continuous .....+200mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin, 4mm x 4mm Thin QFN (T2444-3)
(derate 27.8mW/°C above +70°C).....2.22W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note: Measurements are valid using a 20MHz bandwidth limit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
IN Input Voltage Range		LDO5 in regulation	6		24	V
IN Standby Supply Current		V_{IN} = 6V to 24V, ON1 = ON2 = GND, ONLDO = RTC		85	175	µA
IN Shutdown Supply Current		V_{IN} = 4.5V to 24V, ON1 = ON2 = ONLDO = GND		40	70	µA
IN Supply Current	I_{IN}	ON1 = ON2 = V_{CC}, V_{SKIP} = V_{CC}; V_{OUT1} = 5.3V, V_{OUT2} = 3.5V		0.1	0.2	mA
V_{CC} Bias Supply Current	I_{VCC}	ON1 = ON2 = V_{CC}, V_{SKIP} = V_{CC}; V_{OUT1} = 5.3V, V_{OUT2} = 3.5V		0.7	1.5	mA
PWM CONTROLLERS						
OUT1 Output-Voltage Accuracy	V_{OUT1}	V_{SKIP} = 1.8V	4.95	5.00	5.05	V
OUT2 Output-Voltage Accuracy	V_{OUT2}	V_{SKIP} = 1.8V	3.267	3.30	3.333	V
Load Regulation Error		Either SMPS, V_{SKIP} = 1.8V, I_{LOAD} = 0 to 5A		-0.1		%
		Either SMPS, V_{SKIP} = GND, I_{LOAD} = 0 to 5A		-1.7		
		Either SMPS, V_{SKIP} = V_{CC}, I_{LOAD} = 0 to 5A		-1.5		
Line Regulation Error		Either SMPS, IN = 6V to 28V		0.005		%/V
DH1 On-Time	t_{ON1}	V_{OUT1} = 5.0V (Note 1)	895	1052	1209	ns
DH2 On-Time	t_{ON2}	V_{OUT2} = 3.3V (Note 1)	833	925	1017	ns
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 1)		300	400	ns
Soft-Start Slew Rate	t_{SS}	Rising/falling edge on ON1 or ON2		1		ms
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	V_{SKIP} = GND	20	34		kHz

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (LDO5)						
LDO5 Output-Voltage Accuracy	V_{LDO5}	V_{IN} = 6V to 24V, ON1 = GND, 0 < I_{LDO5} < 100mA	4.90	5.0	5.10	V
LDO5 Short-Circuit Current		LDO5 = GND	100		260	mA
LDO5 Regulation Reduction/ Bootstrap Switchover Threshold		Falling edge of OUT1	-11.0	-8.8	-6.0	%
		Rising edge of OUT1		-7.0		
LDO5 Bootstrap Switch Resistance		LDO5 to OUT1, V_{OUT1} = 5V (Note 3)		1.9	4.5	Ω
V_{CC} Undervoltage Lockout Threshold		Falling edge of V_{CC}, PWM disabled below this threshold	3.8	4.0	4.3	V
		Rising edge of V_{CC}		4.2		
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 10°C		160		°C
3.3V ALWAYS-ON LINEAR REGULATOR (RTC)						
RTC Output-Voltage Accuracy	V_{RTC}	ON1 = ON2 = GND, V_{IN} = 6V to 24V, 0 < I_{RTC} < 5mA	3.23	3.33	3.43	V
		ON1 = ON2 = ONLDO = GND, V_{IN} = 6V to 24V, 0 < I_{RTC} < 5mA	3.19		3.47	
RTC Short-Circuit Current		RTC = GND	5		22	mA
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	1.980	2.00	2.020	V
Reference Load Regulation Error	ΔV_{REF}	I_{REF} = -20µA to +50µA	-10		+10	mV
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, 350mV (typ) hysteresis		1.95		V
OUT1 FAULT DETECTION						
OUT1 Overvoltage and PGOOD Trip Threshold		With respect to error comparator threshold	10	13	16	%
OUT1 Overvoltage Fault Propagation Delay	t_{OVP}	OUT1 forced 50mV above trip threshold		10		µs
OUT1 Undervoltage Protection Trip Threshold		With respect to error comparator threshold	65	70	75	%
OUT1 Output Undervoltage Fault Propagation Delay	t_{UVP}			10		µs
OUT2 FAULT DETECTION						
OUT2 Overvoltage and PGOOD Trip Threshold		With respect to error comparator threshold	10	13	16	%
OUT2 Overvoltage Fault Propagation Delay	t_{OVP}	OUT2 forced 50mV above trip threshold		10		µs
OUT2 Undervoltage Protection Trip Threshold		With respect to error comparator threshold	65	70	75	%
OUT2 Output Undervoltage Fault Propagation Delay	t_{UVP}			10		µs

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-GOOD							
PGOOD Lower Trip Threshold		With respect to **either** error comparator threshold, falling edge, hysteresis = 1%		-16	-13	-10	%
PGOOD Propagation Delay	t_{PGOOD}	OUT1 or OUT2 forced 50mV beyond PGOOD trip threshold, falling edge			10		µs
PGOOD Output Low Voltage		ON1 or ON2 = GND (PGOOD low impedance), I_{SINK} = 4mA				0.3	V
PGOOD Leakage Current	I_{PGOOD}	OUT1 and OUT2 in regulation (PGOOD high impedance), PGOOD forced to 5.5V, T_A = +25°C				1	µA
CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2	V
ILIM_ Current					5		µA
Valley Current-Limit Threshold (Adjustable)	$V_{LIM_(VAL)}$	V_{AGND} - $V_{LX_}$	$R_{ILIM_}$ = 100kΩ ($V_{ILIM_}$ = 500mV)	44	50	56	mV
			$R_{ILIM_}$ = 200kΩ ($V_{ILIM_}$ = 1.00V)	90	100	110	
			$R_{ILIM_}$ = 400kΩ ($V_{ILIM_}$ = 2.00V)	180	200	220	
Current-Limit Threshold (Negative)	V_{NEG}	With respect to valley current-limit threshold, V_{SKIP} = V_{REF}			-120		%
Ultrasonic Current-Limit Threshold	$V_{NEG(US)}$	V_{OUT2} = 3.5V, V_{OUT1} = 5.3V			20		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{AGND} - $V_{LX_}$, V_{SKIP} = V_{CC} or GND			1.5		mV
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST1 - LX1 and BST2 - LX2 forced to 5V			1.5	3.5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL1, DL2; high state			1.4	4.5	Ω
		DL1, DL2; low state			0.5	1.5	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH1, DH2 forced to 2.5V, BST1 - LX1 and BST2 - LX2 forced to 5V			2		A
DL_ Gate-Driver Source Current	I_{DL} (SOURCE)	DL1, DL2 forced to 2.5V			1.7		A
DL_ Gate-Driver Sink Current	$I_{DL\ (SINK)}$	DL1, DL2 forced to 2.5V			3.3		A
Dead Time	t_{DEAD}	DL1, DL2 rising (Note 4)			30		ns
		DH1, DH2 rising (Note 4)			35		
Internal BST_ Switch On-Resistance	R_{BST}	$I_{BST_}$ = 10mA, V_{DD} = 5V			5.5		Ω
BST_Leakage Current		$V_{BST_}$ = 26V, T_A = +25°C; OUT1 and OUT2 above regulation threshold			0.1	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUTS AND OUTPUTS							
SKIP Input Thresholds		Upper SKIP/PWM threshold falling edge, 33mV hysteresis		1.94	2.0	2.06	V
		Lower PWM/ultrasonic threshold		0.4		1.6	
SKIP Leakage Current		V_{SKIP} = 0 or 5V, T_A = +25°C		-1		+1	µA
ON_ Input-Logic Levels		ONLDO, ON1, ON2	High (SMPS on)	2.4			V
			Low (SMPS off)			0.8	
ON_ Leakage Current		V_{ON1} = V_{ON2} = V_{ONLDO} = 0 or 5V, T_A = +25°C		-2		+2	µA
OUT_ Leakage Current		V_{ON1} = V_{ON2} = V_{CC}	V_{OUT1} = 5.3V	15		65	µA
			V_{OUT2} = 3.5V	5		30	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
IN Input Voltage Range		LDO5 in regulation	6		24	V
IN Standby Supply Current		V_{IN} = 6V to 24V, ON1 = ON2 = GND, ONLDO = RTC			200	µA
IN Shutdown Supply Current		V_{IN} = 4.5V to 24V, ON1 = ON2 = ONLDO = GND			70	µA
IN Supply Current	I_{IN}	ON1 = ON2 = V_{CC}, V_{SKIP} = V_{CC}, V_{OUT1} = 5.3V, V_{OUT2} = 3.5V			0.2	mA
V_{CC} Bias Supply Current	I_{VCC}	ON1 = ON2 = V_{CC}, V_{SKIP} = V_{CC}, V_{OUT1} = 5.3V, V_{OUT2} = 3.5V			1.5	mA
PWM CONTROLLERS						
OUT1 Output-Voltage Accuracy	V_{OUT1}	V_{SKIP} = 1.8V	4.90		5.10	V
OUT2 Output-Voltage Accuracy	V_{OUT2}	V_{SKIP} = 1.8V	3.234		3.366	V
DH1 On-Time	t_{ON1}	V_{OUT1} = 5.0V (Note 1)	895		1209	ns
DH2 On-Time	t_{ON2}	V_{OUT2} = 3.3V (Note 1)	833		1017	ns
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 1)			400	ns
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	V_{SKIP} = GND	18			kHz

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (LDO5)						
LDO5 Output-Voltage Accuracy	V_{LDO5}	V_{IN} = 6V to 24V, ON1 = GND; 0mA < I_{LDO5} < 100mA	4.85		5.15	V
LDO5 Short-Circuit Current		LDO5 = GND			260	mA
LDO5 Regulation Reduction/ Bootstrap Switchover Threshold		Falling edge of OUT1	-12.0		-5.0	%
LDO5 Bootstrap Switch Resistance		LDO5 to OUT1, V_{OUT1} = 5V (Note 3)			4.5	Ω
V_{CC} Undervoltage Lockout Threshold		Falling edge of V_{CC}, PWM disabled below this threshold	3.8		4.3	V
3.3V ALWAYS-ON LINEAR REGULATOR (RTC)						
RTC Output-Voltage Accuracy	V_{RTC}	ON1 = ON2 = GND, V_{IN} = 6V to 24V, 0 < I_{RTC} < 5mA	3.18		3.45	V
		ON1 = ON2 = ONLDO = GND, V_{IN} = 6V to 24V, 0 < I_{RTC} < 5mA	3.16		3.50	
RTC Short-Circuit Current		RTC = GND	5		22	mA
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	1.975		2.025	V
Reference Load Regulation Error	ΔV_{REF}	I_{REF} = -20µA to +50µA	-10		+10	mV
OUT1 FAULT DETECTION						
OUT1 Overvoltage and PGOOD Trip Threshold		With respect to error comparator threshold	10		16	%
OUT1 Undervoltage Protection Trip Threshold		With respect to error comparator threshold	63		77	%
OUT2 FAULT DETECTION						
OUT2 Overvoltage and PGOOD Trip Threshold		With respect to error comparator threshold	10		16	%
OUT2 Undervoltage Protection Trip Threshold		With respect to error comparator threshold	63		77	%
POWER-GOOD						
PGOOD Lower Trip Threshold		With respect to **either** error comparator threshold, falling edge, hysteresis = 1%	-16		-10	%
PGOOD Output Low Voltage		ON1 or ON2 = GND (PGOOD low impedance), I_{SINK} = 4mA			0.3	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, no load on LDO5, RTC, OUT1, OUT2, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SKIP} = 5V, ONLDO = RTC, ON1 = ON2 = V_{CC}, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2	V
Valley Current-Limit Threshold (Adjustable)	$V_{LIM_ (VAL)}$	V_{AGND} - $V_{LX_}$	$R_{ILIM_}$ = 100kΩ ($V_{ILIM_}$ = 500mV)	40		60	mV
			$R_{ILIM_}$ = 200kΩ ($V_{ILIM_}$ = 1.00V)	85		115	
			$R_{ILIM_}$ = 400kΩ ($V_{ILIM_}$ = 2.00V)	164		236	
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST1 - LX1 and BST2 - LX2 forced to 5V				3.5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL1, DL2; high state				4.5	Ω
		DL1, DL2; low state				1.5	
INPUTS AND OUTPUTS							
SKIP Input Thresholds		Upper SKIP/PWM threshold falling edge, 33mV hysteresis		1.94		2.06	V
		Lower PWM/ultrasonic threshold		0.4		1.6	
ON_ Input-Logic Levels		ONLDO, ON1, ON2	High (SMPS on)	2.4			V
			Low (SMPS off)			0.8	

Note 1: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

Note 2: Specifications to T_A = -40°C are guaranteed by design and not production tested.

Note 3: Specification increased by 1Ω to account for test measurement error.

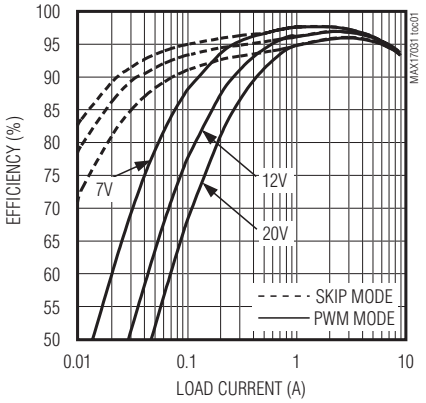
Note 4: Production tested for functionality only.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

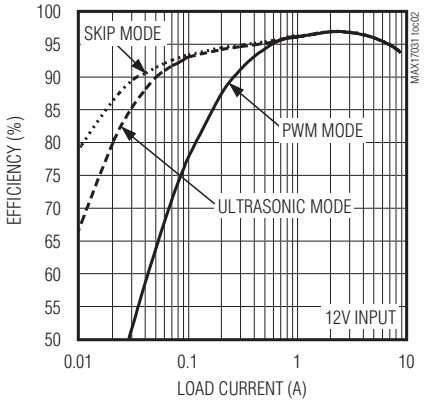
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

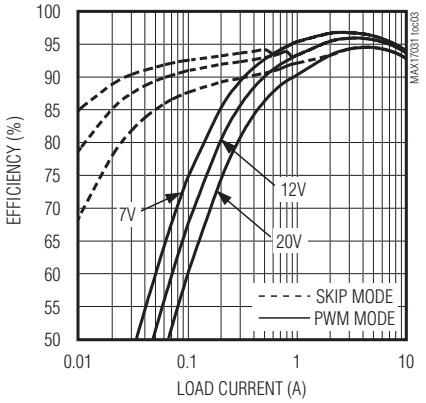
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



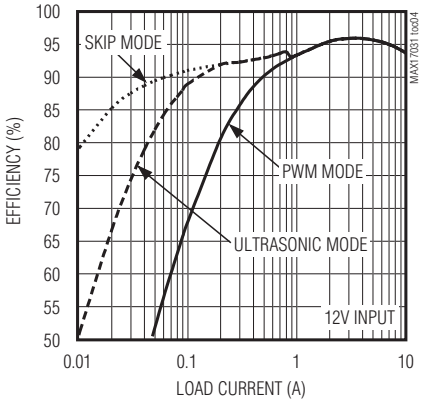
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



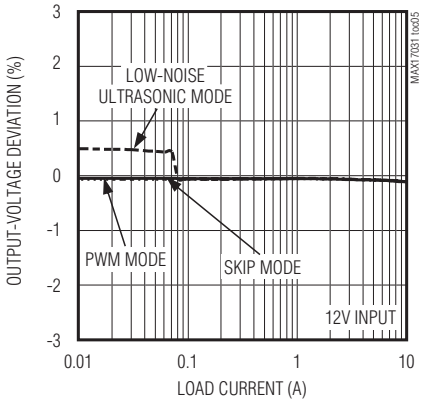
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



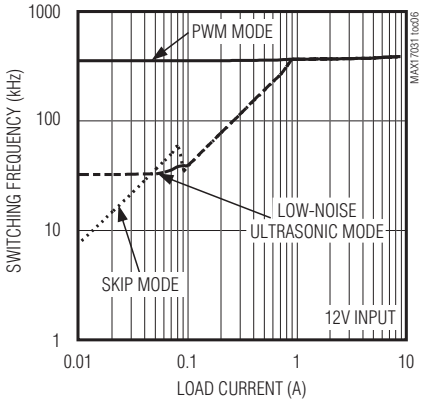
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



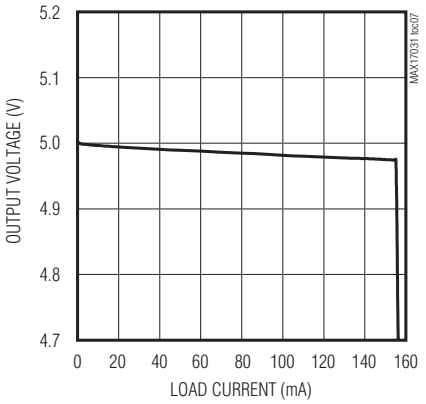
SMPS OUTPUT-VOLTAGE DEVIATION vs. LOAD CURRENT



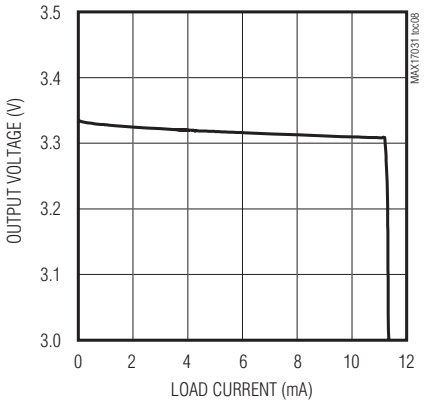
SWITCHING FREQUENCY vs. LOAD CURRENT



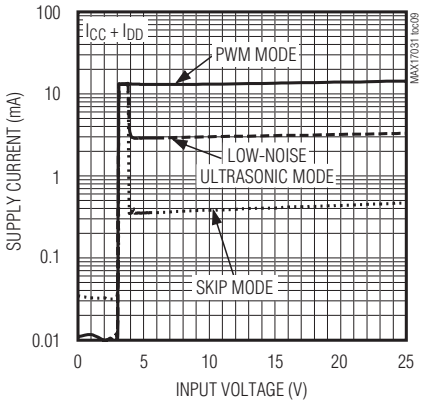
5V LDO OUTPUT VOLTAGE vs. LOAD CURRENT



3.3V RTC OUTPUT VOLTAGE vs. LOAD CURRENT



NO-LOAD INPUT SUPPLY CURRENT vs. INPUT VOLTAGE

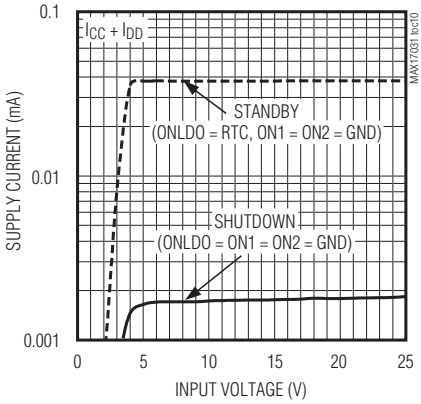


Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

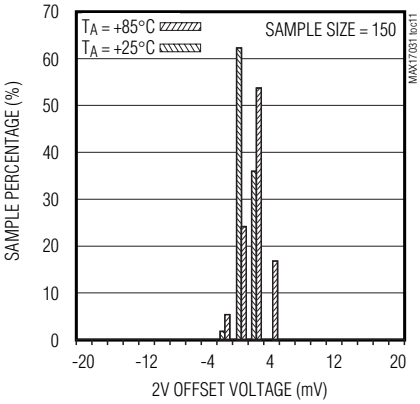
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

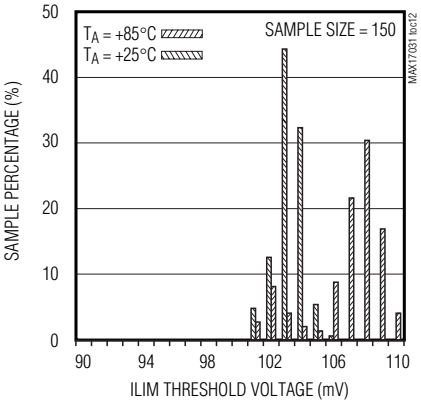
STANDBY AND SHUTDOWN INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



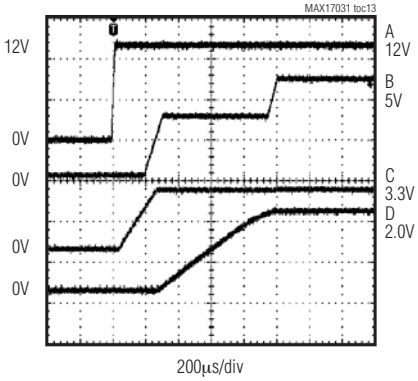
REFERENCE OFFSET VOLTAGE DISTRIBUTION



100mV ILIM THRESHOLD VOLTAGE DISTRIBUTION

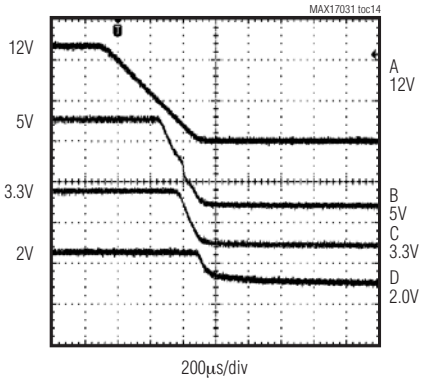


LDO AND RTC POWER-UP



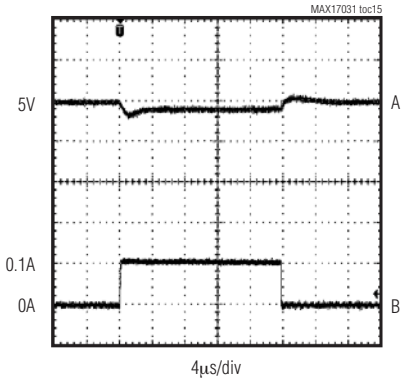
A. INPUT SUPPLY, 5V/div
B. 5V LDO, 2V/div
C. 3.3V RTC, 2V/div
D. 1.0 REF, 1V/div

LDO AND RTC POWER REMOVAL



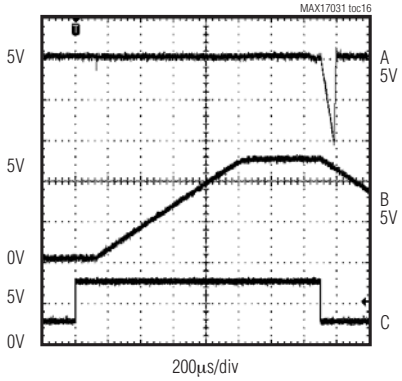
A. INPUT SUPPLY, 5V/div
B. 5V LDO, 2V/div
C. 3.3V RTC, 2V/div
D. 2.0 REF, 1V/div

5V LDO LOAD TRANSIENT



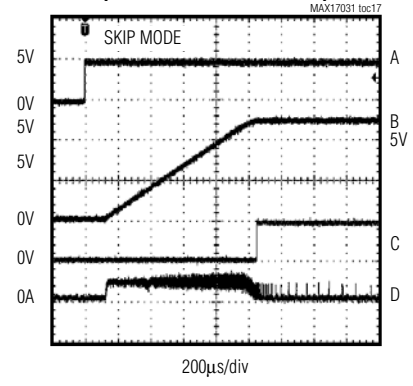
A. LDO OUTPUT, 100mV/div
B. LDO CURRENT, 100mA/div

5V SMPS STARTUP AND SHUTDOWN



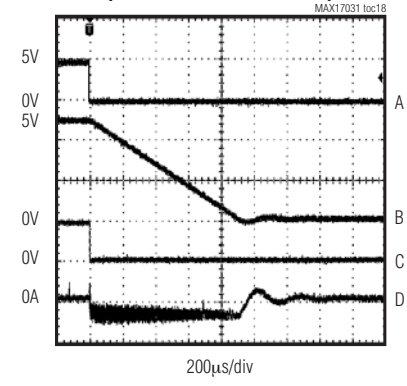
A. 5V LDO OUTPUT, 0.2V/div
B. 5V SMPS OUTPUT, 2V/div
C. ON1, 5V/div

STARTUP WAVEFORMS (SWITCHING REGULATORS)



A. ON1, 5V/div
B. 5V SMPS OUTPUT, 2V/div
C. PGOOD, 5V/div
D. INDUCTOR CURRENT, 5A/div

SHUTDOWN WAVEFORMS (SWITCHING REGULATORS)



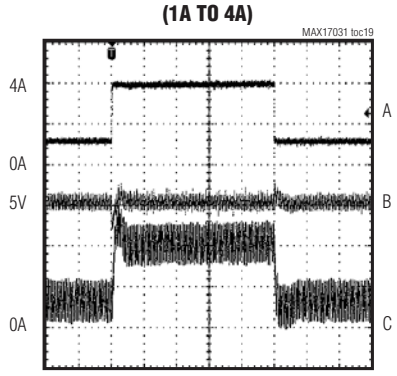
A. ON1, 5V/div
B. 5V SMPS OUTPUT, 2V/div
C. PGOOD, 2V/div
D. INDUCTOR CURRENT, 5A/div

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Typical Operating Characteristics (continued)

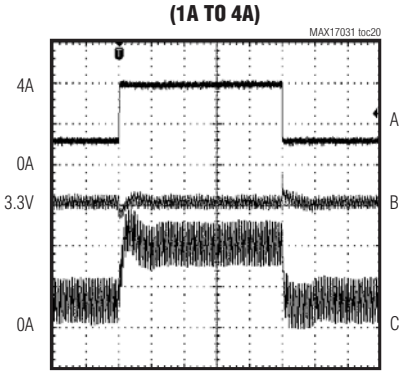
(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

5V SMPS LOAD TRANSIENT (1A TO 4A)



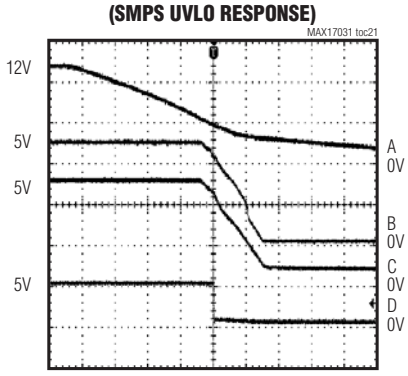
A. LOAD CURRENT, 2A/div C. INDUCTOR CURRENT, 2A/div
B. 5V SMPS OUTPUT, 100mV/div

3.3V SMPS LOAD TRANSIENT (1A TO 4A)



A. LOAD CURRENT, 2A/div C. INDUCTOR CURRENT, 2A/div
B. 3.3V SMPS OUTPUT, 100mV/div

POWER REMOVAL (SMPS UVLO RESPONSE)



A. INPUT VOLTAGE, 5V/div C. 5V SMPS, 2V/div
B. 5V LDO OUTPUT, 2V/div D. PGOOD, 5V/div

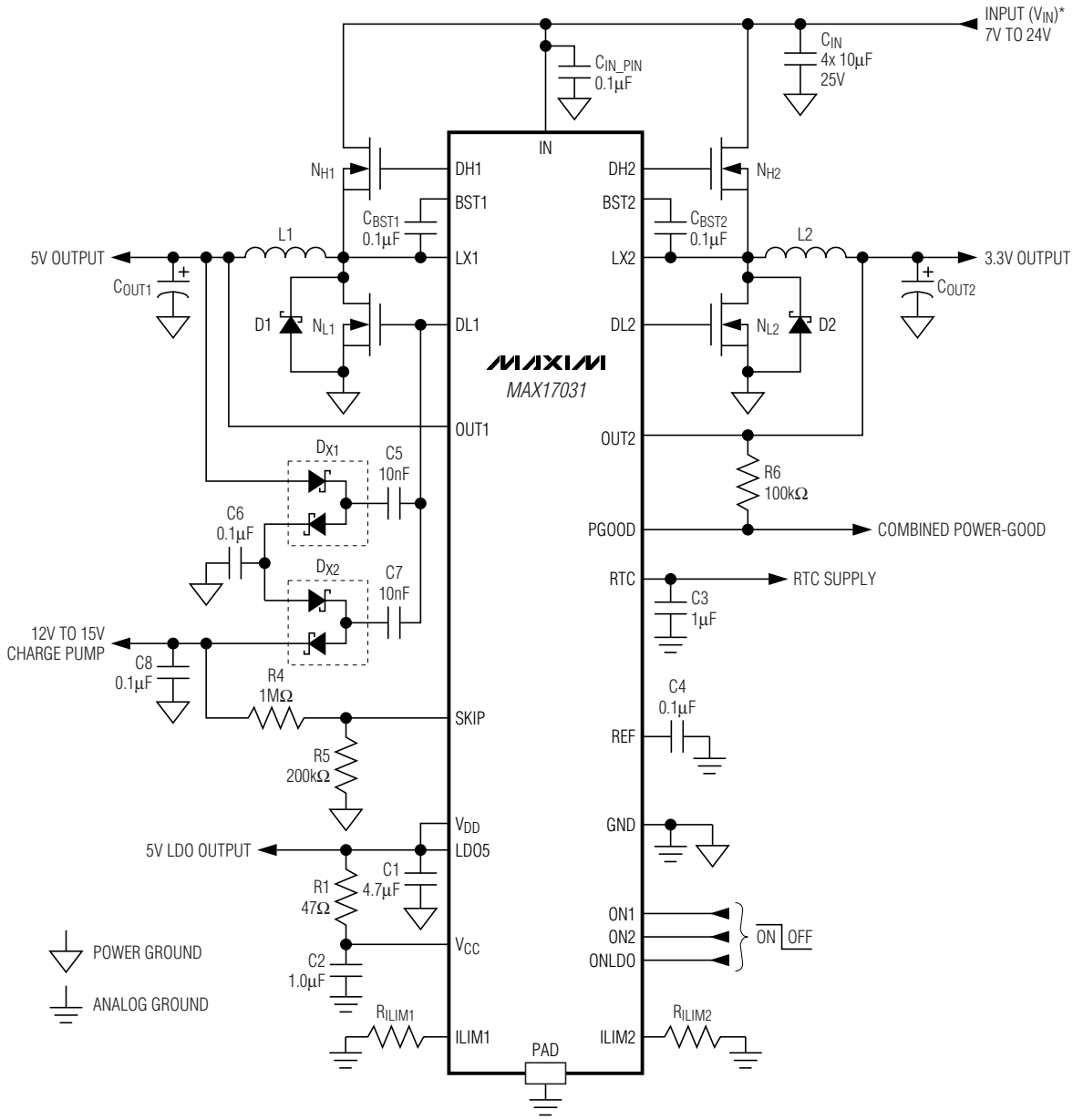
Pin Description

PIN	NAME	FUNCTION
1	REF	2V Reference Voltage Output. Bypass REF to analog ground with a 0.22µF or greater ceramic capacitor. The reference can source up to 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error (see *Typical Operating Characteristics*). The reference shuts down when ON1, ON2, and ONLDO are all pulled low.
2	ONLDO	Enable Input for LDO5. Drive ONLDO high (**pull up to RTC**) to enable the linear regulator (LDO5) output. Drive ONLDO low to shut down the linear regulator output. When ONLDO is high, LDO5 must supply V_{CC} and V_{DD}.
3	V_{CC}	Analog Supply Voltage Input. Connect V_{CC} to the system supply voltage with a series 50Ω resistor, and bypass to analog ground using a 1µF or greater ceramic capacitor.
4	RTC	3.3V Always-On Linear Regulator Output for RTC Power. Bypass RTC with a 1µF or greater ceramic capacitor to analog ground. RTC can source up to 5mA for external loads.
5	IN	Power Input Supply. Bypass IN with a 0.1µF or greater ceramic capacitor to GND. IN powers the linear regulators (RTC and LDO5) and senses the input voltage for the Quick-PWM on-time one-shot timer. The DH on-time is inversely proportional to input voltage.
6	LDO5	5V Linear Regulator Output. Bypass LDO5 with a 4.7µF or greater ceramic capacitor to GND. LDO5 can source 100mA for external load support. LDO5 is powered from IN.
7	OUT1	Output-Voltage Sense Input for SMPS1 and Linear Regulator Bypass Input. OUT1 is an input to the Quick-PWM on-time one-shot timer. OUT1 also serves as the feedback input for the SMPS1. When OUT1 exceeds 93.5% of the LDO5 voltage, the controller bypasses the LDO5 output to OUT1. The bypass switch is disabled if the OUT1 voltage drops by 8.5% from LDO5 nominal regulation threshold.
8	ILIM1	Valley Current-Limit Adjustment for SMPS1. The GND - LX1 current-limit threshold is 1/10 the voltage present on ILIM1 over a 0.2V to 2V range. An internal 5µA current source allows this voltage to be set with a single resistor between ILIM1 and analog ground.

Pin Description (continued)

PIN	NAME	FUNCTION
9	PGOOD	Open-Drain Power-Good Output for SMPS1 and SMPS2. PGOOD is low when either output voltage is more than 15% (typ) below the nominal regulation threshold, during soft-start, in shutdown, **when either SMPS is disabled,** and after the fault latch has been tripped. After the soft-start circuit has terminated, PGOOD becomes high impedance if both outputs are in regulation.
10	ON1	Enable Input for SMPS1. Drive ON1 high to enable SMPS1. Drive ON1 low to shut down SMPS1.
11	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1.
12	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 is the lower supply rail for the DH1 high-side gate driver.
13	BST1	Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST1 allows the DH1 turn-on current to be adjusted.
14	DL1	Low-Side Gate-Driver Output for SMPS1. DL1 swings from power GND to V_{DD}.
15	V_{DD}	Supply Voltage Input for the DL_ Gate Drivers. V_{DD} is internally connected to the drain of the HVPV BST diode switch. Connect to a 5V supply, and bypass V_{DD} to power GND with a 1µF or greater ceramic capacitor.
16	GND	Analog and Power Ground
17	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from power GND to V_{DD}.
18	BST2	Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST2 allows the DH2 turn-on current to be adjusted.
19	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower supply rail for the DH2 high-side gate driver.
20	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2.
21	ON2	Enable Input for SMPS2. Drive ON2 high to enable SMPS2. Drive ON2 low to shut down SMPS2.
22	SKIP	Pulse-Skipping Control Input. This three-level input determines the operating mode for the switching regulators: High (> 2V) = pulse-skipping mode Middle (1.8V) = forced-PWM mode GND = ultrasonic mode
23	OUT2	Output-Voltage Sense Input for SMPS2. OUT2 is an input to the Quick-PWM on-time one-shot timer. OUT2 also serves as the feedback input for the preset 3.3V.
24	ILIM2	Valley Current-Limit Adjustment for SMPS2. The GND - LX2 current-limit threshold is 1/10 the voltage present on ILIM2 over a 0.2V to 2V range. An internal 5µA current source allows this voltage to be set with a single resistor between ILIM2 and analog ground.
—	EP	Exposed Pad. Connect backside exposed pad to analog GND and power GND.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies



*__NOTE:__ LOWER INPUT VOLTAGES REQUIRE ADDITIONAL INPUT CAPACITANCE. IF OPERATING NEAR DROPOUT, COMPONENT SELECTION MUST BE CAREFULLY DONE TO ENSURE PROPER OPERATION.

Figure 1. Standard Application Circuit—Main Supply

Table 1. Component Selection for Standard Applications

COMPONENT	400kHz/300kHz SMPS1: 5V AT 5A SMPS2: 3.3V AT 8A
Input Voltage	V_{IN} = 7V to 24V
Input Capacitor (C_{IN})	4X 10µF, 25V Taiyo Yuden TMK432BJ106KM
SMPS 1	
Output Capacitor (C_{OUT1})	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB
Inductor (L1)	4.3µH, 11.4mΩ, 11A Sumida CEP125U
High-Side MOSFET (N_{H1})	Siliconix Si4800BDY 23mΩ/30mΩ 30V
Low-Side MOSFET (N_{L1})	Siliconix Si4812BDY 16.5mΩ/20mΩ 30V
Current-Limit Resistor (R_{ILIM1})	71kΩ
SMPS 2	
Output Capacitor (C_{OUT2})	2x 150µF, 4V, 35mΩ SANYO 4TPE150MAZB
Inductor (L2)	2.2µH, 5.4mΩ, 14A Sumida CEP125U
High-Side MOSFET (N_{H2})	Siliconix Si4684DY 9.2mΩ/11.5mΩ, 30V
Low-Side MOSFET (N_{L2})	Siliconix Si4430BDY 4.8mΩ/6.0mΩ, 30V
Current-Limit Resistor (R_{ILIM2})	71kΩ

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avx.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC/TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.coml
Philips/nxp Semiconductor	www.semiconductors.philips.com
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www,sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com
Würth Elektronik GmbH & Co. KG	www.we-online.com

Detailed Description

The MAX17031 step-down controller is ideal for high-voltage, low-power supplies for notebook computers. Maxim's Quick-PWM pulse-width modulator in the MAX17031 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. Figure 2 is the functional diagram overview and Figure 3 is the Quick-PWM core functional diagram.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

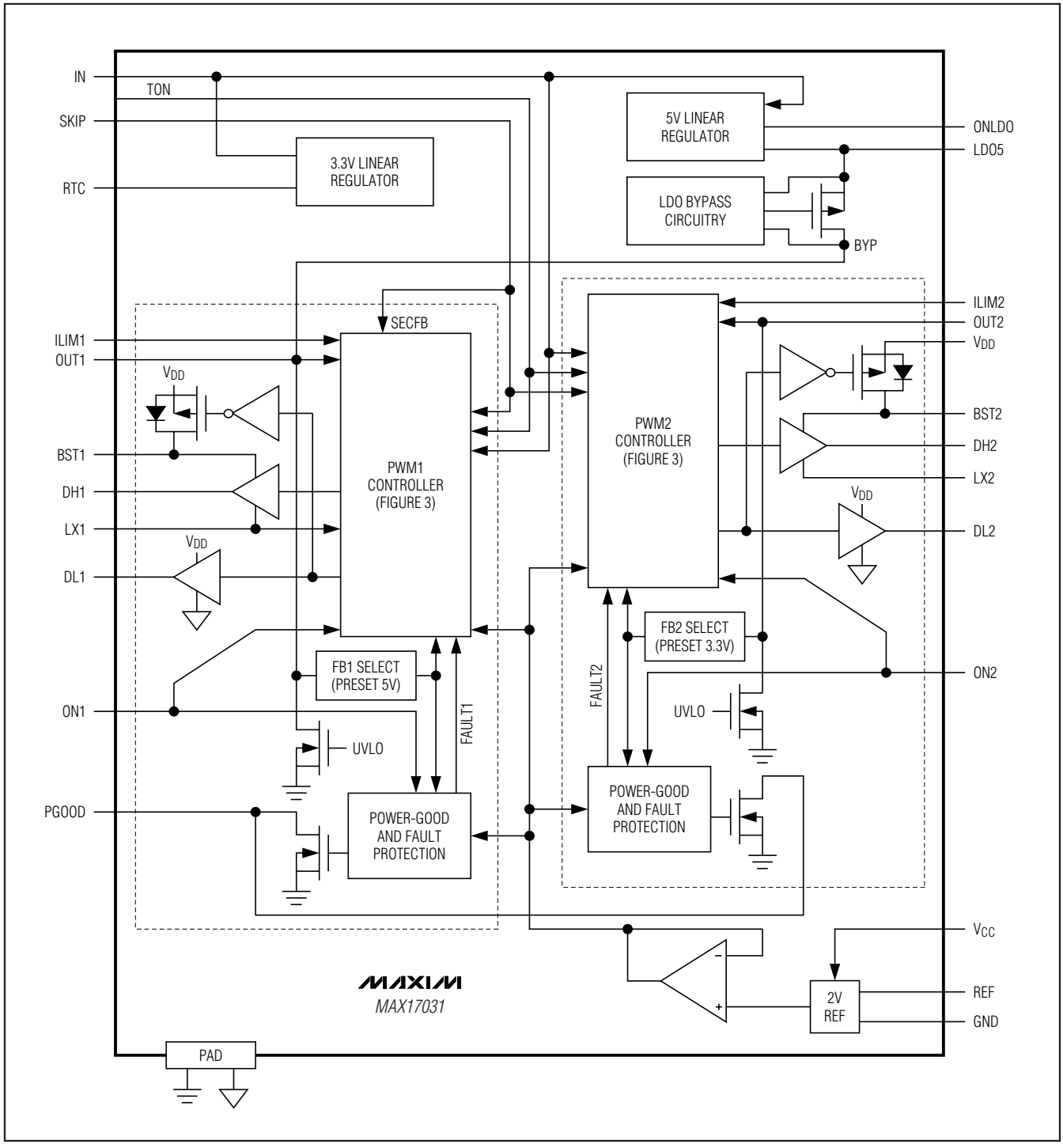


Figure 2. Functional Diagram Overview

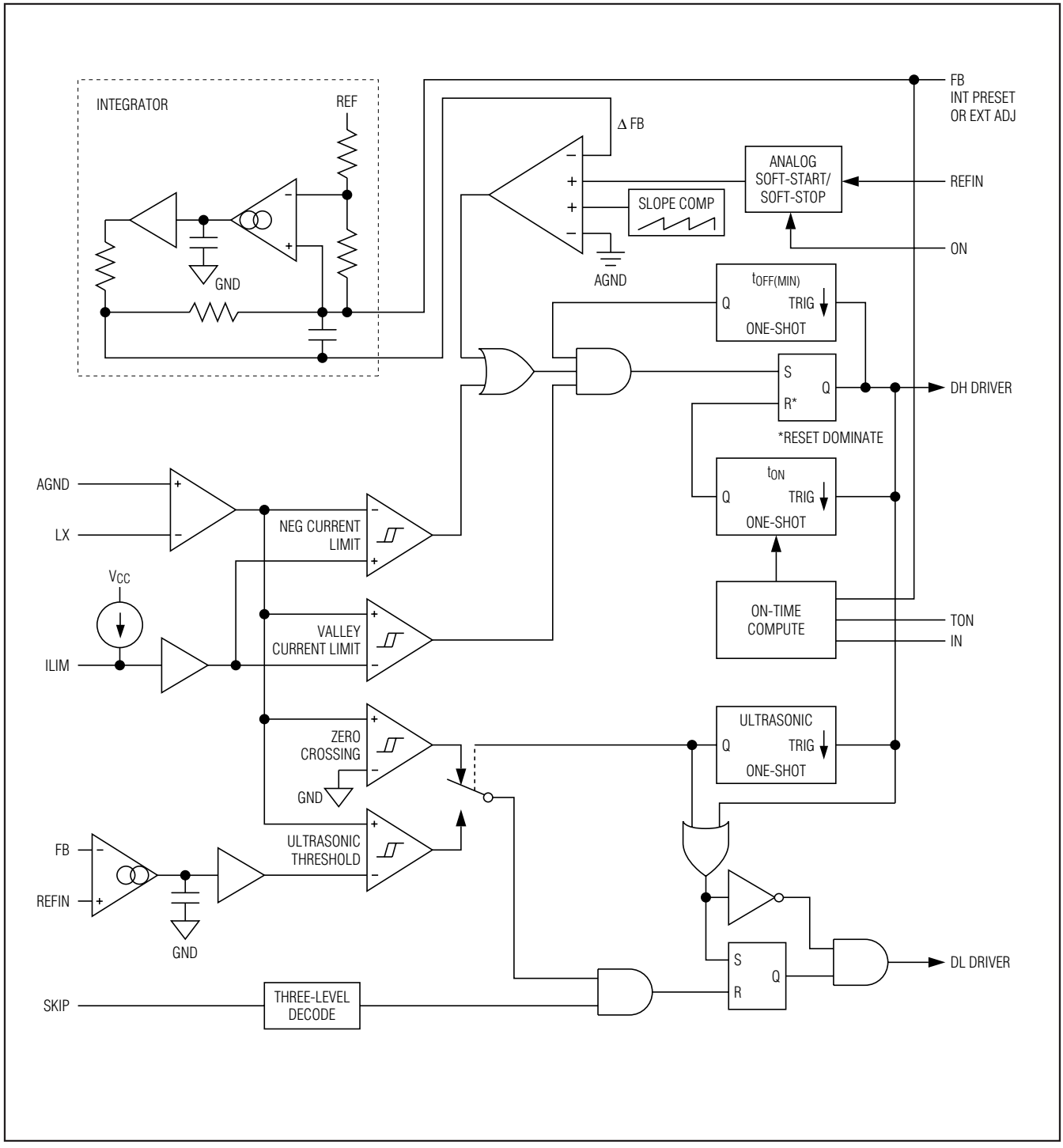


Figure 3. Functional Diagram—Quick-PWM Core

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

The MAX17031 includes several features for multipurpose notebook functionality, and is specifically designed for 5V/3.3V main power-supply rails. The MAX17031 includes a 100mA, 5V linear regulator (LDO5) ideal for initial power-up of the notebook and main supply. Additionally, the MAX17031 includes a 3.3V, 5mA RTC supply that remains always enabled, which can be used to power the RTC supply and system pullups when the notebook shuts down. The MAX17031 also includes a SKIP mode control input with an accurate threshold that allows an unregulated charge pump or secondary winding to be automatically refreshed—ideal for generating the low-power 12V to 15V load switch supply.

3.3V RTC Power

The MAX17031 includes a low-current (5mA) linear regulator that remains active as long as the input supply (IN) exceeds 2V (typ). The main purpose of this "always-enabled" linear regulator is to power the RTC when all other notebook regulators are disabled. The RTC regulator sources at least 5mA for external loads.

Preset 5V, 100mA Linear Regulator

The MAX17031 includes a high-current (100mA) 5V linear regulator. This LDO5 is required to generate the 5V bias supply necessary to power up the switching regulators. Once the 5V switching regulator (MAX17031 OUT1) is enabled, LDO5 is bypassed to OUT1. The MAX17031 LDO5 sources at least 100mA of supply current.

Bypass Switch

The MAX17031 includes an LDO5 bypass switch that allows the LDO5 to be bypassed to OUT1. When OUT1 exceeds 93.5% of the LDO5 output voltage for 500µs, then the MAX17031 reduces the LDO5 regulation threshold and turns on an internal p-channel MOSFET to short OUT1 to LDO5. Instead of disabling the LDO5 when the MAX17031 enables the bypass switch, the controller reduces the LDO5 regulation voltage, which effectively places the linear regulator in a standby state while switched over, allowing a fast recovery if the OUT1 drops by 8.5% from LDO5 nominal regulation threshold.

5V Bias Supply (V_{CC}/V_{DD})

The MAX17031 requires an external 5V bias supply (V_{DD} and V_{CC}) in addition to the battery. Typically, this 5V bias supply is generated by the internal 100mA LDO5 or from the notebook's 95%-efficient 5V main supply. Keeping these bias supply inputs independent improves the overall efficiency. When ONLDO is enabled, V_{DD} and V_{CC} must be supplied from LDO5.

The V_{DD} bias supply input powers the internal gate drivers and the V_{CC} bias supply input powers the analog control blocks. The maximum current required is dominated by the switching losses of the drivers and can be estimated as follows:

$$I_{BIAS(MAX)} = I_{CC(MAX)} + f_{SW}Q_G \approx 30mA \text{ to } 60mA \text{ (typ)}$$

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as sensed by IN, and proportional to the feedback voltage:

$$t_{ON} = \frac{K \times V_{OUT}}{V_{IN}}$$

where K (switching period) is set 2.5µs for side 1 and 3.3µs for side 2. For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON} \times (V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{DROP2} is the sum of the parasitic voltage drops in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the MAX17031.

Modes of Operation

Forced-PWM Mode (V_{SKIP} = 1.8V)

The low-noise forced-PWM mode (V_{SKIP} = 1.8V) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 20mA to 60mA depending on the switching frequency and MOSFET selection.

The MAX17031 automatically uses forced-PWM operation during shutdown regardless of the SKIP configuration.

Automatic Pulse-Skipping Mode (V_{SKIP} > 2V)

In skip mode (V_{SKIP} > 2V), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator output is set by the differential voltage across LX and GND.

DC output-accuracy specifications refer to the integrated threshold of the error comparator. When the inductor is in continuous conduction, the MAX17031 regulates the valley of the output ripple and the internal integrator removes the actual DC output-voltage error caused by the output-ripple voltage and internal slope compensation. In discontinuous conduction (V_{SKIP} > 2V and I_{OUT} < $I_{LOAD(SKIP)}$), the integrator cannot correct for the low-frequency output ripple error, so the output voltage has a DC regulation level higher than the error comparator threshold by approximately 1.5% due to slope compensation and output ripple voltage.

Ultrasonic Mode (V_{SKIP} = GND)

Shorting SKIP to ground activates a unique pulse-skipping mode with a guaranteed minimum switching frequency of 20kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(SKIP)}$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs (Figure 4) when the controller detects that no switching has occurred within the last 37µs. Once triggered, the ultrasonic circuitry pulls DL high, turning on the low-side MOSFET to induce a negative inductor current. After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the inductor current drops below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, corresponding to:

$$V_{NEG(US)} = I_L R_{CS}$$

where R_{CS} is the current-sense resistance seen across LX to GND.

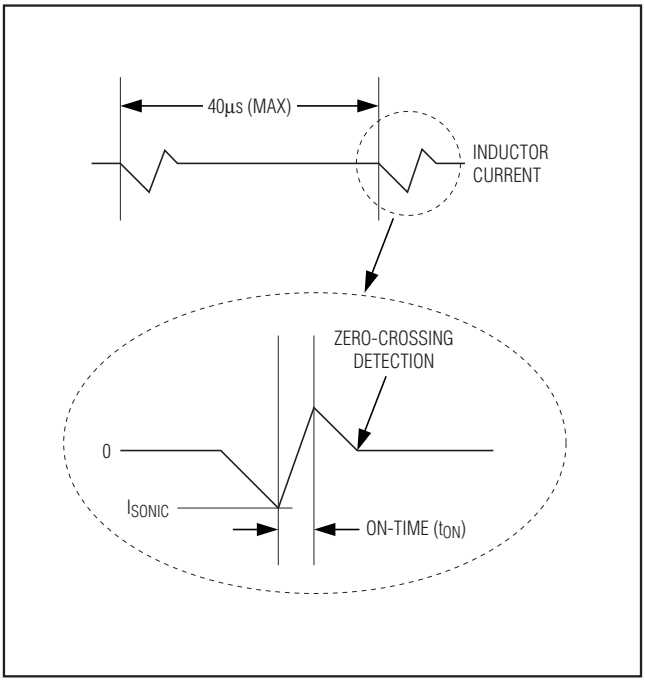


Figure 4. Ultrasonic Waveforms

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Secondary Feedback (SKIP)

When the controller skips pulses (V_{SKIP} > 2V), the long time between pulses (especially if the output is sinking current) allows the external charge-pump voltage or transformer secondary winding voltage to drop. Connecting a resistor-divider between the secondary output to SKIP to ground sets up a minimum refresh threshold. When the SKIP voltage drops below its 2V threshold, the MAX17031 enters forced-PWM mode. This forces the controller to begin switching, allowing the external unregulated charge pump (or transformer secondary winding) to be refreshed.

Valley Current-Limit Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current through the low-side MOSFET—across LX to analog GND. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX17031 also implements a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

POR, UVLO

When V_{CC} rises above the power-on reset (POR) threshold, the MAX17031 clears the fault latches, forces the low-side MOSFET to turn on (DL high), and resets the soft-start circuit, preparing the controller for power-up. However, the V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching until V_{CC} reaches 4.2V (typ). When V_{CC} rises above 4.2V and the controller has been enabled (ON_ pulled high), the controller activates the enabled PWM controllers and initializes soft-start.

When V_{CC} drops below the UVLO threshold (falling edge), the controller stops switching, and DH and DL are pulled low. When the 2V POR falling-edge threshold is reached, the DL state no longer matters since there is not enough voltage to force the switching MOSFETs into a low on-resistance state, so the controller pulls DL high, allowing a soft discharge of the output capacitors (damped response). However, if the V_{CC} recovers before reaching the falling POR threshold, DL remains low until the error comparator has been properly powered up and triggers an on-time.

Soft-Start and Soft-Shutdown

The MAX17031 includes voltage soft-start and soft-shutdown—slowly ramping up and down the target voltage. During startup, the slew-rate control softly slews the target voltage over a 1ms startup period. This long startup period reduces the inrush current during startup.

When ON1 or ON2 is pulled low or the output undervoltage fault latch is set, the respective output automatically enters soft-shutdown; the regulator enters PWM mode and ramps down its output voltage over a 1ms period. After the output voltage drops below 0.1V, the MAX17031 pulls DL high, clamping the output and LX switching node to ground, preventing leakage currents from pulling up the output and minimizing the negative output voltage undershoot during shutdown.

Output Voltage

DC output-accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold. When the inductor continuously conducts, the MAX17031 regulates the valley of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM} + \left(\frac{V_{RIPPLE}}{2A_{CCV}} \right)$$

where V_{NOM} is the nominal feedback voltage, A_{CCV} is the integrator's gain, and V_{RIPPLE} is the output ripple voltage (V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$, as described in the *Output Capacitor Selection* section).

In discontinuous conduction (I_{OUT} < $I_{LOAD(SKIP)}$), the longer off-times allow the slope compensation to increase the threshold voltage by as much as 1%, so the output voltage regulates slightly higher than it would in PWM operation.

Internal Integrator

The internal integrator improves the output accuracy by removing any output accuracy errors caused by the slope compensation, output ripple voltage, and error-amplifier offset. Therefore, the DC accuracy (in forced-PWM mode) depends on the integrator's gain, the integrator's offset, and the accuracy of the integrator's reference input.

Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors both output voltages for undervoltage and overvoltage conditions. PGOOD is actively held low in shutdown (ON1 or ON2 = GND), during soft-start, and soft-shutdown. Approximately 20µs (typ) after the soft-start terminates, PGOOD becomes high impedance as long as both output voltages exceed 85% of the nominal fixed-regulation voltage. PGOOD goes low if the output voltage drops 15% below the regulation voltage, or if the SMPS controller is shut down. For a logic-level PGOOD output voltage, connect an external pullup resistor between PGOOD and the logic power supply. A 100kΩ pullup resistor works well in most applications.

Overvoltage Protection (OVP)

When the output voltage rises 15% above the fixed-regulation voltage, the controller immediately pulls PGOOD low, sets the overvoltage fault latch, and immediately pulls the respective DL_ high—clamping the output fault to GND. Toggle either ON1 or ON2 input, or cycle V_{CC} power below its POR threshold to clear the fault latch and restart the controller.

Undervoltage Protection (UVP)

When the output voltage drops 30% below the fixed-regulation voltage, the controller immediately pulls the PGOOD low, sets the undervoltage fault latch, and begins the shutdown sequence. After the output voltage drops below 0.1V, the synchronous rectifier turns on, clamping the output to GND regardless of the output voltage. Toggle either ON1 or ON2 input, or cycle V_{CC} power below its POR threshold to clear the fault latch and restart the controller.

Thermal-Fault Protection (T_{SHDN})

The MAX17031 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, enables the 10Ω discharge circuit, and disables the controller—DH and DL pulled low. Toggle ONLDO or cycle IN power to reactivate the controller after the junction temperature cools by 15°C.

Design Procedure

Firmly establish the input-voltage range and maximum load current before choosing an inductor operating point (ripple-current ratio). The primary design goal is choosing a good inductor operating point, and the following three factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

Table 3. Fault Protection and Shutdown Operation Table

MODE	CONTROLLER STATE	DRIVER STATE
Shutdown (ON_ = High to Low) Output UVP (Latched)	Voltage soft-shutdown initiated. Internal error-amplifier target slowly ramped down to GND and output actively discharged (automatically enters forced-PWM mode).	DL driven high and DH pulled low after soft-shutdown completed (output < 0.1V).
Output OVP (Latched)	Controller shuts down and EA target internally slewed down. Controller remains off until ON_ toggled or V_{CC} power cycled.	DL immediately driven high, DH pulled low.
UVLO (V_{CC} Falling-Edge) Thermal Fault (Latched)	SMPS controller disabled (assuming ON_ pulled high), 10Ω output discharge active.	DL and DH pulled low.
UVLO (V_{CC} Rising Edge)	SMPS controller disabled (assuming ON_ pulled high), 10Ω output discharge active.	DL driven high, DH pulled low.
V_{CC} Below POR	SMPS inactive, 10Ω output discharge active.	DL driven high, DH pulled low.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Inductor Operating Point: This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 4A, V_{IN} = 12V, V_{OUT2} = 2.5V, f_{SW} = 355kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{2.5V \times (12V - 2.5V)}{12V \times 355kHz \times 4A \times 0.3} = 4.65\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)}LIR}{2}\right)$$

where $I_{LIM(VAL)}$ equals the minimum valley current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). When using a 100kΩ ILIM resistor, the minimum valley current-limit threshold is 40mV.

Connect a resistor between ILIM_ and analog ground to set the adjustable current-limit threshold. The valley current-limit threshold is approximately 1/10 the ILIM voltage formed by the external resistance and internal 5µA current source. The 40kΩ to 400kΩ adjustment range corresponds to a 20mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors to prevent significant inaccuracy in the valley current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)}LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that might affect the overall stability (see the *Output Capacitor Stability Considerations* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support $25mV_{P-P}$ ripple is 25mV/1.2A = 20.8mΩ. One 220µF/4V SANYO polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly on OUT1 and OUT2 pins to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability results in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX17031 is operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX17031 DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems could occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\ (NH\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (NH\ Switching) = \left(\frac{V_{IN(MAX)} I_{LOAD} f_{SW} Q_{G(SW)}}{I_{GATE}}\right) + \left(\frac{V_{IN}^2 C_{OSS} f_{SW}}{2}\right)$$

where C_{OSS} is the high-side MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the high-side MOSFET, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation provided above. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\ (NL\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Applications Information

Step-Down Converter Dropout Performance

The output voltage-adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{DROP2}}{1 - \left(\frac{h \times t_{OFF(MIN)}}{K}\right)}$$

where V_{DROP2} is the parasitic voltage drop in the charge path (see the *On-Time One-Shot* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table, and K ($1/f_{SW}$) is the switching period. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT2} = 2.5V

f_{SW} = 355kHz

K = 3.0µs, worst-case K_{MIN} = 3.3µs

$t_{OFF(MIN)}$ = 500ns

V_{DROP2} = 100mV

h = 1.5:

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 500ns}{3.0\mu s}\right)} = 3.47V$$

Calculating again with h = 1 and the typical K-factor value (K = 3.3µs) gives the absolute limit of dropout:

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1 - \left(\frac{1 \times 500ns}{3.3\mu s}\right)} = 3.06V$$

Therefore, V_{IN} must be greater than 3.06V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.47V.

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting LX_ directly to the drain of the low-side MOSFET.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, and OUT_).

A sample layout is available in the MAX17031 Evaluation Kit data sheet.

Dual Quick-PWM Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies

Layout Procedure

1) Place the power components first, with ground terminals adjacent ($N_{L_}$ source, C_{IN}, $C_{OUT_}$, and $D_{L_}$ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite $N_{L_}$ and $N_{H_}$ in order to keep LX_, GND, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
3) Group the gate-drive components (BST_ capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Chip Information

TRANSISTOR COUNT: 12,197

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN	T2444-3	**21-0139**

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