Click here for production status of specific part numbers.

MAX17506

4.5V–60V, 5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

General Description

The MAX17506 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFET operates over a 4.5V to 60V input. The converter can deliver up to 5A and generates output voltages from 0.9V up to 0.9 x V_{IN}. The feedback (FB) voltage is accurate to within ±1.4% over -40°C to 125°C.

The MAX17506 uses peak current-mode control. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous conduction mode (DCM) control schemes.

The device is available in a 20-pin (5mm x 5mm) Thin QFN (TQFN) package. Simulation models are available.

Applications

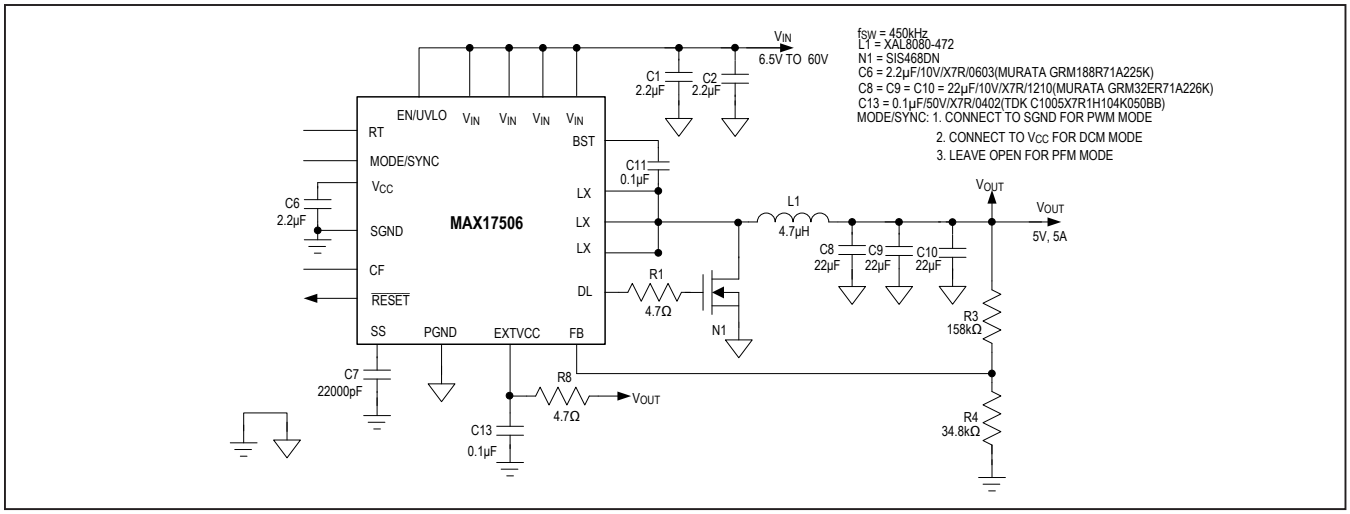
- Industrial Power Supplies
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage Single-Board Systems
- General-Purpose Point-of-Load

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - Built-In Soft-Start
  - All-Ceramic Capacitors, Compact Layout
- Reduce Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable Output-Voltage Range from 0.9V up to 90% of V_{IN}
  - 100kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- Reduces Power Dissipation
  - Peak Efficiency > 95%
  - PFM/DCM Modes Enables Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 3.5µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup or Latchoff Mode Overload Protection
  - DL to LX Short Detection Feature
  - Built-In Output Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature / -40°C to +150°C Junction Temperature Range

Typical Application Circuit for 5V Output



maxim integrated™

Absolute Maximum Ratings

V_{IN} to PGND .....-0.3V to +65V
EN/UVLO, SS to SGND .....-0.3V to +65V
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
BST to PGND .....-0.3V to +70V
BST to LX .....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +65V
FB, CF, $\overline{RESET}$, MODE/SYNC, RT to SGND .....-0.3V to +6.5V
DL, V_{CC} to PGND .....-0.3V to +6.5V
SGND to PGND.....-0.3V to +0.3V
EXTVCC to PGND .....-0.3V to +26V

LX Total RMS Current .....±9.9A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C) (multilayer board)
TQFN (derate 33.3mW/°C above T_A = +70°C).....2666.7mW
Operating Temperature Range (Note 1)..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2055+4
Outline Number	**21-0140**
Land Pattern Number	**90-0009**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA}) (Note 2)	23°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.
Note 2: Applicable only to the Evaluation Kit in free space with no airflow.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		3.5	5.5	µA
Input Quiescent Current	I_{Q_PFM}	V_{FB} = 1V, MODE = RT= open		128		µA
		V_{FB} = 1V, MODE = open, R_{RT} = 40.2k		168		µA
	I_{Q_DCM}	DCM mode, V_{LX} = 0.1V		1.27	2	mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.112	V
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 1.245V, T_A = +25ºC	-50	0	+50	nA
LDO						
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, I_{VCC} = 1mA	4.75	5	5.25	V
		1mA ≤ I_{VCC} ≤ 45mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6V	50	90	140	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 45mA	4.1			V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.1	4.2	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.7	3.8	3.9	V
EXT LDO						
EXT V_{CC} Operating Voltage Range			4.84		24	V
EXT V_{CC} Switchover Voltage		EXT V_{CC} rising	4.56	4.7	4.84	V
EXT V_{CC} Switchover Voltage Hysteresis			0.205	0.232	0.255	V
EXT V_{CC} Dropout	EXT V_{CC-DO}	EXT V_{CC} = 4.75V, $I_{EXT\ VCC}$ = 45mA			0.4	V
EXT V_{CC} Current Limit	EXT IV_{CC-MAX}	V_{CC} = 4.3V, EXT V_{CC} = 5V	45	85	140	mA
POWER MOSFET AND LOW-SIDE DRIVER						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 1.0A		45	90	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = V_{IN} - 1V, V_{LX} = V_{PGND} + 1V, T_A = +25ºC	-4	1	+4	µA
Pullup Resistance		I_{SOURCE} = 100mA		1.9	2.9	Ω
Pulldown Resistance		I_{SINK} = 100mA		1	1.65	Ω
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0V	4.7	5	5.3	µA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}	MODE = SGND or MODE = V_{CC}	0.887	0.9	0.912	V
		MODE = open	0.887	0.915	0.936	
FB Input Bias Current	I_{FB}	0 < V_{FB} < 1V, T_A = +25ºC	-75		+75	nA
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE = V_{CC} (DCM mode)	V_{CC} - 0.6			V
	V_{M-PFM}	MODE = open (PFM mode)		V_{CC}/2		
	V_{M-PWM}	MODE = GND (PWM mode)			0.6	
SYNC Frequency Capture Range		f_{SW} set bt R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$	R_{DL} = open or R_{DL} = 174kΩ	6.5	7.8	9.1	A
		R_{DL} = 61.9k or R_{DL} = 26.1k	5.85	7	8.15	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$	R_{DL} = open or R_{DL} = 174kΩ	7.33	8.8	10.4	A
		R_{DL} = 61.9k or R_{DL} = 26.1k	6.7	8.05	9.4	A
Negative Current Limit Comparator Voltage Reference		MODE = open or MODE = V_{CC}		0		mV
		MODE = GND	42	50	58	
PFM Current-Limit Threshold	I_{PFM}	MODE = open		2		A
RT						
Switching Frequency	f_{SW}	R_{RT} = 196kΩ	90	100	110	kHz
		R_{RT} = 93.1kΩ	180	200	220	
		R_{RT} = open	420	450	480	
		R_{RT} = 6.98kΩ	1950	2200	2450	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$		0.56	0.58	0.61	V
HICCUP Timeout		(Note 4)		32768		Cycles
Minimum On-Time	t_{ON-MIN}			95	160	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		160	ns
LX Dead Time				22		ns

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			0.200	V
$\overline{RESET}$ Output Leakage Current		T_A = T_J = +25ºC, $V_{\overline{RESET}}$ = 5.5V	-0.1		+0.1	µA
V_{OUT} Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.4	92.5	94.6	%
V_{OUT} Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.4	95.5	97.7	%
$\overline{RESET}$ Deassertion Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		165		ºC
Thermal-Shutdown Hysteresis				10		ºC

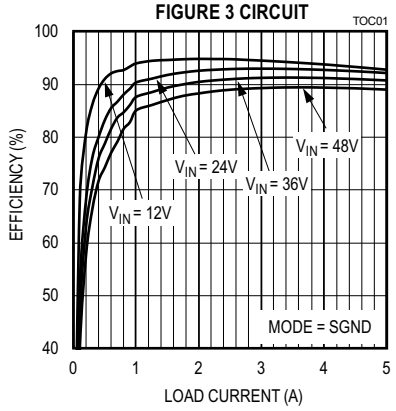
Note 3: All Electrical Specifications are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

Note 4: See the *Overcurrent Protection/HICCUP Mode* section for more details.

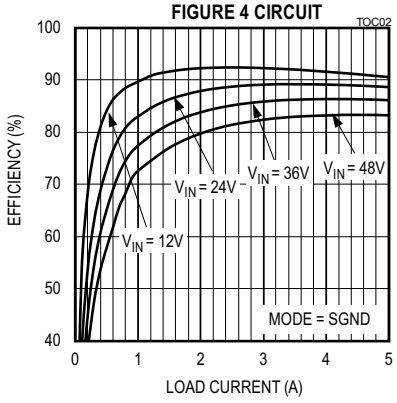
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

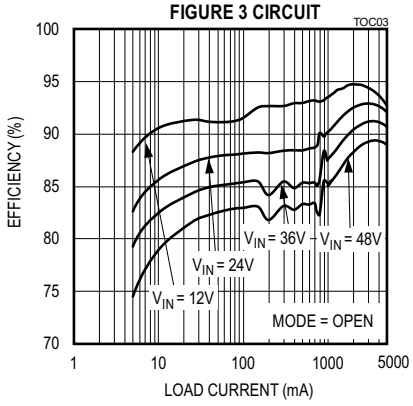
EFFICIENCY vs. LOAD CURRENT 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



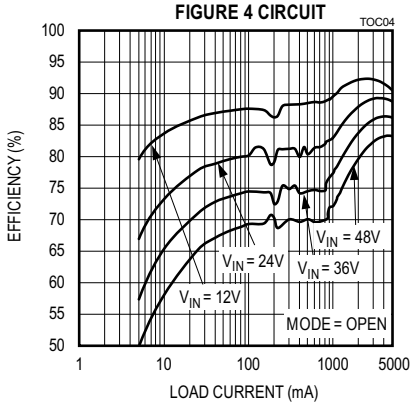
EFFICIENCY vs. LOAD CURRENT 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



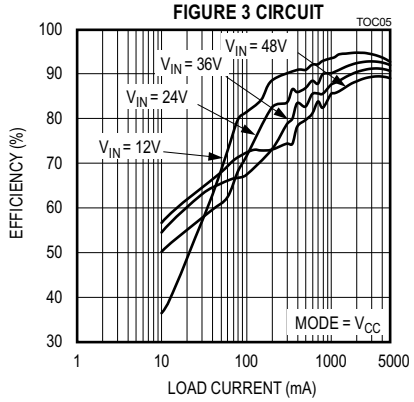
EFFICIENCY vs. LOAD CURRENT 5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT



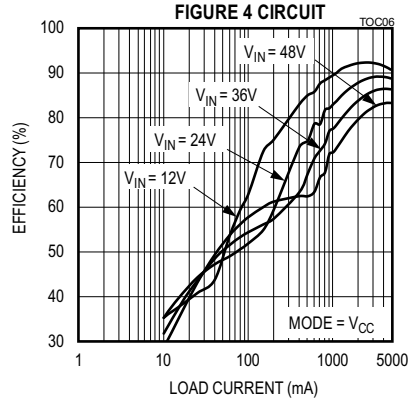
EFFICIENCY vs. LOAD CURRENT 3.3V OUTPUT, PFM MODE, FIGURE 4 CIRCUIT



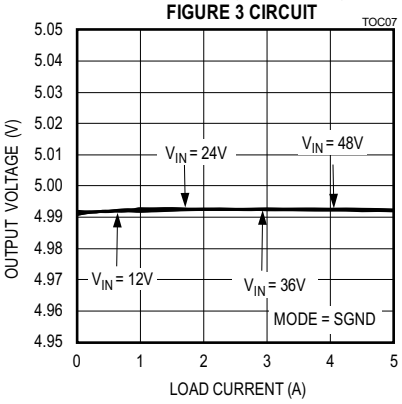
EFFICIENCY vs. LOAD CURRENT 5V OUTPUT, DCM MODE, FIGURE 3 CIRCUIT



EFFICIENCY vs. LOAD CURRENT 3.3V OUTPUT, DCM MODE, FIGURE 4 CIRCUIT



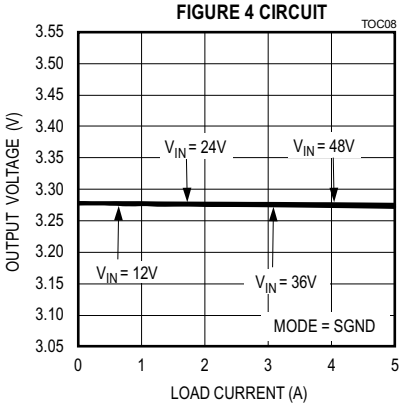
LOAD AND LINE REGULATION 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



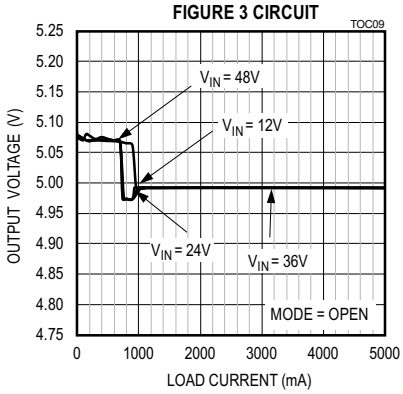
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

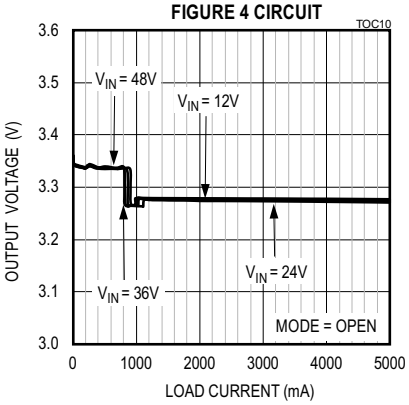
LOAD AND LINE REGULATION 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



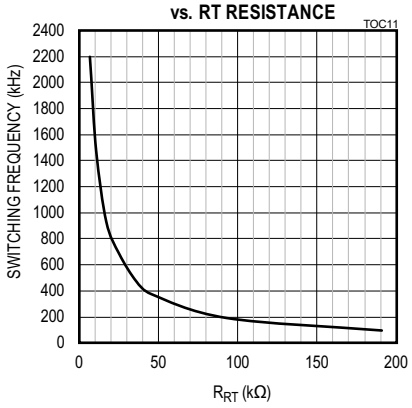
LOAD AND LINE REGULATION 5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT



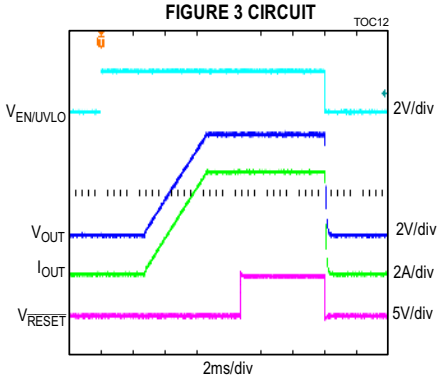
LOAD AND LINE REGULATION 3.3V OUTPUT, PFM MODE, FIGURE 4 CIRCUIT



SWITCHING FREQUENCY vs. RT RESISTANCE

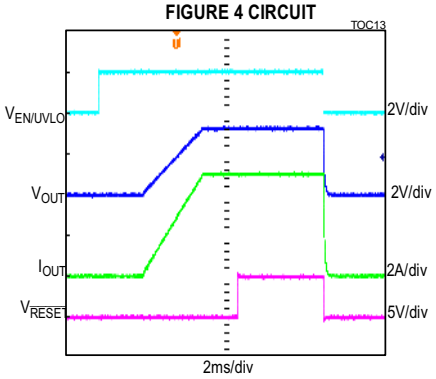


SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, 5A LOAD CURRENT, FIGURE 3 CIRCUIT



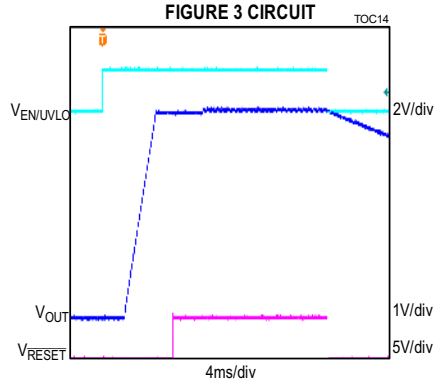
CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, 5A LOAD CURRENT, FIGURE 4 CIRCUIT



CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, PFM MODE, 5mA LOAD CURRENT, FIGURE 3 CIRCUIT

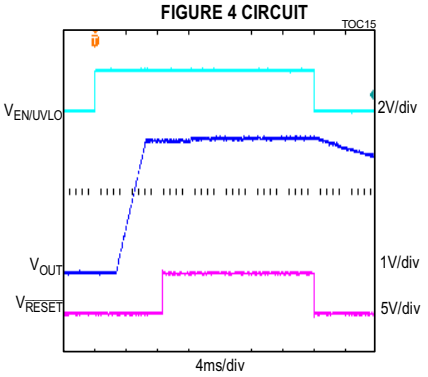


CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

Typical Operating Characteristics

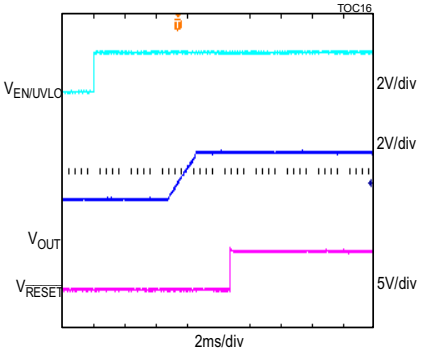
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, PFM MODE, 50mA LOAD CURRENT, FIGURE 4 CIRCUIT



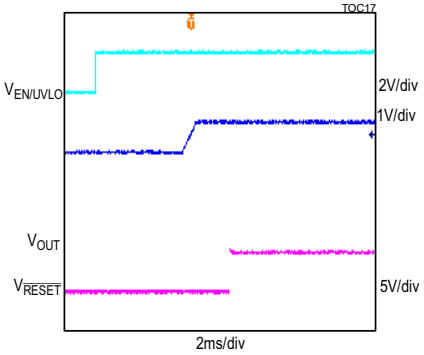
CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH 2.5V PREBIAS, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



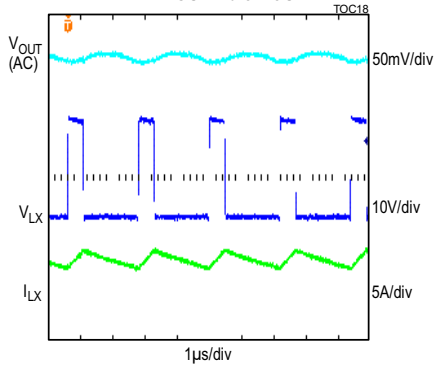
CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH 2.5V PREBIAS, 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT

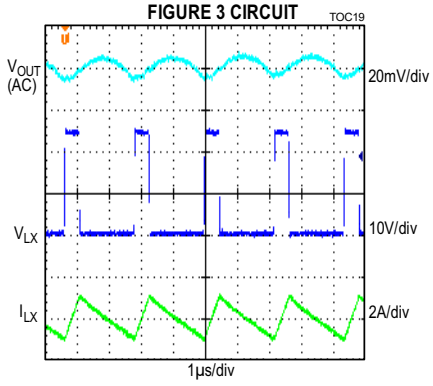


CONDITION: $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

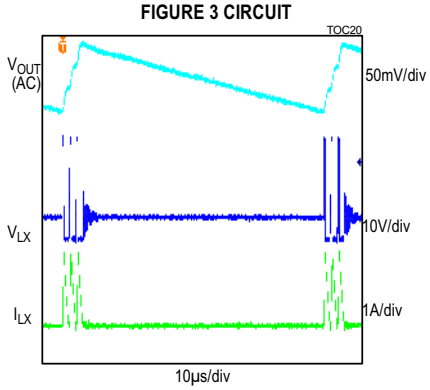
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 5A LOAD CURRENT, FIGURE 3 CIRCUIT



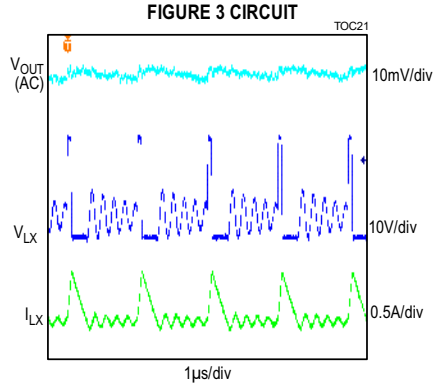
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, NO LOAD CURRENT, FIGURE 3 CIRCUIT



STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, PFM MODE, 25mA LOAD CURRENT, FIGURE 3 CIRCUIT



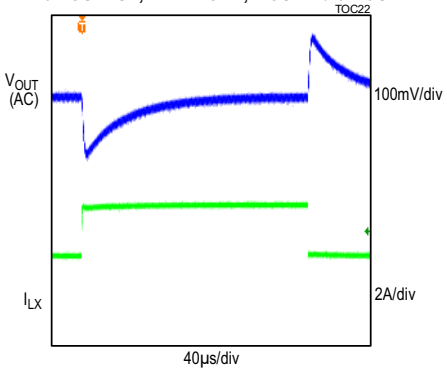
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, DCM MODE, 25mA LOAD CURRENT, FIGURE 3 CIRCUIT



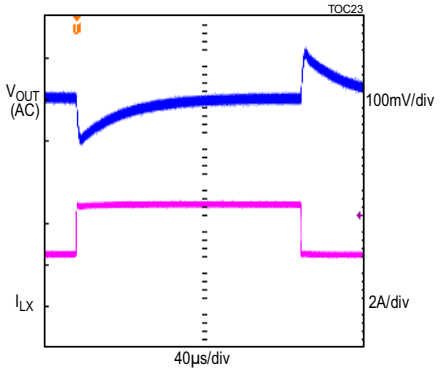
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

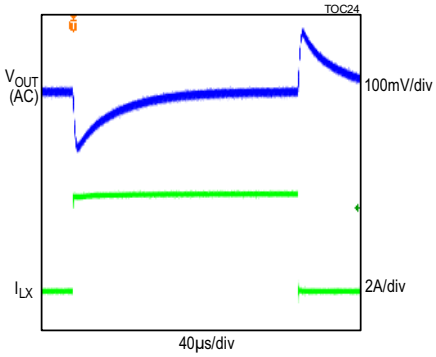
LOAD CURRENT STEPPED FROM 2.5A TO 5A
5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



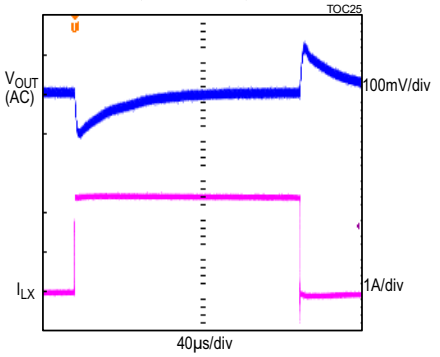
LOAD CURRENT STEPPED FROM 2.5A TO 5A
3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



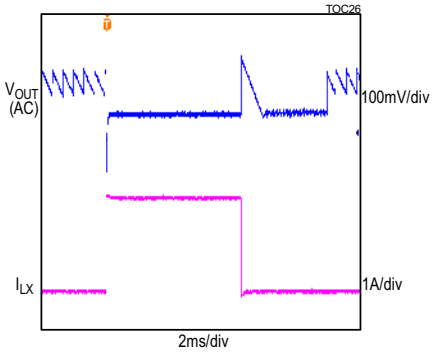
LOAD CURRENT STEPPED FROM NO LOAD TO 2.5A
5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



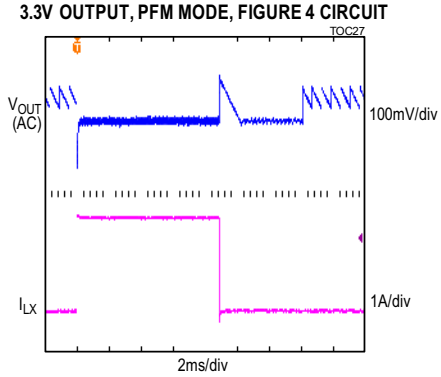
LOAD CURRENT STEPPED FROM NO LOAD TO 2.5A
3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



LOAD CURRENT STEPPED FROM 5mA TO 2.5A
5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT



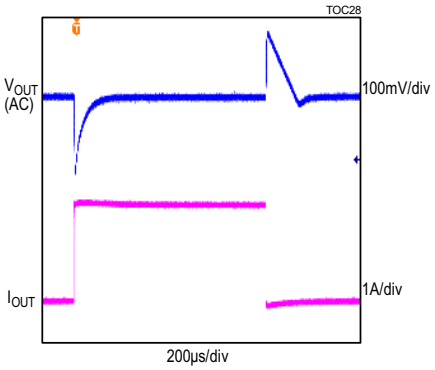
LOAD CURRENT STEPPED FROM 50mA TO 2.5A
3.3V OUTPUT, PFM MODE, FIGURE 4 CIRCUIT



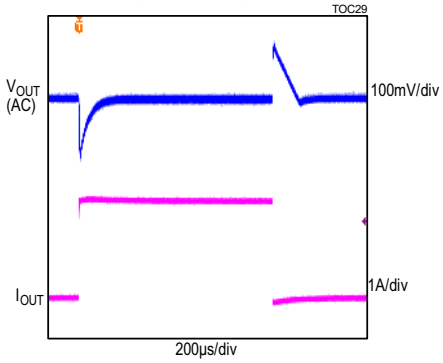
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

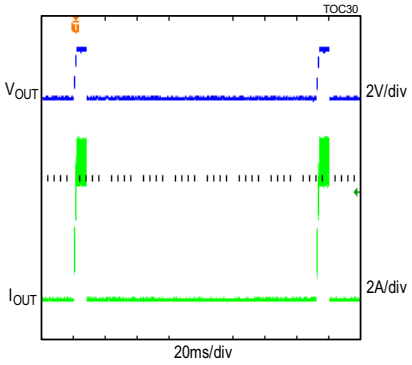
LOAD CURRENT STEPPED FROM 50mA TO 2.5A
5V OUTPUT, DCM MODE, FIGURE 3 CIRCUIT



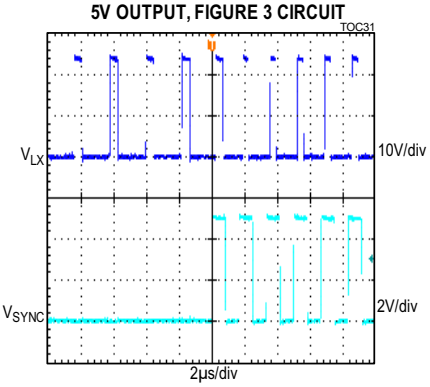
LOAD CURRENT STEPPED FROM 50mA TO 2.5A
3.3V OUTPUT, DCM MODE, FIGURE 4 CIRCUIT



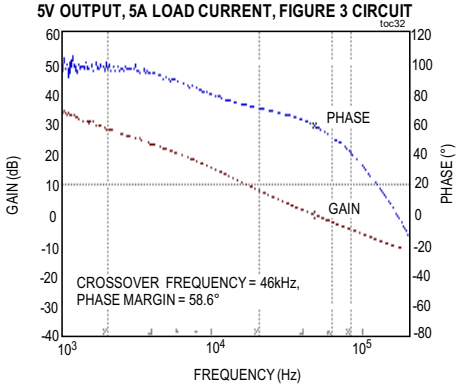
OVERLOAD PROTECTION
5V OUTPUT, FIGURE 3 CIRCUIT



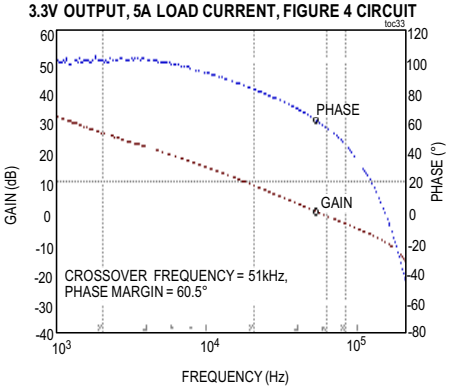
APPLICATION OF EXTERNAL CLOCK AT 600kHz
5V OUTPUT, FIGURE 3 CIRCUIT



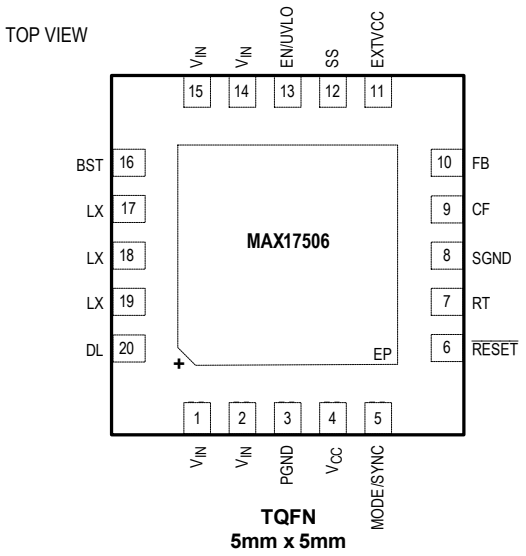
BODE PLOT,
5V OUTPUT, 5A LOAD CURRENT, FIGURE 3 CIRCUIT



BODE PLOT,
3.3V OUTPUT, 5A LOAD CURRENT, FIGURE 4 CIRCUIT



Pin Configuration



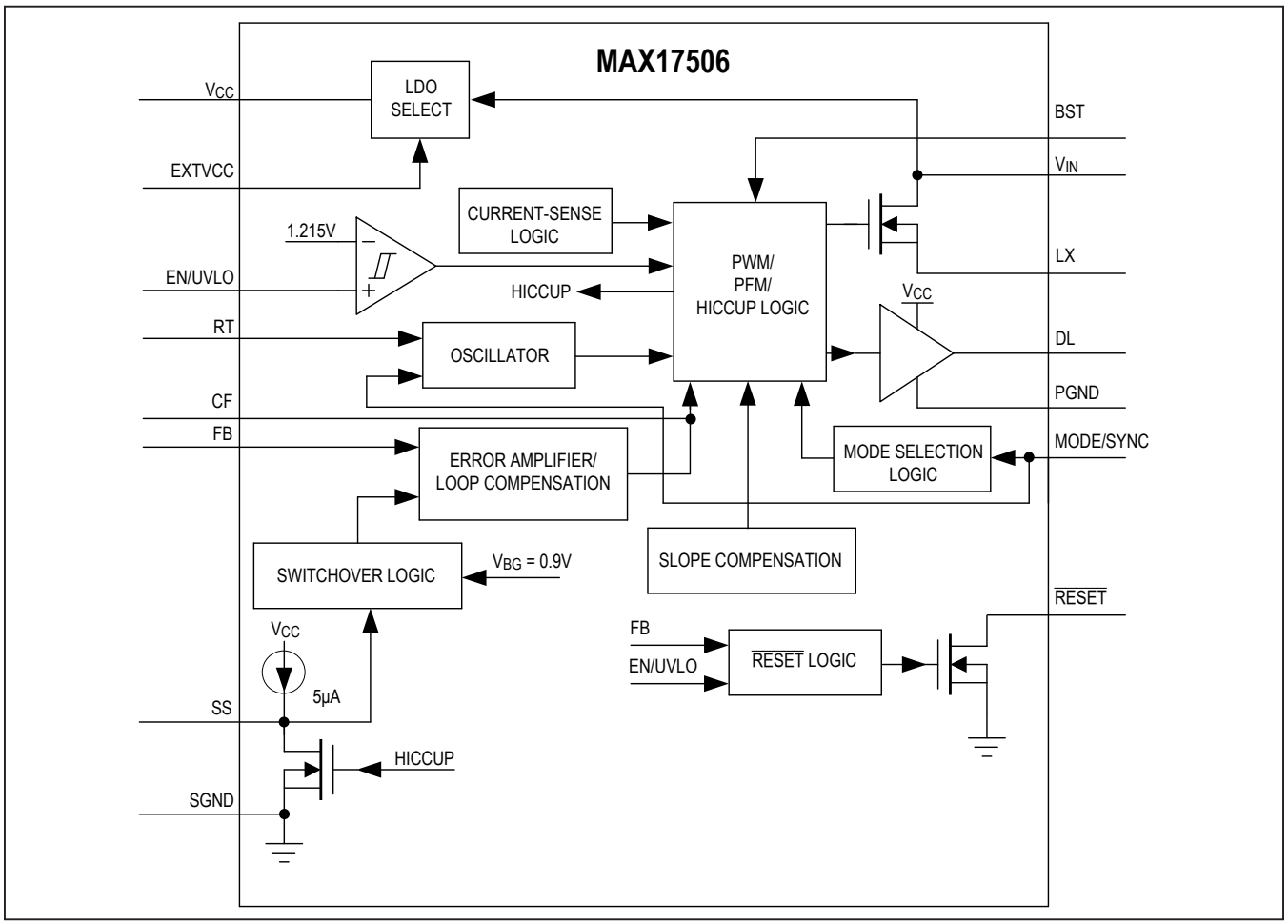
Pin Description

PIN	NAME	FUNCTION
1, 2, 14,15	V_{IN}	Power-Supply Input. 4.5V to 60V input supply range. Connect the V_{IN} pins together. Decouple to PGND with two 2.2µF capacitors; place the capacitors close to the V_{IN} and PGND pins. Refer to the MAX17506 Evaluation Kit datasheet for a layout example.
3	PGND	Power Ground. Connect the PGND pins externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor. Refer to the MAX17506 Evaluation Kit datasheet for a layout example.
4	V_{CC}	5V LDO Output. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND.
5	MODE/ SYNC	MODE/SYNC configures the MAX17506 to operate in PWM, PFM or DCM modes of operation. Leave MODE/SYNC unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to V_{CC} for DCM operation. The device can be synchronized to an external clock using this pin. See the *MODE Selection* section ant the *External Frequency Synchronization* section for more details.
6	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92.2% of its set value. $\overline{\text{RESET}}$ goes high 1024 clock cycles after FB rises above 95.6% of its set value.
7	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the regulator's switching frequency. Leave RT open for the default 450kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
8	SGND	Analog Ground
9	CF	At switching frequencies lower than 450kHz, connect a capacitor from CF to FB. Leave CF open if the switching frequency is equal to or more than 450kHz. See the *Loop Compensation* section for more details.
10	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
11	EXTVCC	External Power Supply Input for the Bootstrap Internal LDO. Applying a voltage between 4.84V and 24V at the EXTVCC pin draws power for the control circuits and driver from the output, by bypassing the V_{CC} internal LDO and improves efficiency. Connect EXTVCC to the Buck regulator output capacitor using an R-C filter (4.7Ω, 0.1µF). Bypass the EXTVCC pin to SGND (Figure 3). Connect the EXTVCC pin to SGND when the pin is not being used.

Pin Description (continued)

PIN	NAME	FUNCTION
12	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
13	EN/UVLO	Enable/Undervoltage Lockout. Drive EN/UVLO high to enable the output voltage. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the MAX17506 turns on. Pull up to V_{IN} for always on operation.
16	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
17, 18, 19	LX	Switching Node. Connect LX pins to the switching side of the inductor.
20	DL	Use DL pin to drive the gate of the low-side external n-MOSFET. A resistor connected between the DL pin and SGND selects the overload protection method and the peak and runaway current limits. See the *Overcurrent Protection/HICCUP Mode* section for more details.
—	EP	Exposed pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large SGND plane with several thermal vias for best thermal performance. Refer to the MAX17506 EV kit data sheet for an example of the correct method for EP connection and thermal vias.

Block Diagram



Detailed Description

The MAX17506 high-efficiency, high-voltage, synchronously rectified step-down converter with integrated high-side MOSFET operates over a 4.5V to 60V input. It delivers up to 5A and 0.9V up to 90% V_{IN} output voltage. Built-in compensation across the output voltage range eliminates the need for external components. The feedback (FB) regulation accuracy over -40°C to +125°C is ±1.4%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node that sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE/SYNC pin that can be used to operate the device in PWM, PFM, or DCM control schemes and to synchronize the switching freqeuncy to an external clock. The device also features adjustable-input undervoltage lockout, adjustable soft-start, open-drain $\overline{RESET}$, auxiliary bootstrap LDO and DL to LX short detection features.

Mode Selection (MODE)

The logic state of the MODE/SYNC pin is latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE/SYNC pin is open at power-up, the device operates in PFM mode at light loads. If the MODE/SYNC pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE/SYNC pin is connected to V_{CC} at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 2A every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes.

Linear Regulator (V_{CC} and EXTVCC)

The MAX17506 has two internal LDO (Low Drop-Out) regulators which powers V_{CC}. One LDO is powered from V_{IN} (INLDO) and the other LDO is powered from EXTVCC (EXTVCC LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC. If EXTVCC voltage is greater than 4.7V (typ), V_{CC} is powered from EXTVCC. If EXTVCC is lower than 4.7V (typ), V_{CC} is powered from V_{IN}. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 24V

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and re-charges the external bootstrap capacitor. Both INLDO and EXTVCC LDO can source up to 45mA for bias requirements. The MAX17506 employs an under-voltage lockout circuit that forces the converter off when V_{CC} falls below 3.8V (typ). The converter is enabled again when V_{CC} > 4.2V. The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

Add a local bypassing capacitor of 0.1µF on the EXTVCC pin to SGND. Also, add a 4.7Ω resistor from the buck converter output node to the EXTVCC pin to limit V_{CC} bypass capacitor discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit conditions. In applications where the buck converter output is connected to EXTVCC pin, if the output is shorted to ground then the transfer from EXTVCCLDO to INLDO happens seamlessly without any impact on the normal functionality. Connect the EXTVCC pin to SGND when the pin is not being used.

Setting the Switching Frequency (RT)

The switching frequency of the MAX17506 can be programmed from 100kHz to 2.2MHz by using a resistor connected from RT to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{19 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 450kHz. See Table 1 for RT resistor values for a few common switching frequencies.

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS-ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF-MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS-ONH(MAX)} - R_{DS-ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON-MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage
$I_{OUT(MAX)}$ = Maximum load current
$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor
$f_{SW(MAX)}$ = Maximum switching frequency
$t_{OFF-MIN(MAX)}$ = Worst-case minimum switch off-time (160ns)
$t_{ON-MIN(MAX)}$ = Worst-case minimum switch on-time (160ns)
R_{DS-ONH} = Worst-case on-state resistances and high-side internal MOSFET
R_{DS-ONL} = Worst-case on-state resistances and low-side external MOSFET

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
100	196
200	93.1
450	OPEN
2200	6.98

External Frequency Synchronization

The internal oscillator of the MAX17506 can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the RT resistor. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT setting) after detecting 16 external clock edges. The converter will operate in PWM mode during synchronization operation. When MODE/SYNC is unconnected for PFM mode, internal 300kΩ pulldown resistor on this pin pulls the node below VIL of the SYNC threshold and maintains the part in PFM mode. When the external clock is applied on-fly then the mode of operation will change to PWM from the initial state of PFM/DCM/PWM. When the external clock is removed on-fly then the internal oscillator frequency changes to the RT set frequency and the converter will still continue to operate in PWM mode. The minimum external clock pulse-width high should be greater than 22ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

DL to LX Short Detection

In MAX17506, DL and LX pins are adjacent to each other. To prevent damage to the low side external FET in case DL pin is shorted to the LX pins, DL to LX short detection feature has been implemented. If the MAX17506 detects that the DL pin is shorted to the LX pins before startup, the startup sequence will not be initiated and output voltage will not be soft-started.

Overcurrent Protection/HICCUP Mode

The MAX17506 is provided with a robust over-current protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit. A runaway current limit on the high-side switch current protects the device under high input voltage, short

circuit conditions when there is insufficient output voltage available to restore the Inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 68% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered.

The MAX17506 has two modes of operation under overload conditions – the hiccup mode and the latchoff mode. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. In latchoff mode, the converter does not attempt to soft-start the output after a timeout period. The power supply to the MAX17506 needs to be cycled to turn-on the part again in latchoff mode of operation. A resistor connected from DL to SGND sets the peak and runaway current limits and the operating mode during overload condition.

RESISTANCE (kΩ)	PEAK CURRENT LIMIT (A)	RUNAWAY CURRENT LIMIT (A)	FAULT OPERATING MODE
Open	7.8	8.8	Hiccup
174	7.8	8.8	Latchoff
61.9	7.2	8.2	Hiccup
26.1	7.2	8.2	Latchoff

$\overline{\text{RESET}}$ Output

The MAX17506 includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high-impedance) 1024 switching cycles after the regulator output increases above 95.6% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92.2% of the set nominal output voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the MAX17506 starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the MAX17506. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The MAX17506 turns ON with soft-start after the junction temperature reduces by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high ripple current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the converter, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the MAX17506 input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX17506: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance

(R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{2.2 \times f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{sw}}\right)$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. Select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 450kHz. If the switching frequency is more than 450kHz, select f_C to be 50kHz.

Soft-Start Capacitor Selection

The MAX17506 implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = C_{SS}/(5.55 \times 10^{-6})$$

For example, to program a 4ms soft-start time, a 22nF capacitor should be connected from the SS pin to SGND.

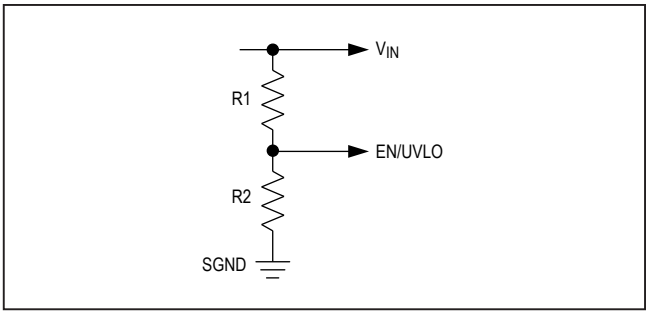


Figure 1. Setting the Input Undervoltage Lockout

Setting the Input Undervoltage Lockout Level

The MAX17506 offers an adjustable input undervoltage lockout level. Set the voltage at which MAX17506 turns on, with a resistive voltage-divider connected from V_{IN} to SGND (see Figure 1). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the MAX17506 is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

Loop Compensation

The MAX17506 is internally loop compensated. However, if the switching frequency is less than 450kHz, connect a 0402 capacitor (C12) between the CF pin and the FB pin. Use Table 2 to select the value of C12.

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R3 from the output to FB as follows:

$$R3 = \frac{451 \times 10^3}{f_C \times C_{OUT_SEL}}$$

where R3 is in kΩ, crossover frequency f_C is in kHz, and C_{OUT_SEL} is actual derated capacitance of the selected output capicitor at DC-bias voltage in µF. Choose f_C to be 1/9th of the switching frequency, f_{SW}, if the switching frequency is less than or equal to 450kHz. If the switching frequency is more than 450kHz, select f_C to be 50kHz.

Calculate resistor R4 from FB to SGND as follows:

Table 2. C12 Capacitor Value at Various Switching Frequencies

SWITCHING FREQUENCY RANGE (kHz)	C12 (pF)
200 to 300	2.2
300 to 450	1.2

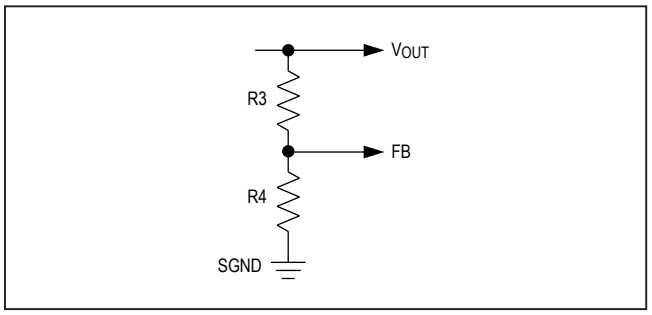


Figure 2. Setting the Output Voltage

$$R4 = \frac{R3 \times 0.9}{(V_{OUT} - 0.9)}$$

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - (I_{OUT}^2 \times R_{DCR}) - (I_{OUT}^2 \times (1 - D) \times R_{LS}$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where, P_{OUT} is the total output power, η is the efficiency of the converter, R_{DCR} is the DC resistances of the inductor, R_{LS} is the on-resistance of the low-side external MOSFET and D = V_{OUT}/V_{IN} is the duty ratio of the converter. (See the typical operating characteristics curves for more information on efficiency at typical operating conditions).

For the MAX17506 EV kit, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 23°C/W$$

$$\theta_{JC} = 2°C/W$$

The junction temperature of the MAX17506 can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the equation below:

$$T_{J_MAX} = T_{A_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal management system that ensures that the exposed pad of the MAX17506 is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the MAX17506 can be estimated at any given maximum ambient temperature from the equation below:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperature greater than = +125°C degrades operating lifetimes

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and give the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17506 evaluation kit layout available at **www.maximintegrated.com**.

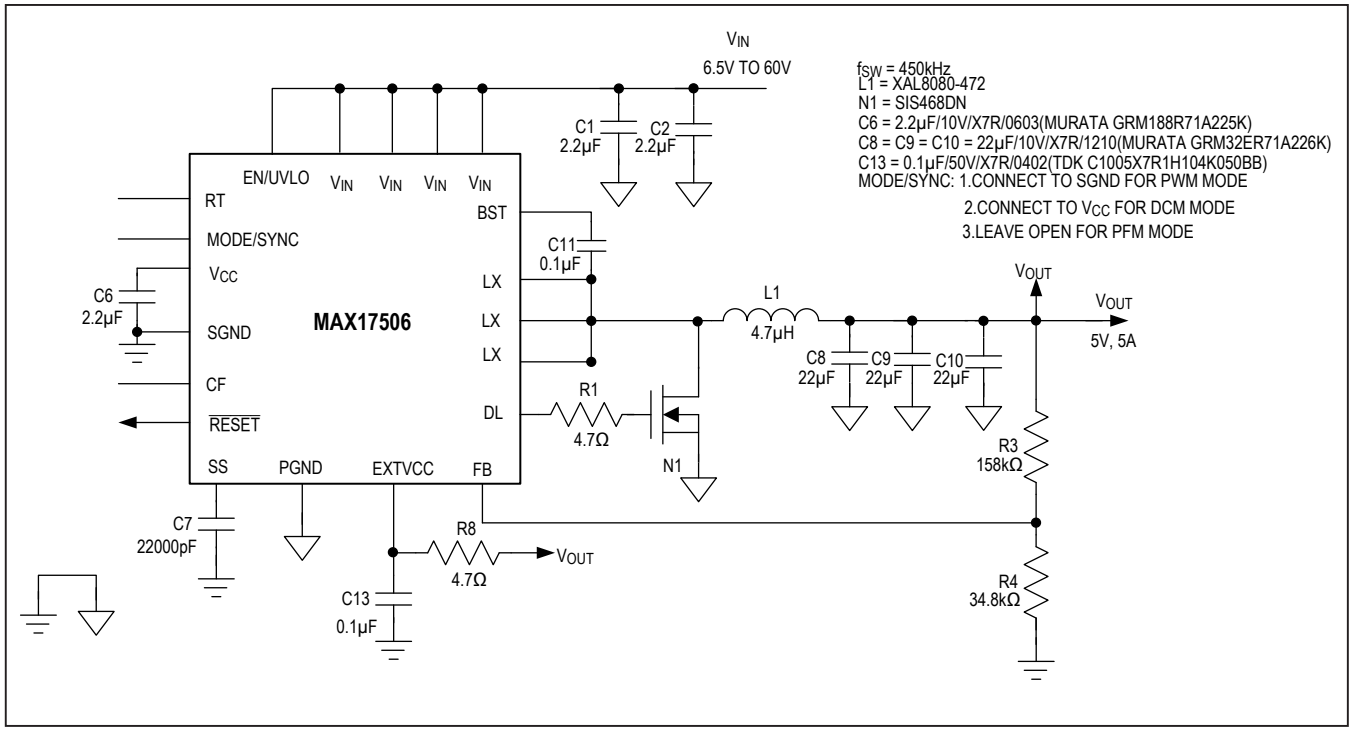


Figure 3. Typical Application Circuit for 5V Output

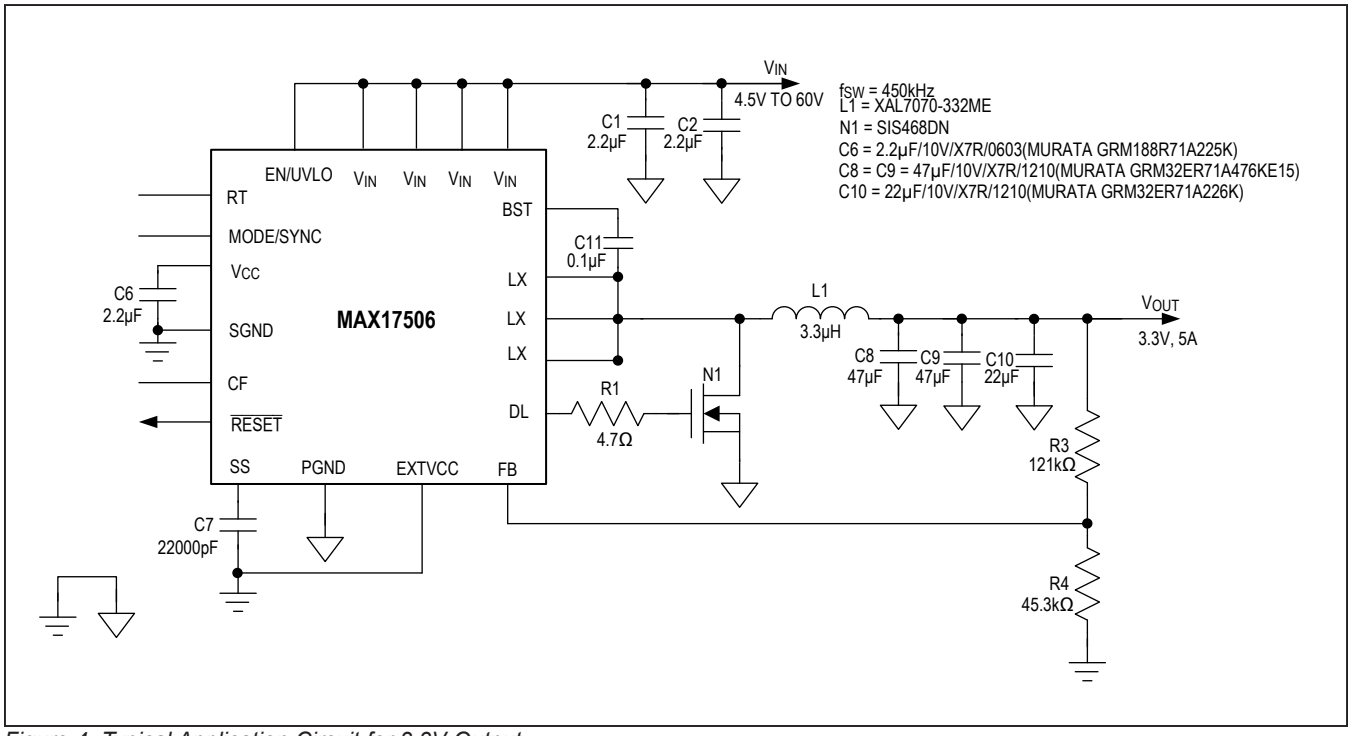


Figure 4. Typical Application Circuit for 3.3V Output

Ordering Information

PART	PIN-PACKAGE
MAX17506ATP+	20 TQFN EP* (5mm x 5mm)

Note: *All devices operate over the temperature range of -40ºC to +125ºC, unless otherwise noted.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/14	Initial release	—
1	5/15	Updated *Typical Application Circuits*, *Absolute Maximum Ratings* and *Electrical Characteristics* table	1–5, 17–18
1.1		Corrected typos in TOCs	5–9
2	3/18	Updated the *Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics* (global conditions, TOC12 and TOC32–33), *Pin Description, Detailed Description, Lindear Regulator (V_{CC} and EXTVCC), Operating Input Voltage Range, External Frequency Synchronization, DL to LX Short Detection, $\overline{RESET}$ Output, Thermal Shutdown Protection, Input Capacitor Selection, Setting the Input Undervoltage Lockout Level, Loop Compensation, Adjusting Output Voltage, Power Dissipation, PCB Layout Guidelines* sections. Updated Tables 1 and 2 and replaced *Typical Application Circuit for 5V Output, Block Diagram*, and Figures 3 and 4.	1–19
3	7/18	Updated all *Typical Application Circuits*, *Package Information* table, *Electrical Characteristics* note numbering, *Pin Description* table, and *Linear Regulator (V_{CC} and EXTVCC), Operating Input Voltage Range,* and *Thermal Shutdown Protection* sections; corrected typos in TOC01, TOC02 and TOC07, and updated TOC12–TOC17.	1–8, 11, 14–15, 18

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