MAX17509 4.5V–16V, Dual 3A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Resistor Programmability

General Description

The MAX17509 integrates two 3A internal switch step-down regulators with programmable features. The device can be configured as two single-phase independent, 3A power supplies or as a dual-phase, single-output 6A power supply. The device operates from 4.5V to 16V input and generates independently adjustable output voltage in the ranges of 0.904V to 3.782V and 4.756V to 5.048V, with ±2% system accuracy.

This device provides maximum flexibility to the end-user by allowing to choose multiple programmable options by connecting resistors to the configuration pins. Two key highlights of the device are the self-configured compensation for any output voltage and the ability to program the slew rate of LX switching nodes to mitigate noise concerns. In noise-sensitive applications, such as high-speed multi-gigabit transceivers in FPGAs, RF, and audio benefit from this unique slew rate control. SYNC input is provided for synchronized operation of multiple devices with system clocks.

MAX17509 offers output overvoltage (OV) and undervoltage (UV) protection, as well as overcurrent (OC) and undercurrent (UC) protection with a selectable hiccup/latch option. It operates over the -40°C to +125°C temperature range, with thermal sensing and shutdown provided for overtemperature (OT) protection. The device is available in a 32-pin 5mm x 5mm TQFN package.

Applications

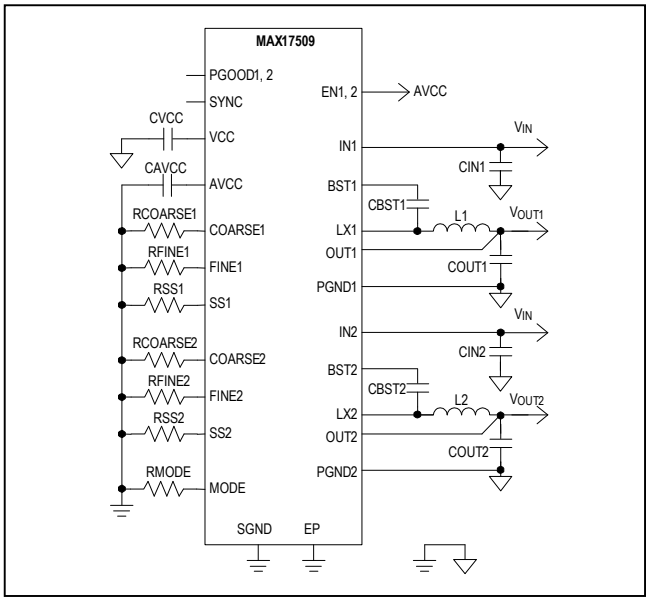
- FPGA and DSP Core Power
- Industrial Control Equipment
- Multiple Point-of-Load (POL) Power Supplies
- Base Station Point-of-Load Regulator

Ordering Information **appears at end of data sheet.**

Benefits and Features

- Reduces Number of DC-DC Regulators in Inventory
  - Output Voltage (0.904V to 3.782V and 4.756V to 5.048V with 20mV Resolution)
  - Configurable Two Independent Outputs (3A/3A) or a Dual-Phase Single Output (6A)
- Mitigate Noise Concerns and EMI
  - Adjustable Switching Frequency with Selectable 0/180° Phase Shift
  - External Frequency Synchronization
  - Adjustable Switching Slew Rate
  - Passes EN55022 (CISPR22) Class-B Radiated and Conducted EMI Standard
- Ease of System Design
  - All Ceramic Capacitors Solution
  - Auto-Configured Internal Compensation
  - Selectable Hiccup or Brickwall Mode
  - Adjustable Soft-Start Rise/Fall Time with Soft Stop Modes and Prebias Startup
  - -40°C to +125°C Operation
- Reliable Operation
  - Robust Fault Protections (VIN_UVLO, UV/OV, UC/OC, OT)
  - Power Good

Application Circuit



19-7051; Rev 0; 2/15

maxim integrated™

Absolute Maximum Ratings

IN_ to PGND_ .....-0.3V to 22V
BST_ to PGND_ .....-0.3V to 28V
BST_ to LX_ .....-0.3V to 6V
BST_ to VCC .....-0.3V to 22V
LX_ to PGND_ ..... -0.3V to the lower of +22V or (VIN_ + 0.3V)
VCC to SGND ..... -0.3V to the lower of +6V or (VIN1 + 0.3V)
AVCC to SGND ..... -0.3V to the lower of +6V or (VIN1 + 0.3V)
OUT_, EN_, PGOOD_, SYNC, COARSE_, FINE_, SS_, MODE to SGND .....-0.3V to 6V
PGND_ to SGND.....-0.3V to 0.3V
EP to SGND .....-0.3V to +0.3V
Operating Temperature Range.....-40ºC to +125ºC
Junction Temperature.....+150°C
Storage Temperature Range.....-65ºC to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 2)

32 TQFN T3255+4
Continuous Power Dissipation (T_A = +70°C)
32 TQFN (derate 34.5 mW/°C above +70°C)
(multilayer board) 2758.6mW
Junction-to-Ambient Thermal Resistance (θ_{JA})
32 TQFN.....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})
32 TQFN.....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{IN_}$ = 10V, $V_{OUT_}$ = 3.3V, CVIN_ = 1µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, $T_A = T_J$ = -40°C to +125°C, with typical value at T_A = 25°C, unless otherwise stated) (See *Typical Application Circuits*) (Note 1).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY VIN_						
IN1-2 Voltage Range	VIN_RANGE		4.5		16	V
IN1 Standby Current	IIN1_STBY	EN1-2 = SGND (shutdown)		1	1.9	mA
IN2 Standby Current	IIN2_STBY	EN1-2 = SGND (shutdown)		10	20	µA
IN1-2 Undervoltage Lockout	VIN_UVLO_R	Rising	4.0	4.2	4.4	V
	VIN_UVLO_F	Falling	3.2	3.4	3.6	V
IN1-2 Undervoltage Lockout for $V_{OUT} \geq 4.75V$	VIN_UVLO_R 5VOUT	Rising	5.8	6.0	6.2	V
	VIN_UVLO_F 5VOUT	Falling	4.1	4.3	4.5	V
ENABLES						
EN_ Rising Threshold	EN_TH_R		1242	1262	1287	mV
EN_ Threshold Hysteresis	EN_TH_HYS			250		mV
EN_ Input Leakage Current	EN_ILEAK	V_{EN} = 5V, T_A = 25°C	-100	0	100	nA
LDO						
V_{CC} Output Voltage Range	VCC_RANGE	$6V < V_{IN1} < 16V$		4.5		V
V_{CC} Output Voltage (Dropout)	VCC_DROP	V_{IN1} = 4.5 V, I_{VCC} = 20mA	4.3			V
V_{CC} Current Capability	I_VCC	V_{CC} = 4.3V, V_{IN1} = 6V	50			mA
INTERNAL CHIP INPUT SUPPLY						
AVCC UVLO	AVCC_TH_R	Rising			3.9	V
	AVCC_TH_F	Falling	3.2			V

Electrical Characteristics (continued)

(VIN_ = 10V, VOUT_ = 3.3V, CVIN_ = 1µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, T_A = -40°C to +125°C with typical value at T_A = 25°C, unless otherwise stated) (See *Typical Application Circuits*) (Note 1).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONFIGURATION PINS						
COARSE_, FINE_, SS_, MODE pins Analog Resolution	#BITS_L			4		Bits
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TW_TH	Temperature rising (Note 3)		160		°C
Thermal Shutdown Hysteresis	TW_HYS	Temperature falling (Note 3)		20		°C
SYNCHRONIZATION						
SYNC Threshold Level High	SYNC_H		1.8			V
SYNC Threshold Level Low	SYNC_L				0.6	V
SYNC Frequency Range	SYNC_FREQ1	6V < $V_{IN_}$ < 16V	0.9		1.3	MHz
	SYNC_FREQ2	4.5V ≤ $V_{IN_}$ ≤ 6V	0.45		2.2	MHz
Minimum SYNC Pulse Width	SYNC_PW		30			ns
SYNC Pull-Down Resistance	SYNC_PD			1		MΩ
POWER SWITCHES						
High-Side RDSon	HS_RON	For converter 1,2		50	90	mΩ
Low-Side RDSon	LS_RON	For converter 1,2		50	90	mΩ
LX_ Leakage Current	LX_LEAK	V_{LX} = V_{IN} – 1V, V_{LX} = V_{PGND} + 1V, T_A = 25°C			5	µA
BST_ On resistance	BST_RON	Note: Min BST capacitance = 10nF; I_{BST} = 10mA, V_{CC} = 5V		4.5		Ω
OSCILLATOR						
Minimum Off-Time	TOFF_MIN	Set by the internal clock. (Note 2)			6.5	%T_{SW}
Frequency Range	FREQ_RANGE1	1MHz; 6V < $V_{IN_}$ < 16V		1000		kHz
	FREQ_RANGE2	500kHz, 1MHz, 1.5MHz, 2MHz; 4.5V ≤ $V_{IN_}$ ≤ 6V	500		2000	kHz
Frequency Accuracy	FREQ_1MHZ	F_{SW} = 1MHz	969		1030	kHz
Frequency Accuracy Range 1	FREQ_ACC1	F_{SW} = 500kHz and 2MHz	-3.1		+3	%
Frequency Accuracy Range 2	FREQ_ACC2	F_{SW} = 1.5MHz. (Note 3)	-4		+4	%
OUTPUT VOLTAGE						
VOUT1-2 Output Voltage Accuracy	VOUT_0.9V	No load output voltage accuracy T = 25°C; V_{OUT} = 0.9V; 4.5V < $V_{IN_}$ < 16V. COARSE_ = 0010; FINE_ = 1101.	0.8927	0.9045	0.9166	V
	VOUT_1.2V	No load output voltage accuracy T = -40°C to 125°C; V_{OUT} = 1.2V; 4.5V < $V_{IN_}$ < 16V COARSE_ = 0011; Fine_ = 1100	1.1750	1.1990	1.2230	V

Electrical Characteristics (continued)

(VIN_ = 10V, VOUT_ = 3.3V, CVIN_ = 1µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, T_A = -40°C to +125°C with typical value at T_A = 25°C, unless otherwise stated) (See *Typical Application Circuits*) (Note 1).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOUT1-2 Output Voltage Lower Range	VOUT_RANGEL	8-bit resolution over 5.048V range. LSB = ~20mV; Min_V_{OUT} = 0010 1101; Max_V_{OUT} = 1011 1111.	0.9045		3.786	V
VOUT1-2 Output Voltage Higher Range	VOUT_RANGEH	8-bit resolution over 5.048V range. LSB = ~20mV; Min_V_{OUT} = 11xx 0000; Max_V_{OUT} = 11xx 1111.	4.752		5.048	V
OUT_ Pull-Down Resistance	OUT_RES	V_{OUT1-2} = 3.3V; ADDR = Disabled T_A = 25°C	30	42.5	55	kΩ
OUTPUT VOLTAGE FAULT THRESHOLDS						
Overvoltage Threshold	OV_TH	V_{OUT1-2} = 0.9V	116.4	119.7	122.9	%VOUT
Undervoltage Threshold	UV_TH	V_{OUT1-2} = 0.9V	78.1	79.9	81.7	%VOUT
Power Good Threshold High	PGOOD_H	V_{OUT1-2} = 0.9V	111.8	114.6	116.8	%VOUT
Power Good Threshold Low	PGOOD_L	V_{OUT1-2} = 0.9V	84.0	86.1	88.1	%VOUT
SOFT-START/STOP TIME						
Programmable Soft-Start Time Duration	SS_00		0.850	1	1.150	ms
	SS_01		3.40	4	4.60	ms
	SS_10		6.80	8	9.20	ms
	SS_11		13.60	16	18.40	ms
CURRENT LIMIT						
Buck1,2 LS Peak Current Limit Fault Threshold	ILIM	(Note 4)	3.59	4.2	4.7	A
Buck1,2 LS Runaway Current Limit Fault Threshold	IRWY	(Note 4)	4.72	5.6	6.82	A
Number of Peak Current Limit Events Before LATCHOFF	#ILIM			7		Events
Number of Runaway Current Limit Events Before HICCUP or LATCHOFF	#RWY			1		Event
Buck HICCUP Timeout	T_{HICCUP}	Cycles of programmable soft-start time before retry		64		Cycles

Note 1: Limits are 100% tested at T_A = 25°C. Maximum and Minimum limits are guaranteed by design and characterization over temperature

Note 2: Design Guaranteed by ATE characterization. Limits are not production tested

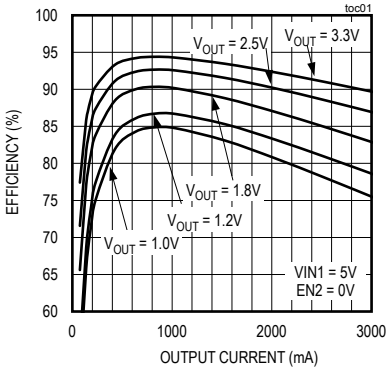
Note 3: Guaranteed by design; not production tested

Note 4: Current Limit and Runaway thresholds tracks in value and in temperature (see Typical Operating Characteristics section).

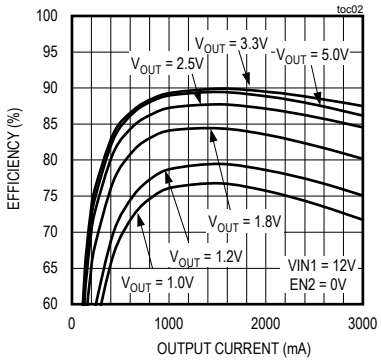
Typical Operating Characteristics

(CVIN_ = 10µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, f_{SW} = 1MHz, T_A = +25°C unless otherwise stated, default state on configuration setting.)

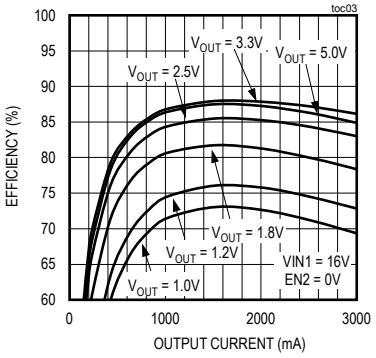
EFFICIENCY vs. OUTPUT CURRENT



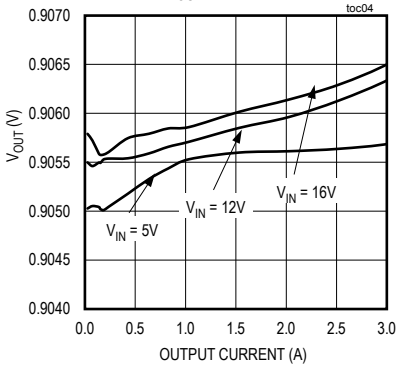
EFFICIENCY vs. OUTPUT CURRENT



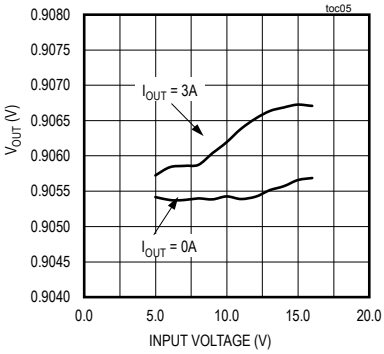
EFFICIENCY vs. OUTPUT CURRENT



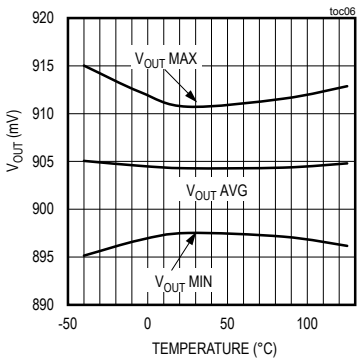
LOAD REGULATION
V_{OUT} = 0.9V



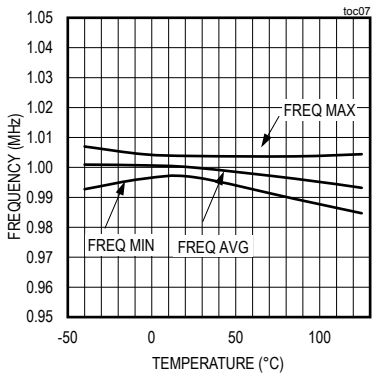
LINE REGULATION
V_{OUT} = 0.9V



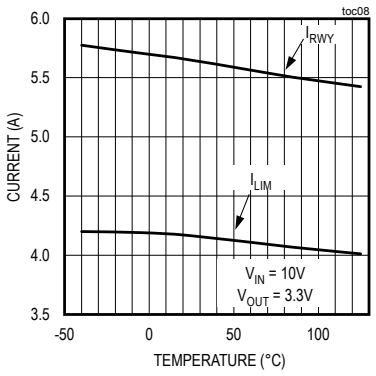
OUTPUT VOLTAGE vs. TEMPERATURE



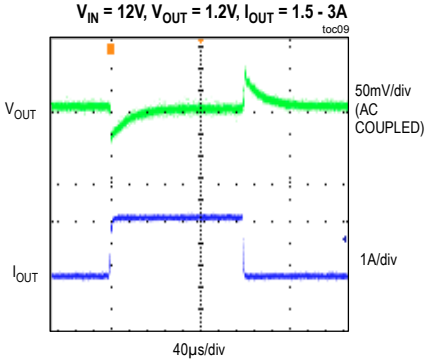
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE



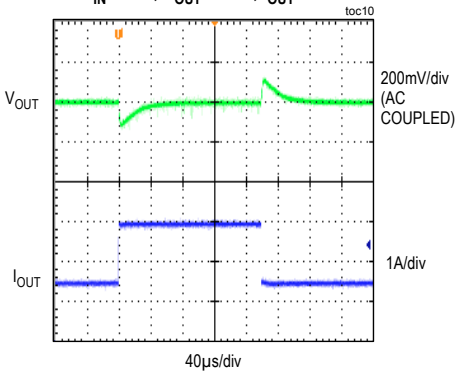
LOAD CURRENT TRANSIENT RESPONSE
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 1.5 - 3A



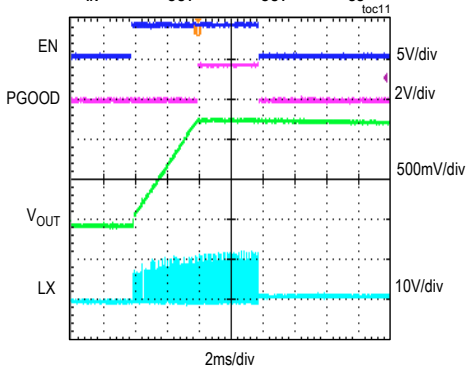
Typical Operating Characteristics (continued)

(CVIN_ = 10µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, f_{SW} = 1MHz, T_A = +25°C unless otherwise stated, default state on configuration setting.)

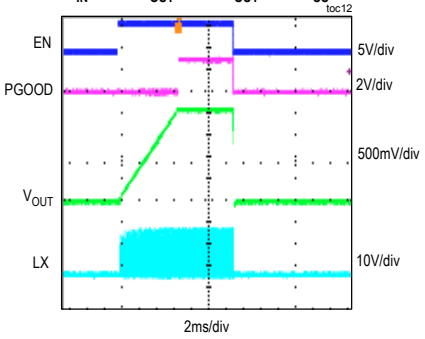
LOAD CURRENT TRANSIENT RESPONSE
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5 - 3A



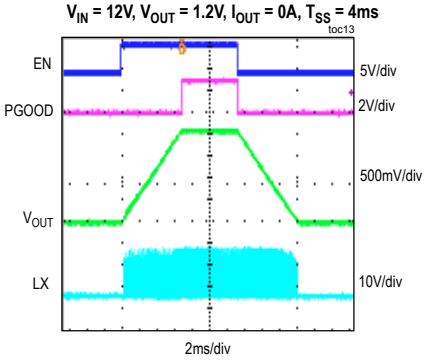
STARTUP/SOFTSTOP DISABLED
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, T_{SS} = 4ms



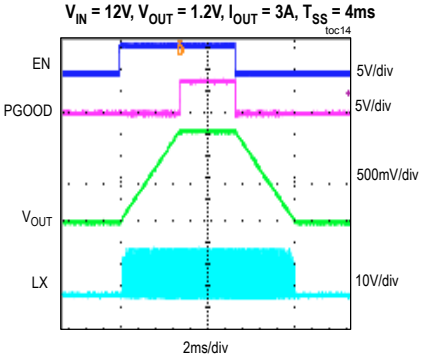
STARTUP/SOFTSTOP DISABLED
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 3A, T_{SS} = 4ms



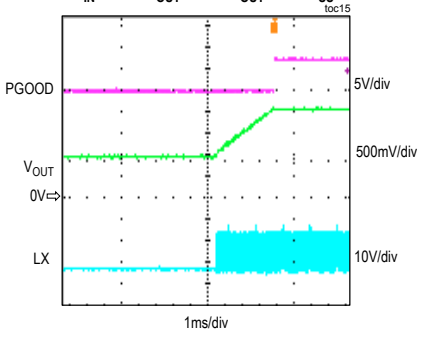
STARTUP/SOFTSTOP ENABLED
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, T_{SS} = 4ms



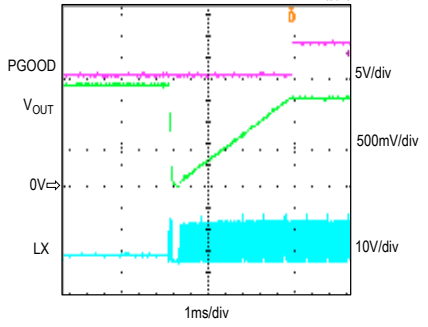
STARTUP/SOFTSTOP DISABLED
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 3A, T_{SS} = 4ms



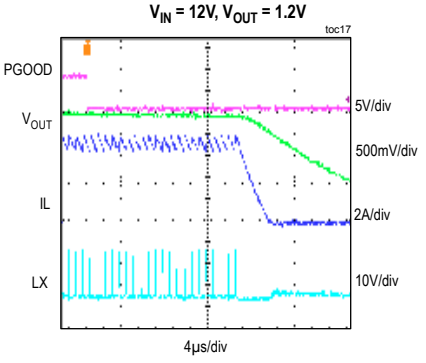
STARTUP INTO PRE-BIAS (50% OF TARGET)
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, T_{SS} = 4ms



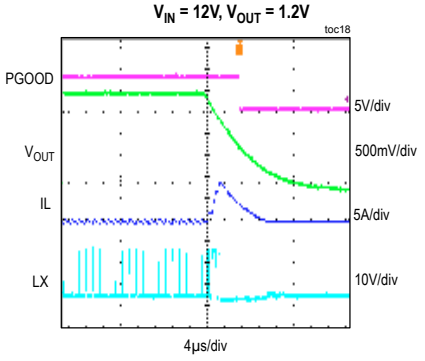
STARTUP INTO PRE-BIAS (120% OF TARGET)
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, T_{SS} = 4ms



LOAD SHORT-CIRCUIT SHUTDOWN (LATCH)
V_{IN} = 12V, V_{OUT} = 1.2V



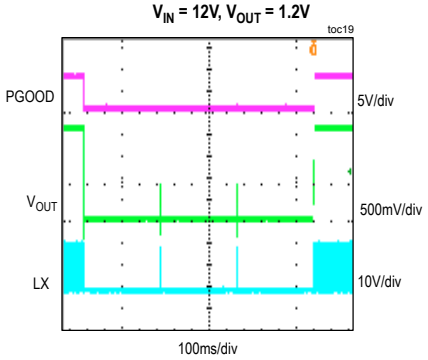
LOAD SHORT-CIRCUIT SHUTDOWN (HICCUP)
V_{IN} = 12V, V_{OUT} = 1.2V



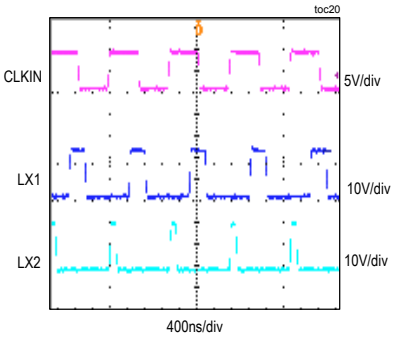
Typical Operating Characteristics (continued)

(CVIN_ = 10µF, CAVCC = 1µF, CVCC = 2.2µF, CBST_ = 0.1µF, f_{SW} = 1MHz, T_A = +25°C unless otherwise stated, default state on configuration setting.)

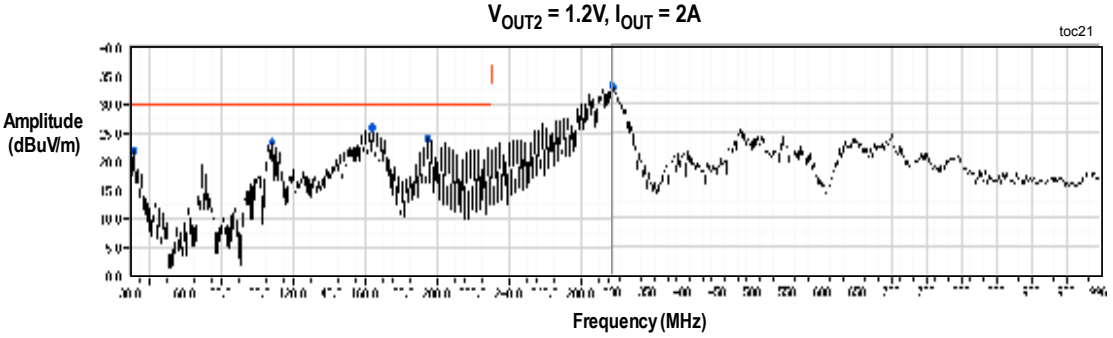
LOAD SHORT-CIRCUIT RECOVERY (HICCUP)
V_{IN} = 12V, V_{OUT} = 1.2V



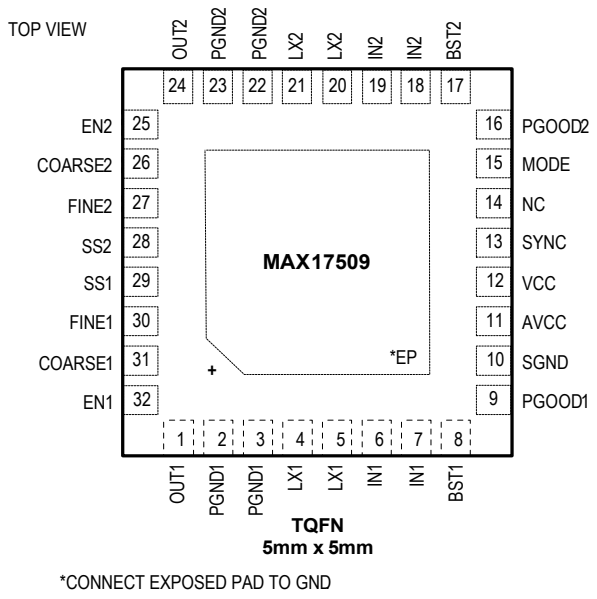
SYNCHRONIZATION vs. LX1 and LX2
180 OUT-OF-PHASE



RADIATED EMISSIONS (EN55022 Class B)
V_{IN} = 12V, V_{OUT1} = 3.3V, I_{OUT} = 2A,
V_{OUT2} = 1.2V, I_{OUT} = 2A



Pin Configuration



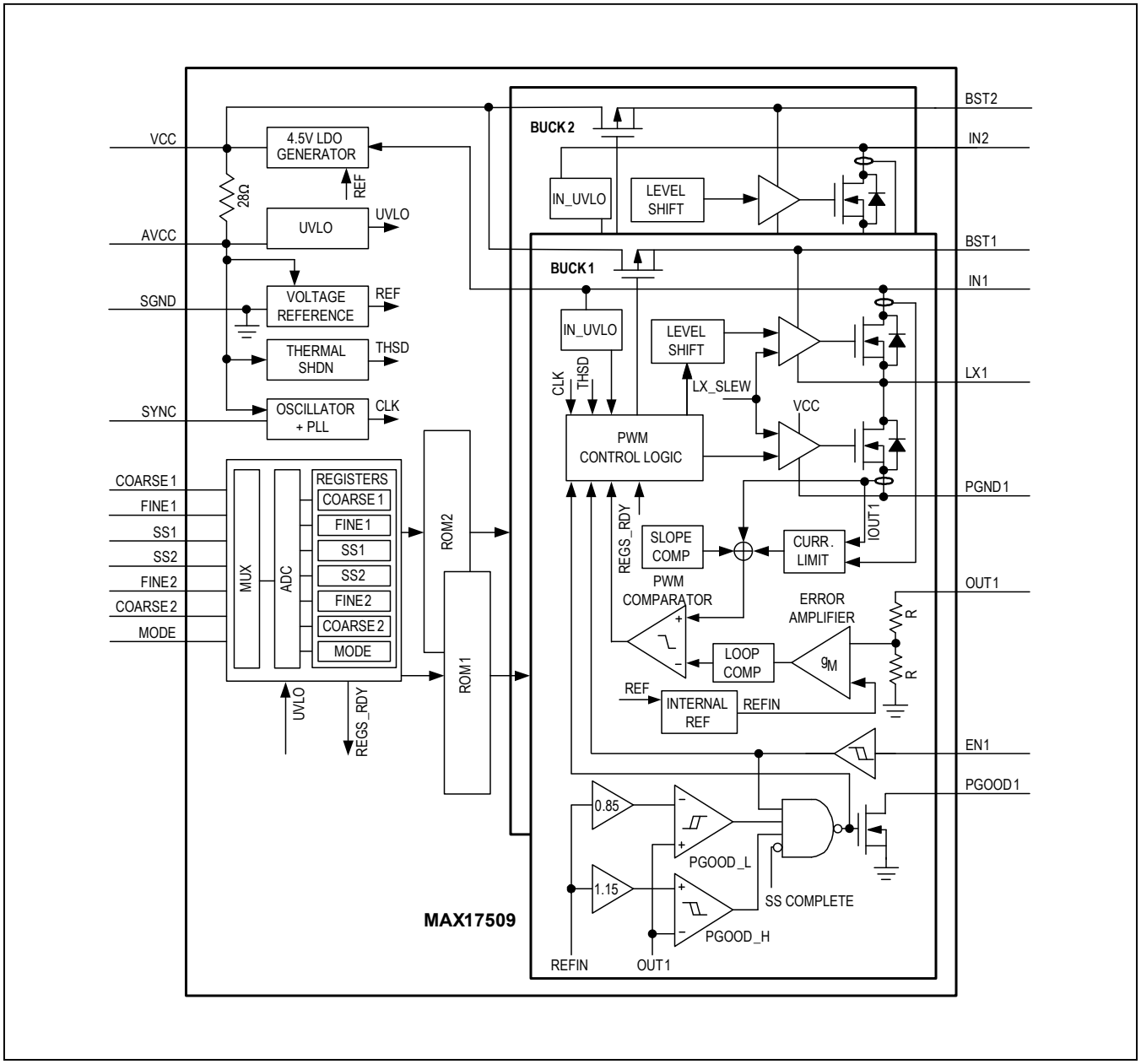
Pin Description

PIN	NAME	FUNCTION
1	OUT1	Regulator 1 Feedback Regulation Point. Connect OUT1 to output of Regulator 1 to sense the output voltage.
2, 3	PGND1	Power Ground Connection for Regulator 1. Connect negative terminal of output capacitor and input capacitor of Regulator 1 to PGND1. Connect PGND1 externally at a single point to SGND.
4, 5	LX1	Inductor Connection for Regulator 1. Connect LX1 to the switched side of the inductor.
6, 7	IN1	Input Supply for Regulator 1 and Internal 5V LDO. Bypass IN1 to PGND1 with a 10µF and 0.1µF ceramic capacitor as close as possible to the device.
8	BST1	Regulator 1 High-Side Gate-Driver Supply. Connect a 0.1µF ceramic capacitor from BST1 to LX1.
9	PGOOD1	Open-Drain Power Good Output for Regulator 1. PGOOD1 is low if OUT1 is 15% (typ) above or below the normal regulation point. PGOOD1 asserts low during soft-start, and when the device is shut down due to disabling or due to fault responses. PGOOD1 becomes high impedance when OUT1 is in regulation. To obtain a logic signal, pullup PGOOD1 with an external resistor (10kΩ) connected to a positive voltage less than 5.5V.
10	SGND	Signal Ground Connection. Connect SGND to PGND_ at a single point typically near the output capacitor ground.
11	AVCC	Input for Internal Analog Circuits. Connect a minimum of 1µF ceramic capacitor from AVCC to SGND. Internally connected to VCC with 28Ω resistor.
12	VCC	Internal 5V LDO Output. it acts as low side gate driver supply. Connect a 2.2µF ceramic capacitor from VCC to PGND_.

Pin Description (continued)

PIN	NAME	FUNCTION
13	SYNC	External Clock Synchronization Input. Connect an external clock for frequency synchronization to within 0.7 - 2.75 of the internal switching frequency with a limit of 450kHz to 2.2MHz before regulation start for stable operation.
14	N.C.	No Connect. Connect this pin to ground.
15	MODE	Mode Selection Pin. Programming input to select: - Two Independent Outputs or Dual-phase Single Output Mode - Phase Shift (0 or 180°) - Internal Clock Frequency (500KHz/1.0MHz/1.5MHz/2MHz at $5V_{IN}$, or 1.0MHz at $12V_{IN}$)
16	PGOOD2	Open-Drain Power-Good Output for Regulator 2. PGOOD2 is low if OUT2 is 15% (typ) above or below the normal regulation point. PGOOD2 asserts low during soft-start, and when the device is shut down due to disabling or due to fault responses. PGOOD2 becomes high impedance when OUT2 is in regulation. To obtain a logic signal, pull up PGOOD2 with an external resistor (10kΩ) connected to a positive voltage less than 5.5V.
17	BST2	Regulator 2 High-Side Gate-Driver Supply. Connect a 0.1µF ceramic capacitor from BST2 to LX2.
18, 19	IN2	Input Supply for Regulator 2. Bypass IN2 to PGND2 with a 10µF and 0.1µF ceramic capacitor as close as possible to the device.
20, 21	LX2	Inductor Connection for Regulator 2. Connect LX2 to the switched side of the inductor.
22, 23	PGND2	Power Ground Connection for Regulator 2. Connect negative terminal of output capacitor and input capacitor of Regulator 2 to PGND2. Connect PGND2 externally at a single point to SGND.
24	OUT2	Regulator 2 Feedback Regulation Point. Connect OUT2 to output of Regulator 2 to sense the output voltage.
25	EN2	Enable Pin for Regulator 2. The voltage at EN2 is compared to internal comparator reference to determine when to enable the regulation. Pull-up to AVCC to enable Regulator 2, or optionally connect to a resistor-divider from IN2 to EN2 to SGND to program the UVLO level. Pull EN2 to SGND to disable the Regulator 2.
26	COARSE2	Regulator 2 Output Voltage Coarse Programming.
27	FINE2	Regulator 2 Output Voltage Fine Programming.
28	SS2	Regulator 2 Soft-Start/Stop Time Programming and Lx-Slew Rate Selection Pin.
29	SS1	Regulator 1 Soft-Start/Stop Time Programming and Overcurrent Response Selection Pin.
30	FINE1	Regulator 1 Output Voltage Fine Programming.
31	COARSE1	Regulator 1 Output Voltage Coarse Programming.
32	EN1	Enable Pin for Regulator 1. The voltage at EN1 is compared to internal comparator reference to determine when to enable the regulation. Pull up to AVCC to enable Regulator 1, or optionally connect to a resistor-divider from IN1 to EN1 to SGND to program the UVLO level. Pull EN1 to SGND to disable the Regulator 1.
	EP	Exposed Paddle. Connect EP to a large copper plane at SGND potential to improve thermal dissipation. Do not use EP as SGND ground connection alone.

Functional Diagram



Detailed Description

The MAX17509 is a valley-current-mode, synchronous pulse-width-modulated (PWM) buck regular designed to provide either two independent 3A outputs (see Figure 1) or a single 6A output (see Figure 2). The device operates over an input-voltage range of 4.5V to 16V and generates independently adjustable output voltage in the ranges of 0.904V to 3.782V and 4.756V to 5.048V in 20mV steps with ±2% system accuracy over load, line, and temperature. The power solution can be completed using only external resistors setting. The self-configured internal compensation scheme allows a simple plug-and-play solution without the need for compensation parameter calculation.

The MAX17509 supports a selectable switching frequency of either 500kHz, 1MHz, 1.5MHz or 2MHz for input supply rails up to 6V. For supply rails greater than 6V, the switching frequency can be programmed only to 1MHz. The device can be synchronized to an external clock (see Switching Frequency/External Synchronization/Phase Shift section for details. The phase shift between the two regulators can be set to either 0 or 180°. Programmable switching slew rate allows for electromagnetic compliant optimization. For sequencing purposes, the device provides enable inputs, power good outputs, the ability to adjust soft-start timing, and the option to power down with soft-stop. Adjustable soft-start reduces the inrush current by gradually ramping up the internal reference voltage, and also powers up glitch-free into a prebiased output. Protection features include internal input undervoltage lockout (UVLO) with hysteresis, lossless, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, undervoltage/overvoltage protection, and thermal shutdown.

Input Supply (IN_)/Internal Linear Regulator (V_{CC})

The input supply voltage ($V_{IN_}$) is the input power supply for internal regulators, which support a voltage range from 4.5V to 16V. In addition, it has an internal linear regulator (V_{CC}) to provide its own bias from a high-voltage input supply at V_{IN1}. V_{CC} bias supply provides up to 50mA typical total current directly for gate drivers for the internal MOSFETs, and through AVCC pin for the analog controller, reference, and logic blocks. The linear regulator has an overcurrent threshold of approximately 150mA. In case of an overcurrent event on V_{CC}, the current is limited, and V_{CC} voltage starts to droop.

At higher input voltages (V_{IN1}) of 5.0V to 16V, V_{CC} is regulated to 4.5V. At 5.0V or below, the internal linear regulator operates in dropout mode, where V_{CC} follows V_{IN1}.

For input voltages of less than 5.5V, connect V_{IN1} and V_{CC} together to power the MAX17509 directly to increase efficiency by bypassing the internal LDO. If V_{CC} is supplied externally and $V_{IN1} < V_{CC}$, switching activities will be inhibited. For input voltage ranges higher than 5.5V, use the internal regulator. Bypass $V_{IN_}$ to PGND_ with a low-ESR, 0.1µF and 10µF or greater ceramic capacitor, and V_{CC} with a low-ESR, ceramic 2.2µF capacitor to PGND_ placed close to the device.

Once the input bias supply rises above its UVLO rising threshold 4.2V (typ), the regulators are allowed to regulate the output voltages. If the $V_{IN_}$ voltage is below the input undervoltage lockout (VIN_UVLO) threshold 3.4V (typ), the controller stops switching and turns off both high-side and low-side gate drivers until the $V_{IN_}$ voltage recovers. In case the 5V range output voltage is selected, VIN_UVLO rising threshold will change in order to allow proper start-up of the respective channel. In this case, the VIN_UVLO_ value is 6V rising threshold and 4.3V falling threshold. See criteria of the device to begin the regulation in the Soft-Start/Soft-Stop and Prebias Condition section.

Internal Chip Supply Input Voltage Range (AVCC)

AVCC is the input for internal analog circuitry. The AVCC input undervoltage lockout (AVCC_UVLO) circuitry inhibits switching if the 4.5V AVCC supply is below its AVCC_ UVLO threshold, 3.2V (typ). Once the 5V bias supply AVCC rises above its UVLO rising threshold and EN1 and EN2 enable the buck controllers, the controllers start switching and the output voltages begin to ramp up using soft-start. Bypass AVCC to SGND with a low-ESR, 1µF or greater ceramic capacitor placed close to the device.

Device Configuration from Pin Programming

Power solution with MAX17509 can be configured completely using 7 configuration pins. The configuration pins are MODE, SS[1,2], COARSE[1,2], and FINE[1,2]. To recognize the value of resistance reliably, connect standard 1% resistors between the configuration pins and SGND, and keep the trace length to below 3cm to minimize the trace capacitance. These pins are read once when the voltage on AVCC is above AVCC_TH_R. The pins are re-read when AVCC rises above AVCC_ TH_R after dropping below AVCC_TH_F. There is a fixed 2ms total time (typ.) required for device configuration. EN_ signals are ignored during this time, and switching activity is only allowed to occur subsequently.

MODE pin chooses between single-phase (two outputs) and dual-phase (one output), sets the relative phase-shift

of the PWM between two regulators, and sets the internal switching frequency. SS1 chooses between brickwall/latchoff and hiccup for the OCP behavior of both regulators, and enables/disables soft-stop along with soft-start/stop time for Regulator 1. SS2 chooses between maximum and minimum Lx-slew rate for both regulators, and enables/disables soft-stop along with soft-start/stop time for Regulator 2. MODE, SS[1,2], COARSE[1,2], and FINE[1,2] have 16 possible selections.

The configuration pins can respond to both pin strapping and resistor programming, and the settings summarized in Table 1. The table also shows a correspondence between the resistor values to the index numbers. Pin strapping takes three possible stages: V_{CC}, OPEN, GND. V_{CC} and OPEN provide the same setting result. The resistor value for each pin is independent from each other, and Table 2 show examples of a few scenarios of the settings. The details of the each functional behavior are described in the corresponding sections subsequently.

Table 1. Summary of Resistor Programming

INDEX	1% RES.	MODE			SS1			SS2			COARSE_	FINE_
	(kΩ)	MODE	PHASE SHIFT	FSW	OC	SSTOP1	TSS1 (ms)	LX-SLEW	SSTOP2	TSS2 (ms)	COARSE VOUT (V)	FINE VOUT (V)
0	475 (OPEN or VCC)	TWO SINGLE-PHASE INDEPENDENT OUTPUTS	180°	500kHz	BRICKWALL AND LATCHOFF	DISABLE	1	MAXIMUM	DISABLE	1	0.650	0.000
1	200			1.0MHz			4			4		0.019
2	115			1.5MHz			8			8		0.037
3	75			2.0MHz			16			16	0.966	0.057
4	53.6		0°	500kHz		ENABLE	1		ENABLE	1	1.281	0.078
5	40.2			1.0MHz			4			4	1.597	0.097
6	30.9			1.5MHz			8			8	1.912	0.115
7	24.3			2.0MHz			16			16	2.228	0.135
8	19.1	DUAL-PHASE, SINGLE-OUTPUT	180°	500kHz	HICCUP	DISABLE	1	MINIMUM	DISABLE	1	2.543	0.157
9	15			1.0MHz			4			4	2.859	0.176
10	11.8			1.5MHz			8			8	3.174	0.194
11	9.09			2.0MHz			16			16	3.490	0.213
12	6.81			500kHz		ENABLE	1		ENABLE	1	4.756 (7V VIN)	0.235
13	4.75			1.0MHz			4			4	4.756 (9V VIN)	0.254
14	3.01			1.5MHz			8			8	4.756 (12V VIN)	0.272
15	GND			2.0MHz			16			16	4.756 (16V VIN)	0.291

Table 2. Examples of Resistor Programming

SETTINGS	MODE	SS1	SS2	COARSE1	FINE1	COARSE2	FINE2
MODE = Single-Phase (Two Outputs), 180° Phase-Shift, 1MHz SS1 = Hiccup OCP, Soft-Stop 1 Disabled, Soft-Start Time 1 = 8ms SS2 = Maximum Lx-Slew Rate, Soft-Stop 2 Enabled, Soft-Start Time 2 = 16ms Note: 12VIN VOUT1 = 5.0V (4.756V + 0.254V) VOUT2 = 1.2V (0.966V + 0.235V)	200kΩ	11.8kΩ	24.3kΩ	3.01kΩ	4.75kΩ	75kΩ	6.81kΩ
MODE = Dual-Phase (Single Output), 180° Phase-Shift, 2.0MHz SS1 = Brickwall and Latchoff OCP, Soft-Stop 1 Disabled, Soft-Start Time 1 = 4ms SS2 = Minimum Lx-slew Rate VOUT = 1.8V (1.597V + 0.194V)	9.09kΩ	200kΩ	GND	40.2kΩ	11.8kΩ	40.2kΩ	11.8kΩ

EN_

A regulator allows to start the regulate output voltage when the voltage on EN_ is above EN_TH_R level of 1.262V (typ.) after device configuration from pin programming is complete. EN_ below EN_TH_F results in regulator disable.

To configure the device to self-enable when input voltage is sufficient, pull EN_ to AVCC. Optionally, to set the voltage at which the device turns on from VIN, connect a resistive voltage-divider from IN_ to GND (Figure 1) with the center node of the divider to EN_. Choose R_U to be 10k - 100kΩ, and then calculate R_B as:

$$R_B = R_U \times \left[\frac{1.262}{V_{INU} - 1.262} \right]$$

where V_{INU} is the voltage at which the device is required to turn on. For adjustable output voltage devices, ensure that IN_ is higher than 0.93 x V_{OUT}.

Soft-Start/Soft-Stop and Prebias Condition

Once a regulator is enabled by driving the corresponding EN_ above EN_rising threshold, the soft-start circuitry gradually ramps up the reference voltage during soft-start time to reduce the input surge currents during startup. The device controls switching activities to have only positive inductor current, and then gradually transition to PWM mode at the end of soft-start. Before the device can begin the soft-start, the following conditions must be met:

1) AVCC_ exceeds the 3.9V (max) AVCC rising threshold (AVCC_TH_R).
2) Reading of pin configuration is complete.
3) IN_ exceeds the 4.4V (max) IN undervoltage lockout threshold (VIN_UVLO_R).
4) EN_ exceeds the 1.3V (max) EN rising threshold (EN_TH_R).
5) The device temperature is below 160°C thermal shutdown threshold.

SS_ pins are used to select the soft-start timing among 1, 4, 8, and 16ms, as well as to enable the soft-stop option. The default setting will be 8ms soft-start timing, and soft-stop disabled. For V_{OUT} ≥ 2.5V, use a minimum of 4ms soft-start time.

There are two scenarios for startup sequence depending on the initial output voltage. During both scenarios, UV and OV are disabled, and overcurrent protection operates in brickwall mode (±4.2A). In the case that the device starts from an initial output voltage below the target, the device will not cause the output voltage to dip down by not sinking current from the output. In the case of starting from an initial output voltage above target, the device smoothly discharges the output voltage by decreasing the internal reference voltage down to 0V in 512µs, and then initiates the soft-start sequence. During this discharge period, the negative current limit is gradually increased to allow up to 4.2A of negative current to prevent a sudden dip in output voltage. During the follow soft-start sequence, the device ramps up the internal reference to the target level with both high-side and low-side switches activated.

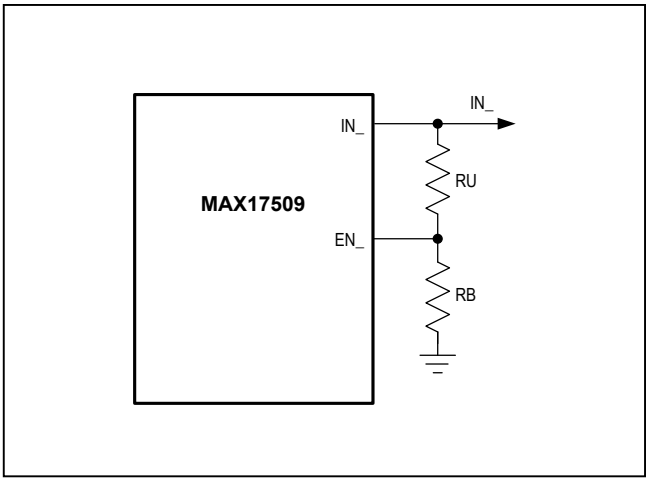


Figure 1. Adjustable EN network

With soft-stop option, when the device is disabled the soft-stop circuitry gradually ramps down the reference voltage with the same time as soft-start timing to discharge the remaining energy in the output capacitor in a controlled manner. During a soft-stop event, faults are masked as during start-up, and no hiccup will occur after a fault even though hiccup is set. To ensure a proper soft-stop sequence the device must be in PWM mode. This requires the duration of the EN_ signal to be longer than the soft-start time. Soft-stop should be used for two-independent-output configuration only, and not in dual-phase, single-output mode.

Switching Frequency/External Synchronization/Phase Shift

The MAX17509 supports a selectable switching frequency of either 500kHz, 1MHz, 1.5MHz, or 2MHz for input supply rails up to 6V. For supply rails greater than 6V, the switching frequency can be programmed only to 1MHz. High-frequency operation optimizes the application for the smallest component size, lower output ripple, and improve transient response, but trading off efficiency to higher switching losses. Low-frequency operation offers

the best overall efficiency at the expense of component size and board space. The device also offers the option to set the relative PWM phase-shift between the regulators to be in-phase (0°) or interleave (180° out-of-phase). With in-phase setting, Regulator 2's low-side MOSFET turn on at the same time as Regulator 1. With out-of-phase setting, the Regulator 2's low-side MOSFET turns on with a time delay corresponding to half of the switching period. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating, allows for fewer or less expensive capacitors, and reduces shielding requirements for electromagnetic interference (EMI). A resistor on the MODE pin allows the user to set the desired switching frequency, phase shift, and independent output/dual-phase operation.

The device can be synchronized to an external clock by connecting the external clock signal to SYNC with frequency within 900kHz to 1.3MHz before regulation start for a stable operation for 1.0MHz internal switching frequency at $12V_{IN}$ range, and within 0.7 - 2.75 of the internal switching frequency with a limit of 450kHz to 2.2MHz for $5V_{IN}$ range. With lower switching frequency, the pre-set peak current limit tends to make the effective DC current limit lower due to higher inductor peak current, but this can be compensated by choosing higher inductance value. Regulator 1's high-side MOSFET turning off with a time delay corresponding to 58% of the switching period (210°) with respect to the rising edge of SYNC signal, and Regulator 2's high-side MOSFET turning on depends on the relative phase-shift setting. The minimum external clock pulse-width high should be greater than 30ns.

Single and Dual-Phase mode

MODE pin is used to configure MAX17509 to produce two single-phase independent outputs or a dual-phase single-output regulator. In single-phase mode, the component selection and operation of each phase is independent from each other.

In dual-phase mode, the two phases operate to supply a shared output current up to 6A with 180° relative phase shift of PWM. The inductor selection must be the same, and EN_ should be connected together. The configuration of both phases is determined by that of Regulator 1 (OC, SSTOP, TSS, COARSE1, FINE1). SS2 is still needed to set Lx-slew of both phases with the option to use only pin strapping: pull-up to V_{CC} for maximum Lx-slew and pull-down to GND for minimum. The OCP behavior is recommended to be set to brickwall and latchoff option. The operation and functional behavior (startup/shutdown, regulation, fault responses) will be uniform between the two phases.

Output Voltage Setting (COARSE_ and FINE_) and Sensing (VOUT_)

COARSE_ and FINE_ pins set the output range of each regulator in MAX17509 in 20mV steps from 0.904V to 3.782V and 4.756V to 5.048V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. VOUT_ senses the output voltage feedback used for output voltage monitoring and fault detection. Connect VOUT_ directly to the point of regulation

The target output voltage is achieved by the sum of coarse voltage (COARSE_) and an offset (FINE_). The resistor value can be found from cross-referencing the index number to the resistor value on Table 1. For a target output voltage between 0.904V to 3.782V, the index of the two resistors can be found from (Equations 2 and 3) with a minimum V_{COARSE} of 0.904V. For 4.756V to 5.048V, COARSE_ resistor is selected based on input voltage with index from 12 to 15, and FINE_ resistor can be found from (Eq.3), where $V_{OUTCOARSE}$ is 4.756V. Table 3 shows resistor setting for typical output voltages.

$$V_{OUT} = \left(\frac{5.048}{256}\left[16 \times Index_{COARSE} + 1 + Index_{FINE}\right]\right)$$

(Equation 1) for $0.904V \le V_{OUT} \le 3.782V$, min. $Index_{COARSE} = 2$

$$Index_{COARSE} = Integer\left(\frac{1}{16}\left[\frac{256 \times V_{OUT}}{5.048} - 1\right]\right)$$

(Equation 2) for $0.904V < V_{OUT} < 3.782V$

$$Index_{FINE} = Integer\left(\frac{256}{5.048}\left[V_{OUT} - V_{OUTCOARSE}\right]\right)$$

(Equation 3)

Table 3. V_{OUT} Setting for Common Output Voltages

V_{OUT} (V)	COARSE INDEX	FINE INDEX	COARSE RESISTOR	FINE RESISTOR
0.9	2	13	115k	4.75k
1.0	3	2	75k	115k
1.2	3	12	75k	6.81k
1.5	4	11	53.6k	9.09k
2.0	6	5	30.9k	40.2k
2.5	7	14	24.3k	3.01k
3.0	9	7	15.0k	24.3k
3.3	10	7	11.8k	24.3k
5.0 (7V V_{IN}) 5.0 (9V V_{IN}) 5.0 (12V V_{IN}) 5.0 (16V V_{IN})	12 13 14 15	13	6.81k 4.75k 3.01k GND	4.75k

High-Side Gate-Driver Supply (BST_)

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_ and transferring the bootstrap capacitor's (at BST_) charge to the gate of the internal high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX_ voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor. The boost capacitor should be a low-ESR ceramic capacitor with a minimum value of 100nF.

Adjustable Switching Slew Rate

Reducing the LX switching transition time has the benefit of improved efficiency; however, the fast slewing of the LX slew nodes results in relatively high radiated EMI. MAX17509 has the ability to program the slew rate of LX switching nodes to address noise requirements in sensitive applications such as multi-GB transceiver supplies in FPGA applications. SS2 pin can set Lx-slew rate of both regulators to be either the maximum (5V/ns) or minimum value (0.25V/ns).

Current Protections (UC/OCP/OCR) and Retry Setting (Hiccup vs. Brickwall and Latchoff)

The current protection circuit monitors the output current levels through both internal high-side and low-side MOSFETs during all switching activities to protect them during overload and short-circuit conditions. Peak positive current limit (OC), valley negative undercurrent limit (UC), and positive runaway overcurrent (OCR) limit are three types current fault events. Peak positive current limit can occur when the load demand is greater than the regulator capability (overloading). Valley negative current limit can occur when the regulator sinks current, where the device draws the energy back from the output, such as during soft-start from above target output voltage level or soft-stop. OCR can occur when the output is short to ground, and the cycle-by-cycle switching results in a rapid increase in current without sufficient voltage across inductor to properly discharge. OCR current limit is declared when the current level reached 5.6A (typ), and the regulator shuts immediately similar to fault response due to output undervoltage (UV) or output overvoltage (OV) events.

SS1 pin sets options to attempt regulation following those fault event(s), in addition to fault response due to UC/OC protection. The two options for fault response due to UC/OC protection are (1) Hiccup and (2) Brickwall and Latchoff.

With Hiccup setting, the UC/OC current fault protection is set to shut down immediately, which implies that the regulators shut down immediately after UC/OC/OCR/UV or OV occurs. An UC or OC event is declared after the device sensed seven consecutives peak positive current limit above 4.2A (typ), or consecutives valley negative undercurrent limit below -4.2A (typ). Subsequently, the regulator attempts a soft-start sequence after the Hiccup timeout period expired, which corresponds to the 64 times period set for soft-start time. This allows the overload current to decay due to power loss in the converter resistances, load, and the inductor before soft-start is attempted again.

With Brickwall and Latchoff setting, the current fault protection is set to constant current mode. The device attempts to provide continuous output current limited by peak positive current-limit (4.2A typ) in current-sourcing event, while in a current-sinking event it attempts to continuously sink current limited by valley negative undercurrent limit (-4.2A typ). With this setting UC/OC status is latched, and the switching activities continue until OCR/UV/OV/OT or disable event(s) occur. If a shutdown due to an OCR/UV or OV event occurs, the regulator remains shutdown until the EN_ input is toggled.

During current-sinking, the input voltage can increase since the energy is delivered back to the input. It is recommended to monitor the input voltage to ensure that it is below the device's limit. In an application where the load is inductive, the output could swing negatively below ground when it is suddenly shorted to ground. In order to withstand such a stress it is recommended to place a 50Ω series resistor close to the IC from OUT_ to the regulation point.

Output Overvoltage Protection (OVP)

The MAX17509 includes an output overvoltage protection (OVP) circuit that begins to monitor the output through VOUT_ pin once the soft-start is complete. If the output voltage rises above 120% (typ) of its nominal regulation voltage, the regulator shuts down. The subsequent response depends on retry setting.

Output Undervoltage Protection (UVP)

The MAX17509 includes an output undervoltage protection (UVP) circuit that begins to monitor the output through VOUT_ pin once the soft-start is complete. If the output voltage drops below 80% (typ) of its nominal regulation voltage, the regulator shuts down. The subsequent response depends on retry setting.

Over Thermal Protection

The MAX17509 features a thermal-fault protection circuit. When the junction temperature rises above +160°C (typ), a thermal sensor activates, pulls down the PGOOD outputs, and shuts down both regulators. The regulators are allowed to restart after the junction temperature cools by 20°C (typ).

Power Good Output (PGOOD_)

PGOOD_ is an open-drain output of the window comparator that continuously monitors output voltage. Effectively, it indicates fault conditions, including UV/OV of output voltage, OCR of regulators' current, and OT. PGOOD_ can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn on subsequent supplies.

Each PGOOD_ goes high (high impedance) when the corresponding channel has completed soft-start, regulator output voltage is in regulation. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 15% (typ) or rises above 15% (typ) of its nominal regulated voltage. PGOOD_ asserts low during soft-start, soft-stop, fault conditions, and when the corresponding regulator is disabled. Connect a 1k – 100kΩ (10kΩ, typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal. PGOOD pins cannot sink more than 10mA of current.

Design Procedure

Input Voltage Range

The maximum value ($V_{IN\ (MAX)}$) and minimum value ($V_{IN\ (MIN)}$) must accommodate the worst-case conditions accounting for the input voltage soars and drops. If there is a choice at all, lower input voltages result in better efficiency. With a maximum duty cycle of 93%, V_{OUT} is limited to 0.93 x V_{IN}.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements of the regulator can be determined by the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller.

The worst-case RMS current requirement occurs when operating with D = 0.5. At this point, the above equation simplifies to I_{RMS} = 0.5 x I_{OUT}.

The minimum input capacitor required can be calculated by the following equation,

$$C_{IN} = \frac{\left(I_{IN_AVG}\right) \times (1 - D)}{\left(\Delta V_{IN}\right) \times F_{SW}}$$

Where,

I_{IN_AVG} is the average input current given by,

$$I_{IN_AVG} = \frac{P_{OUT}}{\eta \times V_{IN}}$$

D is the operating duty cycle, which is approximately equal to V_{OUT}/V_{IN}

ΔV_{IN} is the required input voltage ripple

f_{SW} is the operating switching frequency

P_{OUT} is the out power, which is equal to V_{OUT} x I_{OUT}

η is the efficiency.

For the MAX17509 system (IN_) supply, ceramic capacitors are preferred due to their resilience to inrush surge currents typical of systems, and due to their low parasitic inductance, which helps reduce the high-frequency ringing on the IN supply when the internal MOSFETs are turned off. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity. A 10µF works well in general

application. Place an additional 0.1µF between IN_ and PGND_ as close to the device as possible.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX17509: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. MAX17509 is optimally designed to work with 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{SUP(MIN)} - V_{OUT}\right)}{V_{SUP(MIN)} \times f_{SW} \times I_{OUT(MAX)} \times LIR}$$

where $V_{SUP(MIN)}$ is the minimum supply voltage, V_{OUT} is the typical output voltage, and $I_{OUT(MAX)}$ is the maximum load current. f_{SW} is the switching frequency. However, if it is necessary, higher inductor values can be selected.

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz

The inductor specification must be large enough not to saturate at the peak inductor current (I_{PEAK}), or at least in a range where the inductance does not degrade significantly. The maximum inductor current equals the maximum load current in addition to half of the peak-to-peak ripple current. The runaway peak current limit (5.6A) can be used directly for the inductor saturation current specification of a conservative system design.

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Table 4 summarizes the optimal inductor and output capacitor value selection for typical $5V_{IN}$ and $12V_{IN}$ range. The requirement is to select an inductor greater than or equal to the value shown, and output capacitor the same actual value (not nominal value) or higher. The components listed optimize the transient response time and set bandwidth to be $f_{SW}/8$.

Table 4. Optimal Inductor and Output Capacitor Selection

V_{OUT} (V)	4.5V ≤ V_{IN} ≤ 6V (TYPICAL 5V_{IN} RANGE)								6 ≤ V_{IN} ≤ 16V (TYPICAL 12V_{IN} RANGE DOWN TO 6V_{IN})	
	F_{SW} = 500KHZ		F_{SW} = 1MHZ		F_{SW} = 1.5MHZ		F_{SW} = 2MHZ		F_{SW} = 1MHZ	
	L_{MIN} (µH)	C_{OUTMIN} (µF)	L_{MIN} (µH)	C_{OUTMIN} (µF)	L_{MIN} (µH)	C_{OUTMIN} (µF)	L_{MIN} (µH)	C_{OUTMIN} (µF)	L_{MIN} (µH)	C_{OUTMIN} (µF)
0.9	2.2	139	1	100	0.82	78	0.56	50	1	100
1	2.2	107	1.2	82	0.82	55	0.56	41	1.2	82
1.2	2.7	89	1.2	68	1	46	0.68	34	1.2	68
1.5	3.3	71	1.5	55	1	36	0.82	27	1.5	55
1.8	3.9	59	1.8	46	1.2	30	0.82	23	1.8	46
2	3.9	54	2.2	41	1.2	27	1	21	2.2	41
2.5	4.7	43	2.2	33	1.5	22	1.2	16	2.2	33
3	4.7	36	2.2	18	1.5	12	1.2	9	2.2	18
3.3	3.3	36	1.5	18	1.2	12	0.82	9	2.2	18
3.6	2.7	36	1.5	18	1.2	12	0.82	9	2.7	18
5.0 (7V_{IN})	(NOT APPLICABLE)								1.8	18
5.0 (9V_{IN})									2.7	18
5.0 (12V_{IN})									3.9	18
5.0 (16V_{IN})									4.7	18

Output Capacitor Selection

The output capacitor selection requires careful evaluation of several different design requirements – DC voltage rating, stability, transient response, and output ripple voltage. Based on these requirements, a combination of low-ESR polymer capacitor (lower cost but higher output-ripple voltage) and ceramic capacitor (higher cost but low output-ripple voltage) should be used to achieve stability with low output ripple.

When choosing the ceramic capacitors, it is recommended to choose the X5R and X7R dielectric formulations, since the dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. It is important to note that the capacitance decreases as the voltage applied increases; thus a ceramic capacitor rated at 47µF 6.3V may measure 47µF at 0V but measure 34µF with an applied voltage of 3.3V depending on the type of capacitor selected. Consult capacitor manufacturer datasheet for the derating.

Loop Compensation

The simplified equation for minimum capacitor is shown in the table below, where f_{SW} is the switch frequency in MHz, and C_{OUT} is the output capacitor in (µF). It is recommended to use all ceramic output capacitor solution, so that the ESR is placed such that the zero frequency formed by output capacitor and ESR is at or above $f_{SW}/2$.

Output Ripple Voltage

With polymer capacitors, the ESR dominates and determines the output ripple voltage. The step-down regulator's output ripple voltage (V_{RIPPLE}) equals the total inductor ripple current (ΔI_L) multiplied by the output capacitor's ESR. Therefore, the maximum ESR to meet the output ripple voltage requirement is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\Delta I_L}$$

where,

$$\Delta I_L = \left(\frac{V_{IN} - V_{OUT}}{L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{f_{SW}}$$

where f_{SW} is the switching frequency and L is the Inductor.

The actual capacitance value required relates to the physical case size needed to achieve the ESR requirement, as well as to the capacitor chemistry. Thus, polymer capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value.

With ceramic capacitors, the ripple voltage due to capacitance dominates the output ripple voltage. Therefore the minimum capacitance needed with ceramic output capacitors is,

$$C_{OUT} = \left(\frac{\Delta I_L}{8 \times f_{SW}}\right) \times \frac{1}{V_{RIPPLE}}$$

Alternatively, combining ceramics (for the low ESR) and polymers (for the bulk capacitance) helps balance the output capacitance vs. output ripple voltage requirements.

Load Transient Response

The load transient response depends on the overall output impedance over frequency, and the overall amplitude and slew rate of the load step. In applications with large, fast load transients (load step > 80% of full load and slew rate > 10A/µs), the output capacitor's high-frequency response–ESL and ESR–needs to be considered. To prevent the output voltage from spiking too low under a load-transient event, the ESR is limited by the following equation (ignoring the sag due to finite capacitance):

$$R_{ESR} \le \left(\frac{V_{RIPPLESTEP}}{\Delta IOUTSTEP}\right)$$

Table 5. Simplified Equation for Minimum Output Capacitor Requirement

PROGRAMMED V_{OUT} (V)	FREQUENCY			
	500kHz	1MHz	1.5MHz	2MHz
0.904 to 2.839	$107/V_{OUT}$		$82/(f_{SW} \times V_{OUT})$	
2.859 to 5.048	$18/f_{SW}$			

where $V_{RIPPLESTEP}$ is the allowed voltage drop during load current transient, $I_{OUTSTEP}$ is the maximum load current step.

The capacitance value dominates the mid frequency output impedance and continues to dominate the load transient response as long as the load transient's slew rate is fewer than two switching cycles. Under these conditions, the sag and soar voltages depend on the output capacitance, inductance value, and delays in the transient response. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step, especially with low differential voltages across the inductor. The sag voltage (V_{SAG}) that occurs after applying the load current can be estimated as:

$$C_{OUT_SAG} = \frac{1}{V_{SAG}} \times \left[\begin{array}{l} \frac{1}{2}\left(\frac{L \times \Delta IOUT_{STEP}^2}{(V_{IN} \times D_{MAX}) - V_{OUT}} \right) \\ +\left(\Delta IOUT_{STEP} \times (T_{SW} - \Delta T)\right) \end{array} \right]$$

Where

D_{MAX} is the maximum duty factor (93%),

T_{SW} is the switching period ($1/f_{SW}$)

ΔT equals V_{OUT}/V_{IN} x T_{SW}

The amount of overshoot voltage (V_{SOAR}) that occurs after load removal (due to stored inductor energy) can be calculated as:

$$C_{OUT_SOAR} = \frac{(\Delta IOUT_{STEP})^2 L}{2V_{OUT}\, V_{SOAR}}$$

When the MAX17509 is operating under low duty cycle the output capacitor size is usually determined by the $C_{OUTSOAR}$.

Power dissipation

Ensure that the junction temperature of the device does not exceed +125ºC under the operating conditions specified for the power supply.

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \text{ x } (\frac{1}{\eta} - 1) - (I_{OUT}^2 \text{ x } R_{DCR})$$

$$P_{OUT} = V_{OUT} \text{ x } I_{OUT}$$

where P_{OUT} is the total output power, η is the efficiency of the converter, and R_{DCR} is the DC resistances of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions.)

For a multilayer board, the thermal-performance metrics for the package are given below:

$$\theta_{JA} = 29°C/W$$

$$\theta_{JC} = 1.7°C/W$$

The junction temperature rise of the devices can be estimated at any given ambient temperature (T_A) from the following equation:

$$T_{J_MAX} = T_A + (\theta_{JA} \text{ x } P_{LOSS})$$

If the application has a thermal-management system that ensures that the devices' exposed pad is maintained at a given temperature (T_{EP_MAX}) by using proper heatsinks, then the junction temperature rise can be estimated at any given maximum ambient temperature from the following equation:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \text{ x } P_{LOSS})$$

where,

P_{LOSS} is the maximum allowed power losses with maximum allowed junction temperature

T_{J_MAX} is the maximum allowed Junction temperature

T_A is operating ambient temperature

θ_{JA} is the junction-to-ambient thermal resistance

θ_{JC} is the junction-to-case thermal resistance

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. Use the following guidelines for good PCB layout shown in Figure 2. The layout of Regulator 2 can be achieved by applying the recommended layout of Regulator 1 symmetrically.

- Keep the bypass capacitors as close as possible to the pins and the return path (1) VIN_ and PGND_ pins, (2) VCC and PGND_ pins, (3) OUT side of the inductor and PGND_ pins, (4) BST_ and LX_ pins, and (5) AVCC and SGND pin.
- Route high-speed switching nodes (BST_ and LX_) away from sensitive analog areas (OUT_, AVCC).
- Connect resistors between device configuration pins and SGND, and keep the trace length to below 3cm to minimize the trace capacitance
- Connect EP to SGND plane, and connect to PGND_ at a single point typically at the output capacitor ground.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full load efficiency. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Use multiple vias to connect internal PGND_ planes (not shown) to the top layer PGND_ plane. Connect PGND1 and PGND2 together to become PGND using large copper plane.

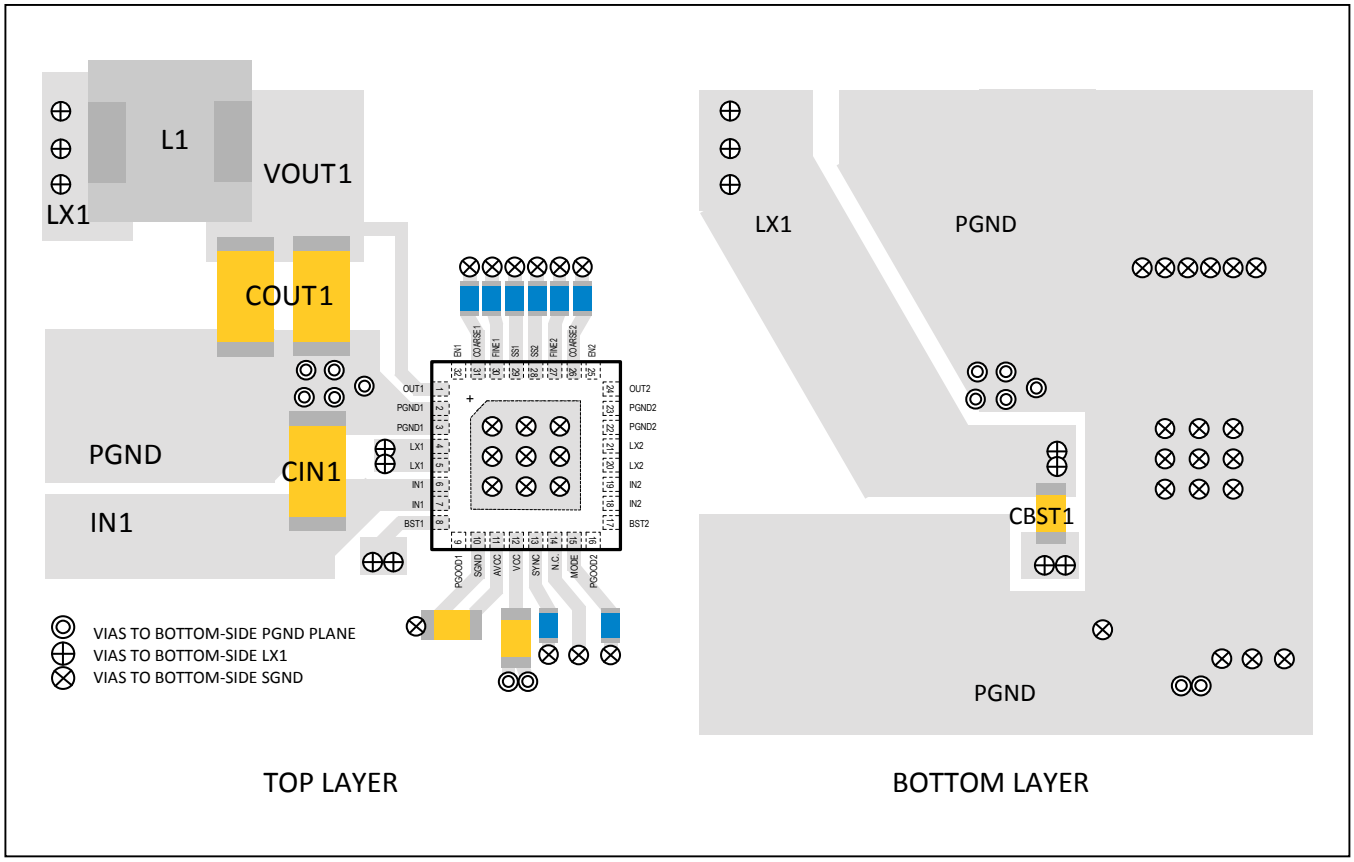


Figure 2. Recommended Layout

Typical Application Circuits

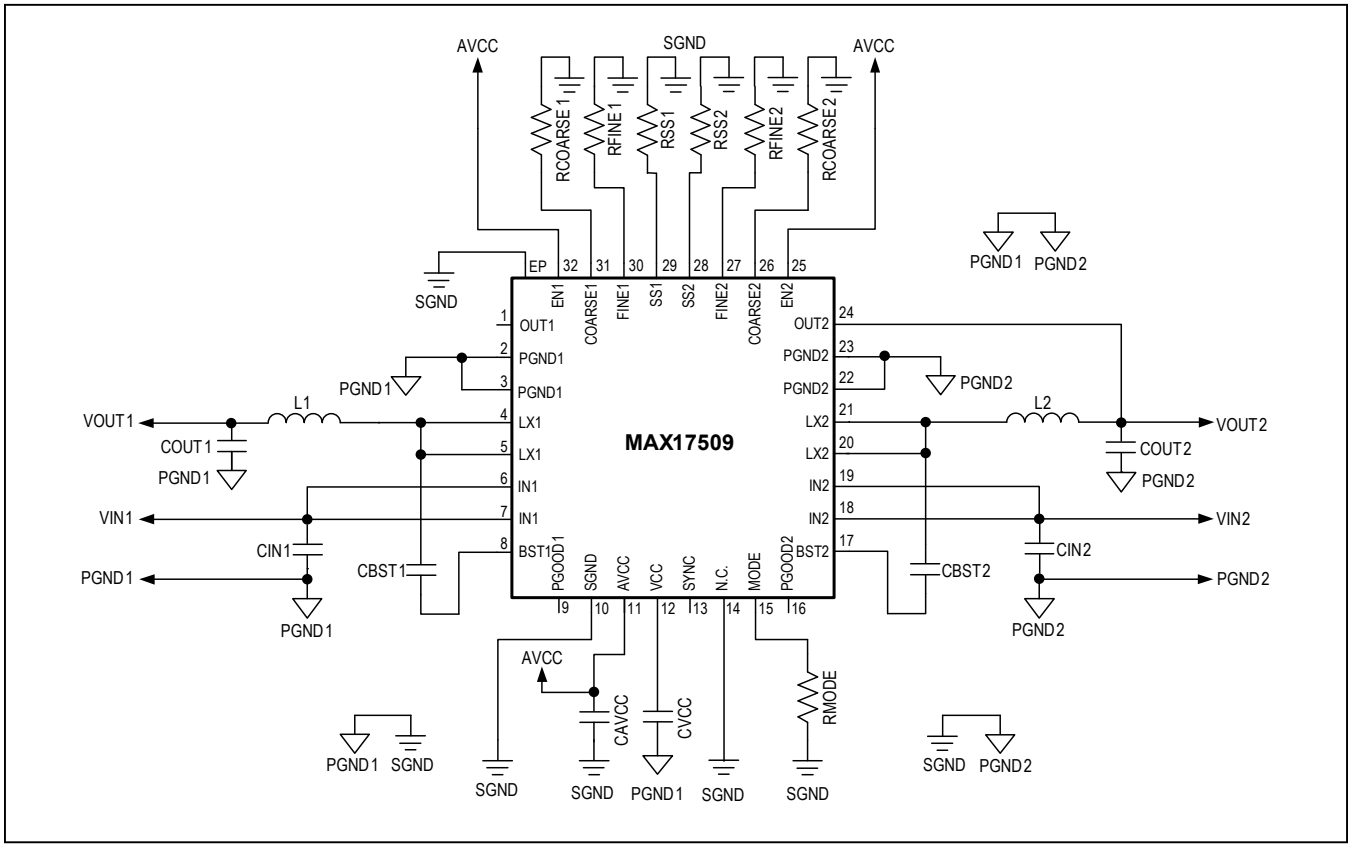


Figure 3. Two Independent Outputs

Typical Application Circuits (continued)

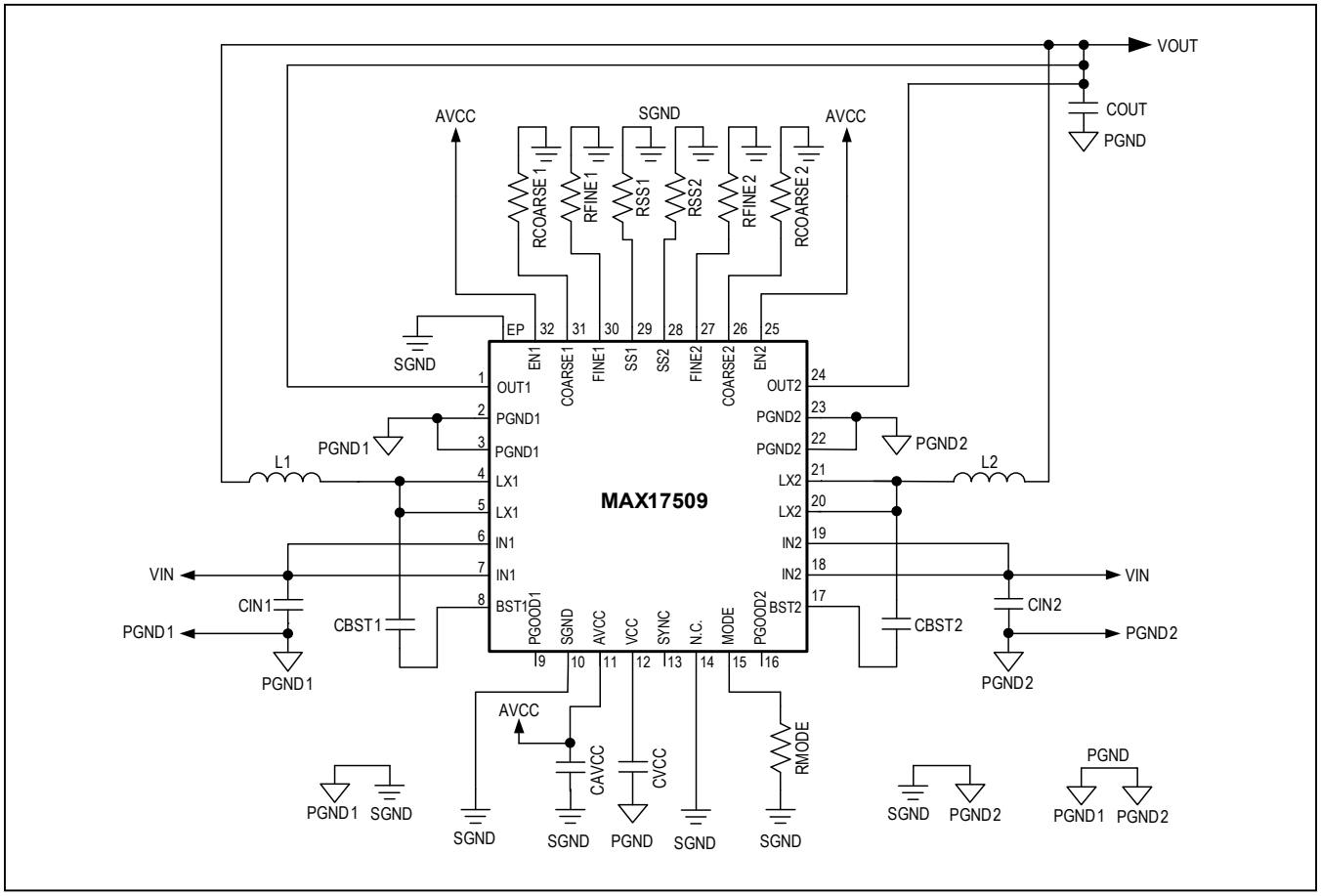


Figure 4: Dual-Phase Single Output

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17509ATJ+	-40ºC to +125ºC	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed paddle.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/15	Initial release	—

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