19-2142; Rev 1; 9/02

MAXIM

3A, 1MHz, DDR Memory Termination Supply

General Description

The MAX1809 is a reversible energy flow, constant-off-time, pulse-width modulated (PWM), step-down DC-DC converter. It is ideal for use in notebook and subnotebook computers that require 1.1V to 5V active termination power supplies. This device features an internal PMOS power switch and internal synchronous rectifier for high efficiency and reduced component count. The internal 90mΩ PMOS power switch and 70mΩ NMOS synchronous-rectifier switch easily deliver continuous load currents up to 3A. The MAX1809 accurately tracks an external reference voltage, produces an adjustable output from 1.1V to V_{IN}, and achieves efficiencies as high as 93%.

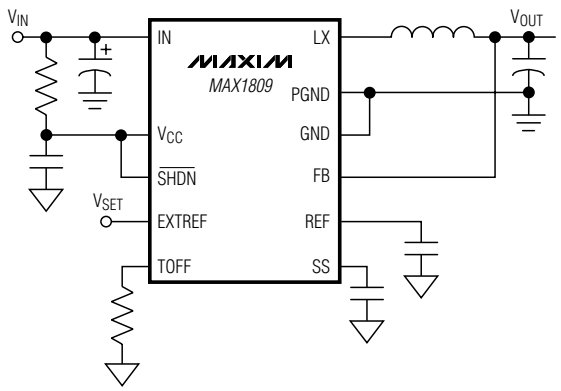
The MAX1809 uses a unique current-mode, constant-off-time, PWM control scheme that allows the output to source or sink current. This feature allows energy to return to the input power supply that otherwise would be wasted. The programmable constant-off-time architecture sets switching frequencies up to 1MHz, allowing the user to optimize performance trade-offs between efficiency, output switching noise, component size, and cost. The MAX1809 features an adjustable soft-start to limit surge currents during startup, a 100% duty-cycle mode for low-dropout operation, and a low-power shutdown mode that disables the power switches and reduces supply current below 1µA. The MAX1809 is available in a 28-pin QFN with an exposed backside pad, a 28-pin thin QFN, or a 16-pin QSOP.

Applications

DDR Memory Termination

Active Termination Buses

Typical Operating Circuit



Features

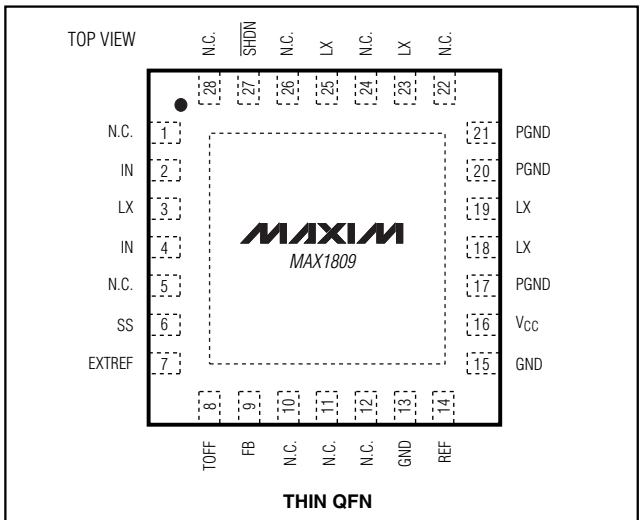
- ♦ **Source/Sink 3A**
- ♦ **±1% Output Accuracy**
- ♦ **Up to 1MHz Switching Frequency**
- ♦ **93% Efficiency**
- ♦ **Internal PMOS/NMOS Switches**
  90mΩ/70mΩ On-Resistance at V_{IN} = 4.5V
  110mΩ/80mΩ On-Resistance at V_{IN} = 3V
- ♦ **1.1V to V_{IN} Adjustable Output Voltage**
- ♦ **3V to 5.5V Input Voltage Range**
- ♦ **<1µA Shutdown Supply Current**
- ♦ **Programmable Constant-Off-Time Operation**
- ♦ **Thermal Shutdown**
- ♦ **Adjustable Soft-Start Inrush Current Limiting**
- ♦ **Output Short-Circuit Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1809EGI*	-40°C to +85°C	28 QFN
MAX1809EEE	-40°C to +85°C	16 QSOP
MAX1809ETI	-40°C to +85°C	28 Thin QFN

**Contact factory for availability.*

Pin Configurations



THIN QFN

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3A, 1MHz, DDR Memory Termination Supply

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN to GND .....-0.3V to +6V
IN to V_{CC}.....±0.3V
GND to PGND.....±0.3V
$\overline{SHDN}$, SS, FB, T_{OFF}, R_{REF}, EXTREF to GND.....-0.3V to (V_{CC} + 0.3V)
LX Current (Note 1).....±4.7A
REF Short Circuit to GND Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin QFN (derate 20mW/°C above +70°C; part mounted on 1in² of 1oz copper).....1.6W
16-Pin QSOP (derate 12.5mW/°C above +70°C; part mounted on 1in² of 1oz copper).....1W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has clamp diodes to PGND and IN. If continuous current is applied through these diodes, thermal limits must be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = 3.3V, V_{EXTREF} = 1.1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN},V_{CC}			3.0		5.5	V
Feedback Voltage Accuracy (V_{FB} - V_{EXTREF})		V_{IN} = V_{CC} = 3V to 5.5V, I_{LOAD} = 0, V_{EXTREF} = 1.25V (Note 2)		-12		+12	mV
Feedback Load Regulation Error	ΔV_{FB}	I_{LOAD} = -3A to +3A, V_{EXTREF} = 1.25V			20		mV
External Reference Voltage Range	V_{EXTREF}	V_{IN} = V_{CC} = 3V to 5.5V		V_{REF} - 0.01		V_{IN} - 1.7	V
Reference Voltage	V_{REF}			1.078	1.100	1.122	V
Reference Load Regulation		I_{REF} = -1µA to +10µA			0.5	2.0	mV
PMOS Switch On-Resistance	R_{PMOS}	I_{LX} = 0.5A	V_{IN} = 4.5V		90	200	mΩ
			V_{IN} = 3V		110	250	
NMOS Switch On-Resistance	R_{NMOS}	I_{LX} = 0.5A	V_{IN} = 4.5V		70	150	mΩ
			V_{IN} = 3V		80	200	
Current-Limit Threshold	I_{LIMIT}	V_{IN} > V_{LX}		3.5	4.1	4.7	A
Switching Frequency	f_{SW}	(Note 3)				1	MHz
No Load Supply Current	I_{CC}	f_{SW} = 500kHz			1		mA
	I_{IN}	f_{SW} = 500kHz			16		
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND, I_{CC} + I_{IN}			<1	15	µA
Thermal-Shutdown Threshold		Hysteresis = 15°C			160		°C
Undervoltage Lockout Threshold		V_{CC} falling, hysteresis = 90mV		2.5	2.6	2.7	V
FB Input Bias Current	I_{FB}	V_{FB} = V_{EXTREF} + 0.1V		0	60	250	nA
Off-Time	t_{OFF}	R_{TOFF} = 30.1kΩ		0.24	0.30	0.37	µs
		R_{TOFF} = 110kΩ		0.9	1.0	1.1	
		R_{TOFF} = 499kΩ		3.8	4.5	5.2	
Startup Off-Time					4 x t_{OFF}		µs
On-Time	t_{ON}	(Note 3)		0.35			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = 3.3V, V_{EXTREF} = 1.1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SS Source Current	I_{SS}		4	5	6	µA
SS Sink Current	I_{SS}	V_{SS} = 1V	1	50		mA
$\overline{SHDN}$ Input Current		$V_{\overline{SHDN}}$ = 0, V_{CC}	-1		+1	µA
$\overline{SHDN}$ Logic Levels	V_{IL}				0.8	V
	V_{IH}		2			
Maximum Output RMS Current	$I_{OUT(RMS)}$				3.1	A_{RMS}

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = 3.3V, V_{EXTREF} = 1.1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Feedback Voltage Accuracy (V_{FB} - V_{EXTREF})		V_{IN} = V_{CC} = 3V to 5.5V, I_{LOAD} = 0, V_{EXTREF} = 1.25V		-24		+24	mV
External Reference Voltage Range	V_{EXTREF}	V_{IN} = V_{CC} = 3 V to 5.5V		V_{REF} - 0.01V		V_{IN} - 1.9V	V
Reference Voltage	V_{REF}			1.067		1.133	V
PMOS Switch On-Resistance	R_{PMOS}	I_{LX} = 0.5A	V_{IN} = 4.5V			200	mΩ
			V_{IN} = 3V			250	
NMOS Switch On-Resistance	R_{NMOS}	I_{LX} = 0.5A	V_{IN} = 4.5V			150	mΩ
			V_{IN} = 3V			200	
Current-Limit Threshold	I_{LIMIT}	V_{IN} > V_{LX}		3.3		4.9	A
FB Input Bias Current	I_{FB}	V_{FB} = V_{EXTREF} + 0.1V				300	nA
Off-Time	t_{OFF}	R_{TOFF} = 110kΩ		0.85		1.15	µs

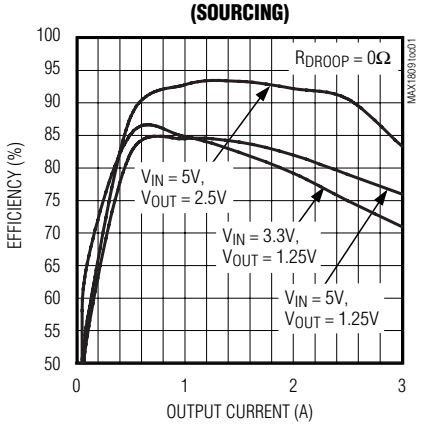
Note 2: The output voltage will have a DC-regulation level lower than the feedback error comparator threshold by 50% of the ripple.
Note 3: Recommended operating frequency, not production tested.
Note 4: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

3A, 1MHz, DDR Memory Termination Supply

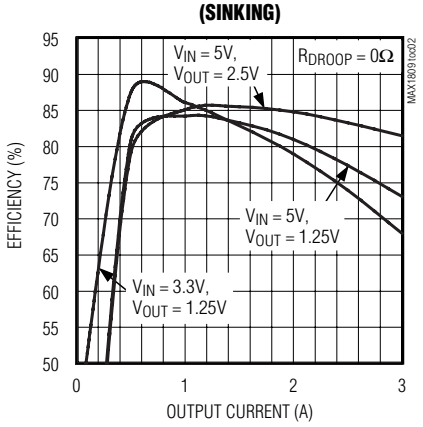
Typical Operating Characteristics

(Circuit of Figure 1, V_{OUT} = 1.25V, for V_{IN} = 5V: L = 1µH, R_{TOFF} = 130kΩ; for V_{IN} = 3.3V: L = 0.68µH, R_{TOFF} = 73.2kΩ.)

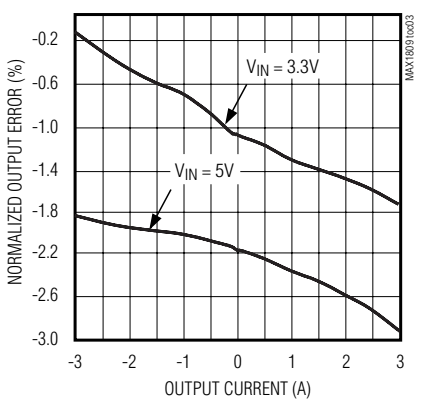
EFFICIENCY vs. OUTPUT CURRENT (SOURCING)



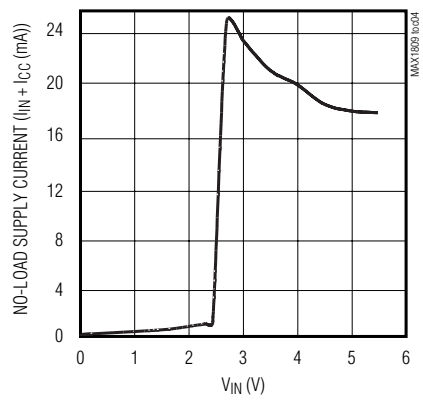
EFFICIENCY vs. OUTPUT CURRENT (SINKING)



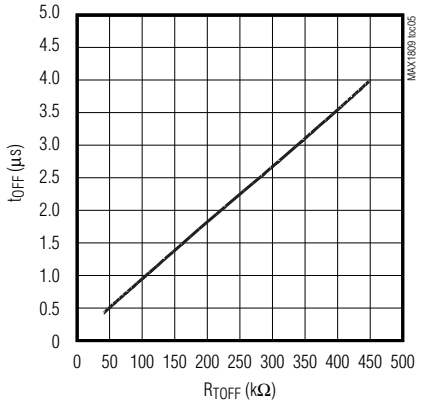
NORMALIZED OUTPUT ERROR vs. OUTPUT CURRENT



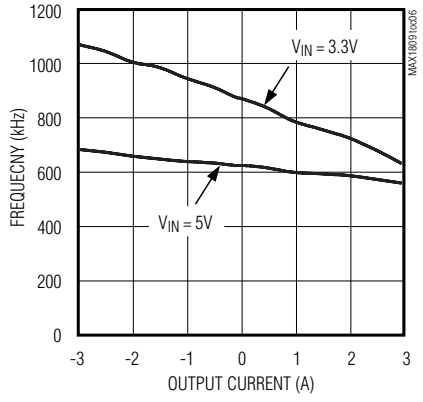
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



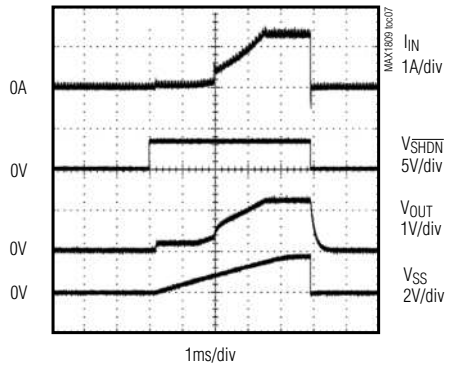
OFF-TIME vs. R_{TOFF}



SWITCHING FREQUENCY vs. OUTPUT CURRENT

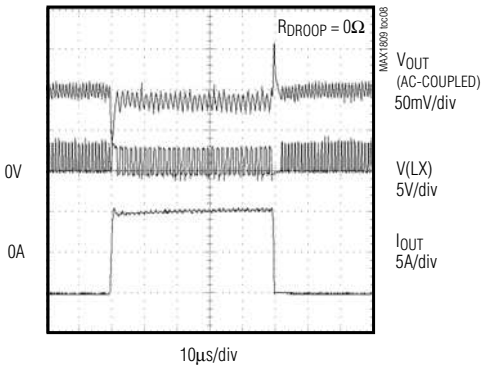


STARTUP AND SHUTDOWN



VIN = 3.3V, ROUT = 0.5Ω

LOAD-TRANSIENT RESPONSE

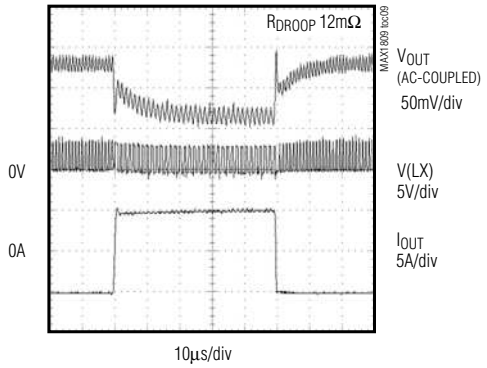


VEXTREF = 1.25V, VIN = 3.3V, IOUT = -2A to +2A to -2A

Typical Operating Characteristics (continued)

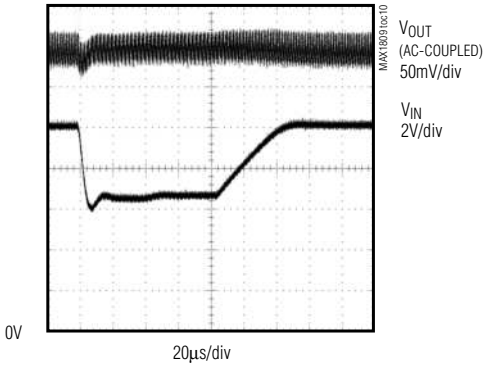
(Circuit of Figure 1, V_{OUT} = 1.25V, for V_{IN} = 5V: L = 1µH, R_{TOFF} = 130kΩ; for V_{IN} = 3.3V: L = 0.68µH, R_{TOFF} = 73.2kΩ.)

LOAD-TRANSIENT RESPONSE



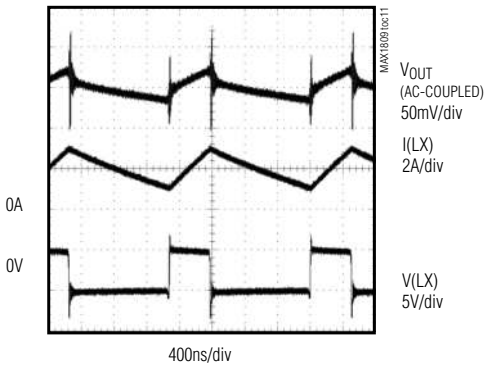
V_{EXTREF} = 1.25V, V_{IN} = 3.3V, I_{OUT} = -2A to +2A to -2A

LINE-TRANSIENT RESPONSE



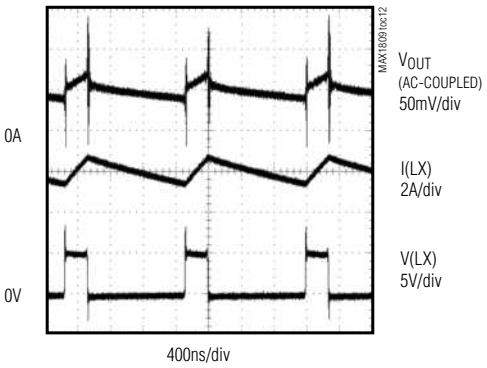
I_{OUT} = 2A, V_{IN} = 5V to 3.3V to 5V

SWITCHING WAVEFORMS (SOURCING)



I_{OUT} = 2A, V_{IN} = 5V

SWITCHING WAVEFORMS (SINKING)



I_{OUT} = -2A, V_{IN} = 5V

Pin Description

PIN (QFN)	PIN (QSOP)	NAME	FUNCTION
1, 5, 10, 11, 12, 22, 24, 26, 28	—	N.C.	No Connection. Not internally connected.
2, 4	2, 4	IN	Supply Voltage Input for the Internal PMOS Power Switch. Not internally connected. Externally connect all pins for proper operation.
3, 18, 19, 23, 25	3, 14, 16	LX	Inductor Connection. Connection for the drains of the PMOS power switch and NMOS synchronous-rectifier switch. Connect the inductor from this node to the output filter capacitor and load. Not internally connected. Externally connect all pins for proper operation.
6	5	SS	Soft-Start. Connect a capacitor from SS to GND to limit inrush current during startup.
7	6	EXTREF	External Reference Input. Feedback input regulates to V_{EXTREF}. The PWM controller remains off until EXTREF is greater than REF.
8	7	TOFF	Off-Time Select Input. Sets the PMOS power switch constant-off-time. Connect a resistor from TOFF to GND to adjust the PMOS switch off-time.
9	8	FB	Feedback Input. Connect directly to output for fixed-voltage operation or to a resistive-divider for adjustable operating modes.
13, backside pad, corner tabs	9	GND	Analog Ground. Connect exposed backside pad and corner tabs to analog GND.
14	10	REF	Reference Output. Bypass REF to GND with a 1µF capacitor.
15	11	GND	Tie to GND (pin 13 QFN; pin 9 QSOP)
16	12	V_{CC}	Analog Supply Voltage Input. Supplies internal analog circuitry. Bypass V_{CC} with a 10Ω and 2.2µF low-pass filter (see Figure 1).
17, 20, 21	13, 15	PGND	Power Ground. Internally connected to the internal NMOS synchronous-rectifier switch.
27	1	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to disable the reference, control circuitry, and internal MOSFETs. Drive high or connect to V_{CC} for normal operation.

Detailed Description

The MAX1809 synchronous, current-mode, constant-off-time, PWM DC-DC converter steps down input voltages of 3V to 5.5V to an adjustable output voltage from 1.1V to V_{IN}, as set by the voltage applied at EXTREF. It sources and sinks up to 3A of output current. Internal switches composed of a 90mΩ PMOS power switch and a 70mΩ NMOS synchronous-rectifier switch improve efficiency, reduce component count, and eliminate the need for an external Schottky diode across the synchronous switch.

The MAX1809 operates in a constant-off-time mode under all loads. A single resistor-programmable constant-off-time control sets switching frequencies up to 1MHz, allowing the user to optimize performance tradeoffs in efficiency, switching noise, component size, and cost.

When power is drawn from a regulated supply, constant-off-time PWM architecture essentially provides constant-frequency operation. This architecture has the inherent advantage of quick response to line and load transients. The MAX1809's current-mode, constant-off-time PWM architecture regulates the output voltage by changing the PMOS switch on-time relative to the constant off-time.

Constant-Off-Time Operation

In the constant-off-time architecture, the FB voltage comparator turns the PMOS switch on at the end of each off-time, keeping the device in continuous-conduction mode. The PMOS switch remains on until the

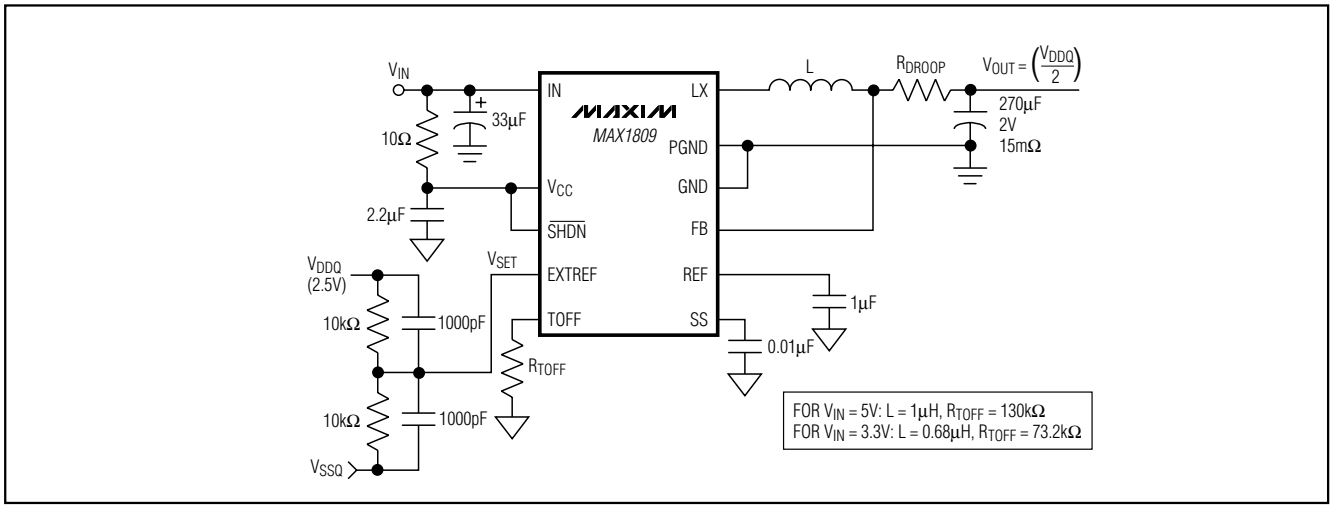


Figure 1. Typical Application Circuit

feedback voltage exceeds the external reference voltage (V_{EXTREF}) or the positive current limit is reached. When the PMOS switch turns off, it remains off for the programmed off-time (t_{OFF}). To control the current under short-circuit conditions, the PMOS switch remains off for approximately $4 \times t_{OFF}$ when $V_{FB} < V_{EXTREF} / 4$.

Synchronous Rectification

In a stepdown regulator without synchronous rectification, an external Schottky diode provides a path for current to flow when the inductor is discharging. Replacing the Schottky diode with a low-resistance NMOS synchronous switch reduces conduction losses and improves efficiency.

The NMOS synchronous-rectifier switch turns on following a short delay (approximately 50ns) after the PMOS power switch turns off, thus preventing cross-conduction or "shoot-through." In constant-off-time mode, the synchronous-rectifier switch turns off just prior to the PMOS power switch turning on. While both switches are off, inductor current flows through the internal body diode of the NMOS switch.

Current Sourcing and Sinking

By operating in a constant-off-time, pseudo-fixed-frequency mode, the MAX1809 can both source and sink current. Depending on the output current requirement, the circuit operates in two modes. In the first mode the output draws current and the MAX1809 behaves as a regular buck controller, sourcing current to the output from the input supply rail. However, when the output is supplied by another source, the MAX1809 operates in a second mode as a synchronous boost, taking power from the output and returning it to the input.

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area immediately surrounding the IC leads. The MAX1809 QFN package has $1in^2$ of copper area and a thermal resistance of 50°C/W with no forced airflow. The MAX1809 16-pin QSOP evaluation kit has $0.5in^2$ of copper area and a thermal resistance of 80°C/W with no forced airflow. Airflow over the board significantly reduces the junction-to-ambient thermal resistance. For heat sinking purposes, it is essential to connect the exposed backside pad of the QFN package to a large analog ground plane.

Shutdown

Drive $\overline{SHDN}$ to a logic-level low to place the MAX1809 in low-power shutdown mode and reduce supply current to less than 1µA. In shutdown, all circuitry and internal MOSFETs turn off, so the LX node becomes high impedance. Drive $\overline{SHDN}$ to a logic-level high or connect to V_{CC} for normal operation.

Power Dissipation

Power dissipation in the MAX1809 is dominated by conduction losses in the two internal power switches. Power dissipation due to charging and discharging the gate capacitance of the internal switches (i.e., switching losses) is approximately:

$$P_{D(CAP)} = C \times V_{IN}^2 \times f_{SW}$$

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where C = 2.5nF and f_{SW} is the switching frequency. Resistive losses in the two power switches are approximated by:

$$P_{D(RES)} = I_{OUT}^2 \times R_{PMOS}$$

where R_{PMOS} is the on-resistance of the PMOS switch. The junction-to-ambient thermal resistance required to dissipate this amount of power is calculated by:

$$\theta_{JA} = (T_{J,MAX} - T_{A,MAX}) / (P_{D(CAP)} + P_{D(RES)})$$

where:

θ_{JA} = junction-to-ambient thermal resistance

$T_{J,MAX}$ = maximum junction temperature

$T_{A,MAX}$ = maximum ambient temperature

Design Procedure

For typical applications, use the recommended component values in Figure 1. For other applications, take the following steps:

1) Select the desired PWM-mode switching frequency. See Figure 4 for maximum operating frequency.
2) Select the constant off-time as a function of input voltage, output voltage, and switching frequency.
3) Select R_{TOFF} as a function of off-time.
4) Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

Setting the Output Voltage

The output voltage of the MAX1809 is set by an external voltage applied to the EXTREF pin. This can come directly from another voltage source or external reference.

As an active termination supply in DDR applications (see Active Bus Termination in the *Applications Information* section), the output of the MAX1809 is regulated at half the DDR supply voltage. In mobile systems, the DDR supply voltage is 2.5V, and the termination voltage is 1.25V ±40mV. To regulate to 1.25V, an external divide-by-2 resistor network is placed across the DDR supply voltage to generate 1.25V. This 1.25V is connected to EXTREF, which sets the output voltage of the MAX1809. When FB is directly tied to the output (Figure 5), the output voltage range is limited by the external reference's input voltage limits (see EC table). External reference may not be set within 1.7V of the minimum supply voltage. V_{EXTREF} should be limited to less than 1.4V for 3.3V input voltage. Failure to comply can cause the part to operate abnormally and may cause part damage.

Alternatively, the output can be adjusted up to V_{IN} by connecting FB to a resistor-divider between the output voltage and ground (Figure 6). Use 50kΩ for R1. R2 is given by:

$$R2 = R1\left(\frac{V_{OUT}}{V_{EXTREF}} - 1\right)$$

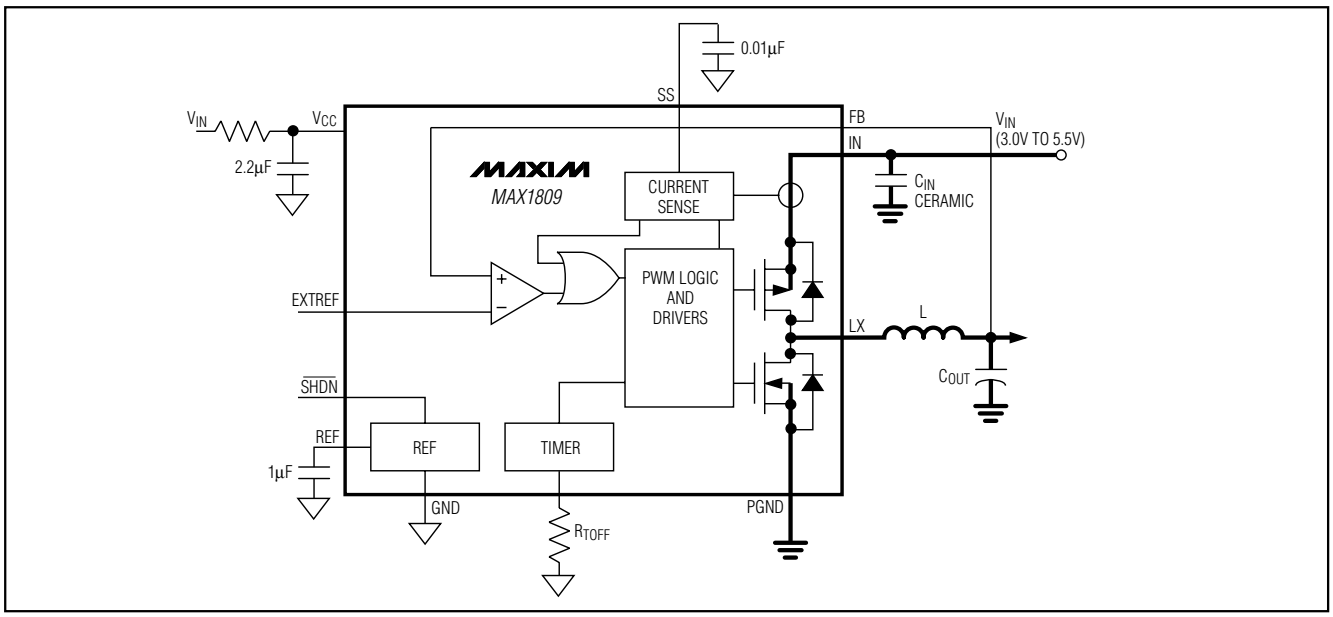


Figure 2. Functional Diagram

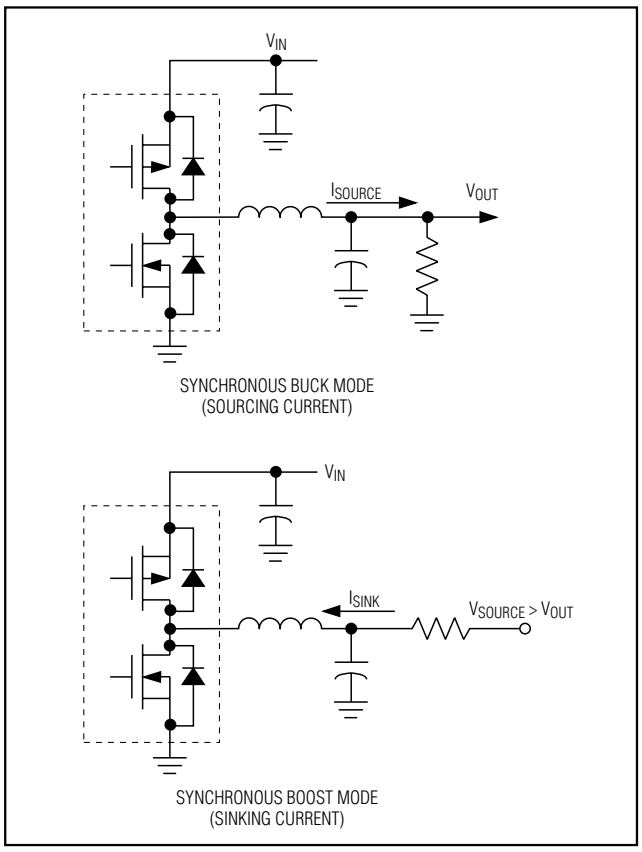


Figure 3. Sourcing and Sinking Capabilities of the MAX1809

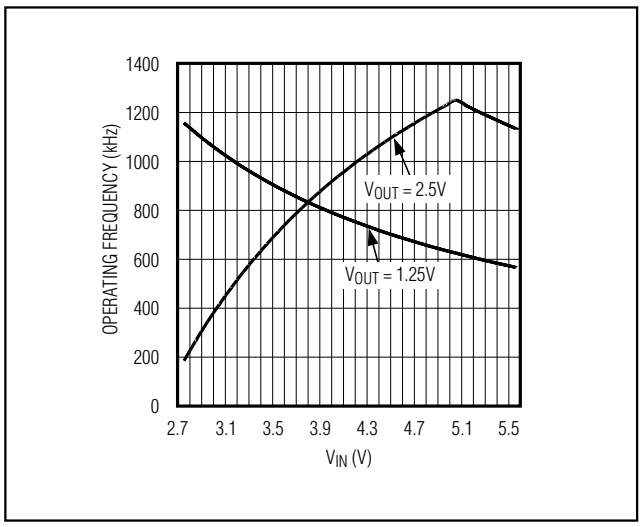


Figure 4. Maximum Recommended Operating Frequency vs. Input Voltage

Programming the Switching Frequency and Off-Time and On-Time

The MAX1809 features a programmable PWM-mode switching frequency, which is set by the input and output voltage and the value of R_{TOFF}, connected from TOFF to GND. R_{TOFF} sets the PMOS power switch off-time in PWM mode. Use the following equation to select the off-time while sourcing current according to the desired switching frequency in PWM mode:

$$t_{OFF} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{f_{SW}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

where:

t_{OFF} = the programmed off-time

V_{IN} = the input voltage

V_{OUT} = the output voltage

V_{PMOS} = the voltage drop across the internal PMOS power switch $|I_{OUT} \times R_{PMOS}|$

V_{NMOS} = the voltage drop across the internal NMOS synchronous-rectifier switch $|I_{OUT} \times R_{NMOS}|$

f_{SW} = switching frequency

Make sure that t_{ON} and t_{OFF} are greater than 400ns when sourcing current. Select R_{TOFF} according to the formula:

$$R_{TOFF} = (t_{OFF} - 0.07\mu s) \times (117k\Omega / 1.00\mu s)$$

Recommended values for R_{TOFF} range from 36kΩ to 430kΩ for off-times of 0.4µs to 4µs.

When sinking current, the switching frequency increases due to the on-resistances of the internal switches adding to the voltage across the inductor, reducing the on-time. Calculate t_{ON} when sinking current using the equation:

$$t_{ON} = t_{OFF}\left[\frac{V_{OUT} - V_{NMOS}}{V_{IN} - V_{OUT} + V_{PMOS}}\right]$$

Check that t_{ON} in the current sinking mode is greater than 350ns.

Inductor Selection

The key inductor parameters must be specified: inductor value (L) and peak current (I_{PEAK}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC current (ripple current)

to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple current to load current ratio (LIR = 0.25).

$$L = \frac{(V_{OUT} \times t_{OFF})}{(I_{SOURCE} - I_{SINK}) \times LIR}$$

The peak inductor current at full load is calculated by:

$$I_{PEAK} = I_{OUT} + \frac{(V_{OUT} \times t_{OFF})}{2 \times L}$$

where I_{OUT} is the maximum source or sink current.

Choose an inductor with a saturation current at least as high as the peak inductor current. Additionally, verify the peak inductor current while sourcing output current ($I_{OUT} = I_{SOURCE}$) does not exceed the positive current limit. The inductor selected should exhibit low losses at the chosen operating frequency.

Input Capacitor Selection

The input filter capacitor reduces peak currents and noise at the voltage source. Use a low-ESR and low-ESL capacitor located no further than 5mm from IN. Select the input capacitor according to the RMS input ripple-current requirements and voltage rating:

$$I_{RIPPLE} = I_{OUT} \left(\frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \right)$$

where I_{RIPPLE} = input RMS current ripple.

Output Capacitor Selection

The output filter capacitor affects the output voltage ripple, output load-transient response, and feedback loop stability. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to guarantee stability and absorb the inductor energy going from a full-load sourcing to full-load sinking condition without exceeding the maximum output tolerance.

For stable operation, the MAX1809 requires a minimum feedback ripple voltage of $V_{RIPPLE} \geq 1\% \times V_{EXTREF}$. The minimum ESR of the output capacitor should be:

$$R_{ESR} > 1\% \times (L / t_{OFF})$$

Stable operation requires the correct output filter capacitor. When choosing the output capacitor, ensure that:

$$C_{OUT} \geq \frac{t_{OFF}}{V_{OUT}} \times 79\mu FV/\mu s$$

In applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \Delta V_{OUT} / \Delta I_{OUT(MAX)}$$

The actual microfarad capacitance value required is defined by the physical size needed to achieve low ESR, and by the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR, size, and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics). When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem. The amount of overshoot and undershoot due to stored inductor energy can be calculated as:

$$V_{SOAR} = L \times \Delta I_{OUT}^2 / (2 \times C_{OUT} \times V_{OUT})$$

$$V_{SAG} = L \times \Delta I_{OUT}^2 / [2 \times C_{OUT} \times (V_{IN} - V_{OUT})]$$

Soft-Start

Soft-start allows a gradual increase of the internal current limit to reduce input surge currents at startup and at exit from shutdown. A timing capacitor, C_{SS}, placed from SS to GND sets the rate at which the internal current limit is changed. Upon power-up, when the device comes out of undervoltage lockout (2.6V typ) or after the $\overline{SHDN}$ pin is pulled high, a 4µA constant current source charges the soft-start capacitor and the voltage on SS increases. When the voltage on SS is less than approximately 0.7V, the current limit is set to zero. As the voltage increases from 0.7V to approximately 1.8V, the current limit is adjusted from 0V to the current-limit threshold (see the *Electrical Characteristics*). The voltage across the soft-start capacitor changes with time according to the equation:

$$V_{SS} = \frac{4\mu A \times t}{C_{SS}}$$

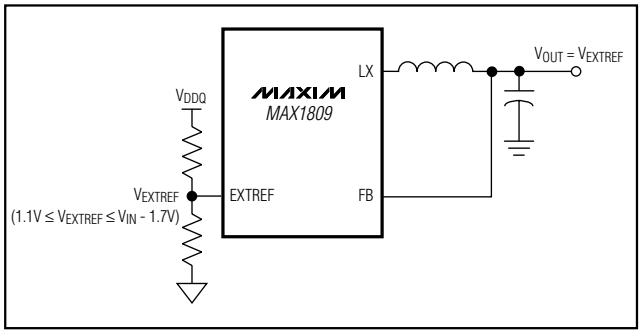


Figure 5. Adjusting the Output Voltage Using EXTREF

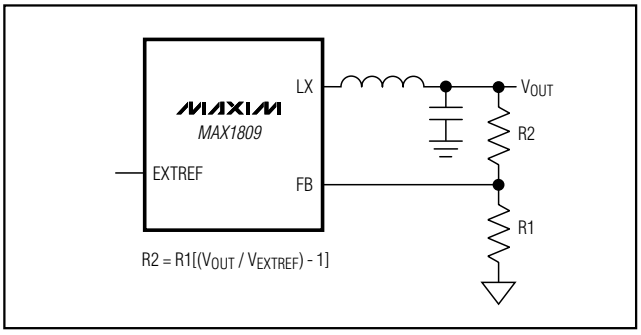


Figure 6. Adjusting the Output Voltage at FB

The output current limit during soft-start varies with the voltage on the soft-start pin, SS, according to the equation:

$$I_{LIM(SS)} = \frac{V_{SS} - 0.7V}{1.1V} \times I_{LIMIT}$$

where I_{LIMIT} is the current-limit threshold from the *Electrical Characteristics*. The constant-current source stops charging once the voltage across the soft-start capacitor reaches 1.8V.

Applications Information

Frequency Variation with Output Current

The operating frequency of the MAX1809 is determined primarily by t_{OFF} (set by R_{TOFF}), V_{IN}, and V_{OUT} as shown in the following formula:

$$f_{SW} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{t_{OFF}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

However, as the output current increases, the voltage drop across the NMOS and PMOS switches increases and the voltage across the inductor decreases. This causes the frequency to drop. Assuming $R_{PMOS} = R_{NMOS}$, the change in frequency can be approximated with the following formula:

$$\Delta f_{SW} = \frac{\Delta I_{OUT} \times R_{PMOS}}{(V_{IN} \times t_{OFF})}$$

where R_{PMOS} is the resistance of the internal MOSFETs (90mΩ typ).

Circuit Layout and Grounding

Good layout is necessary to achieve the MAX1809's intended output power level, high efficiency, and low noise. Good layout includes the use of ground planes, careful component placement, and correct routing of traces using appropriate trace widths. The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND close together. Connect the resulting PGND plane to GND at only one point.
2) Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
3) Place the LX node components as close together and as near to the device as possible. This reduces resistive and switching losses as well as noise.
4) Ground planes are essential for optimum performance. In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad of the QFN package to a large analog ground plane, preferably on a surface of the board that receives good airflow. If the ground plane is located on the top layer, make use of the N.C. pins adjacent to GND to lower thermal resistance to the ground plane. If the ground is located elsewhere, use several vias to lower thermal resistance. Typical applications use multiple ground planes to minimize thermal resistance. Avoid large AC currents through the analog ground plane.

Voltage Positioning

In applications where the load transients are extremely fast (>10A/µs), the total output capacitance has to be large enough to handle the V_{SAG} and V_{SOAR} requirements while keeping within the output tolerance limits. Voltage positioning reduces the total amount of output capacitance needed to meet a given transient response requirement. With voltage positioning, the

3A, 1MHz, DDR Memory Termination Supply

output regulates at a slightly lower voltage under a given load, allowing more voltage headroom as the load changes suddenly to zero or to the opposite polarity (sinking mode). By utilizing the full-voltage tolerance limits, the total output capacitance can be reduced and the capacitor's ESR can be increased.

Choose R_{DROOP} such that the output voltage at the maximum load current, including ripple, is just above the lower limit of the output tolerance.

$$R_{DROOP} \times I_{OUT(MAX)} \le V_{OUT(TYP)} - V_{OUT(MIN)} - (V_{RIPPLE} / 2)$$

Voltage positioning results in some loss in efficiency due to the power dissipated in R_{DROOP}. The maximum power loss is given by $R_{DROOP} \times I_{OUT(MAX)}^2$. R_{DROOP} must be able to handle this power.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. They are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively low output-voltage ripple (affecting stability in nonvoltage-positioned circuits). In addition, their relatively low capacitance value can cause output overshoot when going abruptly from full-load sourcing to full-load sinking conditions, unless the inductor value can be made small (high switching frequency), or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored energy in the inductor. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The MAX1809 can take full advantage of the small size and low ESR of ceramic output capacitors in a voltage-positioned circuit. The addition of the positioning resistor increases the ripple at FB, satisfying the minimum feedback ripple voltage requirement.

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see *the Output Capacitor Selection*). Often the switching frequency is set as high as possible (near 1000kHz), and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery.

Input Source

The output of the MAX1809 can accept current due to the reversible properties of the buck and the boost converter. When voltage at the output of the MAX1809 (low-voltage port) exceeds or equals the output set voltage the flow of energy reverses, going from the output to the input (high-voltage port). If the input (high-voltage port) is not connected to a low-impedance

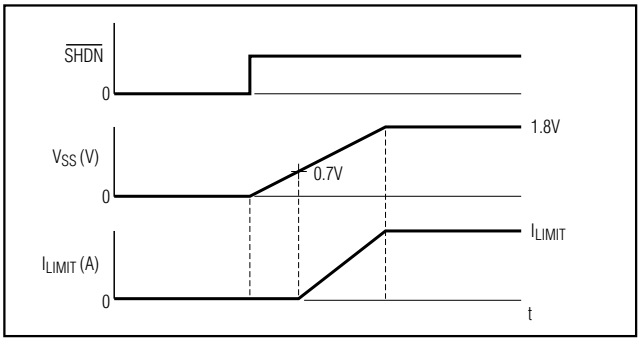


Figure 7. Soft-Start Current Limit Over Time

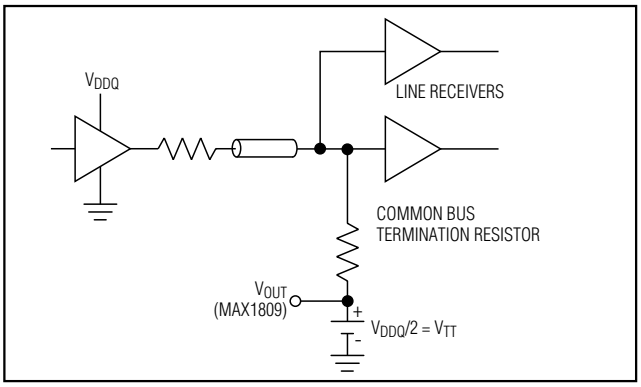


Figure 8. Active Bus Termination

source capable of absorbing energy, the voltage at the input will rise. This voltage can violate the absolute maximum voltage at the input of the MAX1809 and destroy the part. This occurs when sinking current because the topology acts as a boost converter, pumping energy from the low-voltage side (the output), to the high-voltage side (the input). The input (high-voltage side) voltage is limited only by the clamping effect of the voltage source connected there. To avoid this problem, make sure the input to the MAX1809 is connected to a low impedance, two quadrant supply or that the load (excluding the MAX1809) connected to that supply consumes more power than the amount being transferred from the MAX1809 output to the input.

Active Bus Termination

DDR memory architecture is a high-speed system that clocks data on both the rising and falling edges of the clock. This increases the data rate, and at the same time increases the system power dissipation. High-speed digital logic requires termination of the buses to minimize ringing and reflection. Using an active termination scheme reduces the power dissipation of the bus. By connecting the termination resistors to a supply voltage (V_{TT}) that is half the memory voltage (V_{DDQ}),

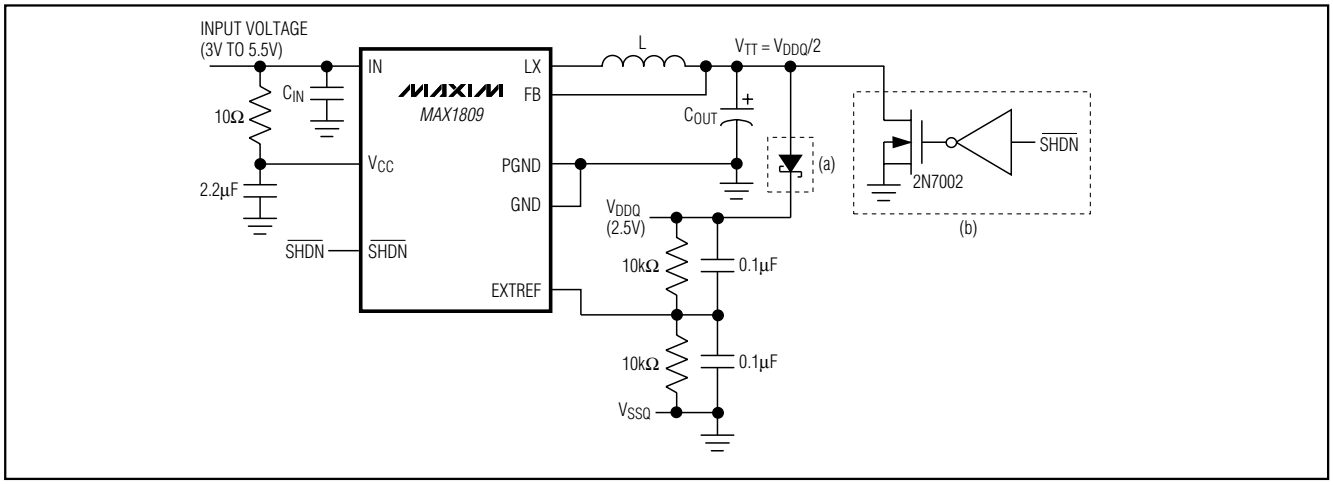


Figure 9. Discharging the Output of the MAX1809 in Shutdown

Pin Configurations (continued)

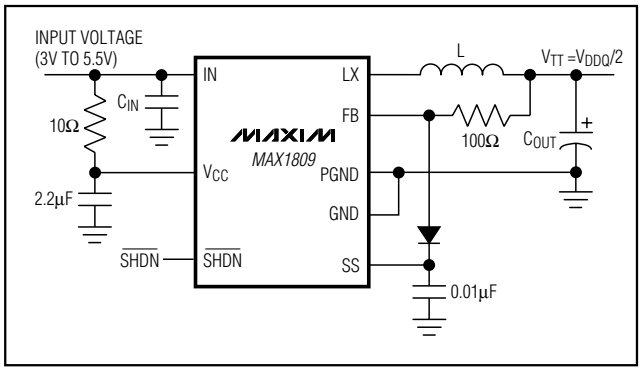
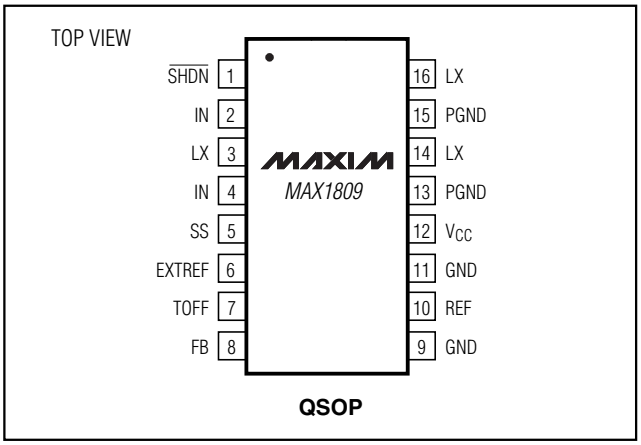


Figure 10. Starting the MAX1809 in Sinking Mode with V_{OUT} >V_{EXTREF}



the dissipation in the termination resistor is halved compared to a termination scheme that connects the resistive terminators to ground.

The V_{TT} supply requires that it regulates to half the memory voltage (V_{DDQ}), tracks the changes of the memory voltage, and is able to source and sink current depending on the state of the bus. These requirements are met in the MAX1809.

Discharging the Output in Shutdown

When $\overline{SHDN}$ is brought low after the controller has been on for a while, the output may remain high if there is no leakage or discharge path to bring the output down. For DDR memory systems, keeping V_{TT} at 1.25V when V_{DDQ} (2.5V) is shut down violates the DDR specifications. This can result in the bus latching if the system is subsequently turned on or possibly damaging the memory subsystem.

When using the MAX1809 to generate the V_{TT} output of 1.25V, several circuits are recommended to discharge the output when the MAX1809 is shut down. These are shown in Figure 9. Solution (a) is a diode added from V_{TT} to V_{DDQ} so that V_{TT} is discharged when VDDQ goes low. Alternatively, solution (b) uses a small signal transistor to discharge V_{TT} when the MAX1809 is shut down.

Startup in Sinking Mode

The MAX1809 will not startup until the feedback voltage is made less than the external reference voltage when power is applied or when the part is exiting shutdown. In applications that cannot guarantee V_{FB} < V_{EXTREF}

3A, 1MHz, DDR Memory Termination Supply

before startup, a 100Ω resistor should be added in the feedback path, and a diode from FB to SS as shown in Figure 10. SS will keep FB low during the startup sequence, ensuring that the MAX1809 enters into PWM mode and begins sinking current. See the Soft-Start Sink Current specification in the *Electrical Characteristics* for resistor selection.

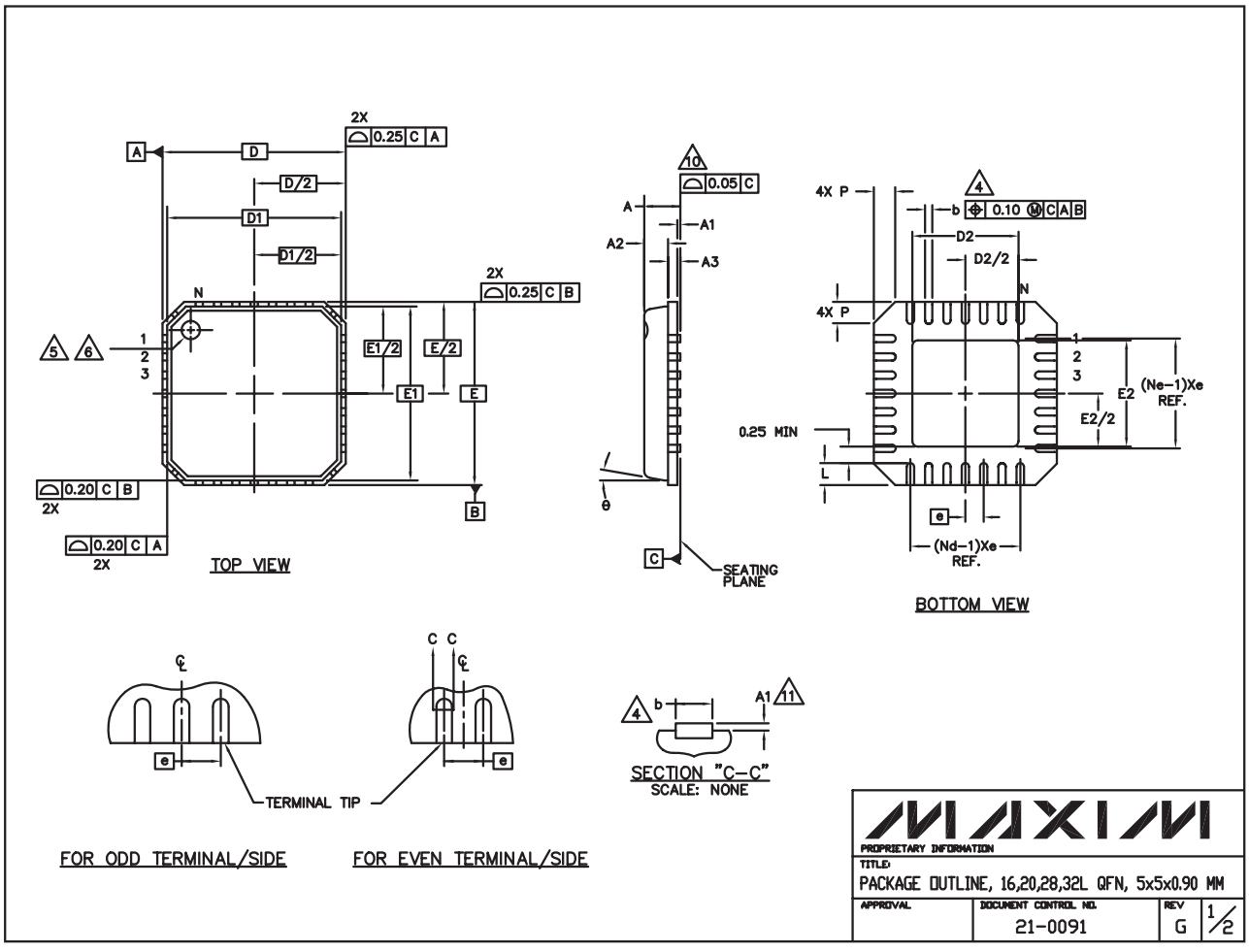
Chip Information

TRANSISTOR COUNT: 3662

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN .EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

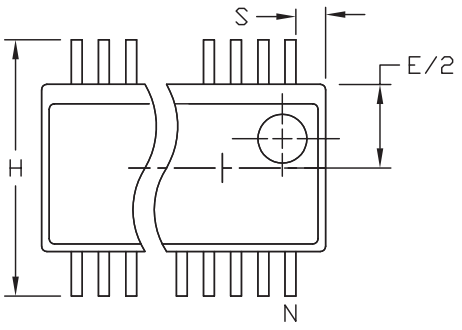
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2

3A, 1MHz, DDR Memory Termination Supply

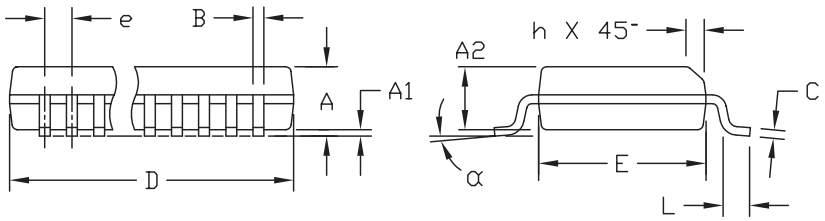
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM

PROPRIETARY INFORMATION

TITLE:

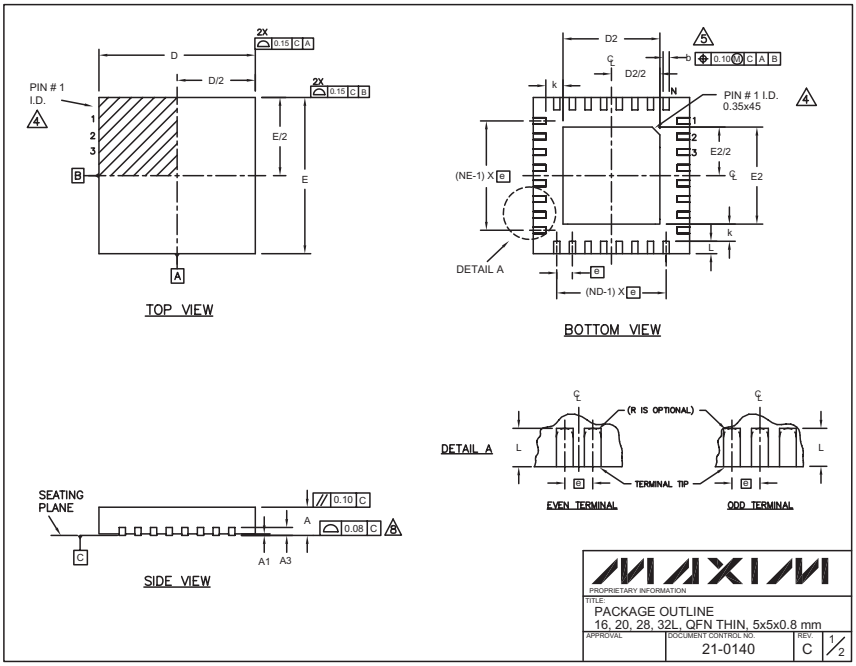
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 5x5x0.8 .EPS



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. C
2/2

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