19-4506; Rev 4; 2/97

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

MAX191

General Description

The MAX191 is a monolithic, CMOS, 12-bit analog-to-digital converter (ADC) featuring differential inputs, track/hold (T/H), internal voltage reference, internal or external clock, and parallel or serial µP interface. The MAX191 has a 7.5µs conversion time, a 2µs acquisition time, and a guaranteed 100ksps sample rate.

The MAX191 operates from a single +5V supply or from dual ±5V supplies, allowing ground-referenced bipolar input signals. The device features a logic power-down input, which reduces the 3mA V_{DD} supply current to 50µA max, including the internal-reference current.

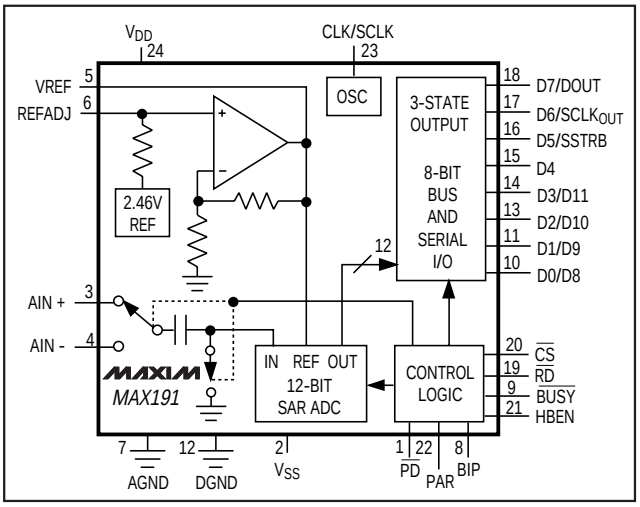
Decoupling capacitors are the only external components needed for the power supply and reference. This ADC operates with either an external reference, or an internal reference that features an adjustment input for trimming system gain errors.

The MAX191 provides three interface modes: two 8-bit parallel modes, and a serial interface mode that is compatible with SPI™, QSPI™, and MICROWIRE™ serial-interface standards.

Applications

Battery-Powered Data Logging
PC Pen Digitizers
High-Accuracy Process Control
Electromechanical Systems
Data-Acquisition Boards for PCs
Automatic Testing Systems
Telecommunications
Digital Signal Processing (DSP)

Functional Diagram



Features

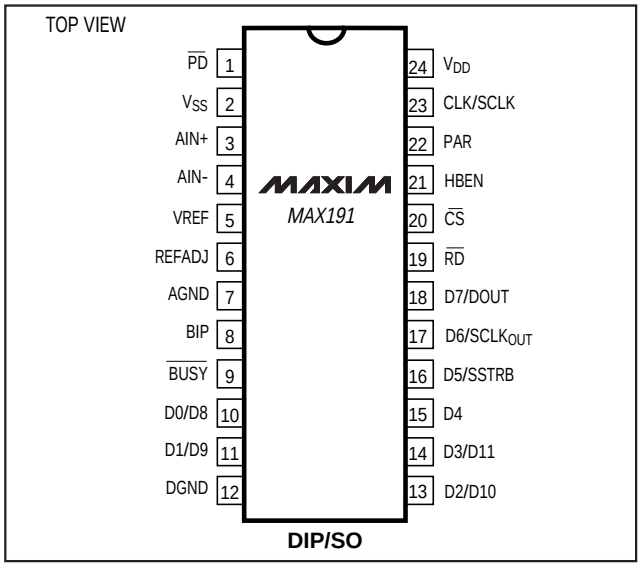
- **12-Bit Resolution, 1/2LSB Linearity**
- **+5V or ±5V Operation**
- **Built-In Track/Hold**
- **Internal Reference with Adjustment Capability**
- **Low Power: 3mA Operating Mode**
  20µA Power-Down Mode
- **100ksps Tested Sampling Rate**
- **Serial and 8-Bit Parallel µP Interface**
- **24-Pin Narrow DIP and Wide SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX191ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX191BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX191ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX191BCWG	0°C to +70°C	24 Wide SO	±1
MAX191BC/D	0°C to +70°C	Dice*	±1
MAX191AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX191BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX191AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX191BEWG	-40°C to +85°C	24 Wide SO	±1
MAX191AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1/2
MAX191BMRG	-55°C to +125°C	24 Narrow CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND.....-0.3V to +7V
V_{SS} to AGND .....-7V to +0.3V
V_{DD} to V_{SS} 12V
AGND, VREF, REFADJ to DGND.....-0.3V to (V_{DD} + 0.3V)
AIN+, AIN-, $\overline{PD}$ to V_{SS}.....-0.3V to (V_{DD} + 0.3V)
$\overline{CS}$, $\overline{RD}$, CLK, BIP, HBEN, PAR, to DGND....-0.3V to (V_{DD} + 0.3V)
$\overline{BUSY}$, D0–D7 to DGND.....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C)....1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW

Operating Temperature Ranges
MAX191_C_ _ .....0°C to +70°C
MAX191_E_ _ .....-40°C to +85°C
MAX191_M_ _ .....-55°C to +125°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode—external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)						
Resolution			12			Bits
Integral Nonlinearity	INL	MAX191A			±1/2	LSB
		MAX191B			±1	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX191A			±1	LSB
		MAX191B			±2	
Gain Error (Note 3)		MAX191A			±2	LSB
		MAX191B			±3	
Gain-Error Tempco (Note 4)		Excludes internal-reference drift		±0.2		ppm/°C
DYNAMIC ACCURACY (sample rate = 100kHz, V_{IN} = 4Vp-p)						
Signal-to-Noise plus Distortion Ratio	SINAD	1kHz input signal, T_A = +25°C	70			dB
Total Harmonic Distortion (up to the 5th Harmonic)	THD	1kHz input signal, T_A = +25°C			-80	dB
Spurious-Free Dynamic Range	SFDR	1kHz input signal, T_A = +25°C	80			dB
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Synchronous CLK (12 to 13 CLKs)	7.50		8.125	µs
		Internal CLK, C_L = 120pF	6	12	18	
Track/Hold Acquisition Time					2	µs
Aperture Delay				25		ns
Aperture Jitter				50		ps
External Clock Frequency Range (Note 6)	f_{CLK}		0.1		1.6	MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode—external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range (Note 7)			V_{SS}		V_{DD}	V
Input Leakage Current		V_{IN} = V_{SS} to V_{DD}			±10	µA
Input Capacitance (Note 6)				45	80	pF
Small-Signal Bandwidth				2		MHz
INTERNAL REFERENCE						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Output Tempco (Note 8)		MAX191_C			50	ppm/°C
		MAX191_E			60	
		MAX191_M			80	
Output Current Capability (Note 9)		T_A = +25°C			2	mA
Load Regulation		T_A = +25°C, I_{OUT} = 0mA to 2mA			4	mV
Output Short-Circuit Current				18		mA
Capacitive Load Required		Reference compensation mode—external	4.7			µF
Power-Supply Rejection		V_{DD} = ±5%, V_{SS} = ±5%		±300		µV
REFADJ Input Adjustment Range (Note 10)			-60		30	mV
REFADJ Disable Threshold			4.5			V
REFADJ Output Voltage				2.4		V
REFADJ Input Current		REFADJ = 5V			60	µA
REFERENCE INPUT						
Input Voltage Range		External-reference mode	2.5		5.0	V
Input Current		External-reference = 5V			1	mA
Input Resistance		External-reference mode	5	10		kΩ
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP	2.4			V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}			±10	µA
Input Current CLK	I_{IN}	$\overline{PD}$ = high/float			±200	µA
		$\overline{PD}$ = low		±0.1		
Input Capacitance (Note 6)	C_{IN}				10	pF
$\overline{PD}$ Input Low Voltage	V_{IL}				0.5	V
$\overline{PD}$ Input High Voltage	V_{IH}		4.5			V
$\overline{PD}$ Input Current	I_{IN}	$\overline{PD}$ = 0V to V_{DD} (Note 11)			±20	µA
$\overline{PD}$ External Leakage for Float State (Note 12)		Maximum current allowed for “floating state”			±100	nA
$\overline{PD}$ Floating-State Voltage	V_{FLT}	Reference compensation mode—external		2.8		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode—external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{OUT} = -200µA		4.0			V
Three-State Leakage Current	I_L	D0/D8-D7/DOUT				±10	µA
Three-State Output Capacitance (Note 6)	C_{OUT}					15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			4.75		5.25	V
Negative Supply Voltage	V_{SS}			-5.25		0	V
Positive Supply Current	I_{DD}	CS = $\overline{RD}$ = V_{DD}, AIN = 5V, D0/D8–D7/DOUT = 0V or V_{DD}, HBEN = PAR = BIP = 0V or V_{DD}	$\overline{PD}$ = high/float		3	5	mA
			$\overline{PD}$ = low		20	50	µA
Negative Supply Current	I_{SS}		$\overline{PD}$ = high/float		20	100	µA
			$\overline{PD}$ = low		1	20	
Positive Supply Rejection (Note 13)		FS change, V_{DD} = 5V ±5%				±1/2	LSB
Negative Supply Rejection (Note 13)		FS change, V_{SS} = -5V ±5%				±1/2	LSB

TIMING CHARACTERISTICS (Figures 6–10)

(V_{DD} =5V ±5%, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX191C/E			MAX191M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0			0			ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF			120			140			160	ns
Data Access Time (Note 15)	t_3	C_L = 100pF			120			140			160	ns
$\overline{RD}$ Pulse Width	t_4		150			150			150			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0			0			ns
Data Setup Time After $\overline{BUSY}$ (Note 15)	t_6				80			100			120	ns
Bus-Relinquish Time (Note 16)	t_7				100			110			120	ns
HBEN to $\overline{RD}$ Setup Time	t_8		80			100			120			ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0			0			ns
Delay Between Read Operations (Note 6)	t_{10}		200			200			200			ns
Delay Between Conversions	t_{11}		2			2			2			µs
Aperture Delay	t_{12}	Jitter < 50ps		25								ns
CLK to $\overline{BUSY}$ Delay (Note 6)	t_{13}				200			230			260	ns
$SCLK_{OUT}$ to SSTRB Rise Delay	t_{14}				100			130			150	ns
$SCLK_{OUT}$ to SSTRB Fall Delay	t_{15}				100			130			150	ns

TIMING CHARACTERISTICS (Figures 6–10) (continued)

(V_{DD} =5V ±5%, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 14)

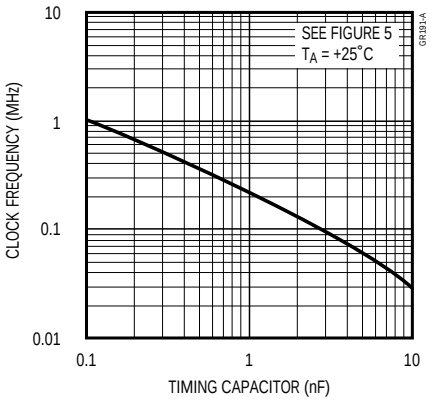
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX191C/E			MAX191M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ or $\overline{RD}$ Hold Time	t_{16}		10			10			10			ns
$\overline{CS}$ or $\overline{RD}$ Setup Time	t_{17}		150			150			150			ns
$\overline{CS}$ to DOUT Three-State	t_{19}				100			110			120	ns
SCLK to $SCLK_{OUT}$ Delay	t_{20}				160			180			200	ns
$SCLK_{OUT}$ to DOUT Delay	t_{21}				100			130			150	ns
SCLK to DOUT Delay	t_{22}				240			260			280	ns
SCLK to SSTRB Delay	t_{23}				260			310			350	ns

Note 1: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
Note 2: V_{DD} = 5V, V_{SS} = 0V, FS = VREF.
Note 3: FS = VREF, offset nulled, ideal last-code transition = FS - 3/2 LSB.
Note 4: Gain-Error Tempco = ΔGE is the gain-error change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has a 50% duty cycle.
Note 6: Guaranteed by design, not production tested.
Note 7: AIN+, AIN- must not exceed supplies for specified accuracy.
Note 8: VREF TC = ΔT, where ΔVREF is reference-voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 9: Output current should not change during conversion. This current is in addition to the current required by the internal DAC.
Note 10: REFADJ adjustment range is defined as the allowed voltage excursion on REFADJ relative to its unadjusted value of 2.4V. This will typically result in a 1.7 times larger change in the REF output (Figure 19a).
Note 11: This current is included in the $\overline{PD}$ supply current specification.
Note 12: Floating the $\overline{PD}$ pin guarantees external compensation mode.
Note 13: V_{REF} = 4.096V, external reference.
Note 14: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 15: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 16: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

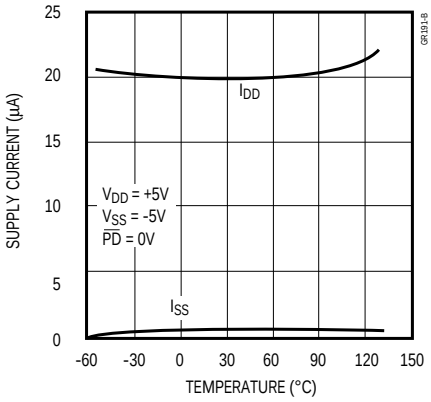
Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Typical Operating Characteristics

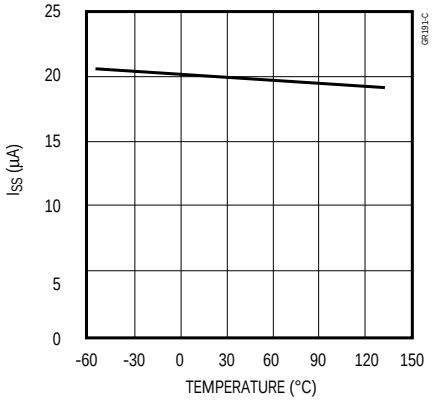
CLOCK FREQUENCY vs. TIMING CAPACITOR



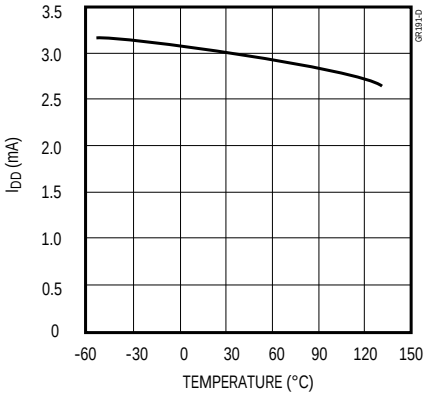
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



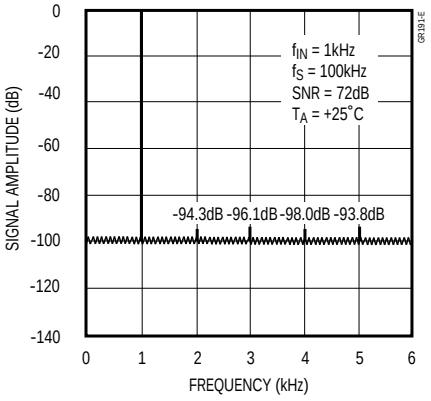
NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



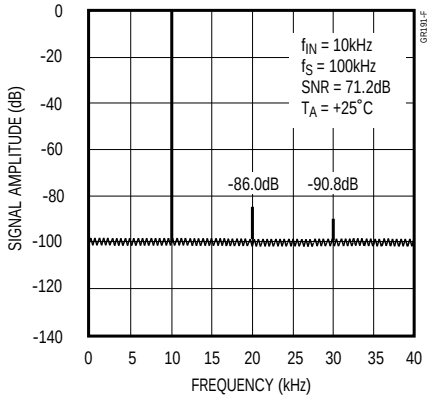
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



1kHz FFT PLOT



10kHz FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1	$\overline{PD}$	Power-Down Input. A logic low at $\overline{PD}$ deactivates the ADC—only the bandgap reference is active. A logic high selects normal operation, internal-reference compensation mode. An open-circuit condition selects normal operation, external-reference compensation mode.
2	V_{SS}	Negative Supply, 0V to -5.25V
3	AIN+	Sampled Analog Input
4	AIN-	Analog Input Return. Pseudo-differential (see *Gain and Offset Adjustment* section).
5	VREF	Reference-Buffer Output for Internal Reference. Input for external reference when REFADJ is connected to V_{DD}.
6	REFADJ	Reference Adjust. Connect to V_{DD} to use an extended reference at VREF.
7	AGND	Analog Ground
8	BIP	BIP = low selects unipolar mode BIP = high selects bipolar mode (see *Gain and Offset Adjustment* section)
9	$\overline{BUSY}$	$\overline{BUSY}$ Output is low during a conversion.
10	D0/D8	Three-State Data Outputs: LSB = D0
11	D1/D9	Three-State Data Outputs
12	DGND	Digital Ground
13	D2/D10	Three-State Data Outputs
14	D3/D11	Three-State Data Outputs: MSB = D11
15	D4	Three-State Data Output
16	D5/SSTRB	Three-State Data Output/Serial Strobe Output in serial mode
17	D6/$SCLK_{OUT}$	Three-State Data Output/Serial Clock Output in serial mode
18	D7/DOUT	Three-State Data Output/Data Output in serial mode
19	$\overline{RD}$	Read Input. In parallel mode, a low signal starts a conversion when $\overline{CS}$ and HBEN are low (memory mode). RD also enables the outputs when $\overline{CS}$ is low. In serial mode, $\overline{RD}$ = low enables $SCLK_{OUT}$ and SSTRB when CS is low. $\overline{RD}$ = high forces $SCLK_{OUT}$ and SSTRB into a high-impedance state.
20	$\overline{CS}$	Chip-Select Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs in parallel mode. The falling edge of $\overline{CS}$ starts a conversion in serial mode. $\overline{CS}$ = high in serial mode forces $SCLK_{OUT}$, SSTRB, and DOUT into a high-impedance state.
21	HBEN	High-Byte Enable Input. In parallel mode, HBEN = high multiplexes the 4 MSBs of the conversion result into the lower bit outputs. HBEN = high also disables conversion starts. HBEN = low places the 8 LSBs onto the data bus. In serial mode, HBEN = low enables $SCLK_{OUT}$ to operate during the conversion only, HBEN = high enables $SCLK_{OUT}$ to operate continuously, provided $\overline{CS}$ is low.
22	PAR	Sets the output mode. PAR = high selects parallel output mode. PAR = low selects serial output mode.
23	CLK/SCLK	Clock Input/Serial Clock Input in serial mode. An external TTL-/CMOS-compatible clock may be applied to this pin, or a capacitor (120pF nominal) may be connected between CLK and DGND to operate the internal oscillator.
24	V_{DD}	Positive Supply, +5V ±5%

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

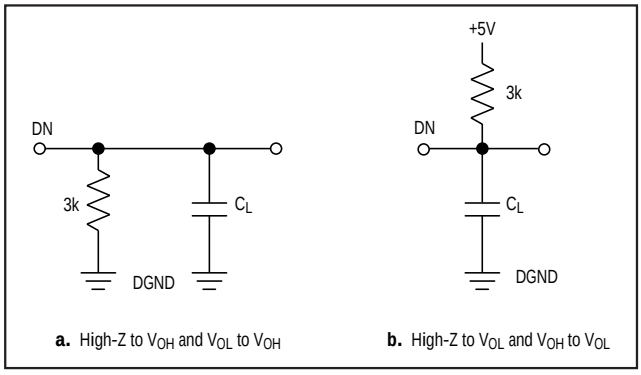


Figure 1. Load Circuits for Access Time

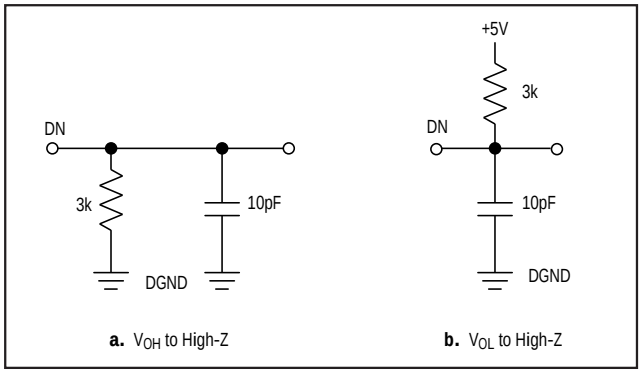


Figure 2. Load Circuits for Bus-Relinquish Time

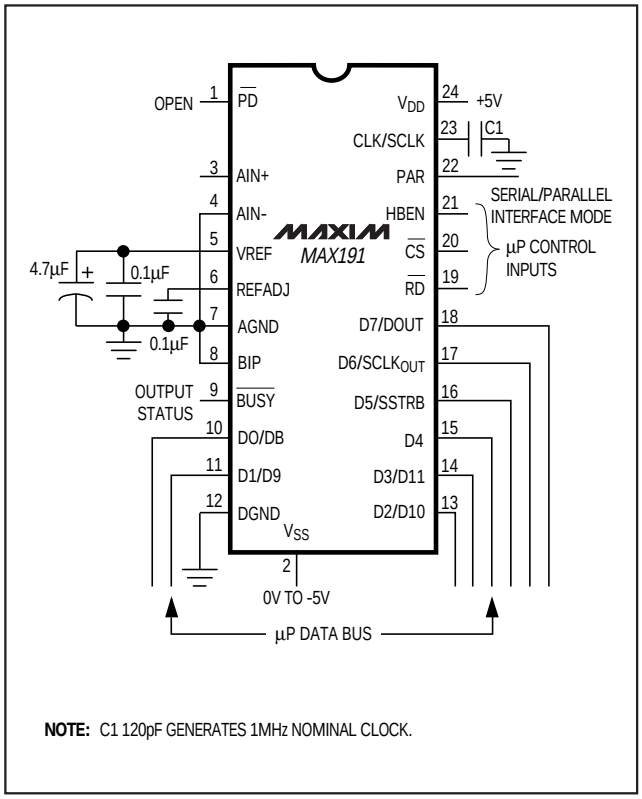


Figure 3. Operational Diagram

Detailed Description

The MAX191 uses successive approximation and input track/hold (T/H) circuitry to convert an analog input signal to a 12-bit digital output. Flexible control logic provides easy interface to microprocessors (μPs), so most applications require only the addition of passive components. No external hold capacitor is required for the T/H. Figure 3 shows the MAX191 in its simplest operational configuration.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). A capacitor switching between the AIN+ and AIN- inputs acquires the signal at the ADC's analog input. At the end of the conversion, the capacitor reconnects to AIN+ and charges to the input signal. An external input buffer is usually not needed for low-bandwidth input signals (<100Hz) because the ADC disconnects from the input during the conversion. In unbuffered applications, an input filter capacitor reduces conversion noise, but also may limit input bandwidth.

When converting a single-ended input signal, AIN- should be connected to AGND. If a differential signal is connected, consider that the configuration is pseudo differential—only the signal side to the input channel is held by the T/H. The return side (AIN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1μF capacitor from AIN- to AGND.

Analog Input—Track/Hold

The T/H enters its tracking mode when the ADC is deselected ($\overline{CS}$ pin is held high and $\overline{BUSY}$ pin is high). Hold mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is about 50ps. Figures 6–10 detail the T/H and interface timing for the

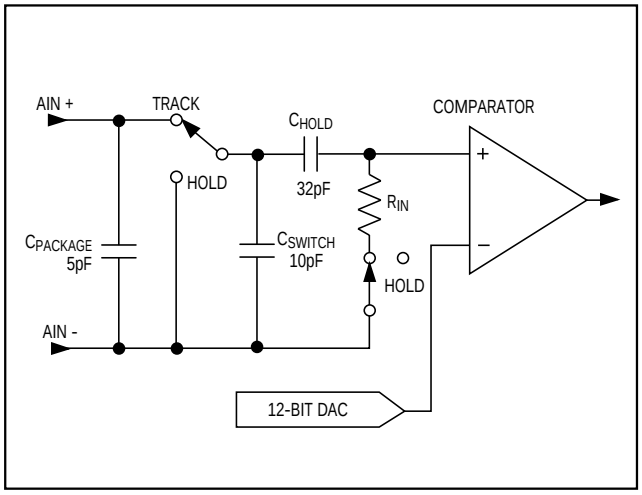


Figure 4. Equivalent Input Circuit

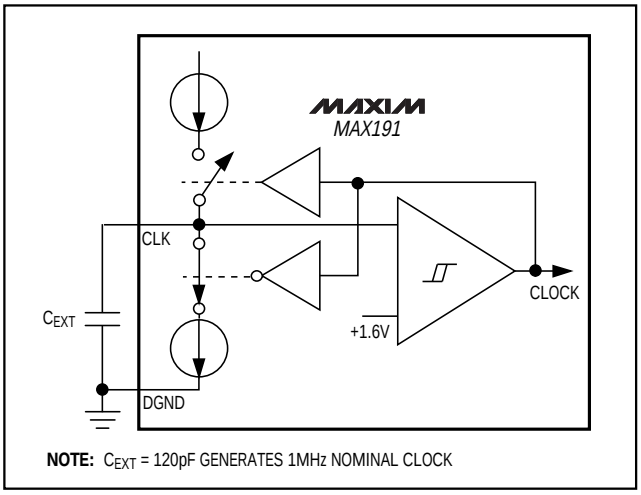


Figure 5. Internal Clock Circuit

various interface modes.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by: $t_{ACQ} = 10(R_S + R_{IN})C_{HOLD}$ (but never less than 2µs), where $R_{IN} = 2k\Omega$, R_S = source impedance of the input signal, and $C_{HOLD} = 32pF$ (see Figure 4).

Input Bandwidth

The ADC's input tracking circuitry has a 1MHz typical large-signal bandwidth characteristic, and a 30V/µs slew rate. It is possible to digitize high-speed transients and measure periodic signals with bandwidths exceeding the ADC's sample rate of 100ksps by using undersampling techniques. Note that if undersampling is used to measure high-frequency signals, special care must be taken to avoid aliasing errors. Without adequate input bandpass filtering, out-of-band signals and noise may be aliased into the measurement band.

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow AIN+ to swing from (V_{SS} - 0.3V) to (V_{DD} + 0.3V) with no risk of damage to the ADC. However, for accurate conversions near full scale, AIN+ should not exceed the power supplies by more than 50mV because ADC accuracy is affected when the protection diodes are even slightly forward biased.

Digital Interface

Starting a Conversion

In parallel mode, the ADC is controlled by the $\overline{CS}$, $\overline{RD}$, and HBEN inputs, as shown in Figure 6. The T/H enters hold mode and a conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN (not shown) is low. $\overline{BUSY}$ goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, $\overline{BUSY}$ goes high and the conversion result is latched into three-state output buffers. In serial mode, the falling edge of $\overline{CS}$ initiates a conversion, and the T/H enters hold mode. Data is shifted out serially as the conversion proceeds (Figure 10). See the *Parallel Digital-Interface Mode* and *Serial-Interface Mode* sections for details.

Internal/External Clock

Figure 5 shows the MAX191 clock circuitry. The ADC includes internal circuitry to generate a clock with an external capacitor. As indicated in the *Typical Operating Characteristics*, a 120pF capacitor connected between the CLK and DGND pins generates a 1MHz nominal clock frequency (Figure 5).

Alternatively, an external clock (between 100kHz and 1.6MHz) can be applied to CLK. When using an external clock source, acceptable clock duty cycles are

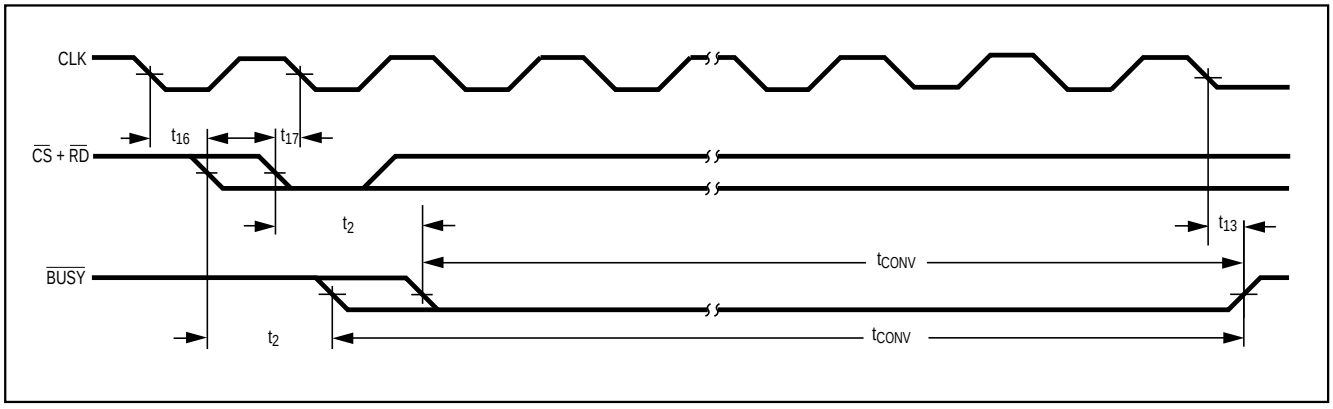


Figure 6. $\overline{CS}$, $\overline{RD}$, and CLK Synchronous Operation

between 45% and 55%.

Clock and Control Synchronization

For best analog performance on the MAX191, the clock should be synchronized to the conversion start signals ($\overline{CS}$ and $\overline{RD}$) as shown in Figure 6. A conversion should not be started in the 50ns before a clock edge nor in the 100ns after it. This ensures that CLK transitions are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough can be a few millivolts. When the clock and conversion start signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be avoided by ensuring that the start of a conversion ($\overline{RD}$ or $\overline{CS}$ falling edge) does not occur close to a clock transition (Figure 6), as described above.

Parallel Digital-Interface Mode

Output-Data Format

The data output from the MAX191 is straight binary in the unipolar mode. In the bipolar mode, the MSB is inverted (see Figure 22). The 12 data bits can be output either in two 8-bit bytes or as a serial output. Table 1 shows the data-bus output format.

A 2-byte read uses outputs D7–D0. Byte selection is controlled by HBEN. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0-D3 with the leading 4 bits low in locations D4–D7.

Timing and Control

Conversion-start and data-read operations are controlled by the HBEN, $\overline{CS}$, and $\overline{RD}$ digital inputs. A logic low is required on all three inputs to start a conversion, and once the conversion is in progress it cannot be restarted. $\overline{BUSY}$ remains low during the entire conversion cycle.

The timing diagrams of Figures 7–10 outline two parallel-interface modes and one serial mode.

Slow-Memory Mode

In slow-memory mode, the device appears to the µP as a slow peripheral or memory. Conversion is initiated with a read instruction (see Figure 7 and Table 2). Set the PAR pin high for parallel interface mode. Beginning with HBEN low, taking $\overline{CS}$ and $\overline{RD}$ low starts the conversion. The analog input is sampled on the falling edge of $\overline{RD}$. $\overline{BUSY}$ remains low while the conversion is in progress. The previous conversion result appears at the digital outputs until the end of conversion, when $\overline{BUSY}$ returns high. The output latches are then updated with the newest results of the 8 LSBs on D7–D0. A second read operation with HBEN high places the 4 MSBs, with 4 leading 0s, on data outputs D7–D0. The second read operation does not start a new conversion because HBEN is high.

ROM Mode

As in slow-memory mode, D7–D0 are used for 2-byte reads. A conversion starts with a read instruction with HBEN and $\overline{CS}$ low. The T/H samples the input on the falling edge of $\overline{RD}$ (see Figure 8 and Table 3). PAR is set high. At this point the data outputs contain the 8 LSBs from the previous conversion. Two more read operations are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading 0s are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Figure 9 and Table 4 show how to read output data within one conversion cycle without starting another conversion. Trigger the falling edge of a read on the ris-

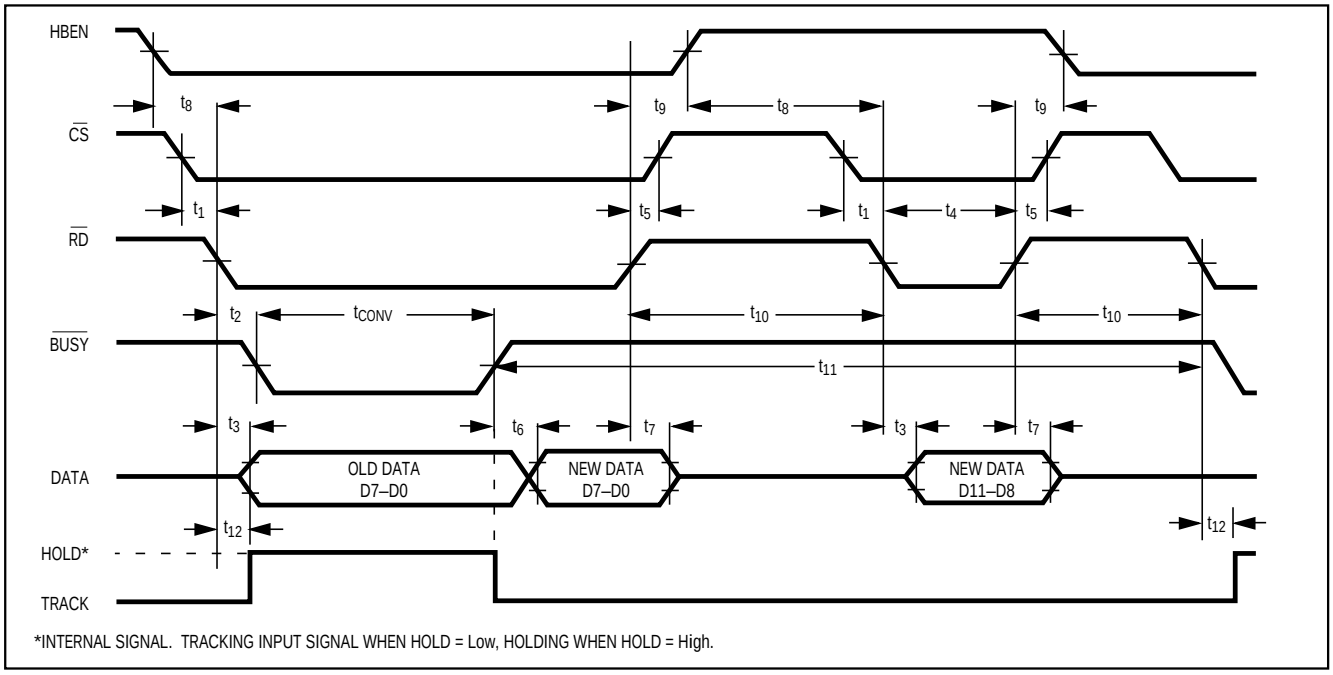


Figure 7. Slow-Memory Mode Timing

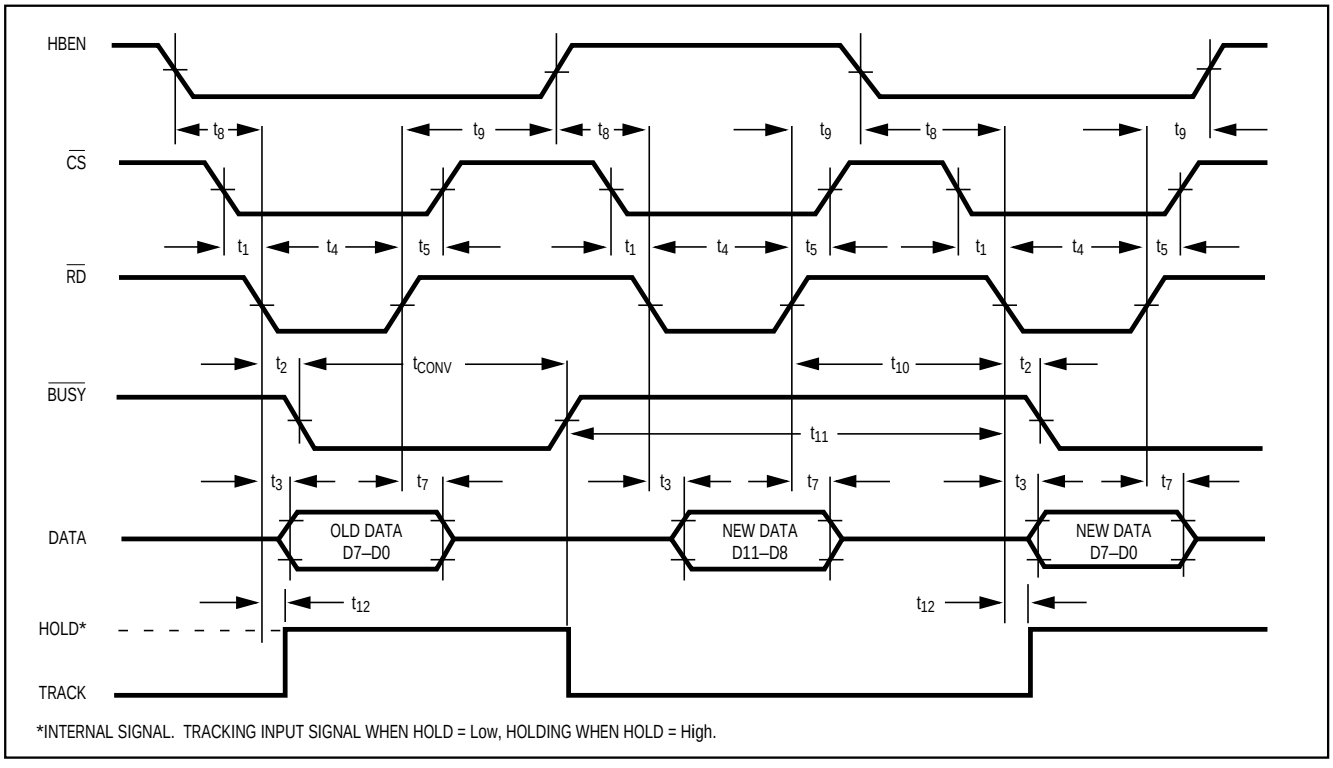


Figure 8. ROM Mode Timing

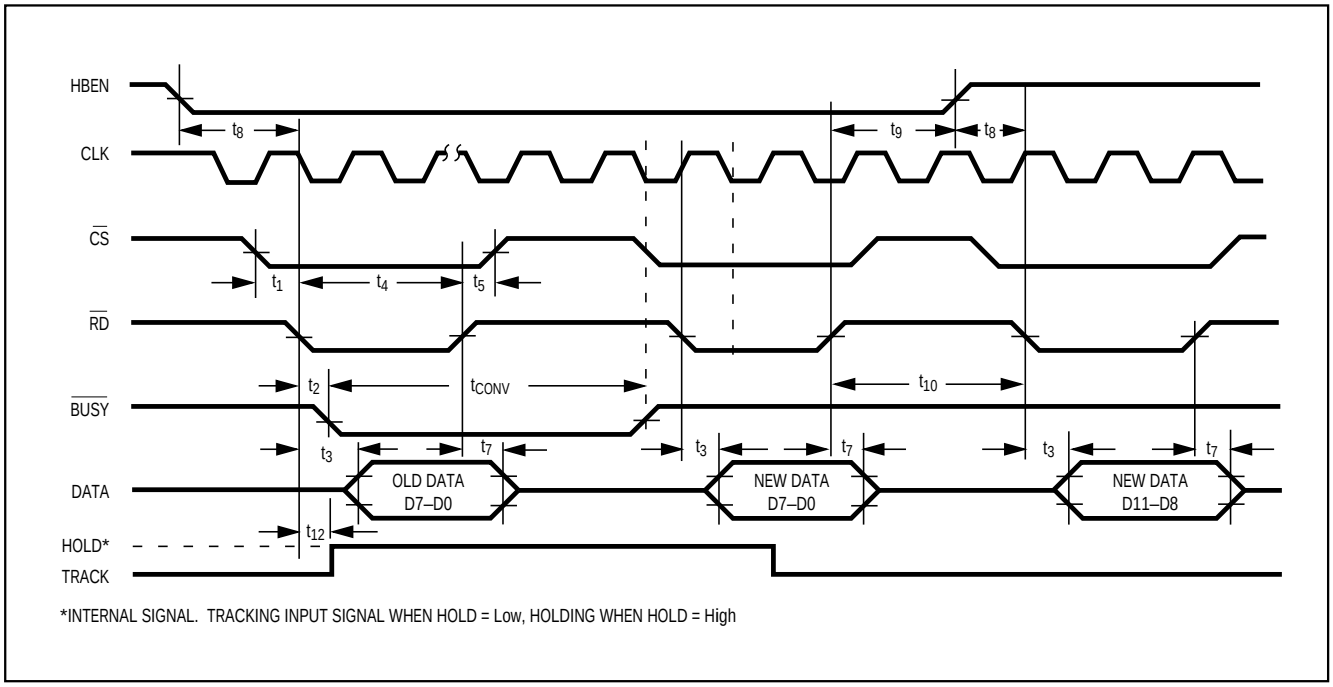


Figure 9. ROM Mode Timing, Reading Data without Starting a Conversion

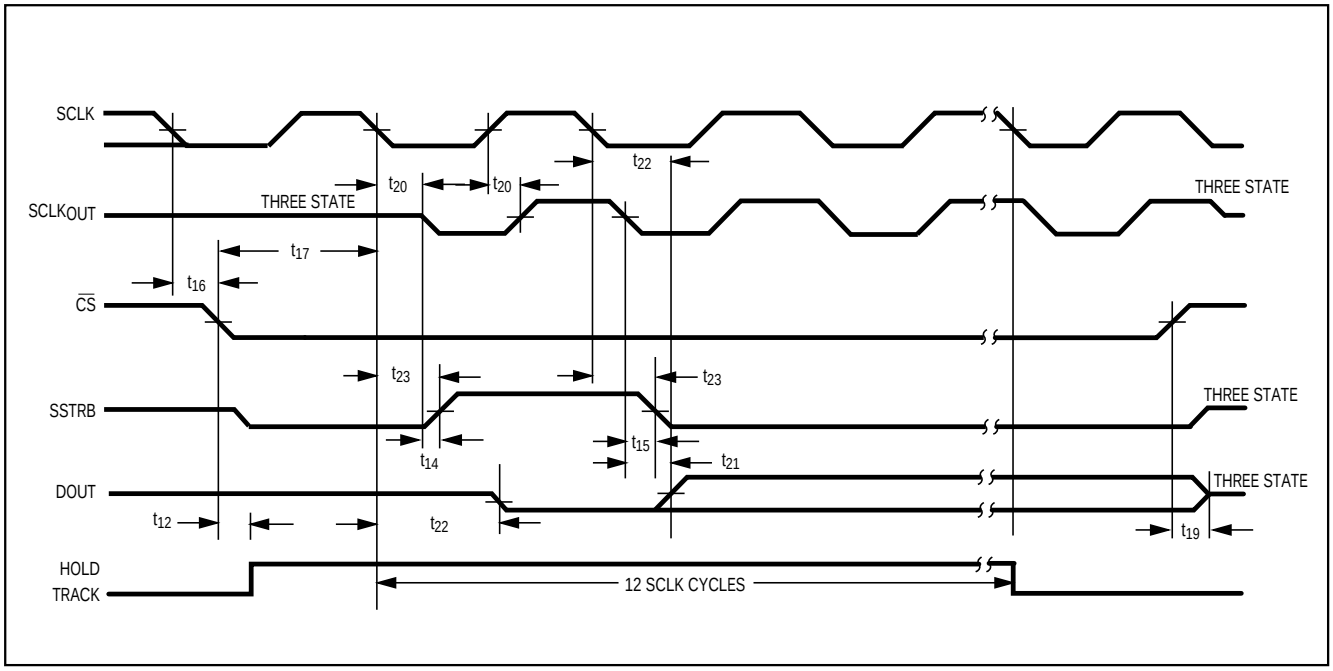


Figure 10. Serial-Interface Mode Timing Diagram ($\overline{RD}$ = low)

Table 1. Data-Bus Output, $\overline{CS}$ = $\overline{RD}$ = Low

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
HBEN = 0, PAR = 1, PARALLEL MODE	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = 1, PAR = 1, PARALLEL MODE	Low	Low	Low	Low	D11	D10	D9	D8
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 0	DOUT	SCLK$_{OUT}$	SSTRB	Low	Low	Low	Low	Low
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 1	DOUT	Three-Stated	Three-Stated	Low	Low	Low	Low	Low

Note: D7/DOUT–D0/D8 are the ADC data output pins.
D11–D0 are the 12-bit conversion results. D11 is the MSB.
DOUT = Three-state data output. Data output in serial mode.
SCLK$_{OUT}$ = Three-state data output. Clock output in serial mode.
SSTRB = Three-state data output. Strobe output in serial mode.

Table 2. Slow-Memory Mode, 2-Byte Read Data-Bus Status

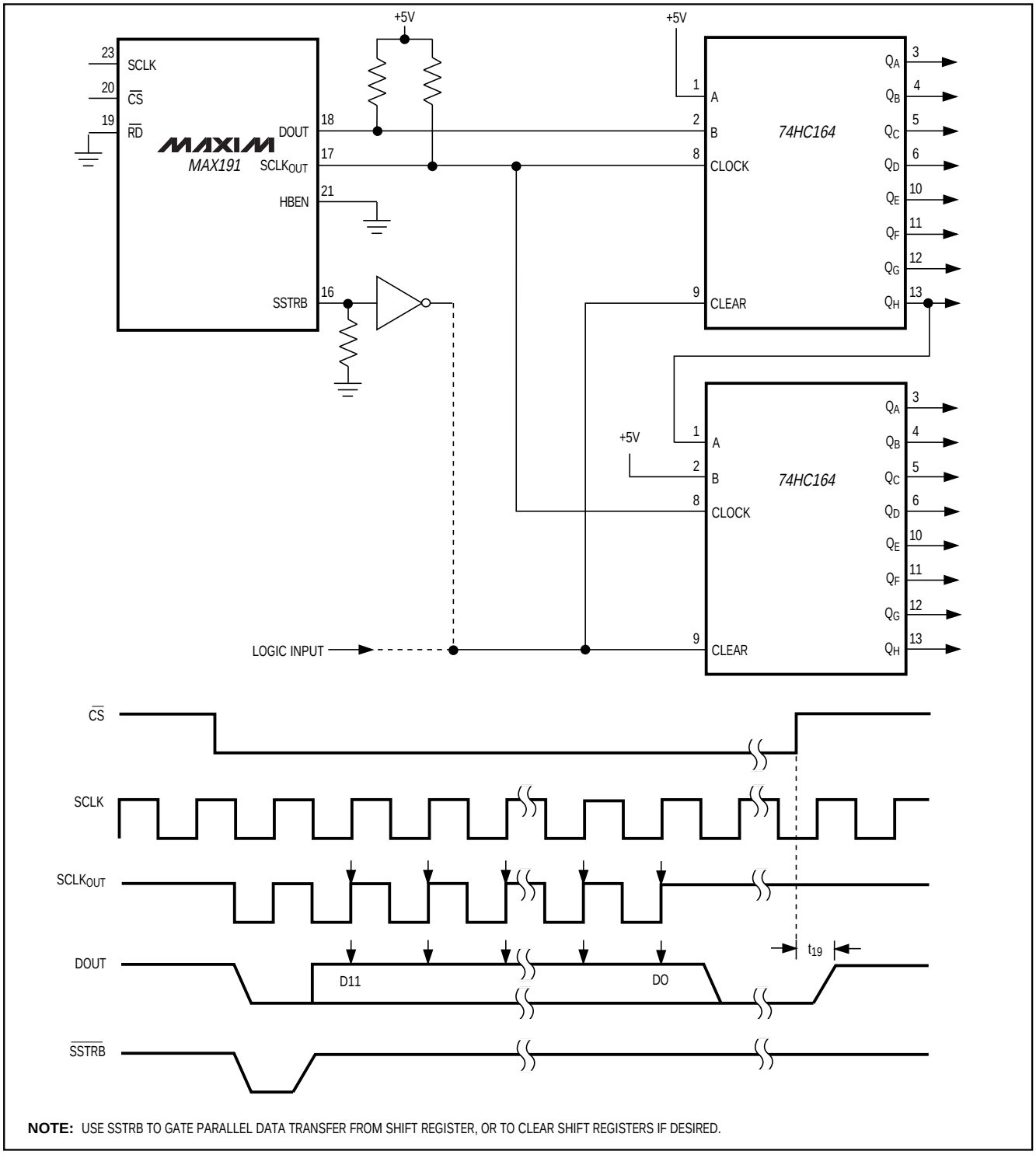
PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8

Table 3. ROM Mode, 2-Byte Read Data-Bus Status

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8
THIRD READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0

Table 4. ROM Mode, 2-Byte Read Data-Bus Status without Starting a Conversion Cycle

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
THIRD READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8



NOTE: USE SSTRB TO GATE PARALLEL DATA TRANSFER FROM SHIFT REGISTER, OR TO CLEAR SHIFT REGISTERS IF DESIRED.

Figure 11. Simple Serial-to-Parallel Interface

ing edge of the first clock cycle after conversion end (when $\overline{BUSY}$ goes high). As mentioned previously, two more read operations (after $\overline{BUSY}$ goes high) are needed to access the conversion results. The only difference is that now the low byte can be read first. This happens by allowing the first read operation to occur with HBEN low, where the 8 LSBs are accessed. The second read, with HBEN high, accesses the 4 MSBs with 4 leading 0s.

Serial-Interface Mode

The serial mode is compatible with Microwire, SPI and QSPI serial interfaces. In addition, a framing signal (SSTRB) is provided that allows the devices to interface with the TMS320 family of DSPs. Set PAR low for serial mode. A falling edge on $\overline{CS}$ causes the T/H to sample the input (Figure 10). Conversion always begins on the next falling edge of SCLK, regardless of where $\overline{CS}$ occurs. The DOUT line remains high-impedance until a conversion begins. During the MSB decision, DOUT remains low (leading 0), while SSTRB goes high to indicate that a data frame is beginning. The data is available at DOUT on the rising edge of SCLK ($SCLK_{OUT}$ when using an internal clock) and transitions on the falling edge. DOUT remains low after all data bits have been shifted out, inserting trailing 0s in the data stream until $\overline{CS}$ returns high. The $SCLK_{OUT}$ signal is synchronous with the internal or external clock.

For interface flexibility, DOUT, $SCLK_{OUT}$ and SSTRB signals enter a high-impedance state when $\overline{CS}$ is high. When $\overline{CS}$ is low, $\overline{RD}$ controls the status of $SCLK_{OUT}$ and SSTRB outputs. A logic low $\overline{RD}$ enables $SCLK_{OUT}$ and SSTRB, while a logic high forces both outputs into a high-impedance state. Also, with $\overline{CS}$ low and HBEN high, $SCLK_{OUT}$ drives continuously, regardless of conversion status. This is useful with µPs that require a continuous serial clock. If $\overline{CS}$ and HBEN are low, $SCLK_{OUT}$ is output only during the conversion cycle, while the converter internal clock runs continuously. This is useful for creating a simple serial-to-parallel interface without shift-register overflow (Figure 11).

Maximum Clock Rate in Serial Mode

The maximum SCLK rate depends on the minimum setup time required at the serial data input to the µP and the ADC's DOUT to SCLK delay (t_{22}) (see Figure 12). The maximum f_{SCLK} is as follows:

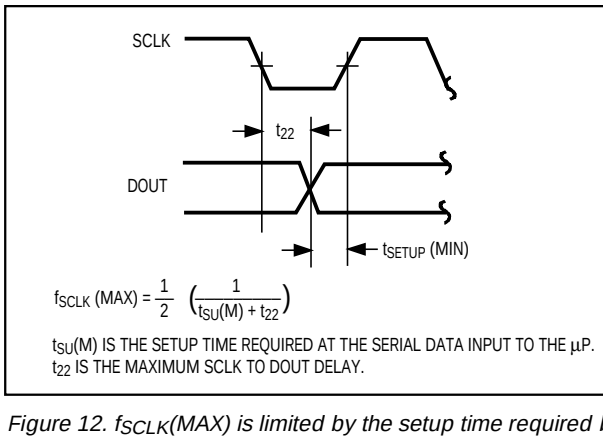


Figure 12. f_{SCLK}(MAX) is limited by the setup time required by the serial data input to the µP.

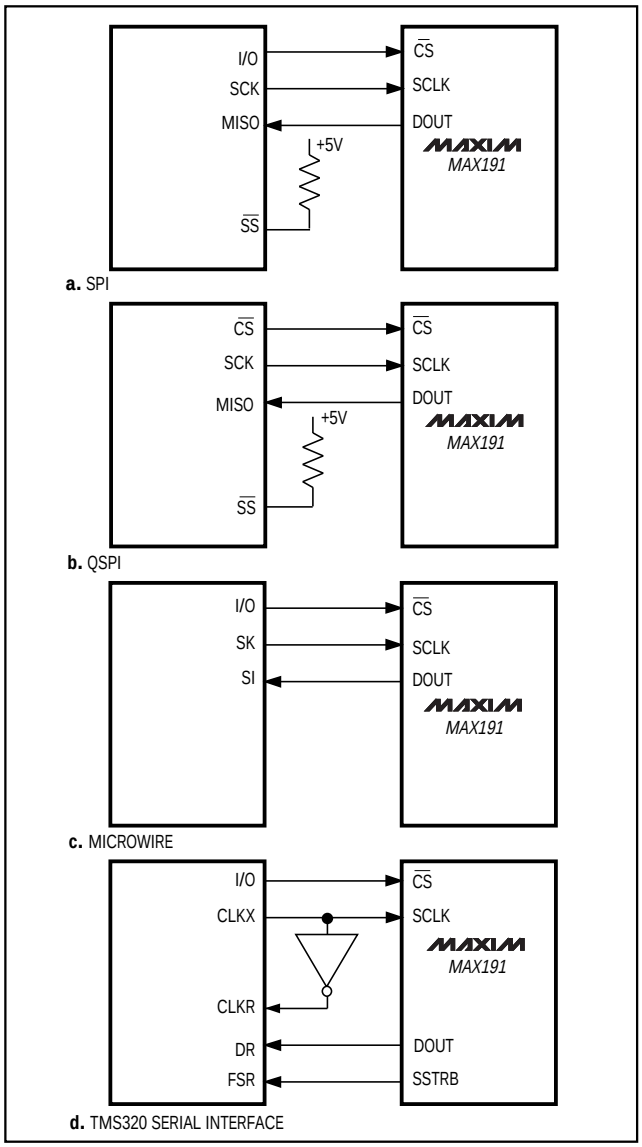


Figure 13. Common Serial-Interface Connections to the MAX191

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

$$f_{SCLK}(MAX) = (1/2) \times 1/ (t_{su}(M) + t_{22})$$

where $t_{su}(M)$ is the minimum data-setup time required at the serial data input to the µP. For example, Motorola's MC68HC11A8 data book specifies a 100ns minimum data-setup time. Using the worst case for a military grade part of t_{22} = 280ns (see *Timing Characteristics*) and substituting in the above equation indicates a maximum SCLK frequency of 1.3MHz.

Using the MAX191 with SPI, QSPI and MICROWIRE Serial Interfaces

Figure 13 shows interface connections to the MAX191 for common serial-interface standards.

SPI and MICROWIRE (CPOL=0, CPHA=0)

The MAX191 is compatible with SPI, QSPI and MICROWIRE serial-interface standards. When using SPI or QSPI, two modes are available to interface with the MAX191. You can set CPOL = 0 and CPHA = 0 (Figure 14a), or set CPOL = 1 and CPHA = 1 (Figure 14b). When using CPOL = 0 and CPHA = 0, the conversion begins on the first falling edge of SCLK following $\overline{CS}$ going low. Data is available from DOUT on the rising edge of SCLK, and transitions on the falling edge. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. The first byte contains the following, in this order: a leading unknown bit (DOUT will still be high-impedance on the first bit), a 0, and the six MSBs. The second byte contains the remaining six LSBs and two trailing 0s.

SPI (CPOL=1, CPHA=1)

Setting CPOL = 1 and CPHA = 1 starts the clock high during a read instruction. The MAX191 will shift out a leading 0 followed by the 12 data bits and three trailing 0s (Figure 14b).

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles required to clock in the data (Figure 15).

TMS320 Serial Interface

Figure 13d shows the pin connections to interface the MAX191 to the TMS320. Since the MAX191 makes data available on the rising edge of SCLK and the TMS320 shifts data in on the falling edge of CLKR, use CLKX of the DSP to drive SCLK, and $\overline{CLKX}$ to drive the DSP's CLKR input. The inverter's propagation delay also provides more data-setup time at the DSP. For example, with no inverter delay, and using t_{22} = 280ns and f_{SCLK} = 1.6MHz, the available setup time before the SCLK transition is:

$$\text{setup time} = 1/ (2 \times f_{SCLK}) - t_{22} = 1/ (2 \times 1.6E6) - 280ns = 32ns$$

This still exceeds the 13ns minimum DR setup time before the CLKR goes low (tsu(DR)), however, a generic 74HC04 provides an additional 20ns setup time (see Figure 13d).

Figure 16 shows the DSP interface timing characteristics. The DSP begins clocking data in on the falling edge of CLKR after the falling edge of SSTRB.

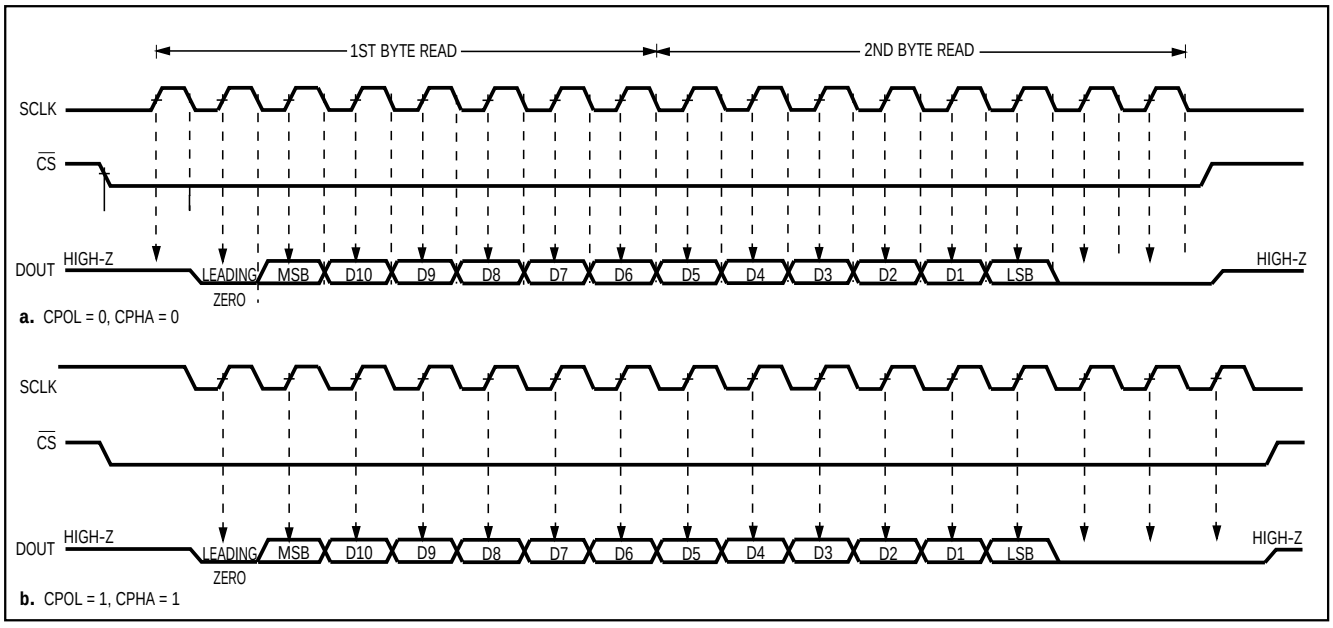


Figure 14. SPI/MICROWIRE Serial-Interface Timing

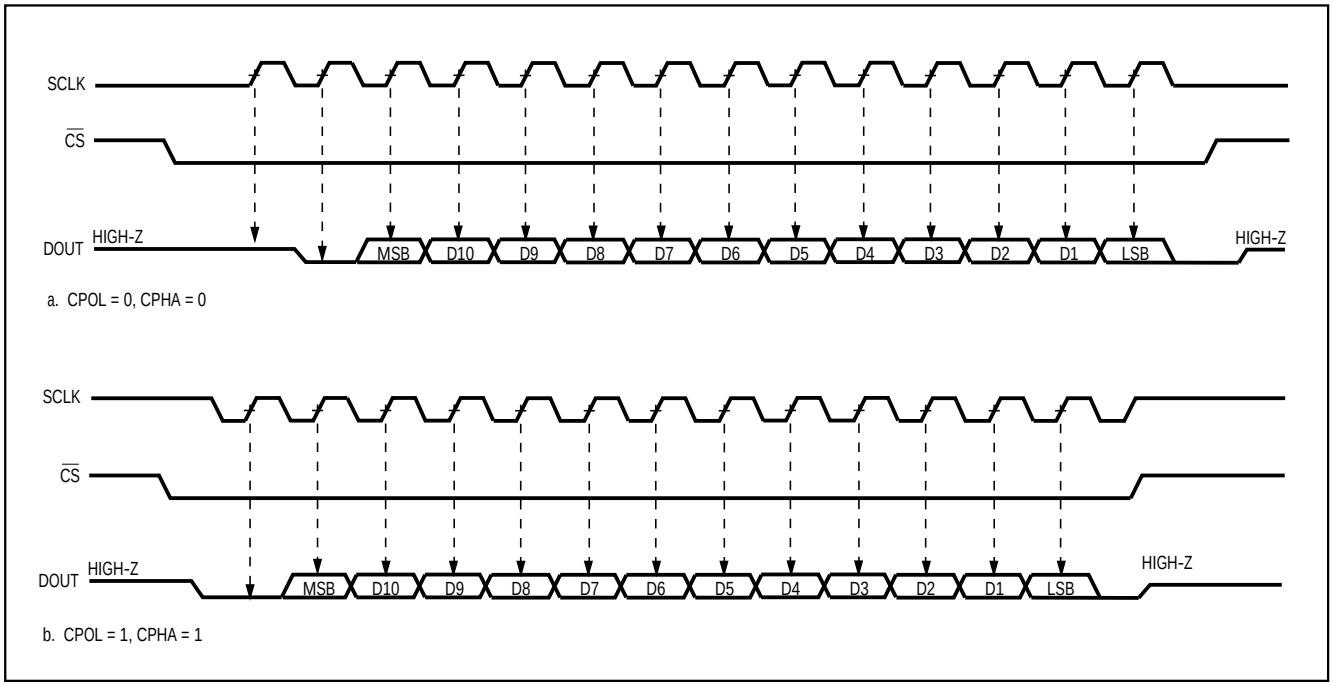


Figure 15. QSPI Serial-Interface Timing

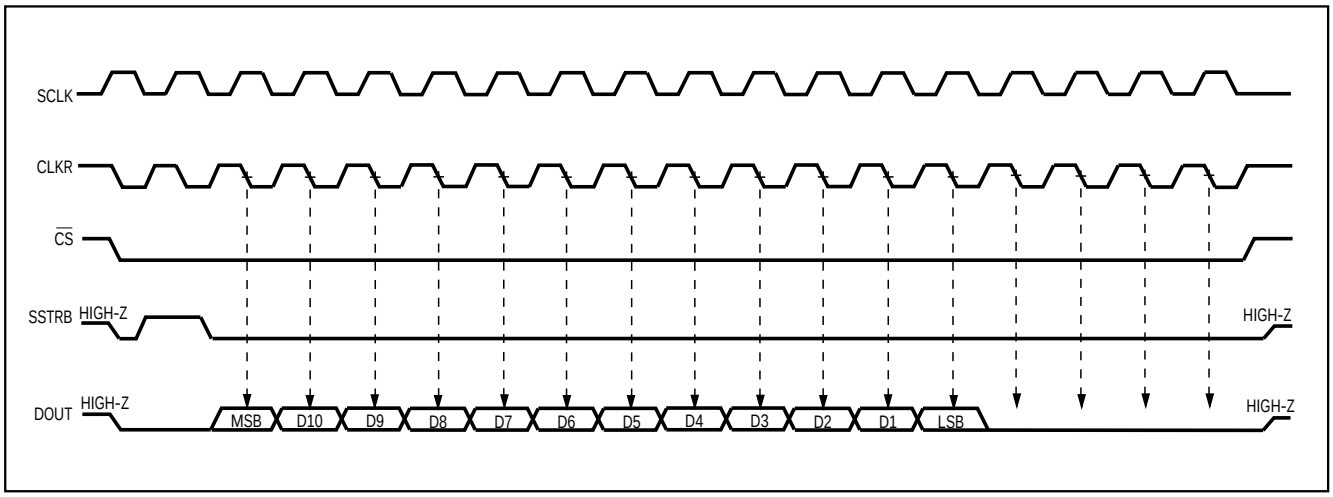


Figure 16. TMS320 Interface Timing

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Following the data transfer, the DSP receive shift register (RSR) contains a 16-bit word consisting of the 12 data bits, MSB first, followed by four trailing 0s.

Applications Information

Power-On Initialization

When the +5V power supply is first applied to the MAX191, perform a single conversion to initialize the ADC (the BUSY signal status is undefined at power-on). Disregard the data outputs.

Power-Down Mode

In some battery-powered systems, it is desirable to power down or remove power from the ADC during inactive periods. To power down the MAX191, drive $\overline{PD}$ low. In this mode, all internal ADC circuitry is off except the reference, and the ADC consumes less than 50µA max (assuming all signals $\overline{CS}$, $\overline{RD}$, CLK, and HBEN are static and within 200mV of the supplies). Figure 17 shows a practical way to drive the $\overline{PD}$ pin. If using internal reference compensation, drive $\overline{PD}$ between V_{DD} and DGND with a µP I/O pin or other logic device (Figure 17a). For external-reference compensation mode, use the circuit in Figure 17b to drive $\overline{PD}$ between DGND and the floating voltage of $\overline{PD}$. An alternative is to drive $\overline{PD}$ with three-state logic or a switch, provided the off leakage does not exceed 100nA.

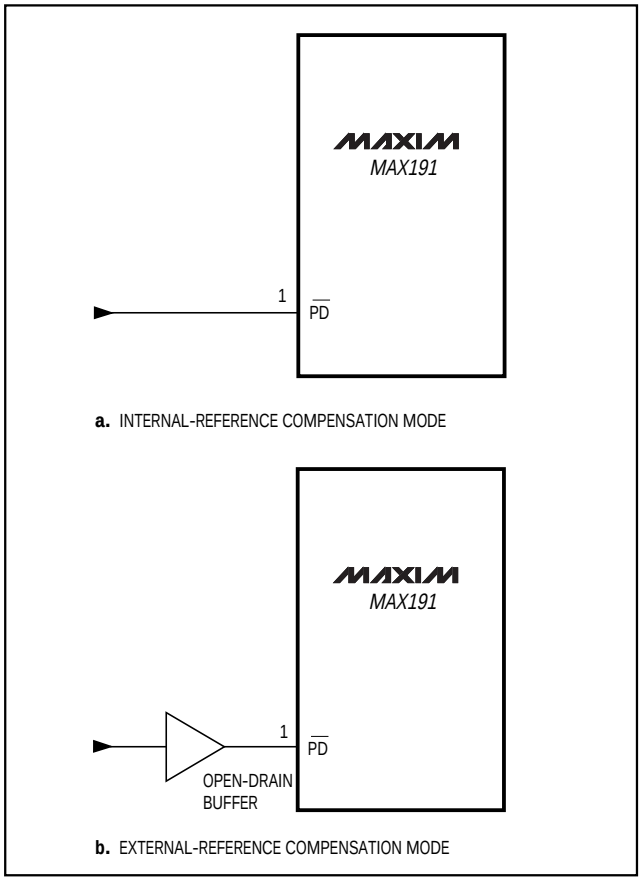


Figure 17. Drive Circuits for $\overline{PD}$ Pin

Internal Reference

The internal 4.096V reference is available at VREF and must be bypassed to AGND with a 4.7µF low-ESR capacitor (less than 1/2Ω) in parallel with a 0.1µF capacitor, unless internal-reference compensation mode is used (see the *Internal Reference Compensation* section). This minimizes noise and maintains a low reference impedance at high frequencies. The reference output can be disabled by connecting REFADJ to V_{DD} when using an external reference.

Reference-Compensation Modes

Power-down performance can be optimized for a given conversion rate by selecting either internal or external reference compensation.

Internal Compensation

The connection for internal compensation is shown in Figure 18a. In this mode, the reference stabilizes quickly enough so that a conversion typically starts within 35µs after the ADC is reactivated ($\overline{PD}$ pulled high). In this compensation mode, the reference buffer requires longer recovery time from SAR transients, therefore requiring a slower clock (and conversion time). With internal reference compensation, the typical conversion time rises to 25µs (Figure 18b). Figure 18c illustrates the typical average supply current vs. conversion rate,

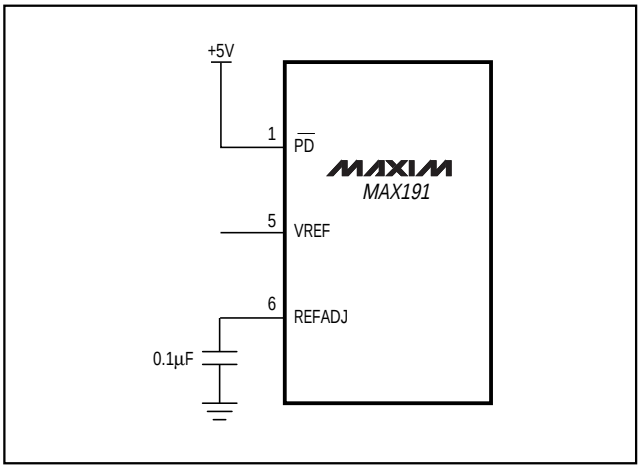


Figure 18a. Internal-Compensation Mode Circuit

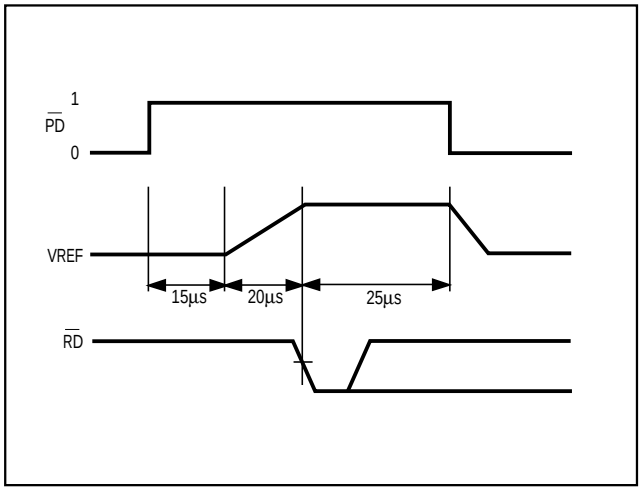


Figure 18b. Low Average-Power Mode Operation (Internal Compensation)

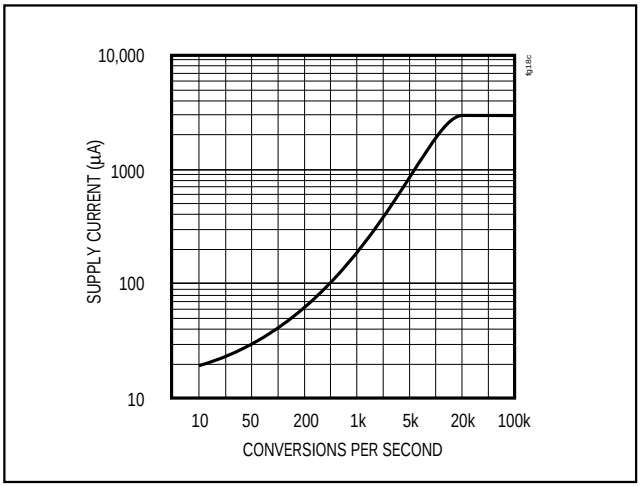


Figure 18c. Average Supply Current vs. Conversion Rate, Powering Down Between Conversions

which can be achieved using power-down between conversions.

External Compensation

Figure 19a shows the connection for external compensation with reference adjustment. In this mode, an external 4.7µF capacitor compensates the reference output amplifier, allowing for maximum conversion speed and lowest conversion noise. However, when reactivating the ADC after power-down, the reference takes typically 2ms to fully charge the 4.7µF capacitor, so more time is required before a conversion can start (Figure 19b). Thus, the average current consumed in power-up/power-down operations is higher in external compensation mode than in internal compensation mode.

Gain and Offset Adjustment

Figure 20 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 22 shows the bipolar I/O transfer function. Code transitions occur halfway between successive integer LSB values. Note that 1LSB = 1.00mV (4.096V/4096) for unipolar operation and 1LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figures 19a and 21a show how to adjust the ADC gain in applications that require full-scale range adjustment. The connection shown in Figure 21a provides ±0.5% for ±20LSBs of adjustment range and is recommended for applications that use an external reference. On the other hand, Figure 19a is recommended for applications that use the internal reference, because it uses fewer external components.

If both offset and full scale need adjustment, the circuit in Figure 21b is recommended. For single-supply

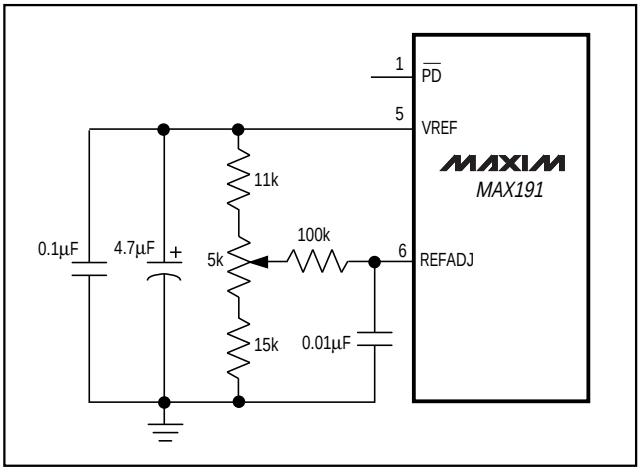


Figure 19a. External-Compensation Mode with Internal Reference Adjustment Circuit

ADCs, it is virtually impossible to null system negative offset errors. However, the MAX191 input configuration is pseudo-differential—only the difference in voltage between AIN+ and AIN- will be converted into its digital representation. By applying a small positive voltage to AIN-, the 0 input voltage at AIN+ can be adjusted to above or below AIN- voltage, thus nulling positive or negative system offset errors. R9 and R10 can be removed for applications that require only positive system errors to be nulled. To trim the offset error of the MAX191, apply 1/2LSB to the analog input and adjust R6 so the digital output code changes between 000 (hex) and 001 (hex). To adjust full scale, apply FS - 1 1/2LSBs and adjust R2 until the output code changes

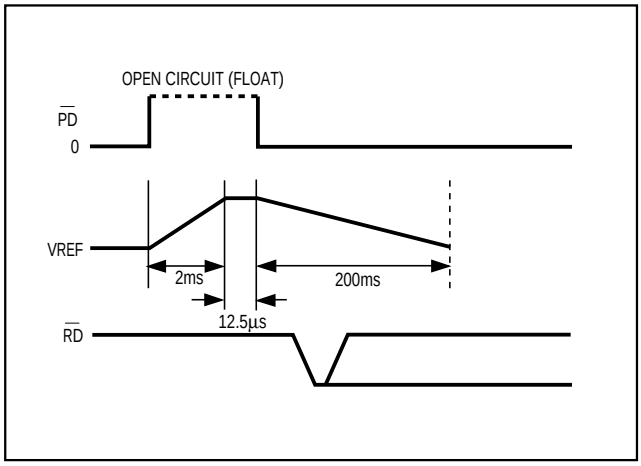


Figure 19b. Low Average-Power Mode Operation (External Compensation)

between FFE (hex) and FFF (hex). Because interaction occurs between adjustments, offset should be adjusted before gain. For an input gain of two, remove R7 and R8.

The MAX191 accepts input voltages from AGND to V_{DD} while operating from a single supply, and V_{SS} to V_{DD} when operating from dual supplies. Figure 22 shows the bipolar input transfer function with AIN- connected to midscale for single-supply operation and connected to GND operating from dual supplies. When operating from a single supply, the MAX191 can be configured for bipolar operation on its pseudo-differential input. Instead of using AIN- as an analog input return, AIN- can be set to a different positive potential voltage above ground (BIP pin is set high). The sampled analog input (AIN+) can swing to any positive voltage above and below AIN-, and the ADC performs bipolar conversions with respect to AIN-. When operating from dual supplies, the MAX191 full-scale range is from $-V_{REF}/2$ to $+V_{REF}/2$.

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, crosstalk from the data pins to the ADC comparator may generate errors. Slow-memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, it should be isolated from the ADC using three-state drivers.

The ADC generates considerable digital noise in ROM mode when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after a conversion has started. This noise can cause large errors if it occurs when the SAR latches a comparator decision. To avoid this problem,

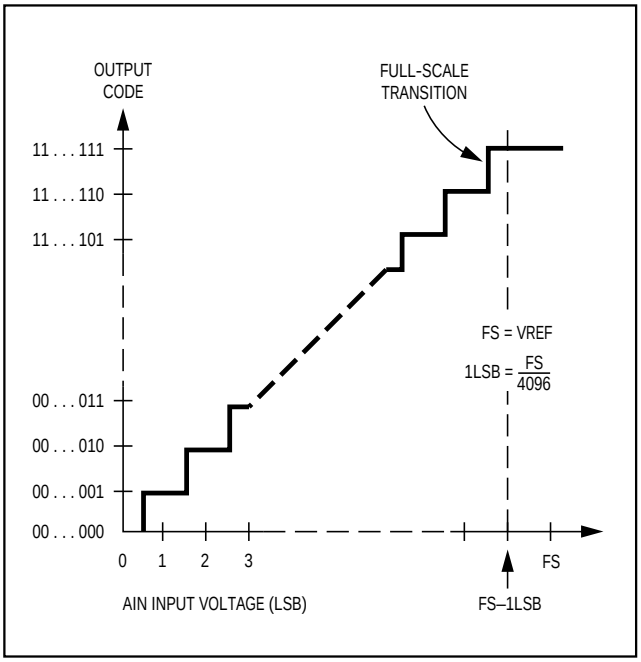


Figure 20. Unipolar Transfer Function

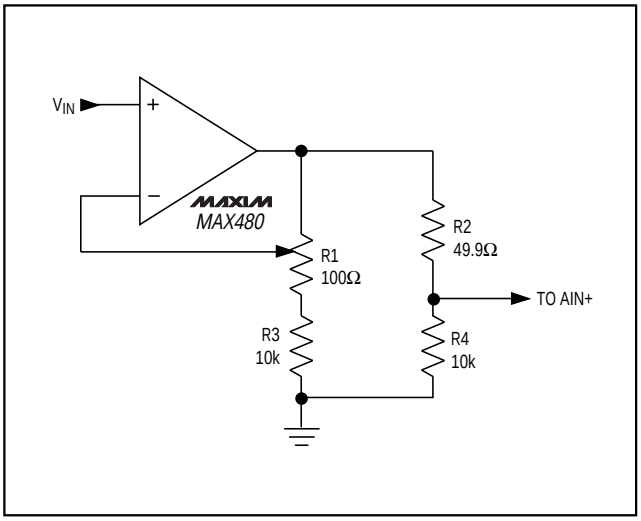


Figure 21a. Trim Circuit for Gain (±0.5%)

$\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high at the rising edge of CLK, since the comparator output is always latched on falling edges of CLK.

Layout, Grounding, Bypassing

Use printed circuit boards for best system performance.

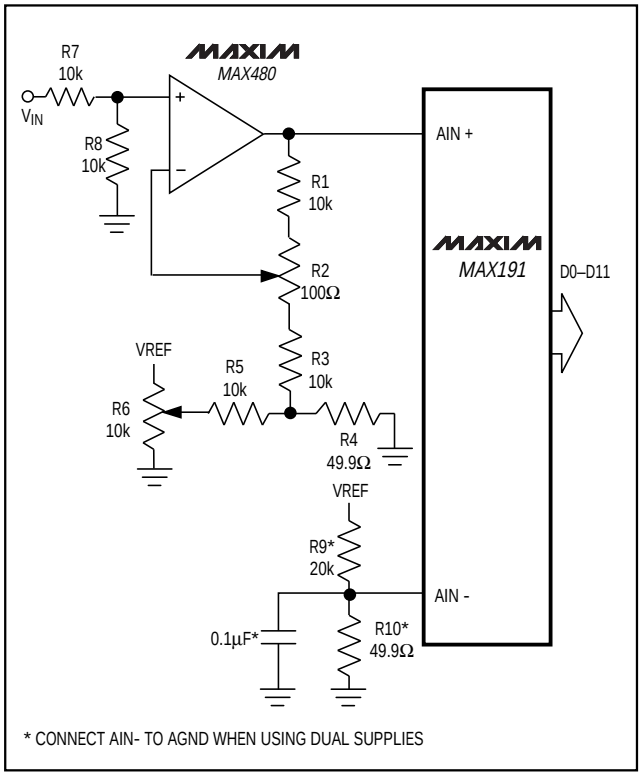


Figure 21b. Offset (±10mV) and Gain (±1%) Trim Circuit

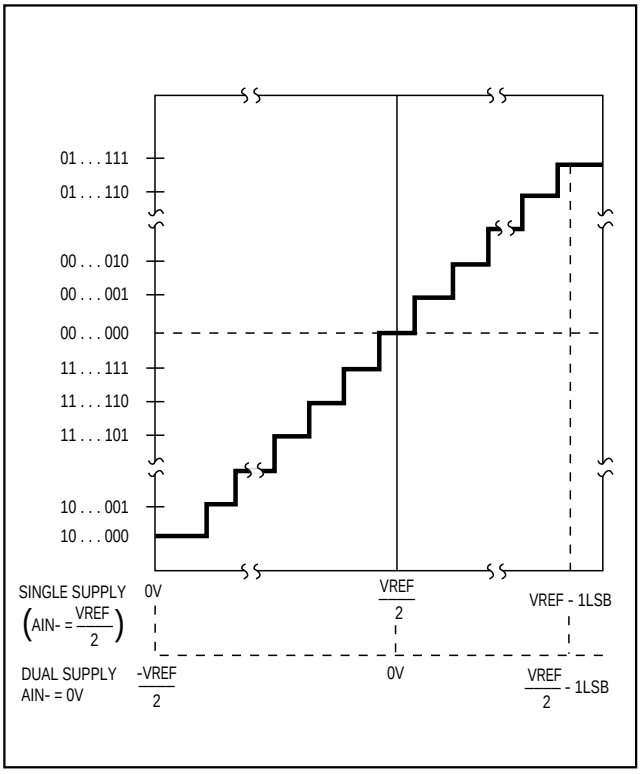


Figure 22. Bipolar Transfer Function

Wire-wrap boards are not recommended. Board layout should ensure that digital- and analog-signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 23 shows the recommended system ground connections. Establish a single-point ground (“star” ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to it. No other digital-system ground should be connected to this single-point analog ground. The ground return to the power supply for this star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with

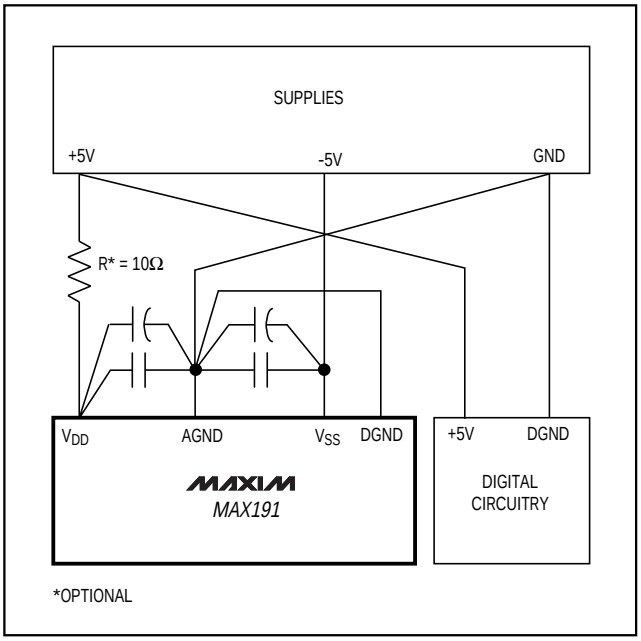


Figure 23. Power-Supply Grounding Connection

0.01µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to filter out supply noise (Figure 23).

Dynamic Performance

High-speed sampling capability and throughput make the MAX191 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency. FFT plots are shown in the *Typical Operating Characteristics*.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL), and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals, except signal harmonics. Signal-to-Noise + Distortion ratio (SINAD) is the same as the SNR, but includes signal harmonics.

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02n + 1.76) dB, where n is the number of bits of resolution. 74dB is the SNR of a perfect 12-bit ADC.

By transposing the equation that converts resolution to SNR we can compute the effective resolution or the "effective number of bits" the ADC provides from the measured SNR:

$$n = (SNR - 1.76)/6.02$$

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This expressed as:

$$THD = 20\log\left[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + \ldots + V_n^2)}/V_1\right]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_n are the amplitudes of the 2nd through n^{th} harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it can occur at a random peak in the ADC's noise floor.

Opto-Isolated A/D Interface

Many industrial applications require isolation to prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. In Figure 24, a MAX250 and four 6N136 opto-couplers create an

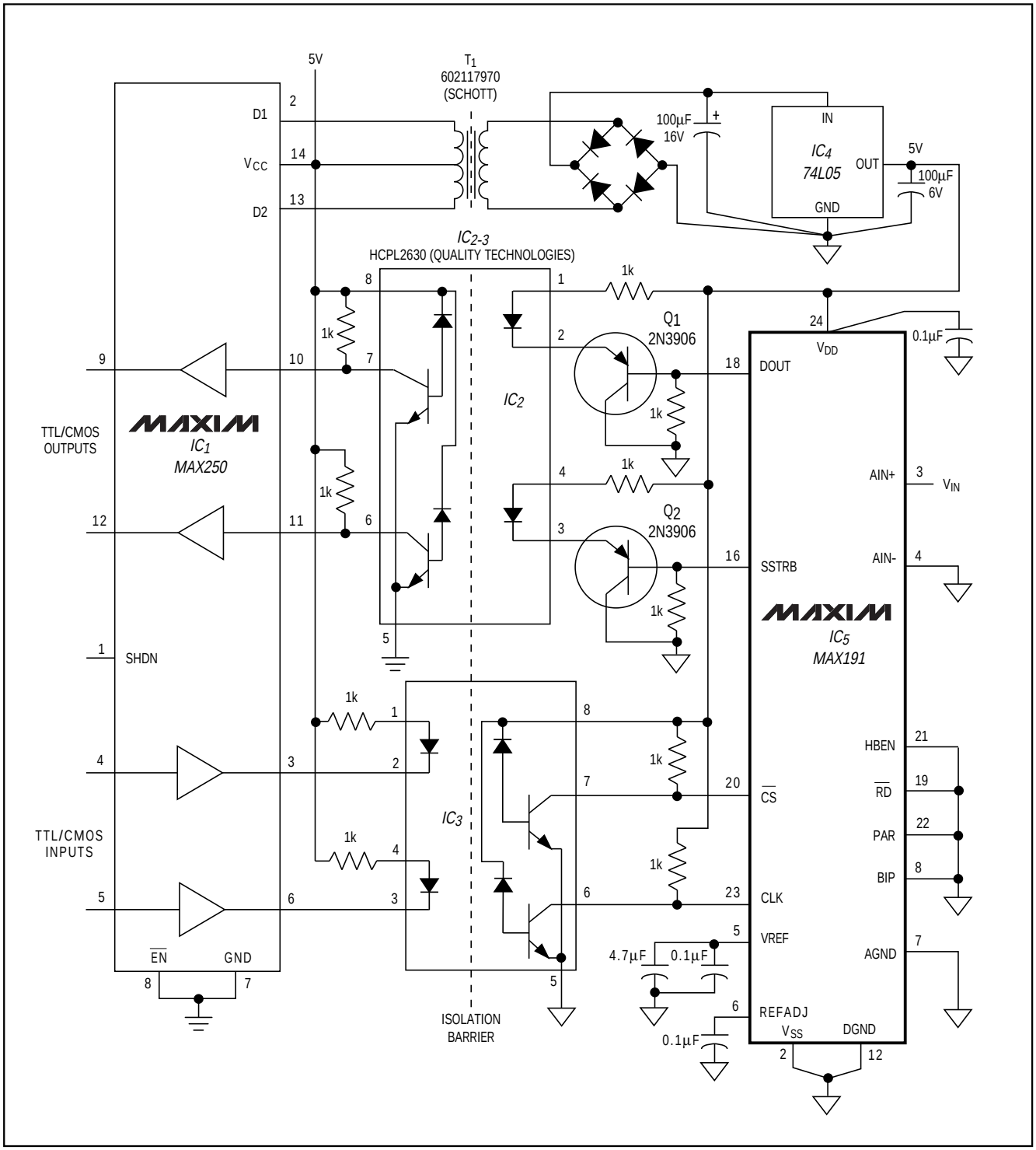
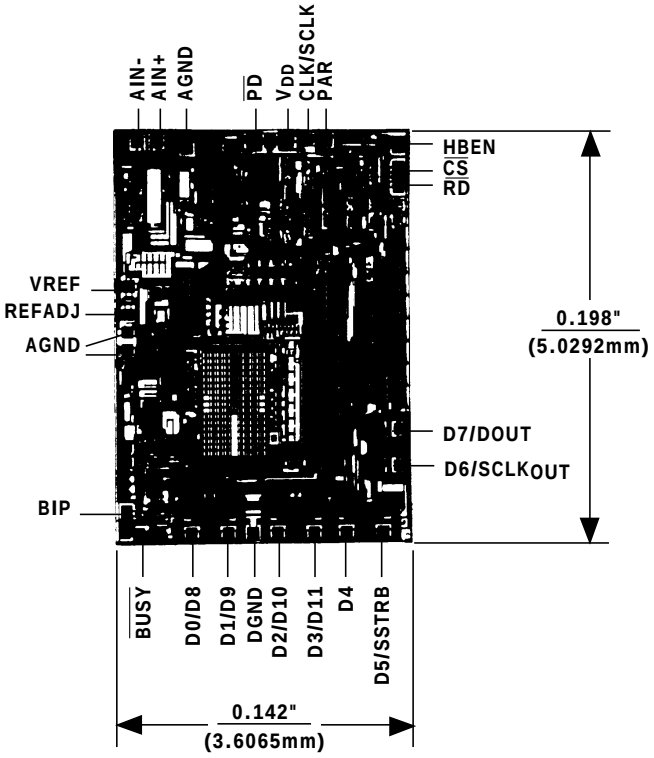


Figure 24. Isolated Data-Acquisition Circuit

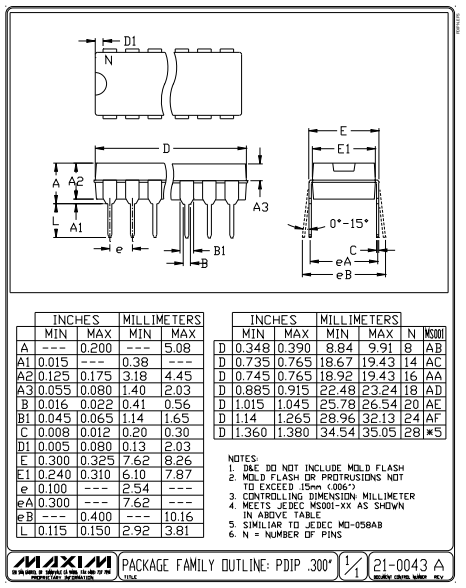
Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Chip Topography



SUBSTRATE CONNECTED TO V_{DD}

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A