19-4226; Rev 2; 9/10

EVALUATION KIT AVAILABLE

Dual-Channel, 10-Bit, 100Msps ADC

MAX19516

General Description

The MAX19516 dual-channel, analog-to-digital converter (ADC) provides 10-bit resolution and a maximum sample rate of 100Msps.

The MAX19516 analog input accepts a wide 0.4V to 1.4V input common-mode voltage range, allowing DC-coupled inputs for a wide range of RF, IF, and baseband front-end components. The MAX19516 provides excellent dynamic performance from baseband to high input frequencies beyond 400MHz, making the device ideal for zero-intermediate frequency (ZIF) and high-intermediate frequency (IF) sampling applications. The typical signal-to-noise ratio (SNR) performance is 60dBFS and typical spurious-free dynamic range (SFDR) is 82dBc at f_{IN} = 70MHz and f_{CLK} = 100MHz.

The MAX19516 operates from a 1.8V supply. Additionally, an integrated, self-sensing voltage regulator allows operation from a 2.5V to 3.3V supply (AVDD). The digital output drivers operate on an independent supply voltage (OVDD) over the 1.8V to 3.5V range. The analog power consumption is only 57mW per channel at V_{AVDD} = 1.8V. In addition to low operating power, the MAX19516 consumes only 1mW in power-down mode and 17mW in standby mode.

Various adjustments and feature selections are available through programmable registers that are accessed through the 3-wire serial-port interface. Alternatively, the serial-port interface can be disabled, with the three pins available to select output mode, data format, and clock-divider mode. Data outputs are available through a dual parallel CMOS-compatible output data bus that can also be configured as a single multiplexed parallel CMOS bus.

The MAX19516 is available in a small 7mm x 7mm 48-pin thin QFN package and is specified over the -40°C to +85°C extended temperature range.

Refer to the MAX19505, MAX19506, and MAX19507 data sheets for pin- and feature-compatible 8-bit, 65Msps, 100Msps, and 130Msps versions, respectively. Refer to the MAX19515 and MAX19517 data sheets for pin- and feature-compatible 10-bit, 65Msps and 130Msps versions, respectively.

Applications

IF and Baseband Communications, Including Cellular Base Stations and Point-to-Point Microwave Receivers

Ultrasound and Medical Imaging

Portable Instrumentation and Low-Power Data Acquisition

Digital Set-Top Boxes

Features

- **Very-Low-Power Operation (57mW/Channel at 100Msps)**
- **1.8V or 2.5V to 3.3V Analog Supply**
- **Excellent Dynamic Performance**
  - **60dBFS SNR at 70MHz**
  - **82dBc SFDR at 70MHz**
- **User-Programmable Adjustments and Feature Selection through an SPI™ Interface**
- **Selectable Data Bus (Dual CMOS or Single Multiplexed CMOS)**
- **DCLK Output and Programmable Data Output Timing Simplifies High-Speed Digital Interface**
- **Very Wide Input Common-Mode Voltage Range (0.4V to 1.4V)**
- **Very High Analog Input Bandwidth (> 850MHz)**
- **Single-Ended or Differential Analog Inputs**
- **Single-Ended or Differential Clock Input**
- **Divide-by-One (DIV1), Divide-by-Two (DIV2), and Divide-by-Four (DIV4) Clock Modes**
- **Two's Complement, Gray Code, and Offset Binary Output Data Format**
- **Out-of-Range Indicator (DOR)**
- **CMOS Output Internal Termination Options (Programmable)**
- **Reversible Bit Order (Programmable)**
- **Data Output Test Patterns**
- **Small 7mm x 7mm 48-Pin Thin QFN Package with Exposed Pad**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX19516ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

SPI is a trademark of Motorola, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual-Channel, 10-Bit, 100Msps ADC

ABSOLUTE MAXIMUM RATINGS

OVDD, AVDD to GND.....-0.3V to +3.6V
CMA, CMB, REFIO, INA+, INA-, INB+, INB- to GND .....-0.3V to +2.1V
CLK+, CLK-, SYNC, $\overline{SPEN}$, $\overline{CS}$, SCLK, SDIN to GND .....-0.3V to the lower of (V_{AVDD} + 0.3V) and +3.6V
DCLKA, DCLKB, D9A–D0A, D9B–D0B, DORA, DORB to GND.....-0.3V to the lower of (V_{OVDD} + 0.3V) and +3.6V

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN, 7mm x 7mm x 0.8mm (derate 40mW/°C above +70°C).....3200mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution				10		Bits
Integral Nonlinearity	INL	f_{IN} = 3MHz	-0.8	±0.25	+0.8	LSB
Differential Nonlinearity	DNL	f_{IN} = 3MHz	-0.7	±0.2	+0.7	LSB
Offset Error	OE	Internal reference	-0.4	±0.1	+0.4	%FS
Gain Error	GE	External reference = 1.25V	-1.5	±0.3	+1.5	%FS
ANALOG INPUTS (INA+, INA-, INB+, INB-) (Figure 3)						
Differential Input-Voltage Range	V_{DIFF}	Differential or single-ended inputs		1.5		V_{P-P}
Common-Mode Input-Voltage Range	V_{CM}	(Note 2)	0.4		1.4	V
Input Resistance	R_{IN}	Fixed resistance		> 100		kΩ
		Differential input resistance, common mode connected to inputs		4		
Input Current	I_{IN}	Switched capacitance input current, each input		54		µA
Input Capacitance	C_{PAR}	Fixed capacitance to ground, each input		0.7		pF
	C_{SAMPLE}	Switched capacitance, each input		1.2		
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		100			MHz
Minimum Clock Frequency	f_{CLK}				50	MHz
Data Latency		Figures 9, 10		9		Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Small-Signal Noise Floor	SSNF	f_{IN} = 70MHz, < -35dBFS		-60.3		dBFS
Signal-to-Noise Ratio	SNR	f_{IN} = 3MHz		60.1		dBFS
		f_{IN} = 70MHz	58.9	60.0		
		f_{IN} = 175MHz		59.7		
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{IN} = 3MHz		59.6		dB
		f_{IN} = 70MHz	58.3	59.5		
		f_{IN} = 175MHz		59.2		
Spurious-Free Dynamic Range (2nd and 3rd Harmonic)	SFDR1	f_{IN} = 3MHz		84		dBc
		f_{IN} = 70MHz	72.2	83		
		f_{IN} = 175MHz		80		
Spurious-Free Dynamic Range (4th and Higher Harmonics)	SFDR2	f_{IN} = 3MHz		82		dBc
		f_{IN} = 70MHz	74	82		
		f_{IN} = 175MHz		82		
Second Harmonic	HD2	f_{IN} = 3MHz		-84		dBc
		f_{IN} = 70MHz		-83	-72.2	
		f_{IN} = 175MHz		-80		
Third Harmonic	HD3	f_{IN} = 3MHz		-86		dBc
		f_{IN} = 70MHz		-86	-74	
		f_{IN} = 175MHz		-82		
Total Harmonic Distortion	THD	f_{IN} = 3MHz		-80		dBc
		f_{IN} = 70MHz		-79	-70.5	
		f_{IN} = 175MHz		-77		
Third-Order Intermodulation	IM3	f_{IN} = 70MHz ±1.5MHz, -7dBFS		-90		dBc
		f_{IN} = 175MHz ±2.5MHz, -7dBFS		-80		
Full-Power Bandwidth	FPBW			850		MHz
Aperture Delay	t_{AD}			850		ps
Aperture Jitter	t_{AJ}			0.3		ps_{RMS}
Overdrive Recovery Time		±10% beyond full scale		1		Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERCHANNEL CHARACTERISTICS						
Crosstalk		f_{INA} or f_{INB} = 70MHz at -1dBFS		95		dBc
		f_{INA} or f_{INB} = 175MHz at -1dBFS		85		
Gain Match		f_{IN} = 70MHz		±0.05		dB
Offset Match		f_{IN} = 70MHz		±0.1		%FSR
Phase Match		f_{IN} = 70MHz		±0.5		Degrees
ANALOG OUTPUTS (CMA, CMB)						
CMA, CMB Output Voltage	V_{COM}	Default programmable setting	0.85	0.9	0.95	V
INTERNAL REFERENCE						
REFIO Output Voltage	V_{REFOUT}		1.23	1.25	1.27	V
REFIO Temperature Coefficient	TC_{REF}			< ±60		ppm/°C
EXTERNAL REFERENCE						
REFIO Input-Voltage Range	V_{REFIN}			1.25 +5/ -10%		V
REFIO Input Resistance	R_{REFIN}			10 ±20%		kΩ
CLOCK INPUTS (CLK+, CLK-)—DIFFERENTIAL MODE						
Differential Clock Input Voltage				0.4 to 2.0		V_{P-P}
Differential Input Common-Mode Voltage		Self-biased		1.2		V
		DC-coupled clock signal		1.0 to 1.4		
Input Resistance	R_{CLK}	Differential, default		10		kΩ
		Differential, internal termination selected		100		Ω
		Common mode		9		kΩ
Input Capacitance	C_{CLK}	To ground, each input		3		pF
CLOCK INPUTS (CLK+, CLK-)—SINGLE-ENDED MODE (V_{CLK-} < 0.1V)						
Single-Ended Mode Selection Threshold (V_{CLK-})					0.1	V
Allowable Logic Swing (V_{CLK+})				0 - V_{AVDD}		V
Single-Ended Clock Input High Threshold (V_{CLK+})			1.5			V
Single-Ended Clock Input Low Threshold (V_{CLK+})					0.3	V
Input Leakage (CLK+)		V_{CLK+} = V_{AVDD} = 1.8V or 3.3V			+0.5	µA
		V_{CLK+} = 0V	-0.5			
Input Leakage (CLK-)		V_{CLK-} = 0V	-150		-50	µA
Input Capacitance (CLK+)				3		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (SYNC)						
Allowable Logic Swing				0 - V_{AVDD}		V
Sync Clock Input High Threshold			1.5			V
Sync Clock Input Low Threshold					0.3	V
Input Leakage		V_{SYNC} = V_{AVDD} = 1.8V or 3.3V			+0.5	µA
		V_{SYNC} = 0V	-0.5			
Input Capacitance				4.5		pF
DIGITAL INPUTS (SHDN, $\overline{SPEN}$)						
Allowable Logic Swing				0 - V_{AVDD}		V
Input High Threshold			1.5			V
Input Low Threshold					0.3	V
Input Leakage		V_{SHDN}/$V_{\overline{SPEN}}$ = V_{AVDD} = 1.8V or 3.3V			+0.5	µA
		V_{SHDN}/$V_{\overline{SPEN}}$ = 0V	-0.5			
Input Capacitance	C_{DIN}			3		pF
SERIAL-PORT INPUTS (SCLK, SDIN, $\overline{CS}$, where $\overline{SPEN}$ = 0V)—SERIAL-PORT CONTROL MODE						
Allowable Logic Swing				0 - V_{AVDD}		V
Input High Threshold			1.5			V
Input Low Threshold					0.3	V
Input Leakage		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = V_{AVDD} = 1.8V or 3.3V			+0.5	µA
		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = 0V	-0.5			
Input Capacitance	C_{DIN}			3		pF
SERIAL-PORT INPUTS (SCLK, SDIN, $\overline{CS}$, where $\overline{SPEN}$ = V_{AVDD})—PARALLEL CONTROL MODE (Figure 5)						
Input Pullup Current		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = V_{AVDD} = 1.8V	7	12	17	µA
		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = V_{AVDD} = 3.3V	16	21	26	
Input Pulldown Current		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = 0V, V_{AVDD} = 1.8V	-65	-50	-35	µA
		V_{SCLK}/V_{SDIN}/$V_{\overline{CS}}$ = 0V, V_{AVDD} = 3.3V	-105	-90	-75	
Open-Circuit Voltage	V_{OC}	V_{AVDD} = 1.8V	1.35	1.45	1.55	V
		V_{AVDD} = 3.3V	2.58	2.68	2.78	
DIGITAL OUTPUTS (75Ω, D0–D9 (A and B Channel), DCLKA, DCLKB, DORA, DORB)						
Output-Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 200µA	V_{OVDD} - 0.2			V
Three-State Leakage Current	I_{LEAK}	V_{OVDD} applied			+0.5	µA
		GND applied	-0.5			

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-MANAGEMENT CHARACTERISTICS						
Wake-Up Time from Shutdown	t_{WAKE}	Internal reference, C_{REFIO} = 0.1µF (10τ)		5		ms
Wake-Up Time from Standby	t_{WAKE}	Internal reference		15		µs
SERIAL-PORT INTERFACE TIMING (Note 2) (Figure 7)						
SCLK Period	t_{SCLK}		50			ns
SCLK to $\overline{CS}$ Setup Time	t_{CSS}		10			ns
SCLK to $\overline{CS}$ Hold Time	t_{CSH}		10			ns
SDIN to SCLK Setup Time	t_{SDS}	Serial-data write	10			ns
SDIN to SCLK Hold Time	t_{SDH}	Serial-data write	0			ns
SCLK to SDIN Output Data Delay	t_{SDD}	Serial-data read			10	ns
TIMING CHARACTERISTICS—DUAL BUS PARALLEL MODE (Figure 9) (Default Timing, see Table 5)						
Clock Pulse-Width High	t_{CH}			5.0		ns
Clock Pulse-Width Low	t_{CL}			5.0		ns
Clock Duty Cycle	t_{CH}/t_{CLK}			30 to 70		%
Data Delay After Rising Edge of CLK+	t_{DD}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	2.1	4.0	5.8	ns
		C_L = 10pF, V_{OVDD} = 3.3V		3.1		
Data to DCLK Setup Time	t_{SETUP}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	8.1	8.7		ns
Data to DCLK Hold Time	t_{HOLD}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	0.6	1.3		ns
TIMING CHARACTERISTICS—MULTIPLEXED BUS PARALLEL MODE (Figure 10) (Default Timing, see Table 5)						
Clock Pulse-Width High	t_{CH}			5.0		ns
Clock Pulse-Width Low	t_{CL}			5.0		ns
Clock Duty Cycle	t_{CH}/t_{CLK}			30 to 70		%
Data Delay After Rising Edge of CLK+	t_{DD}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	2.1	3.9	5.8	ns
		C_L = 10pF, V_{OVDD} = 3.3V		3.1		
Data to DCLK Setup Time	t_{SETUP}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	2.9	3.9		ns
Data to DCLK Hold Time	t_{HOLD}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	0.4	1.1		ns
DCLK Duty Cycle	t_{DCH}/t_{CLK}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	41	50	59	%
MUX Data Duty Cycle	t_{CHA}/t_{CLK}	C_L = 10pF, V_{OVDD} = 1.8V (Note 2)	41	50	59	%
TIMING CHARACTERISTICS—SYNCHRONIZATION (Figure 12)						
Setup Time for Valid Clock Edge	t_{SUV}	Edge mode (Note 2)	0.7			ns
Hold-Off Time for Invalid Clock Edge	t_{HO}	Edge mode (Note 2)	0.5			ns
Minimum Synchronization Pulse Width		Relative to input clock period		2		Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{AVDD}	Low-level V_{AVDD}	1.7		1.9	V
		High-level V_{AVDD} (regulator mode, invoked automatically)	2.3		3.5	
Digital Output Supply Voltage	V_{OVDD}		1.7		3.5	V
Analog Supply Current	I_{AVDD}	Dual channel		63	77	mA
		Single channel active		37		
		Standby mode		9.5	13	
		Power-down mode		0.65	0.9	
		Power-down mode, V_{AVDD} = 3.3V		1.6		
Analog Power Dissipation	P_{DA}	Dual channel		113	139	mW
		Dual channel, V_{AVDD} = 3.3V		208		
		Single channel active		67		
		Standby mode		17	24	
		Power-down mode		1.2	1.6	
		Power-down mode, V_{AVDD} = 3.3V		2.9		
Digital Output Supply Current	I_{OVDD}	Dual-channel mode, C_L = 10pF		20		mA
		Power-down mode		< 0.1		

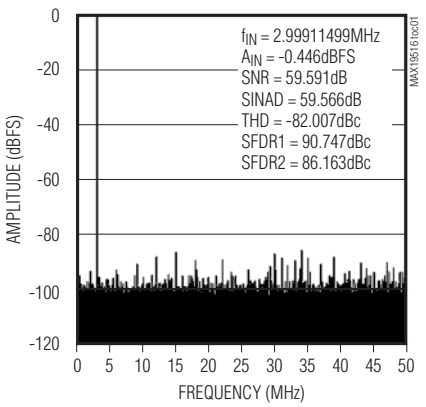
Note 1: Specifications ≥ +25°C guaranteed by production test, specifications < +25°C guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization.

Dual-Channel, 10-Bit, 100Msps ADC

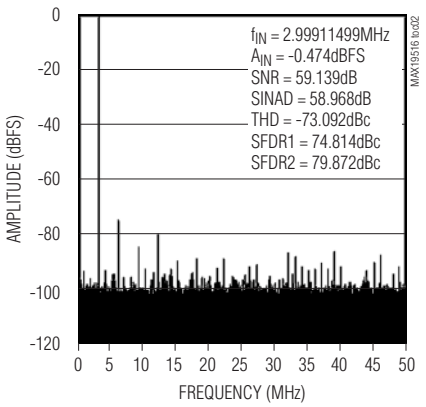
Typical Operating Characteristics

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = +25°C, unless otherwise noted.)

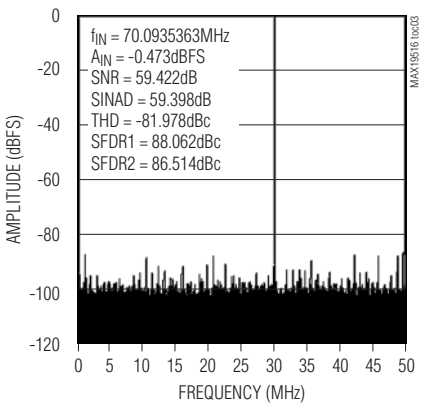
3MHz INPUT FFT PLOT



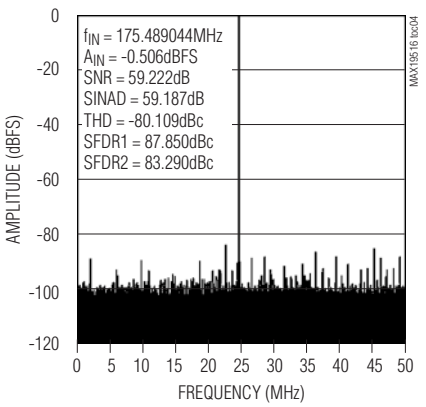
3MHz SINGLE-ENDED INPUT FFT PLOT



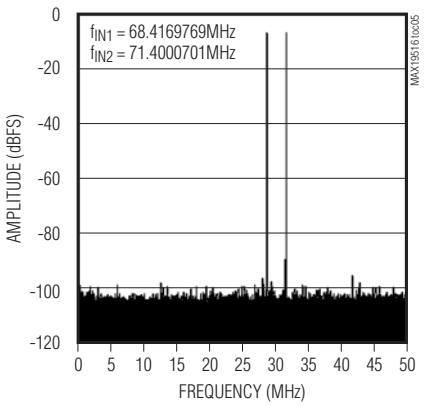
70MHz INPUT FFT PLOT



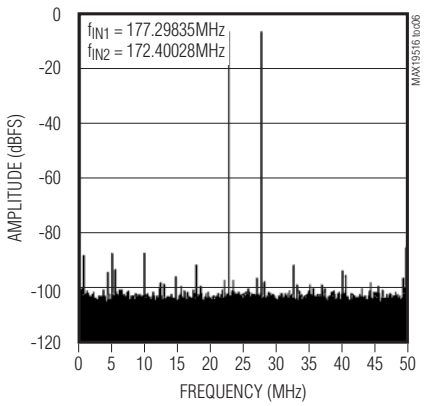
175MHz INPUT FFT PLOT



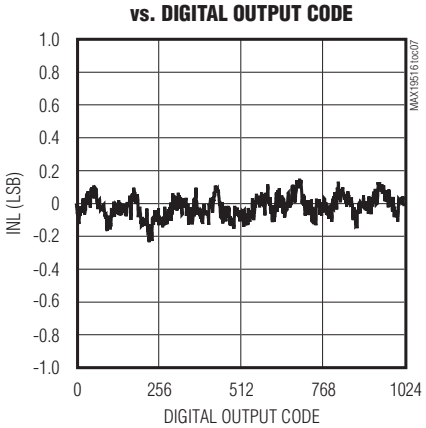
70MHz TWO-TONE IMD PLOT



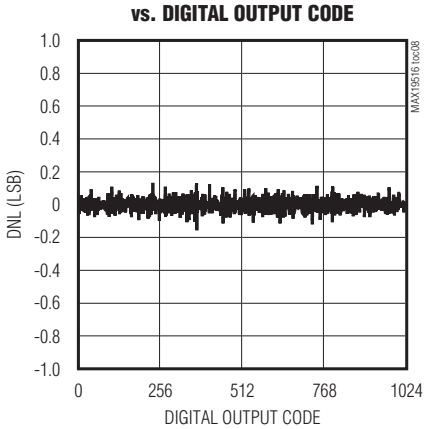
175MHz TWO-TONE IMD PLOT



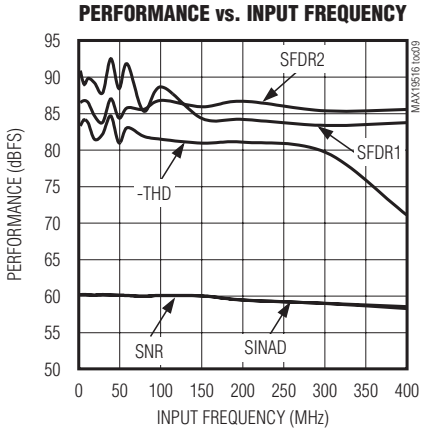
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



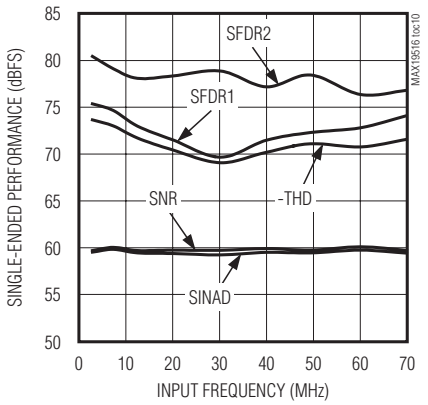
PERFORMANCE vs. INPUT FREQUENCY



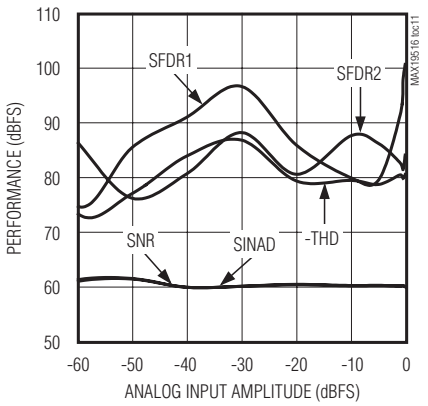
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = +25°C, unless otherwise noted.)

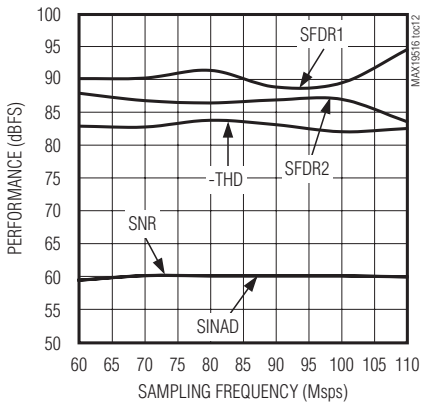
SINGLE-ENDED PERFORMANCE vs. INPUT FREQUENCY



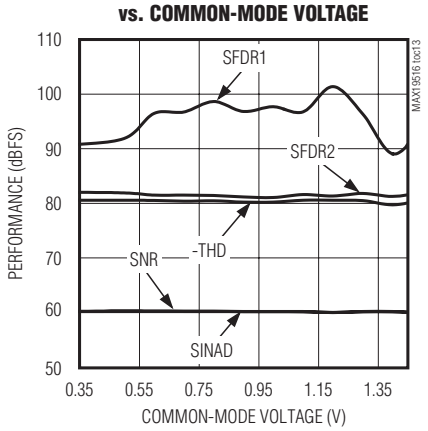
PERFORMANCE vs. ANALOG INPUT AMPLITUDE



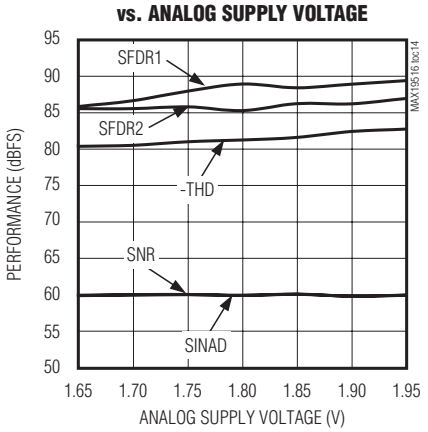
PERFORMANCE vs. SAMPLING FREQUENCY



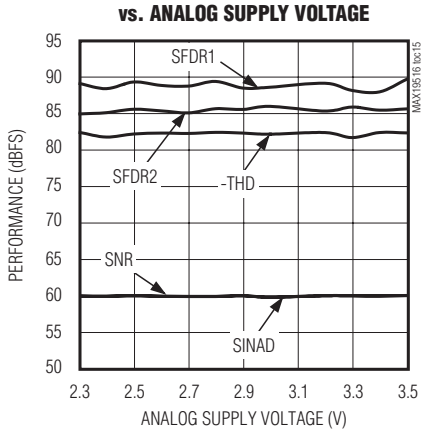
PERFORMANCE vs. COMMON-MODE VOLTAGE



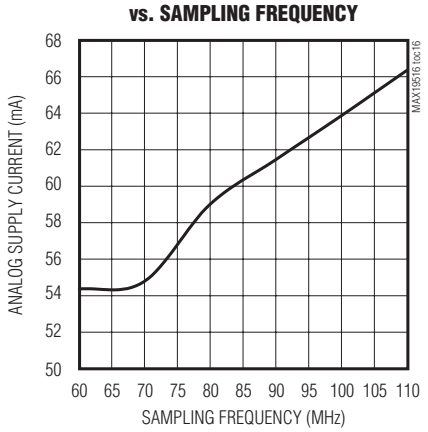
PERFORMANCE vs. ANALOG SUPPLY VOLTAGE



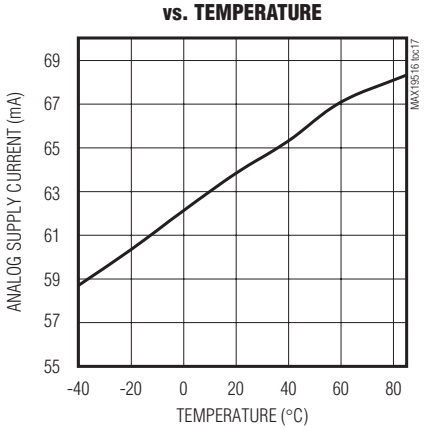
PERFORMANCE vs. ANALOG SUPPLY VOLTAGE



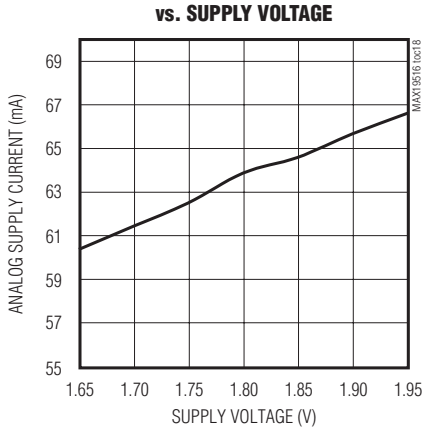
ANALOG SUPPLY CURRENT vs. SAMPLING FREQUENCY



ANALOG SUPPLY CURRENT vs. TEMPERATURE



ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE

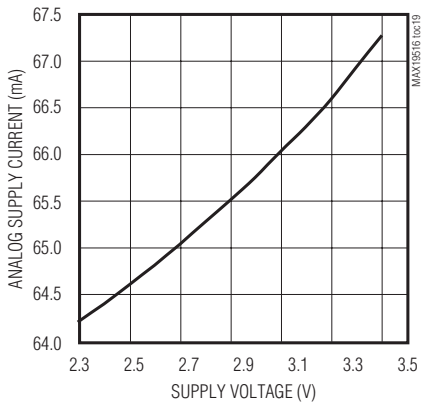


Dual-Channel, 10-Bit, 100Msps ADC

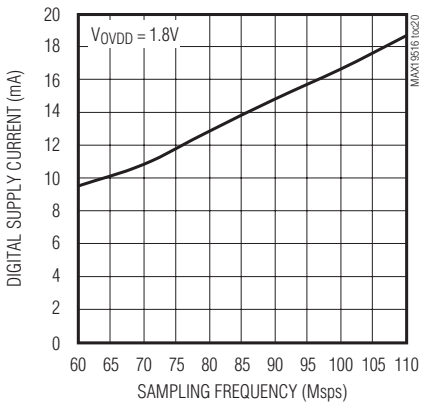
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = +25°C, unless otherwise noted.)

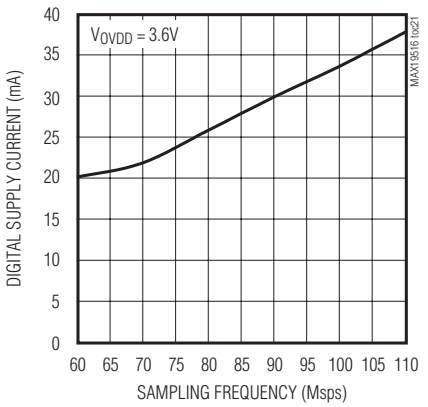
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



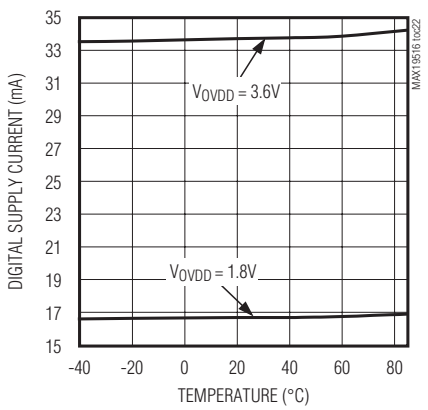
DIGITAL SUPPLY CURRENT vs. SAMPLING FREQUENCY



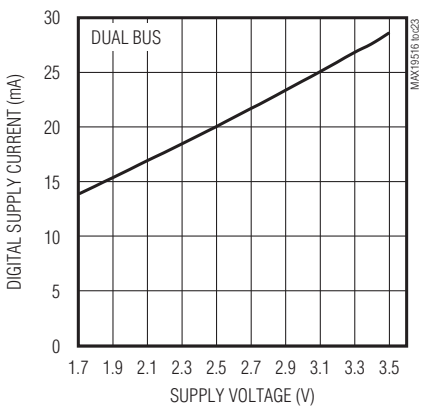
DIGITAL SUPPLY CURRENT vs. SAMPLING FREQUENCY



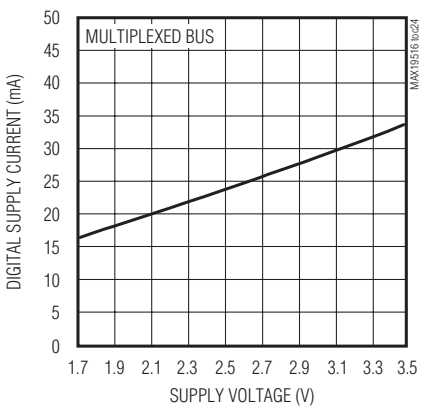
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



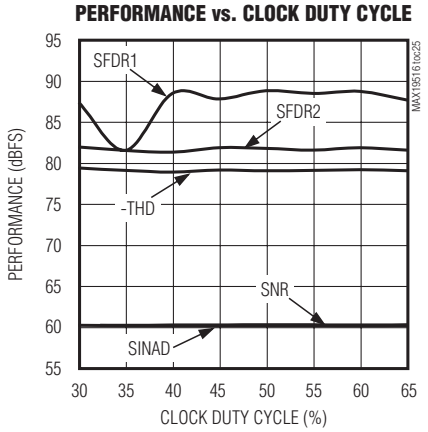
DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



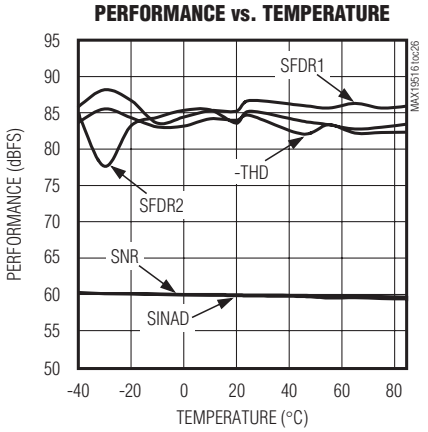
DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



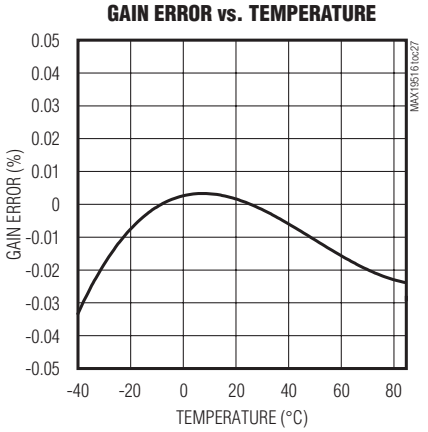
PERFORMANCE vs. CLOCK DUTY CYCLE



PERFORMANCE vs. TEMPERATURE



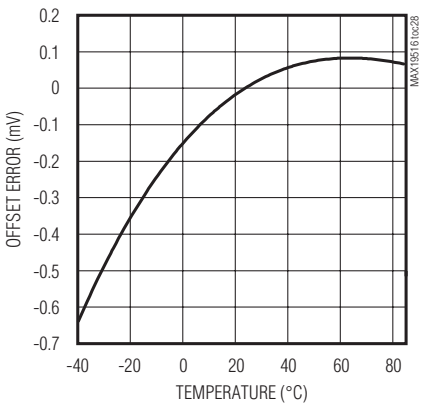
GAIN ERROR vs. TEMPERATURE



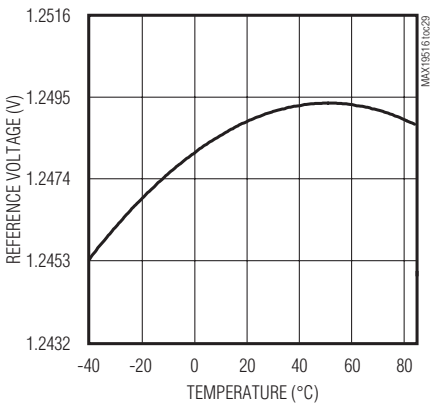
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{OVDD} = 1.8V, internal reference, differential clock, V_{CLK} = 1.5V_{P-P}, f_{CLK} = 100MHz, A_{IN} = -0.5dBFS, data output termination = 50Ω, T_A = +25°C, unless otherwise noted.)

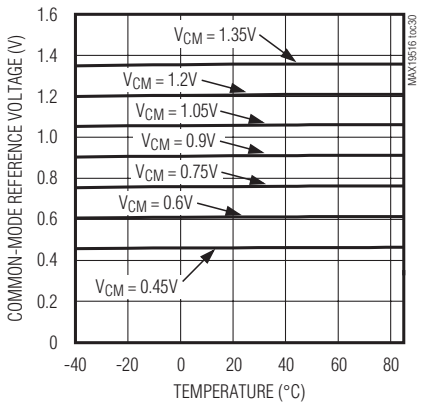
OFFSET ERROR vs. TEMPERATURE



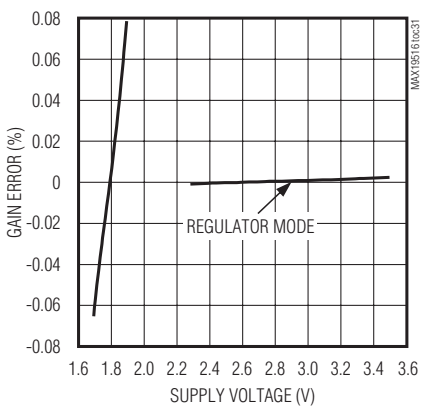
REFERENCE VOLTAGE vs. TEMPERATURE



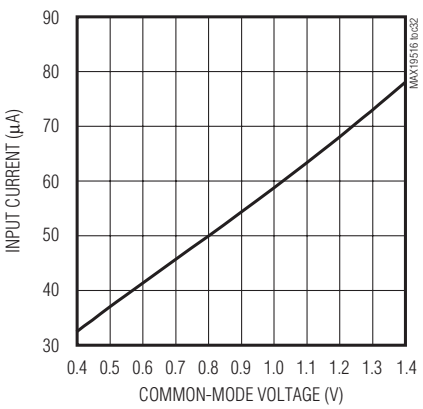
COMMON-MODE REFERENCE VOLTAGE vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



INPUT CURRENT vs. COMMON-MODE VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 48	AVDD	Analog Supply Voltage. Bypass each AVDD input pair (1, 48) and (12, 13) to GND with 0.1µF.
2	CMA	Channel A Common-Mode Input-Voltage Reference
3	INA+	Channel A Positive Analog Input
4	INA-	Channel A Negative Analog Input
5	$\overline{SPEN}$	Active-Low SPI Enable. Drive high to enable parallel programming mode.
6	REFIO	Reference Input/Output. To use internal reference, bypass to GND with a > 0.1µF capacitor. See the *Reference Input/Output (REFIO)* section for external reference adjustment.
7	SHDN	Active-High Power-Down. If $\overline{SPEN}$ is high (parallel programming mode), a register reset is initiated on the falling edge of SHDN.
8	I.C.	Internally Connected. Leave unconnected.
9	INB+	Channel B Positive Analog Input
10	INB-	Channel B Negative Analog Input
11	CMB	Channel B Common-Mode Input-Voltage Reference
14	SYNC	Clock-Divider Mode Synchronization Input
15	CLK+	Clock Positive Input
16	CLK-	Clock Negative Input. If CLK- is connected to ground, CLK+ is a single-ended logic-level clock input. Otherwise, CLK+/CLK- are self-biased differential clock inputs.
17, 18	GND	Ground. Connect all ground inputs and EP (exposed pad) together.
19	DORB	Channel B Data Over Range
20	DCLKB	Channel B Data Clock
21	D0B	Channel B Three-State Digital Output, Bit 0 (LSB)
22	D1B	Channel B Three-State Digital Output, Bit 1
23	D2B	Channel B Three-State Digital Output, Bit 2
24	D3B	Channel B Three-State Digital Output, Bit 3
25, 36	OVDD	Digital Supply Voltage. Bypass each OVDD input to GND with 0.1µF capacitor.
26	D4B	Channel B Three-State Digital Output, Bit 4
27	D5B	Channel B Three-State Digital Output, Bit 5
28	D6B	Channel B Three-State Digital Output, Bit 6
29	D7B	Channel B Three-State Digital Output, Bit 7
30	D8B	Channel B Three-State Digital Output, Bit 8
31	D9B	Channel B Three-State Digital Output, Bit 9 (MSB)
32	D0A	Channel A Three-State Digital Output, Bit 0 (LSB)
33	D1A	Channel A Three-State Digital Output, Bit 1
34	D2A	Channel A Three-State Digital Output, Bit 2
35	D3A	Channel A Three-State Digital Output, Bit 3
37	D4A	Channel A Three-State Digital Output, Bit 4
38	D5A	Channel A Three-State Digital Output, Bit 5
39	D6A	Channel A Three-State Digital Output, Bit 6

Pin Description (continued)

PIN	NAME	FUNCTION
40	D7A	Channel A Three-State Digital Output, Bit 7
41	D8A	Channel A Three-State Digital Output, Bit 8
42	D9A	Channel A Three-State Digital Output, Bit 9 (MSB)
43	DORA	Channel A Data Over Range
44	DCLKA	Channel A Data Clock
45	SDIN/FORMAT	SPI Data Input/Format. Serial-data input when $\overline{SPEN}$ is low. Output data format when $\overline{SPEN}$ is high.
46	SCLK/DIV	Serial Clock/Clock Divider. Serial clock when $\overline{SPEN}$ is low. Clock divider when $\overline{SPEN}$ is high.
47	$\overline{CS}$/OUTSEL	Serial-Port Select/Data Output Mode. Serial-port select when $\overline{SPEN}$ is low. Data output mode selection when $\overline{SPEN}$ is high.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance.

Detailed Description

The MAX19516 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. From input to output the total latency is 9 clock cycles. Each pipeline converter stage converts its input voltage to a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed on to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX19516 functional diagram.

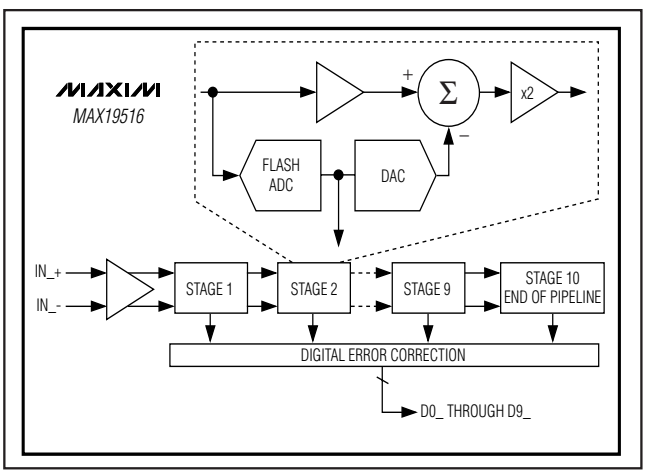


Figure 1. Pipeline Architecture—Stage Blocks

Analog Inputs and Common-Mode Reference

Apply the analog input signal to the analog inputs (INA+/INA- or INB+/INB-), which are connected to the input sampling switch (Figure 3). When the input sampling switch is closed, the input signal is applied to the sampling capacitors through the input switch resistance. The input signal is sampled at the instant the input switch opens. The pipeline ADC processes the sampled voltage and the digital output result is available 9 clock cycles later. Before the input switch is closed to begin the next sampling cycle, the sampling capacitors are reset to the input common-mode potential.

Common-mode bias can be provided externally or internally through 2kΩ resistors. In DC-coupled applications, the signal source provides the external bias and the bias current. In AC-coupled applications, the input current is supplied by the common-mode input voltage. For example, the input current can be supplied through the center tap of a transformer secondary winding. Alternatively, program the appropriate internal register through the serial-port interface to supply the input DC current through internal 2kΩ resistors (Figure 3). When the input current is supplied through the internal resistors, the input common-mode potential is reduced by the voltage drop across the resistors. The common-mode input reference voltage can be adjusted through programmable register settings from 0.45V to 1.35V in 0.15V increments. The default setting is 0.90V. Use this feature to provide a common-mode output reference to a DC-coupled driving circuit.

Dual-Channel, 10-Bit, 100Msps ADC

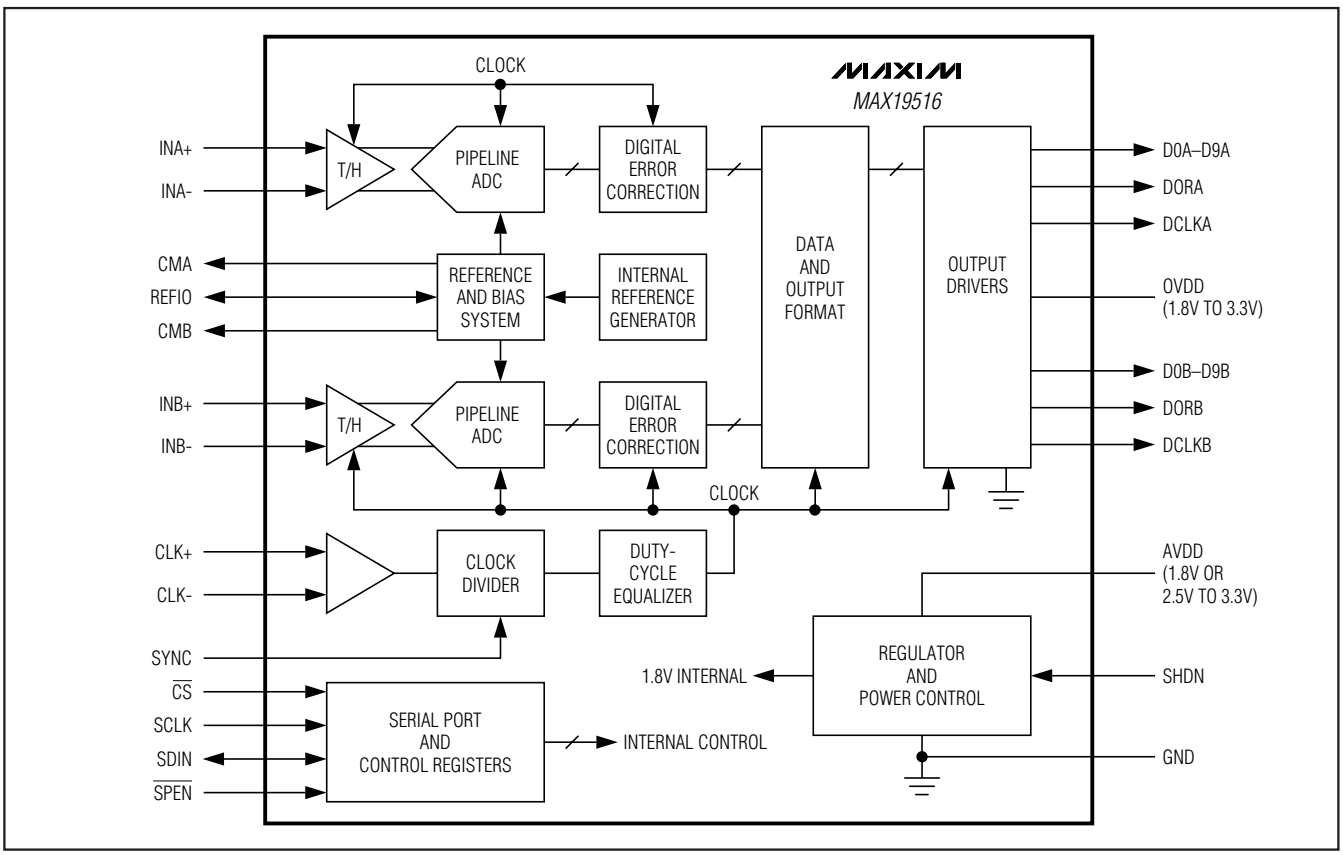


Figure 2. Functional Diagram

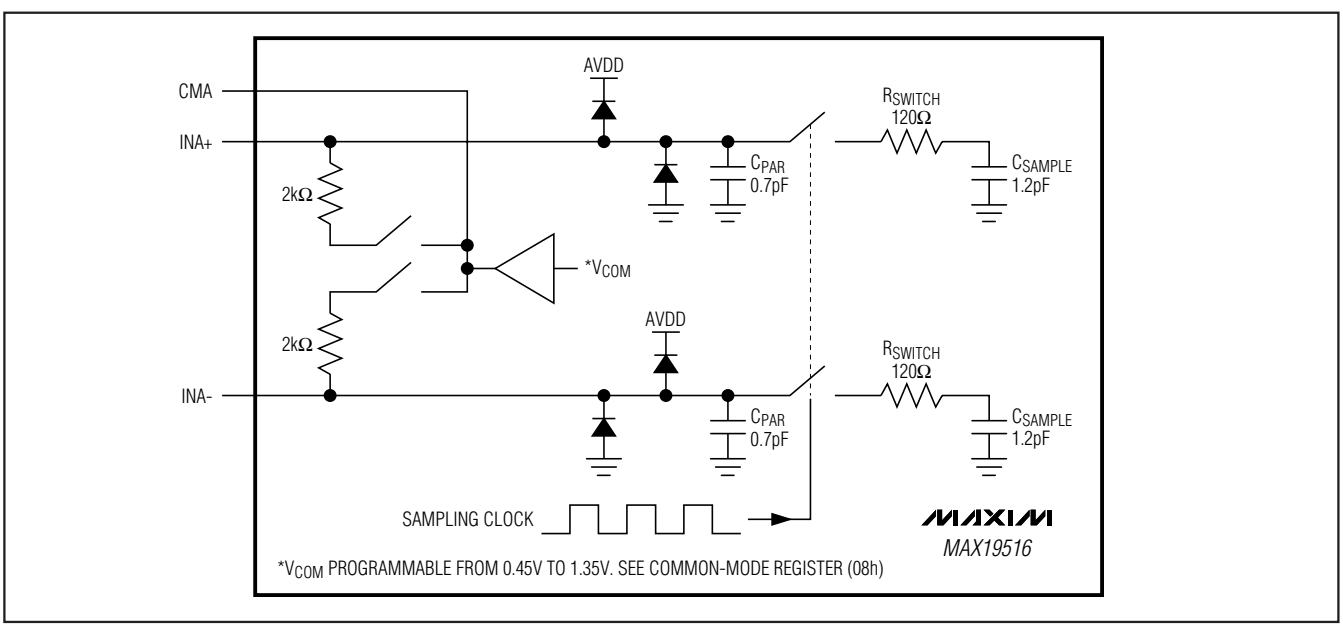


Figure 3. Internal Track-and-Hold (T/H) Circuit

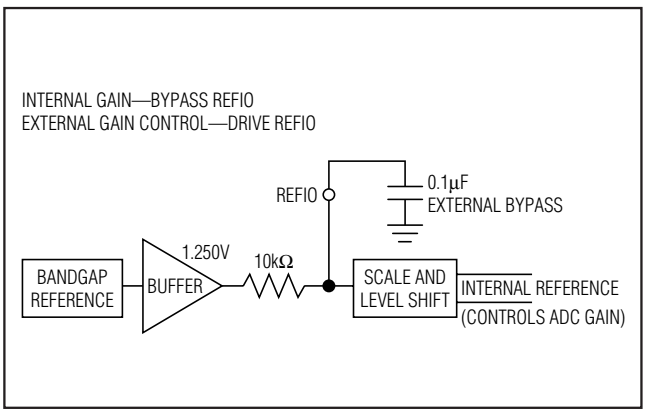


Figure 4. Simplified Reference Schematic

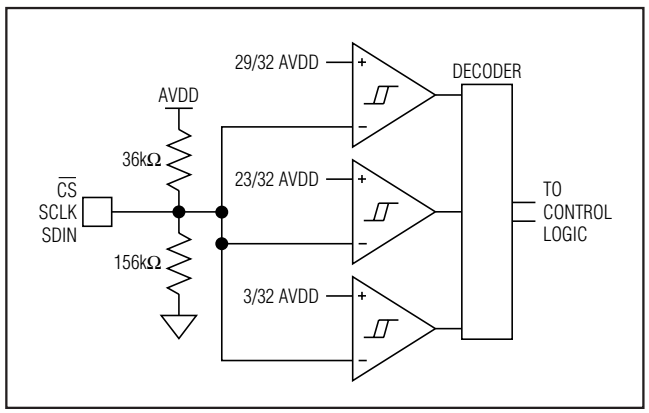


Figure 5. Simplified Parallel-Interface Input Schematic

Table 1. Parallel-Interface Pin Functionality

SPEN	SDIN/FORMAT	SCLK/DIV	CS/OUTSEL	DESCRIPTION
0	SDIN	SCLK	CS	SPI interface active. Features are programmed through the serial port (see the *Serial Programming Interface* section).
1	0	X	X	Two's complement
1	AVDD	X	X	Offset binary
1	Unconnected	X	X	Gray code
1	X	0	X	Clock divide-by-1
1	X	AVDD	X	Clock divide-by-2
1	X	Unconnected	X	Clock divide-by-4
1	X	X	0	CMOS (dual bus)
1	X	X	AVDD	MUX CMOS (channel A data bus)
1	X	X	Unconnected	MUX CMOS (channel B data bus)

X = Don't care.

Reference Input/Output (REFIO)

REFIO adjusts the reference potential, which, in turn, adjusts the full-scale range of the ADC. Figure 4 shows a simplified schematic of the reference system. An internal bandgap voltage generator provides an internal reference voltage. The bandgap potential is buffered and applied to REFIO through a 10kΩ resistor. Bypass REFIO with a 0.1µF capacitor to GND. The bandgap voltage is applied to a scaling and level-shift circuit, which creates internal reference potentials that establish the full-scale range of the ADC. Apply an external voltage on REFIO to trim the ADC full scale. The allowable adjustment range is +5/-15%. The REFIO-to-ADC gain transfer function is:

$$V_{FS} = 1.5 \times [V_{REFIO}/1.25] \text{ Volts}$$

Programming and Interface

There are two ways to control the MAX19516 operating modes. Full feature selection is available using the SPI interface, while the parallel interface offers a limited set of commonly used features. The programming mode is selected using the SPEN input. Drive SPEN low for SPI interface; drive SPEN high for parallel interface.

Parallel Interface

The parallel interface offers a pin-programmable interface with a limited feature set. Connect SPEN to AVDD to enable the parallel interface. See Table 1 for pin functionality; see Figure 5 for a simplified parallel-interface input schematic.

Dual-Channel, 10-Bit, 100Msps ADC

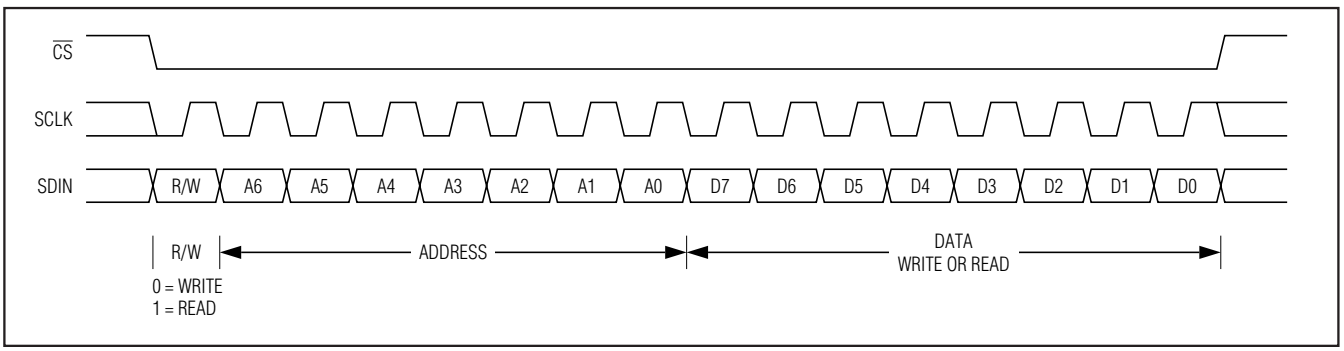


Figure 6. Serial-Interface Communication Cycle

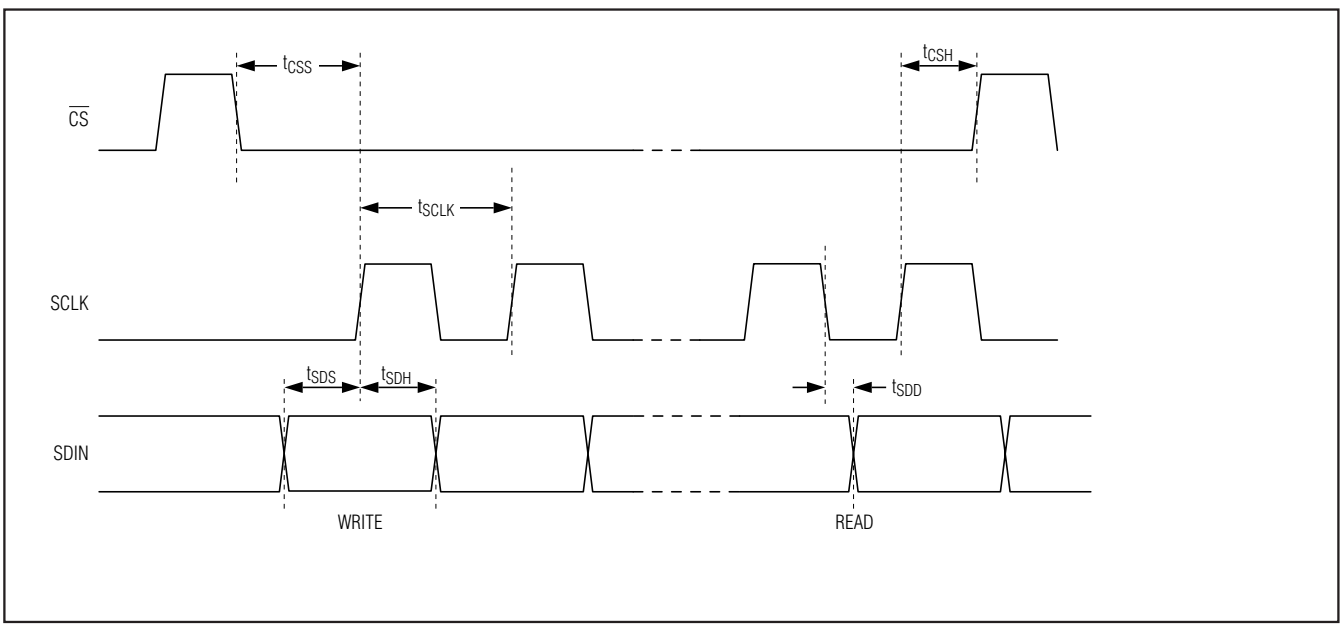


Figure 7. Serial-Interface Timing Diagram

Serial Programming Interface

A serial interface programs the MAX19516 control registers through the $\overline{CS}$, SDIN, and SCLK inputs. Serial data is shifted into SDIN on the rising edge of SCLK when $\overline{CS}$ is low. The MAX19516 ignores the data presented at SDIN and SCLK when $\overline{CS}$ is high. **$\overline{CS}$ must transition high after each read/write operation**. SDIN also serves as the serial-data output for reading control registers. The serial interface supports two-byte transfer in a communication cycle. The first byte is a control byte, containing the address and read/write instruction, written to the MAX19516. The second byte is a data byte and can be written to or read from the MAX19516.

Figure 6 shows a serial-interface communication cycle. The first SDIN bit clocked in establishes the communication cycle as either a write or read transaction (0 for write operation and 1 for read operation). The following 7 bits specify the address of the register to be written or read. The final 8 SDIN bits are the register data. All address and data bits are clocked in or out MSB first. During a read operation, the MAX19516 serial port drives read data (D7) into SDIN after the falling edge of SCLK following the 8th rising edge of SCLK. Since the minimum hold time on SDIN input is zero, the master can stop driving SDIN any time after the 8th rising edge of SCLK. Subsequent data bits are driven into SDIN on the falling edge of SCLK. Output data in a read operation is latched on the rising edge of SCLK. Figure 7 shows the detailed serial-interface timing diagram.

Register address 0Ah is a special-function register. Writing data 5Ah to register 0Ah initiates a register reset. When this operation is executed, all control registers are reset to default values. A read operation of register 0Ah returns a status byte with information described in Table 2.

Table 2. Register 0Ah Status Byte

BIT NO.	VALUE	DESCRIPTION
7	0	Reserved
6	0	Reserved
5	0 or 1	1 = ROM read in progress
4	0 or 1	1 = ROM read completed and register data is valid (checksum is OK)
3	0	Reserved
2	1	Reserved
1	0 or 1	Reserved
0	0 or 1	1 = Duty-cycle equalizer DLL is locked

User-Programmable Registers

Table 3. User-Programmable Registers

ADDRESS	POR DEFAULT	FUNCTION
00h	00000011	Power management
01h	00000000	Output format
02h	00000000	Digital output power management
03h	10110110	Data/DCLK timing
04h	00000000	CHA data output termination control
05h	00000000	CHB data output termination control
06h	00000000	Clock divide/data format/test pattern
07h	Reserved	Reserved—do not use
08h	00000000	Common mode
0Ah	—	Software reset

Power Management (00h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPS_SHDN1	STBY_SHDN1	CHB_ON_SHDN1	CHA_ON_SHDN1	HPS_SHDN0	STBY_SHDN0	CHB_ON_SHDN0	CHA_ON_SHDN0

The SHDN input (pin 7) toggles between any two power-management states. The Power Management register defines each power-management state. In the default state, SHDN = 1 shuts down the MAX19516 and SHDN = 0 returns to full power.

In addition to power management, the HPS_SHDN1 and HPS_SHDN0 activate an A+B adder mode. In this mode, the results from both channels are averaged. The MUX_CH bit selects which bus the (A+B)/2 data is presented.

Control Bits:

HPS_SHDN0	STBY_SHDN0	CHA_ON_SHDN0	CHB_ON_SHDN0	SHDN INPUT = 0*
HPS_SHDN1	**STBY_SHDN1**	**CHA_ON_SHDN1**	**CHB_ON_SHDN1**	**SHDN INPUT = 1****
X	0	0	0	Complete power-down
0	0	0	1	Channel B active, channel A full power-down
0	0	1	0	Channel A active, channel B full power-down
0	X	1	1	Channels A and B active
0	1	0	0	Channels A and B in standby mode
0	1	0	1	Channel B active, channel A standby
0	1	1	0	Channel A active, channel B standby
1	1	0	0	Channels A and B in standby mode
1	X	X	1	Channels A and B active, output is averaged
1	X	1	X	Channels A and B active, output is averaged

**HPS_SHDN0, STBY_SHDN0, CHA_ON_SHDN0, and CHB_ON_SHDN0 are active when SHDN = 0.*

***HPS_SHDN1, STBY_SHDN1, CHA_ON_SHDN1, and CHB_ON_SHDN1 are active when SHDN = 1.*

X = Don't care.

Note: *When HPS_SHDN_ = 1 (A+B adder mode), CHA_ON_SHDN_ and CHB_ON_SHDN_ must* ***BOTH*** *equal 0 for power-down or standby.*

Output Format (01h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	BIT_ORDER_B	BIT_ORDER_A	MUX_CH	MUX	0

Bit 7, 6, 5 Set to 0 for proper operation

Bit 4 BIT_ORDER_B: Reverse CHB output bit order
0 = Defined data bus pin order (default)
1 = Reverse data bus pin order

Bit 3 BIT_ORDER_A: Reverse CHA output bit order
0 = Defined data bus pin order (default)
1 = Reverse data bus pin order

Bit 2 MUX_CH: Multiplexed data bus selection
0 = Multiplexed data output on CHA (CHA data presented first, followed by CHB data) (default)
1 = Multiplexed data output on CHB (CHB data presented first, followed by CHA data)

Bit 1 MUX: Digital output mode
0 = Dual data bus output mode (default)
1 = Single multiplexed data bus output mode
MUX_CH selects the output bus

Bit 0 Set to 0 for proper operation

Digital Output Power Management (02h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	PD_DOUT_1	PD_DOUT_0	DIS_DOR	DIS_DCLK

Bit 7–4 Don't care

Bit 3, 2 PD_DOUT_1, PD_DOUT_0: Power-down digital output state control
00 = Digital output three state (default)
01 = Digital output low
10 = Digital output three state
11 = Digital output high

Bit 1 DIS_DOR: DOR driver disable
0 = DOR active (default)
1 = DOR disabled (three state)

Bit 0 DIS_DCLK: DCLK driver disable
0 = DCLK active (default)
1 = DCLK disabled (three state)

Data/DCLK Timing (03h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DA_BYPASS	DLY_HALF_T	DCLKTIME_2	DCLKTIME_1	DCLKTIME_0	DTIME_2	DTIME_1	DTIME_0

Bit 7 DA_BYPASS: Data aligner bypass

0 = Nominal

1 = Bypasses data aligner delay line to minimize output data latency with respect to the input clock. Rising clock to data transition is approximately 6ns with DTIME = 000b settings (default)

Bit 6 DLY_HALF_T: Data and DCLK delayed by T/2

0 = Normal, no delay (default)

1 = Delays data and DCLK outputs by T/2

Disabled in MUX data bus mode

Bit 5, 4, 3 DCLKTIME_2, DCLKTIME_1, DCLKTIME_0: DCLK timing adjust (controls both channels)

000 = Nominal

001 = +T/16

010 = +2T/16

011 = +3T/16

100 = Reserved, do not use

101 = -1T/16

110 = -2T/16 (default)

111 = -3T/16

Bit 2, 1, 0 DTIME_2, DTIME_1, DTIME_0: Data timing adjust (controls both channels)

000 = Nominal

001 = +T/16

010 = +2T/16

011 = +3T/16

100 = Reserved, do not use

101 = -1T/16

110 = -2T/16 (default)

111 = -3T/16

CHA Data Output Termination Control (04h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	CT_DCLK_2_A	CT_DCLK_1_A	CT_DCLK_0_A	CT_DATA_2_A	CT_DATA_1_A	CT_DATA_0_A

Bit 7, 6 Don't care

Bit 5, 4, 3 CT_DCLK_2_A, CT_DCLK_1_A, CT_DCLK_0_A: CHA DCLK termination control
000 = 50Ω (default)
001 = 75Ω
010 = 100Ω
011 = 150Ω
1xx = 300Ω

Bit 2, 1, 0 CT_DATA_2_A, CT_DATA_1_A, CT_DATA_0_A: CHA data output termination control
000 = 50Ω (default)
001 = 75Ω
010 = 100Ω
011 = 150Ω
1xx = 300Ω

CHB Data Output Termination Control (05h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	CT_DCLK_2_B	CT_DCLK_1_B	CT_DCLK_0_B	CT_DATA_2_B	CT_DATA_1_B	CT_DATA_0_B

Bit 7, 6 Don't care

Bit 5, 4, 3 CT_DCLK_2_B, CT_DCLK_1_B, CT_DCLK_0_B: CHB DCLK termination control
000 = 50Ω (default)
001 = 75Ω
010 = 100Ω
011 = 150Ω
1xx = 300Ω

Bit 2, 1, 0 CT_DATA_2_B, CT_DATA_1_B, CT_DATA_0_B: CHB data output termination control
000 = 50Ω (default)
001 = 75Ω
010 = 100Ω
011 = 150Ω
1xx = 300Ω

Clock Divide/Data Format/Test Pattern (06h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEST_PATTERN	TEST_DATA	FORMAT_1	FORMAT_0	TERM_100	SYNC_MODE	DIV1	DIV0

Bit 7 TEST_PATTERN: Test pattern selection

0 = Ramps from 0 to 1023 (offset binary) and repeats (subsequent formatting applied) (default)

1 = Data alternates between D[9:0] = 0101010101, DOR = 1, and D[9:0] = 1010101010, DOR = 0 on both channels

Bit 6 TEST_DATA: Data test mode

0 = Normal data output (default)

1 = Outputs test data pattern

Bit 5, 4 FORMAT_1, FORMAT_0: Data numerical format

00 = Two's complement (default)

01 = Offset binary

10 = Gray code

11 = Two's complement

Bit 3 TERM_100: Select 100Ω clock input termination

0 = No termination (default)

1 = 100Ω termination across differential clock inputs

Bit 2 SYNC_MODE: Divider synchronization mode select

0 = Slip mode (Figure 11) (default)

1 = Edge mode (Figure 12)

Bit 1, 0 DIV1, DIV0: Input clock-divider select

00 = No divider (default)

01 = Divide-by-2

10 = Divide-by-4

11 = No divider

Reserved (07h)—Do not write to this register

Common Mode (08h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMI_SELF_B	CMI_ADJ_2_B	CMI_ADJ_1_B	CMI_ADJ_0_B	CMI_SELF_A	CMI_ADJ_2_A	CMI_ADJ_1_A	CMI_ADJ_0_A

Bit 7 CMI_SELF_B: CHB connect input common-mode to analog inputs
0 = Internal common-mode voltage is NOT applied to inputs (default)
1 = Internal common-mode voltage applied to analog inputs through 2kΩ resistors

Bit 6, 5, 4 CMI_ADJ_2_B, CMI_ADJ_1_B, CMI_ADJ_0_B: CHB input common-mode voltage adjustment
000 = 0.900V (default)
001 = 1.050V
010 = 1.200V
011 = 1.350V
100 = 0.900V
101 = 0.750V
110 = 0.600V
111 = 0.450V

Bit 3 CMI_SELF_A: CHA connect input common-mode to analog inputs
0 = Internal common-mode voltage is NOT applied to inputs (default)
1 = Internal common-mode voltage applied to analog inputs through 2kΩ resistors

Bit 2, 1, 0 CMI_ADJ_2_A, CMI_ADJ_1_A, CMI_ADJ_0_A: CHA input common-mode adjustment
000 = 0.900V (default)
001 = 1.050V
010 = 1.200V
011 = 1.350V
100 = 0.900V
101 = 0.750V
110 = 0.600V
111 = 0.450V

Software Reset (0Ah)

Bit 7–0 SWRESET: Write 5Ah to initiate software reset

Dual-Channel, 10-Bit, 100Msps ADC

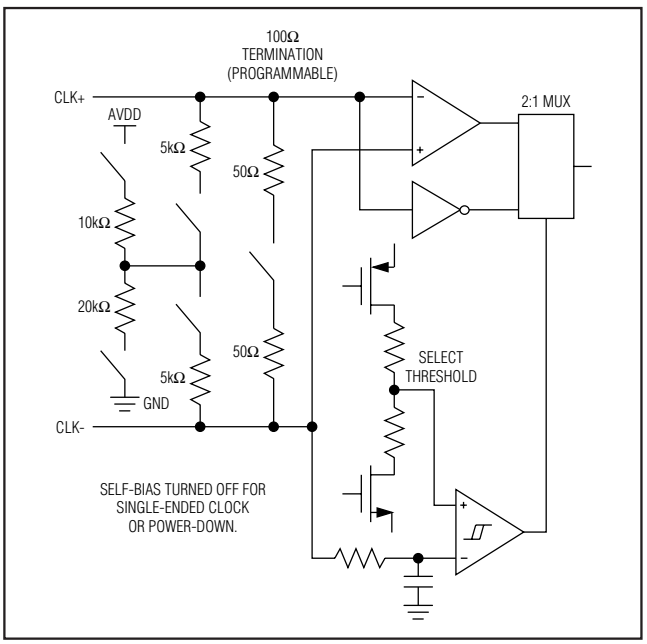


Figure 8. Simplified Clock Input Schematic

Clock Inputs

The input clock interface provides for flexibility in the requirements of the clock driver. The MAX19516 accepts a fully differential clock or single-ended logic-level clock. For differential clock operation, connect a differential clock to the CLK+ and CLK- inputs. In this mode, the input common mode is established internally to allow for AC-coupling. The differential clock signal can also be DC-coupled if the common mode is constrained to the specified 1V to 1.4V clock input common-mode range. For single-ended operation, connect CLK- to GND and drive the CLK+ input with a logic-level signal. When the CLK- input is grounded (or pulled below the threshold of the clock mode detection comparator) the differential-to-single-ended conversion stage is disabled and the logic-level inverter path is activated.

Clock Divider

The MAX19516 offers a clock-divider option. Enable clock division either by setting DIV0 and DIV1 through the serial interface; see the Clock Divide/Data

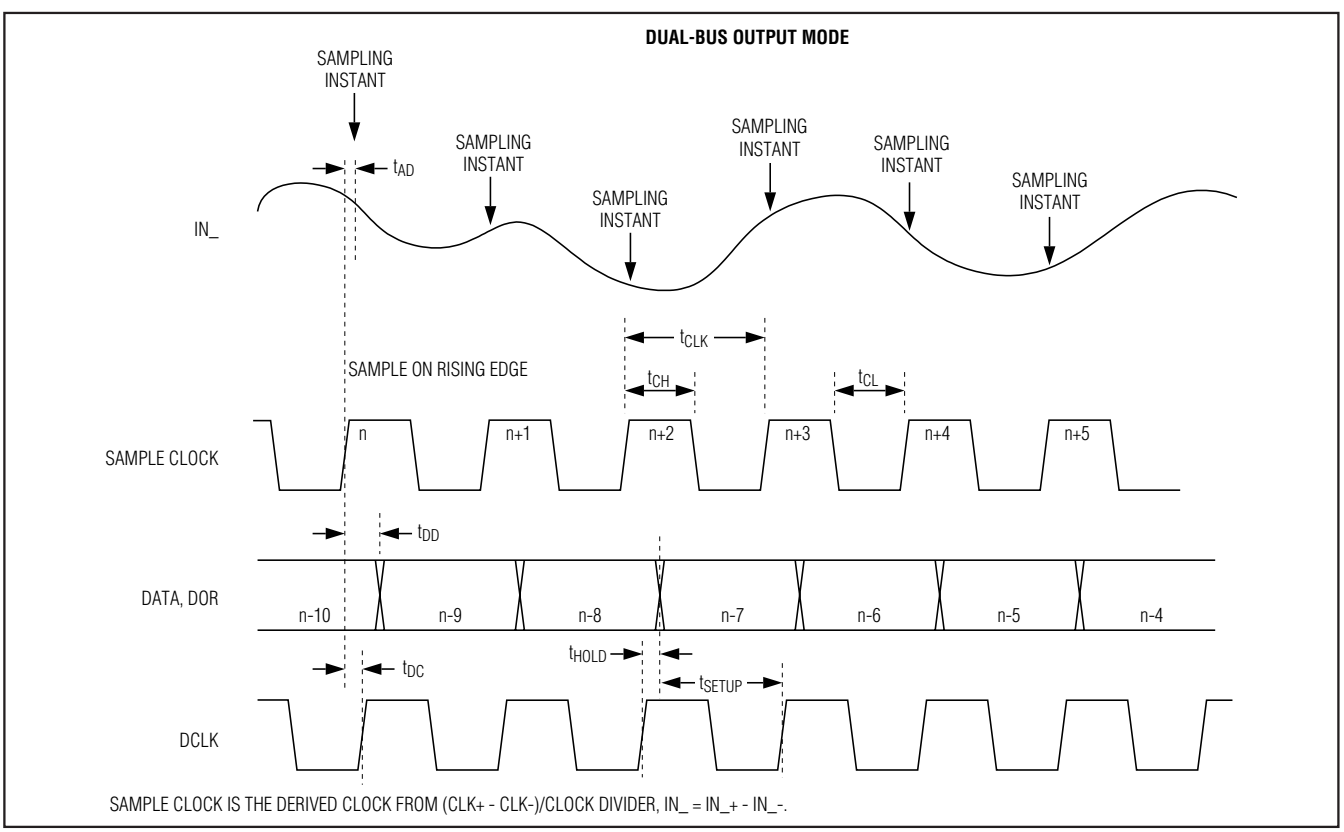


Figure 9. Dual-Bus Output Mode Timing

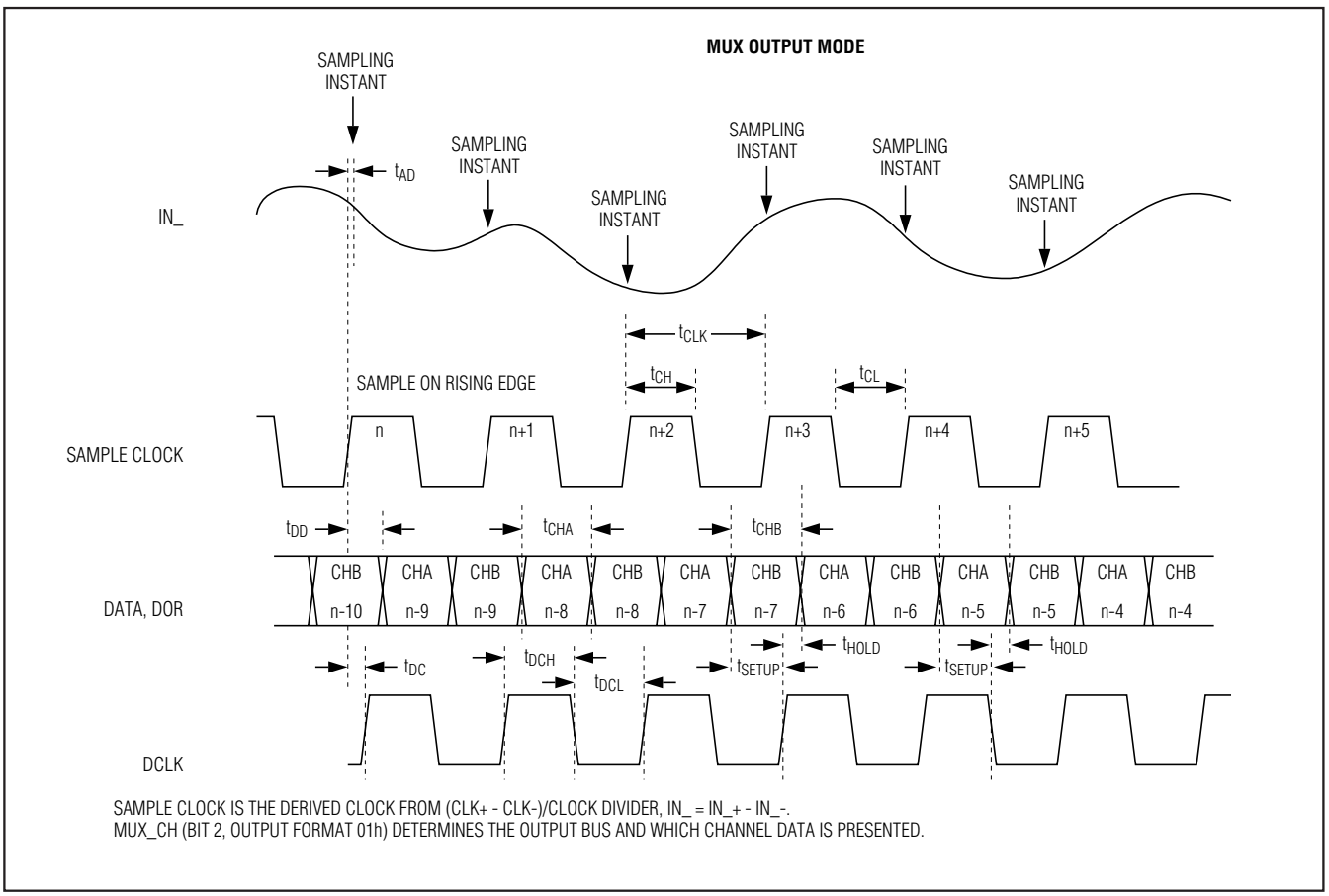


Figure 10. Multiplexed Output Mode Timing

Format/Test Pattern register (06h) for clock-divider options, or in parallel programming configuration ($\overline{SPEN}$ = 1) by using the DIV input.

System Timing Requirements

Figures 9 and 10 depict the relationship between the clock input and output, analog input, sampling event, and data output. The MAX19516 samples on the rising edge of the sampling clock. Output data is valid on the next rising edge of DCLK after a nine-clock internal latency. For applications where the clock is divided, the sample clock is the divided internal clock derived from:

[(CLK+ - CLK-)/DIVIDER]

Synchronization

When using the clock divider, the phase of the internal clock can be different than that of the FPGA, microcontroller, or other MAX19516s in the system. There are two mechanisms to synchronize the internal clock: slip synchronization and edge synchronization. Select the synchronization mode using SYNC_MODE (bit 2) in the Clock Divide/Data Format/Test Pattern register (06h) and drive the SYNC input high to synchronize.

Slip Synchronization Mode, SYNC_MODE = 0 (default): On the third rising edge of the input clock (CLK) after the rising edge of SYNC (provided set-up and hold times are met), the divided output is forced to skip a state transition (Figure 11).

Edge Synchronization Mode, SYNC_MODE = 1: On the third rising edge of the input clock (CLK) after the rising edge of SYNC (provided set-up and hold times are met), the divided output is forced to state 0. A divided clock rising edge occurs on the fourth (/2 mode) or fifth (/4 mode) rising edge of CLK, after a valid rising edge of SYNC (Figure 12).

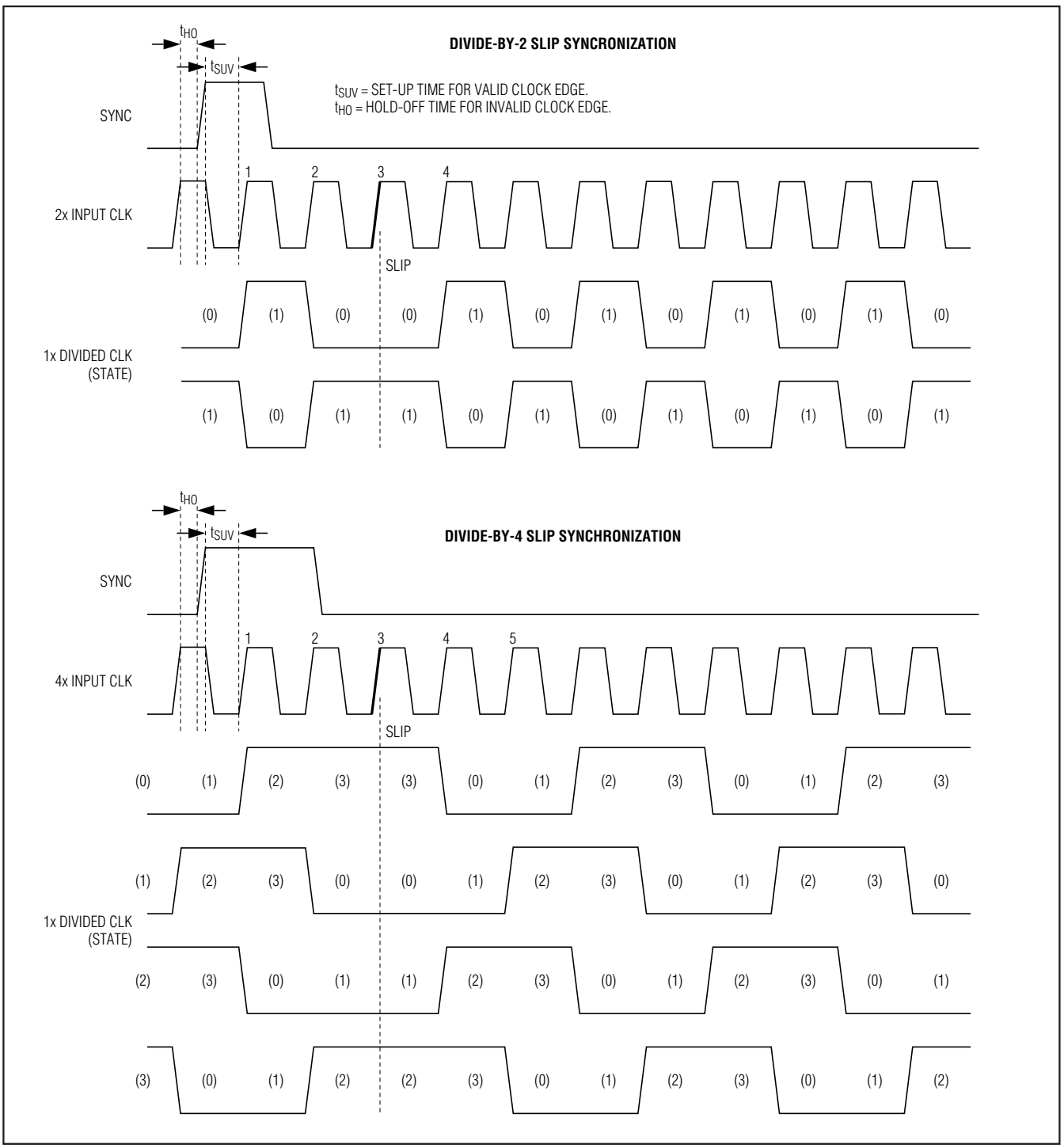


Figure 11. Slip Synchronization Mode

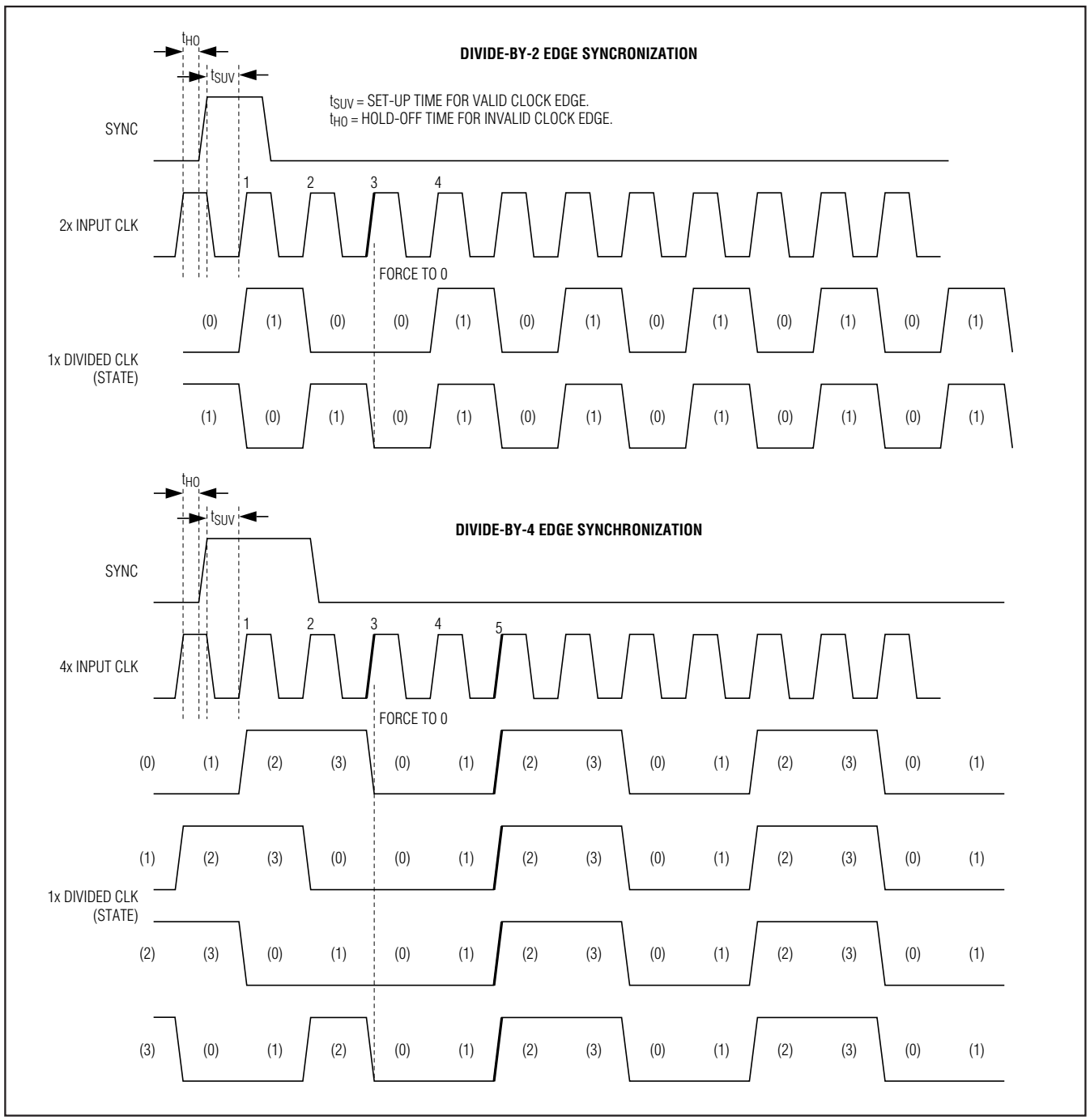


Figure 12. Edge Synchronization Mode

Table 4. Data Timing Controls

DATA TIMING CONTROL	DESCRIPTION
DA_BYPASS	Data aligner bypass. When this control is active (high), data and DCLK delay is reduced by approximately 3.4ns (relative to DA_BYPASS = 0).
DLY_HALF_T	When this control is active, data output is delayed by half clock period (T/2). This control does not delay data output if MUX mode is active.
DTIME<2:0>	Allows adjustment of data output delay in T/16 increments, where T is the sample clock period.
DCLKTIME<2:0>	Provides adjustment of DCLK delay in T/16 increments, where T is the sample clock period. When DTIME and DCLKTIME are adjusted to the same setting, the rising edge of DCLK occurs T/8 prior to data transitions.

Table 5. Data Timing Control Default Settings

DATA TIMING CONTROL	DEFAULT	DESCRIPTION
DA_BYPASS	1	Data aligner disabled
DLY_HALF_T	0	No delay
DTIME<2:0>	110	-2T/16 (1.25ns at 100Msps)
DCLKTIME<2:0>	110	-2T/16 (1.25ns at 100Msps)

Digital Outputs

The MAX19516 features a dual CMOS, multiplexable, reversible data bus. In parallel programming mode, configure the data outputs (D0_–D9_) for offset binary, two's complement, or gray code using the FORMAT input. Select multiplexed or dual-bus operation using the OUTSEL input. See the Output Format register (01h) for details on output formatting using the SPI interface. The SPI interface offers additional flexibility where D0_–D9_ are reversed, so the LSB appears at D9_ and the MSB at D0_. OVDD sets the output voltage; set OVDD between 1.8V and 3.3V. The digital outputs feature programmable output impedance from 50Ω to 300Ω. Set the output impedance for each bus using the CH_ Data Output Termination Control registers (04h and 05h).

Programmable Data Timing

The MAX19516 provides programmable data timing control to allow for optimization of timing characteristics to meet the system timing requirements. The timing adjustment feature also allows for ADC performance improvements by shifting the data output transition away from the sampling instant. The data timing control signals are summarized in Table 4. The default settings for timing adjustment controls are given in Table 5. Many applications will not require adjustment from the default settings.

The effects of the data timing adjustment settings are illustrated in Figures 13 and 14. The x axis is sampling rate and the y axis is data delay in units of clock period. The solid lines are the nominal data timing characteristics for the 14 available states of DTIME and DLY_HALF_T. The heavy line represents the nominal data timing characteristics for the default settings. Note that the default timing adjustment setting for the MAX19516 100Msps ADC results in an additional period of data latency.

Tables 6 and 7 show the recommended timing control settings versus sampling rate.

The nominal data timing characteristics versus sampling rate for these recommended timing adjustment settings are shown in Figures 15 and 16.

When DA_BYPASS = 1, the DCLKTIME delay setting must be equal to or less than the DTIME delay setting, as shown in Table 8.

Power Management

The SHDN input (pin 7) toggles between any two power-management states. The Power Management register (00h) defines each power-management state. In default state, SHDN = 1 shuts down the MAX19516 and SHDN = 0 returns to full power. Use of the SHDN input is not required for power management. For either state of SHDN, complete power-management flexibility is provided, including individual ADC channel power-management control, through the Power Management register (00h). The available reduced-power modes are shutdown and standby. In standby mode, the reference and duty-cycle equalizer circuits remain active for rapid wake-up time. In standby mode, the externally applied clock signal must remain active for the duty-cycle equalizer to remain locked. Typical wake-up time from standby mode is 15µs. In shutdown mode, all circuits are turned off except for the reference circuit required for the integrated self-sensing voltage regulator. If the regulator is active, there is additional supply current associated with the regulator circuit when the device is in shutdown. Typical wake-up time from shutdown mode is 5ms, which is dominated by the RC time constant on REFIO.

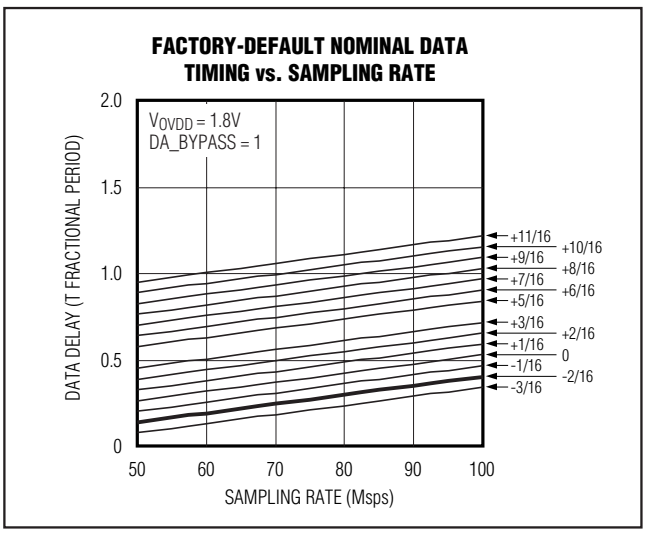


Figure 13. Default Data Timing (V_{OVDD} = 1.8V)

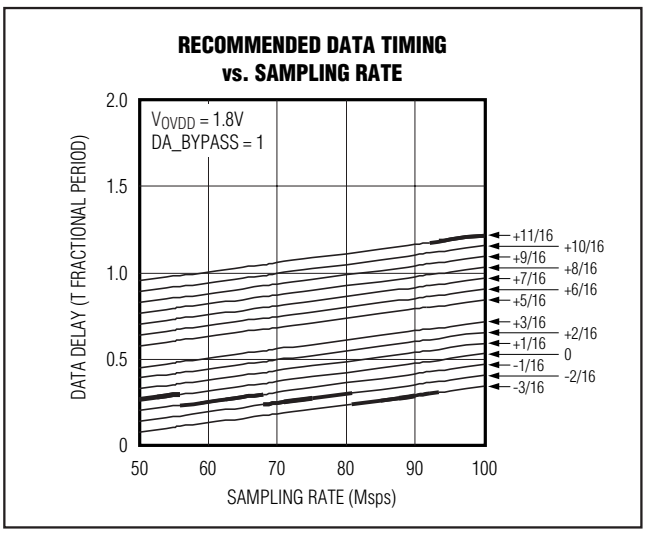


Figure 15. Recommended Data Timing (V_{OVDD} = 1.8V)

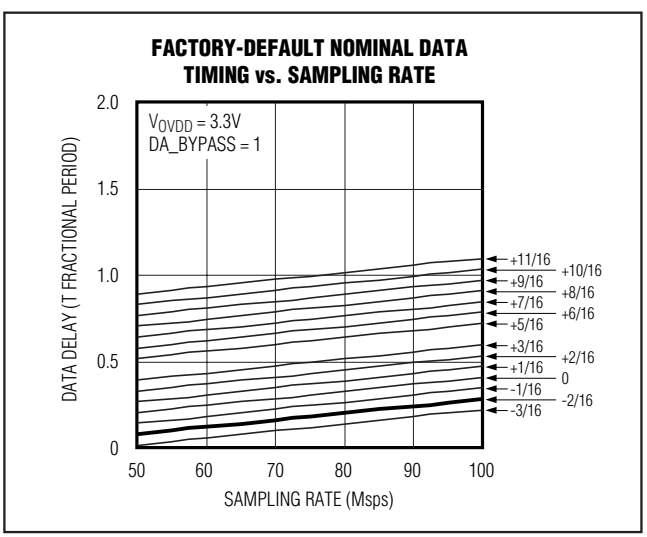


Figure 14. Default Data Timing (V_{OVDD} = 3.3V)

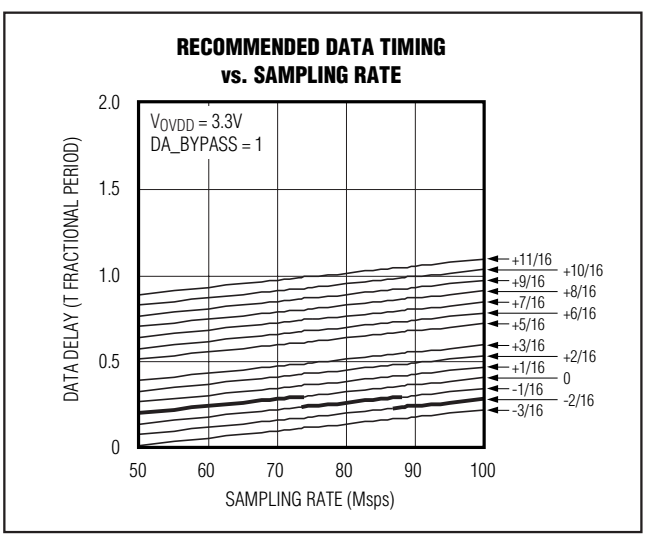


Figure 16. Recommended Data Timing (V_{OVDD} = 3.3V)

Table 6. Recommended Timing Adjustments (V_{OVDD} = 1.8V)

SAMPLING RATE (Msps)		V_{OVDD} = 1.8V			
FROM	TO	DA_BYPASS	DLY_HALF_T	DTIME<2:0>	DCLKTIME<2:0>
50	56	1	0	000	000
56	68	1	0	101	101
68	80	1	0	110	110
80	92	1	0	111	111
92	100	1	1	011	011

Table 7. Recommended Timing Adjustments (V_{OVDD} = 3.3V)

SAMPLING RATE (Msps)		V_{OVDD} = 3.3V			
FROM	TO	DA_BYPASS	DLY_HALF_T	DTIME<2:0>	DCLKTIME<2:0>
50	73	1	0	000	000
73	88	1	0	101	101
88	100	1	0	110	110

Table 8. Allowed Settings of DCLKTIME and DTIME for DA_BYPASS = 1

DTIME<2:0>	ALLOWED DCLKTIME<2:0> SETTINGS
111 (-3T/16)	111 (-3T/16)
110 (-2T/16)	110 (-2T/16); 111 (-3T/16)
101 (-1T/16)	101 (-1T/16); 110 (-2T/16); 111 (-3T/16)
000 (nominal)	000 (nominal); 101 (-1T/16); 110 (-2T/16); 111 (-3T/16)
001 (+1T/16)	001 (+1T/16); 000 (nominal); 101 (-1T/16); 110 (-2T/16); 111 (-3T/16)
010 (+2T/16)	010 (+2T/16); 001 (+1T/16); 000 (nominal); 101 (-1T/16); 110 (-2T/16); 111 (-3T/16)
011 (+3T/16)	011 (+3T/16); 010 (+2T/16); 001 (+1T/16); 000 (nominal); 101 (-1T/16); 110 (-2T/16); 111 (-3T/16)

Table 9. Reset Methods

RESET MODE	DESCRIPTION
Power-On Reset	Upon power-up (AVDD supply voltage and clock signal applied), the POR (power-on-reset) circuit initiates a register reset.
Software Reset	Write data 5Ah to address 0Ah to initiate register reset.
Hardware Reset	A register reset is initiated by the falling edge on the SHDN pin when $\overline{SPEN}$ is high.

Integrated Voltage Regulator

The MAX19516 includes an integrated self-sensing linear voltage regulator on the analog supply (AVDD). See Figure 17. When the applied voltage on AVDD is below 2V, the voltage regulator is bypassed, and the core analog circuitry operates from the externally applied voltage. If the applied voltage on AVDD is higher than 2V, the regulator bypass switches off, and voltage regulator mode is enabled. When in voltage regulation mode, the internal-core analog circuitry operates from a stable 1.8V supply voltage provided by the regulator. The regulator provides an output voltage of 1.8V over a 2.3V to 3.5V AVDD input-voltage range. Since the power-supply current is constant over this voltage range, analog power dissipation is proportional to the applied voltage.

Power-On and Reset

The user-programmable register default settings and other factory-programmed settings are stored in nonvolatile memory. Upon device power-up, these values are loaded into the control registers. This operation occurs after application of supply voltage to AVDD and application of an input clock signal. The register values are retained as long as AVDD is applied. While AVDD is applied, the registers can be reset, which will overwrite all user-programmed registers with the default values. This reset operation can be initiated by software command through the serial-port interface or by hardware control using the $\overline{SPEN}$ and SHDN inputs. The reset time is proportional to the ADC clock period and requires 85µs at 100Msps. Table 9 summarizes the reset methods.

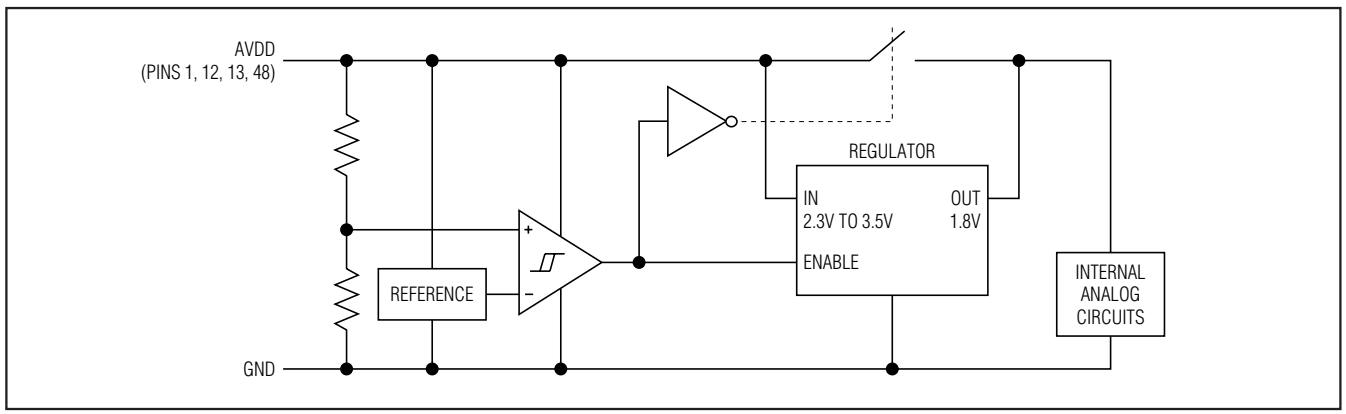


Figure 17. Integrated Voltage Regulator

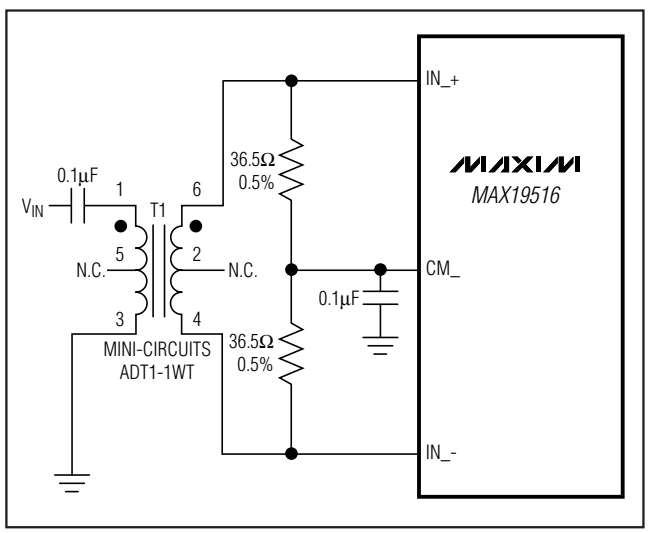


Figure 18. Transformer-Coupled Input Drive for Input Frequencies Up to Nyquist

Applications Information

Analog Inputs

Transformer-Coupled Differential Analog Input

The MAX19516 provides better SFDR and THD with fully differential input signals than a single-ended input drive. In differential input mode, even-order harmonics are lower as both inputs are balanced, and each of the ADC inputs only require half the signal swing compared to single-ended input mode.

An RF transformer (Figure 18) provides an excellent solution for converting a single-ended signal to a fully differential signal. Connecting the center tap of the transformer to CM_ provides a common-mode voltage. The transformer shown has an impedance ratio of 1:1.4. Alternatively, a different step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver can also improve the overall distortion. The configuration of Figure 18 is good for frequencies up to Nyquist ($f_{CLK}/2$).

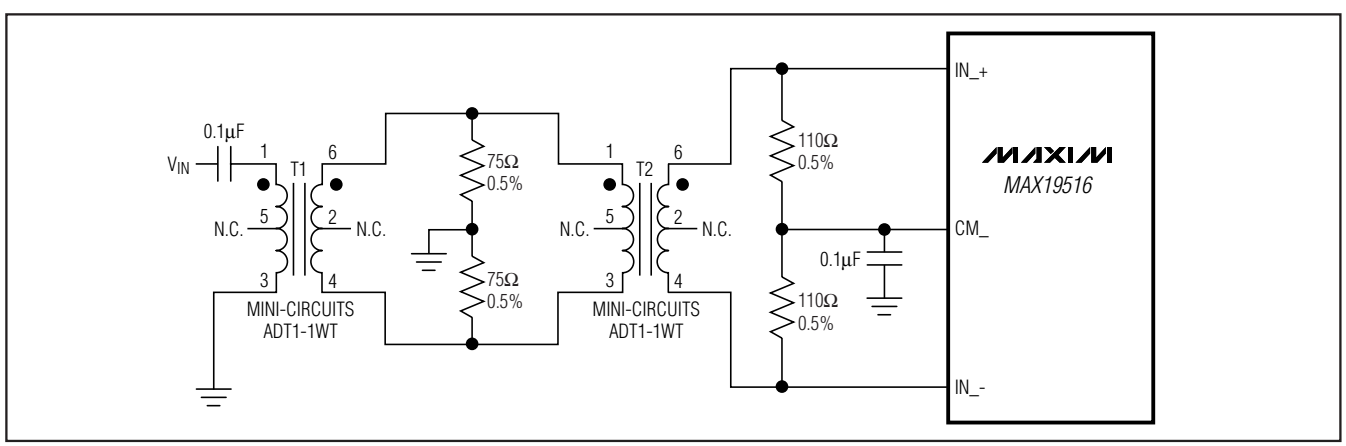


Figure 19. Transformer-Coupled Input Drive for Input Frequencies Beyond Nyquist

Dual-Channel, 10-Bit, 100Msps ADC

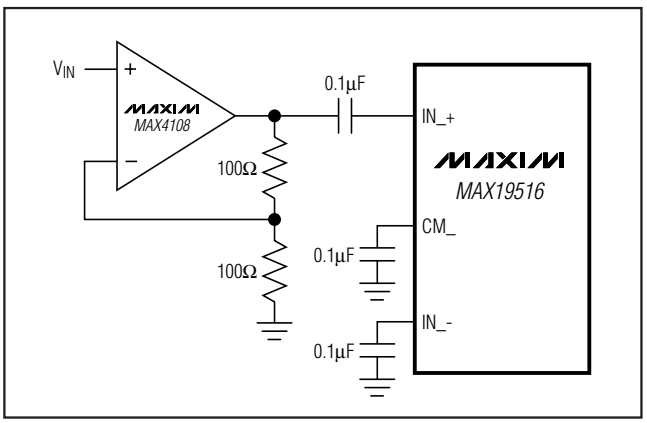


Figure 20. Single-Ended, AC-Coupled Input Drive

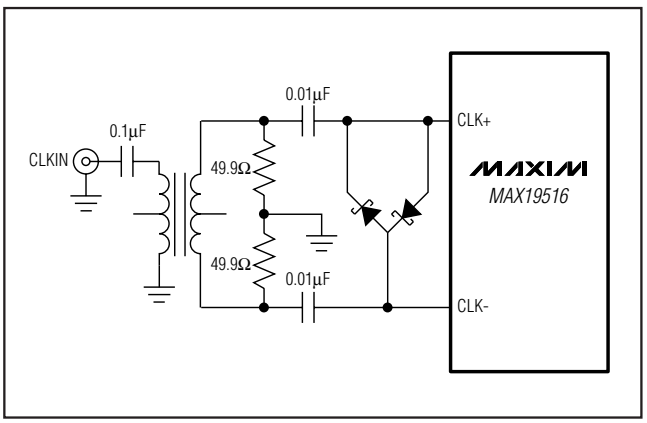


Figure 21. Single-Ended-to-Differential Clock Input

The circuit of Figure 19 also converts a single-ended input signal to a fully differential signal. Figure 19 utilizes an additional transformer to improve the common-mode rejection allowing high-frequency signals beyond the Nyquist frequency. A set of 75Ω and 110Ω termination resistors provide an equivalent 50Ω termination to the signal source. The second set of termination resistors connect to CM_ providing the correct input common-mode voltage.

Single-Ended AC-Coupled Input Signal

Figure 20 shows a single-ended, AC-coupled input application. The MAX4108 provides high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity. Bias voltage is applied to the inputs through internal 2kΩ resistors. See Common Mode register 08h for further details.

DC-Coupled Input

The MAX19516's wide common-mode voltage range (0.4V to 1.4V) allows DC-coupled signals. Ensure that the common-mode voltage remains between 0.4V and 1.4V.

Clock Input

Figure 21 shows a single-ended-to-differential clock input converting circuit.

Grounding, Bypassing, and Board-Layout Considerations

The MAX19516 requires high-speed board-layout design techniques. Locate all bypass capacitors as close as possible to the device, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass AVDD, OVDD, REFIO, CMA, and CMB with 0.1µF ceramic capacitors to GND. Multilayer boards with ground and power planes produce the highest level of signal integrity. Route high-speed digital signal traces away from the sensitive analog traces of either channel. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a best-fit straight line. Worst-case deviation is defined as INL.

Differential Nonlinearity (DNL)

DNL is the difference between the measured transfer function step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. DNL deviations are measured at each step of the transfer function and the worst-case deviation is defined as DNL.

Offset Error

Offset error is a parameter that indicates how well the actual transfer function matches the ideal transfer function at midscale. Ideally, the midscale transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the measured transfer function matches the slope of the ideal transfer function based on the specified full-scale input-voltage range. The gain error is defined as the relative error of the measured transfer function and is expressed as a percentage.

Small-Signal Noise Floor (SSNF)

SSNF is the integrated noise and distortion power in the Nyquist band for small-signal inputs. The DC offset is excluded from this noise calculation. For this converter, a small signal is defined as a single tone with an amplitude less than -35dBFS. This parameter captures the thermal and quantization noise characteristics of the converter and can be used to help calculate the overall noise figure of a receive channel. Refer to **www.maxim-ic.com** for application notes on Thermal + Quantization Noise Floor.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{[max]} = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise (e.g., thermal noise, reference noise, clock jitter, etc.). SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

$$SNR = 20 \times \log\left(\frac{SIGNAL_{RMS}}{NOISE_{RMS}}\right)$$

Signal-to-Noise and Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus the RMS distortion. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset. RMS distortion includes the first six harmonics (HD2–HD7).

$$SINAD = 20 \times \log\left(\frac{SIGNAL_{RMS}}{\sqrt{NOISE_{RMS}^2 + DISTORTION_{RMS}^2}}\right)$$

Single-Tone Spurious-Free Dynamic Range (SFDR1 and SFDR2)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS amplitude of the next largest spurious component, excluding DC offset. SFDR1 reflects the spurious performance based on worst 2nd-order or 3rd-order harmonic distortion. SFDR2 is defined by the worst spurious component excluding 2nd- and 3rd-order harmonics and DC offset.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude and V_2–V_7 are the amplitudes of the 2nd-order through 7th-order harmonics (HD2–HD7).

Third-Order Intermodulation (IM3)

IM3 is the total power of the third-order intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -7dBFS. The third-order intermodulation products are: $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$.

Aperture Delay

The input signal is sampled on the rising edge of the sampling clock. There is a small delay between the rising edge of the sampling clock and the actual sampling instant, which is defined as aperture delay (t_{AD}).

Aperture Jitter

Aperture jitter (t_{AJ}) is defined as the sample-to-sample time variation in the aperture delay.

Overdrive Recovery Time

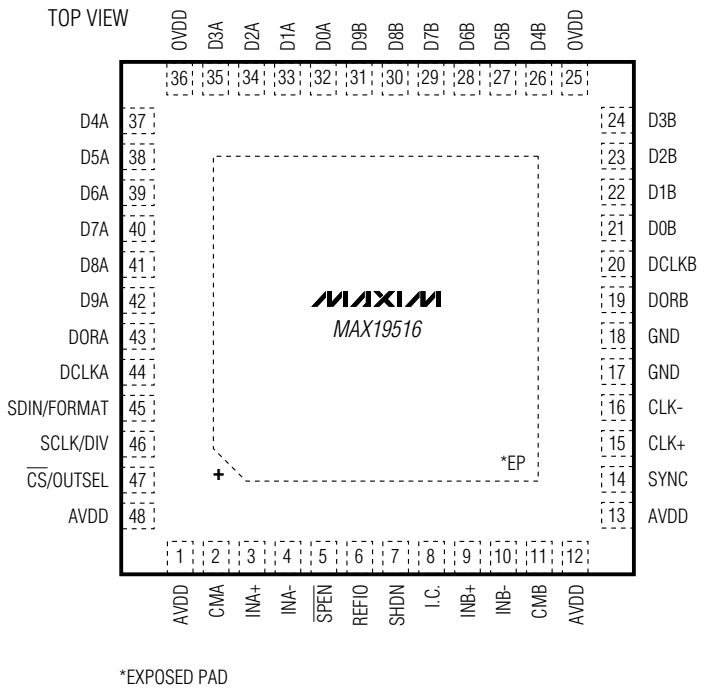
Overdrive recovery time is the time required for the ADC to recover from an input transient that exceeds the full-scale limits. The specified overdrive recovery time is measured with an input transient that exceeds the full-scale limits by ±10%.

Chip Information

PROCESS: CMOS

Dual-Channel, 10-Bit, 100Msps ADC

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	10/08	Corrected error in vertical scale for TOC 32	11
2	9/10	Updated timing characteristics due to CMOS output driver changes	5, 6, 28, 29, 30

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