MAX1968/MAX1969

Power Drivers for Peltier TEC Modules

General Description

The MAX1968/MAX1969 are highly integrated and cost-effective, high-efficiency, switch-mode drivers for Peltier thermoelectric cooler (TEC) modules. Both devices utilize direct current control to eliminate current surges in the TEC. On-chip FETs minimize external components while providing high efficiency. A 500kHz/1MHz switching frequency and a unique ripple cancellation scheme reduce component size and noise.

The MAX1968 operates from a single supply and provides bipolar ±3A output by biasing the TEC between the outputs of two synchronous buck regulators. Bipolar operation allows for temperature control without "dead zones" or other nonlinearities at low load currents. This arrangement ensures that the control system does not hunt when the set point is very close to the natural operating point, requiring a small amount of heating or cooling. An analog control signal precisely sets the TEC current. The MAX1969 provides unipolar output up to 6A. Reliability is optimized with settable limits for both TEC voltage and current, with independently set limits for heating and cooling current. An analog output also monitors TEC current.

The MAX1968/MAX1969 are available in a low-profile 28-pin TSSOP-EP package and is specified over the -40°C to +85°C temperature range. The thermally enhanced TSSOP-EP package with exposed metal pad minimizes operating junction temperature. An evaluation kit is available to speed designs.

Applications

Fiber Optic Laser Modules

WDM, DWDM Laser Diode Temperature Control

Fiber Optic Network Equipment

EDFA Optical Amplifiers

Telecom Fiber Interfaces

ATE

Biotech Lab Equipment

Pin Configuration and Functional Diagram appear at end of data sheet.

Benefits and Features

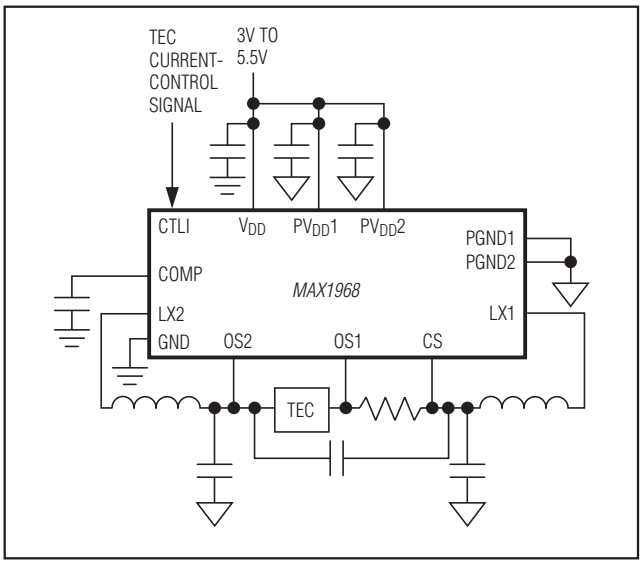
- High Accuracy and Adjustability Improves System Performance by Optimizing TEC Operation
  - Direct Current Control Prevents TEC Current Surges
  - Ripple Cancellation for Low Noise
  - No Dead-Zone or Hunting at Low-Output Current
  - 1% Accurate Voltage Reference
  - Adjustable TEC Voltage Limit
  - Separately Adjustable Heating and Cooling Current Limits
  - ITEC Output Provides Proportional Voltage to TEC Current for Monitoring
- High-Efficiency Switch-Mode Design
  - On-Chip Power MOSFETs Improve Efficiency While Reducing External Components
  - 500kHz/1MHz Switching Frequency
- Choose from ±3A Output Current (MAX1968) or 6A Output Current (MAX1969)
- Thermally Enhanced TSSOP-EP Package Minimizes Operating Junction Temperature

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1968EUI	-40°C to +85°C	28 TSSOP-EP*
MAX1969EUI	-40°C to +85°C	28 TSSOP-EP*

**EP = Exposed pad.*

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
$\overline{SHDN}$, MAXV, MAXIP, MAXIN, CTLI, FREQ to GND .....-0.3V to +6V
COMP, OS1, OS2, CS, REF, ITEC to GND .....-0.3V to (V_{DD} + 0.3V)
$PV_{DD}1$, $PV_{DD}2$ to GND .....-0.3V to (V_{DD} + 0.3V)
$PV_{DD}1$, $PV_{DD}2$ to V_{DD} .....-0.3V to +0.3V
PGND1, PGND2 to GND .....-0.3V to +0.3V
COMP, REF, ITEC Short to GND .....Indefinite
Peak LX Current (MAX1968) (Note 1).....±4.5A
Peak LX Current (MAX1969) (Note 1).....+9A
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP-EP (derate 23.8mW/°C above +70°C).....1.9W
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND and $PV_{DD}_$. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, PGND1 = PGND2 = FREQ = GND, CTLI = MAXV = MAXIP = MAXIN = REF, C_{REF} = 1µF, C_{COMP} = 0.1µF, $L_{LX_}$ = 3.3µH, C_{CS} = C_{OS2} = 1µF, I_{TEC} < $3A_{RMS}$ (MAX1968), I_{TEC} < $6A_{RMS}$ (MAX1969), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}			3.0		5.5	V
Output Voltage Range	V_{OUT}	V_{DD} = 5V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1968)		-4.3		+4.3	V
		V_{DD} = 5V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1969)				4.3	
		V_{DD} = 3V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1968)		-2.3		+2.3	
		V_{DD} = 3V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1969)				2.3	
Maximum TEC Current	$I_{TEC(MAX)}$	MAX1968				±3	A
		MAX1969				6	
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.485	1.500	1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = +10µA to -1mA			1.2	5	mV
Current-Sense Threshold Accuracy		V_{OS1} < V_{CS}	$V_{MAXI_}$ = V_{REF}	140	150	160	mV
			$V_{MAXI_}$ = V_{REF}/3	40	50	60	
		V_{OS1} > V_{CS}	$V_{MAXI_}$ = V_{REF}	140	150	160	
			$V_{MAXI_}$ = V_{REF}/3	40	50	60	
Switch-Fault Reset Voltage				50	150	250	mV
NFET On-Resistance	$R_{DS(ON-N)}$	V_{DD} = 5V, I = 0.5A			0.04	0.07	Ω
		V_{DD} = 3V, I = 0.5A			0.06	0.08	
PFET On-Resistance	$R_{DS(ON-P)}$	V_{DD} = 5V, I = 0.5A			0.06	0.10	Ω
		V_{DD} = 3V, I = 0.5A			0.09	0.12	
NFET Leakage	$I_{LEAK(N)}$	V_{LX} = V_{DD} = 5V, T_A = +25°C			0.02	10	µA
		V_{LX} = V_{DD} = 5V, T_A = +85°C			1		

Electrical Characteristics (continued)

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, PGND1 = PGND2 = FREQ = GND, CTLI = MAXV = MAXIP = MAXIN = REF, C_{REF} = 1µF, C_{COMP} = 0.01µF, $L_{LX_}$ = 3.3µH, C_{CS} = C_{OS2} = 1µF, I_{TEC} < $3A_{RMS}$ (MAX1968), I_{TEC} < $6A_{RMS}$ (MAX1969), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PFET Leakage	$I_{LEAK(P)}$	V_{LX} = 0, T_A = +25°C		0.02	10	µA
		V_{LX} = 0, T_A = +85°C		1		
No Load Supply Current	I_{DD} (NO LOAD)	V_{DD} = 5V		32	100	mA
		V_{DD} = 3.3V		20	30	
Shutdown Supply Current	I_{DD-SD}	V_{DD} = 5V (Note 2)		2	3	mA
Thermal Shutdown	$T_{SHUTDOWN}$	Hysteresis = 15°C		+165		°C
UVLO Threshold	V_{UVLO}	V_{DD} rising	2.4	2.6	2.8	V
		V_{DD} falling	2.25	2.5	2.75	
Switching Frequency Internal Oscillator	f_{SW-INT}	FREQ = GND	400	550	650	kHz
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0 or V_{DD}	-100		+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, I_{FREQ}	0 or V_{DD}	-5		+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V			V_{DD} x 0.25	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V	V_{DD} x 0.75			V
MAXV Threshold Accuracy		V_{MAXV} = V_{REF} x 0.67, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V	-2		+2	%
		V_{MAXV} = V_{REF} x 0.33, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V	-2		+2	%
MAXV, MAXIP, MAXIN Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	V_{MAXV} = $V_{MAXI_}$ = 0.1V or 1.5V	-0.1		+0.1	µA
CTLI Gain Accuracy	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 3)	9.5	10	10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF	0.5	1.0	2.0	MΩ
Error-Amp Transconductance	g_m		50	100	175	µA/V
ITEC Accuracy		V_{OS1} to V_{CS} = +100mV or -100mV	-10		+10	%
ITEC Load Regulation	ΔV_{ITEC}	V_{OS1} to V_{CS} = +100mV or -100mV, I_{ITEC} = ±10µA	-0.1		+0.1	%

Electrical Characteristics

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, PGND1 = PGND2 = FREQ = GND, CTLI = MAXV = MAXIP = MAXIN = REF, C_{REF} = 1µF, C_{COMP} = 0.1µF, $L_{LX_}$ = 3.3µH, C_{CS} = C_{OS2} = 1µF, I_{TEC} < $3A_{RMS}$ (MAX1968), I_{TEC} < $6A_{RMS}$ (MAX1969), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}			3.0		5.5	V
Output Voltage Range	V_{OUT}	V_{DD} = 5V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1968)		-4.3		+4.3	V
		V_{DD} = 5V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1969)				4.3	
		V_{DD} = 3V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1968)		-2.3		+2.3	
		V_{DD} = 3V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1969)				2.3	
Maximum TEC Current	$I_{TEC(MAX)}$	MAX1968				±3	A
		MAX1969				6	
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.475		1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = +10µA to -1mA				5	mV
Current-Sense Threshold Accuracy		V_{OS1} < V_{CS}	$V_{MAXI_}$ = V_{REF}	135		165	mV
			$V_{MAXI_}$ = V_{REF} / 3	35		65	
		V_{OS1} > V_{CS}	$V_{MAXI_}$ = V_{REF}	135		165	
			$V_{MAXI_}$ = V_{REF} / 3	35		65	
Switch-Fault Reset Voltage				50		250	mV
NFET On-Resistance	$R_{DS(ON-N)}$	V_{DD} = 5V, I = 0.5A				0.07	Ω
		V_{DD} = 3V, I = 0.5A				0.08	
PFET On-Resistance	$R_{DS(ON-P)}$	V_{DD} = 5V, I = 0.5A				0.07	Ω
		V_{DD} = 3V, I = 0.5A				0.12	
NFET Leakage	$I_{LEAK(N)}$	V_{LX} = V_{DD} = 5V, T_A = +25°C				10	µA
		V_{LX} = V_{DD} = 5V, T_A = -40°C				10	
PFET Leakage	$I_{LEAK(P)}$	V_{LX} = 0, T_A = +25°C				10	µA
		V_{LX} = 0, T_A = -40°C				10	
No Load Supply Current	$I_{DD(NO\ LOAD)}$	V_{DD} = 5V				100	mA
		V_{DD} = 3.3V				30	
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = GND, V_{DD} = 5V (Note 2)				3	mA
UVLO Threshold	V_{UVLO}	V_{DD} rising		2.4		2.8	V
		V_{DD} falling		2.25		2.75	
Switching-Frequency Internal Oscillator	f_{SW-INT}	FREQ = GND		400		650	kHz

Electrical Characteristics (continued)

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, PGND1 = PGND2 = FREQ = GND, CTLI = MAXV = MAXIP = MAXIN = REF, C_{REF} = 1µF, C_{COMP} = 0.01µF, $L_{LX_}$ = 3.3µH, C_{CS} = C_{OS2} = 1µF, I_{TEC} < $3A_{RMS}$ (MAX1968), I_{TEC} < $6A_{RMS}$ (MAX1969), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0 or V_{DD}	-100		+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, I_{FREQ}	0 or V_{DD}	-5		+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V			V_{DD} x 0.25	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V	V_{DD} x 0.75			
MAXV Threshold Accuracy		V_{MAXV} = V_{REF} x 0.67, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V	-2		+2	%
		V_{MAXV} = V_{REF} x 0.33, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V				
MAXV, MAXIP, MAXIN Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	V_{MAXV} = $V_{MAXI_}$ = 0.1V or 1.5V	-0.1		+0.1	µA
CTLI Gain Accuracy	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 3)	9.5		10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF	0.5		2.0	MΩ
Error-Amp Transconductance	g_m		50		175	µA/V
ITEC Accuracy		V_{OS1} to V_{CS} = +100mV or -100mV	-10		+10	%

Note 2: Includes power FET leakage.

Note 3: CTLI Gain is defined as:

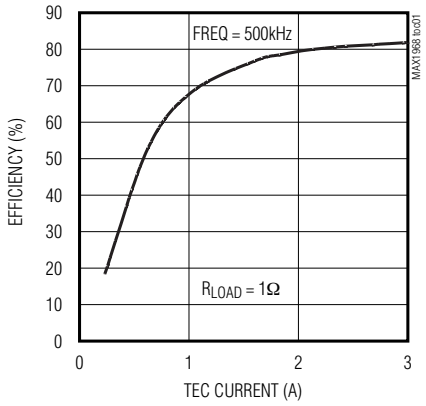
$$A_{CTLI} = \frac{(V_{CTLI} - V_{REF})}{V_{OS1} - V_{CS}}$$

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

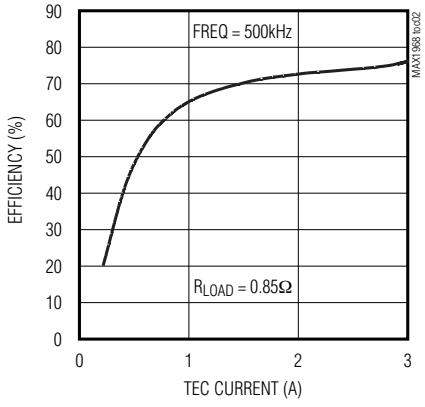
Typical Operating Characteristics

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, R_{LOAD} = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

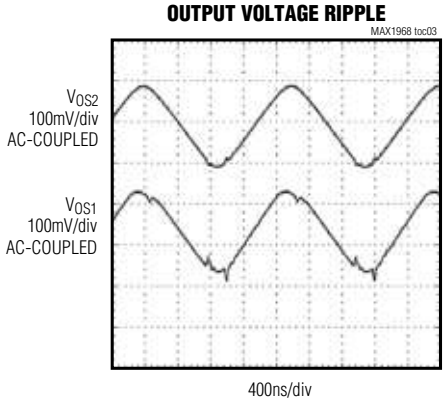
EFFICIENCY vs. TEC CURRENT
V_{DD} = 5V



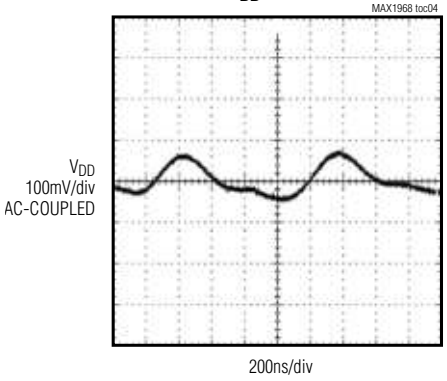
EFFICIENCY vs. TEC CURRENT
V_{DD} = 3.3V



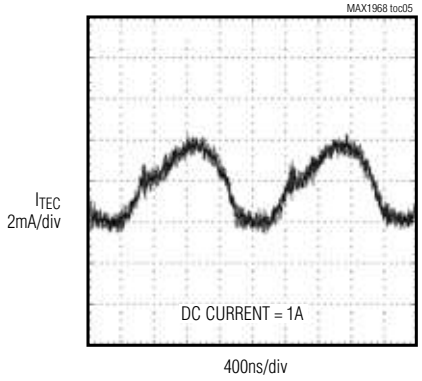
OUTPUT VOLTAGE RIPPLE



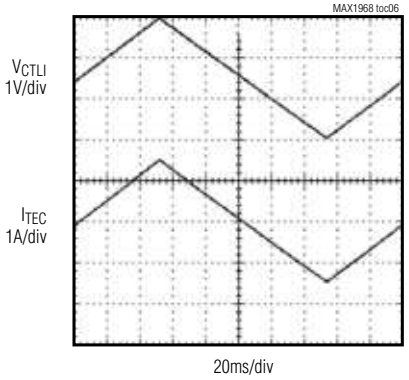
V_{DD} RIPPLE



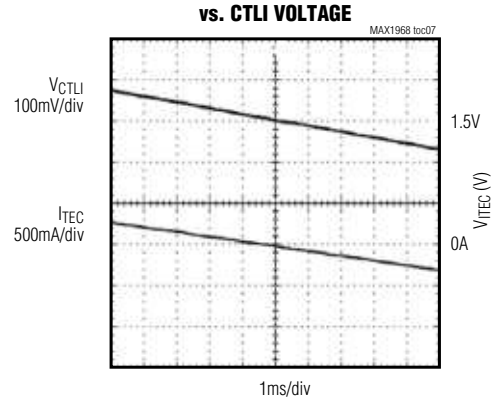
TEC CURRENT RIPPLE



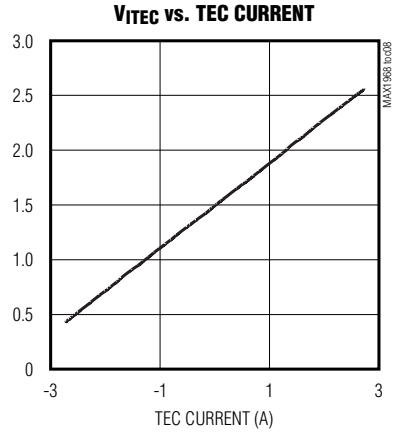
TEC CURRENT vs. CTLI VOLTAGE



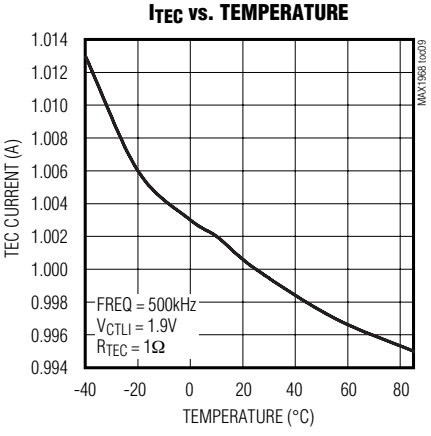
ZERO-CROSSING TEC CURRENT vs. CTLI VOLTAGE



V_{ITEC} vs. TEC CURRENT



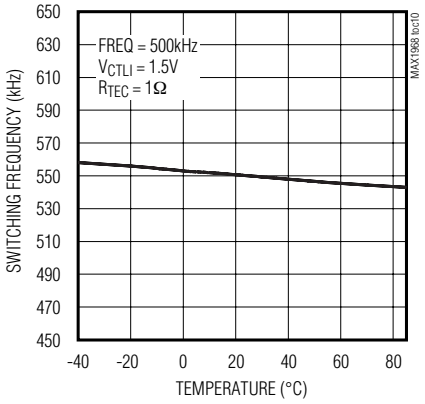
I_{TEC} vs. TEMPERATURE



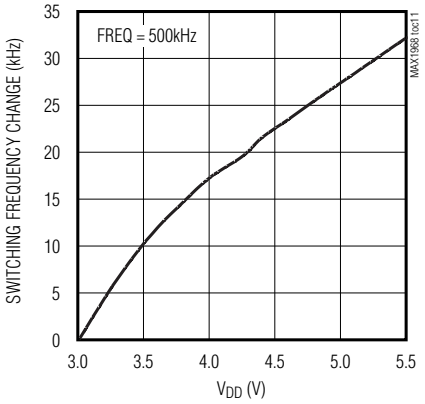
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, R_{LOAD} = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

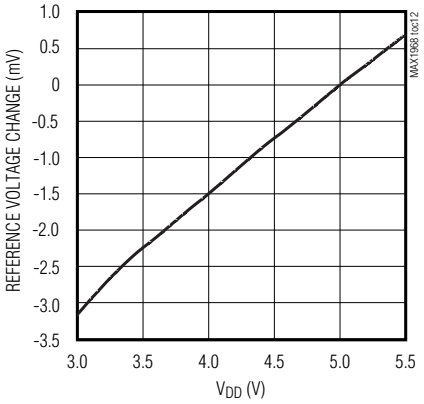
SWITCHING FREQUENCY vs. TEMPERATURE



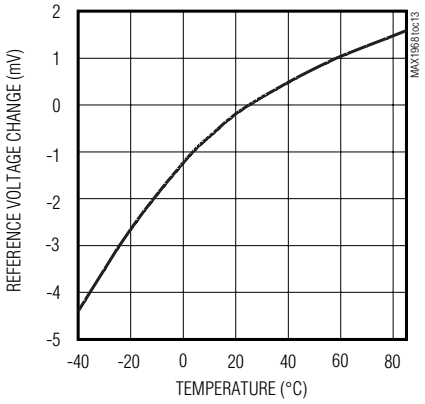
SWITCHING FREQUENCY CHANGE vs. V_{DD}



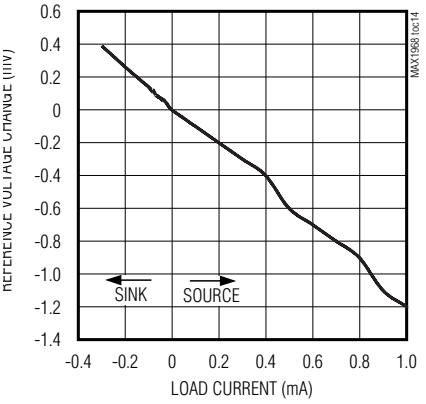
REFERENCE VOLTAGE CHANGE vs. V_{DD}



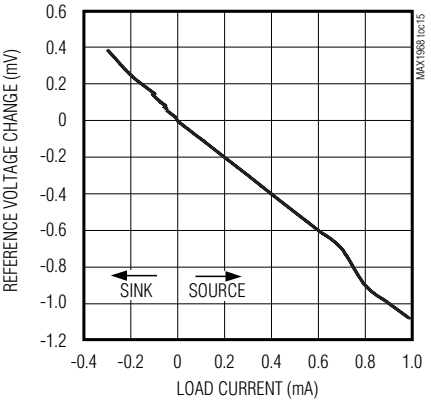
REFERENCE VOLTAGE CHANGE vs. TEMPERATURE



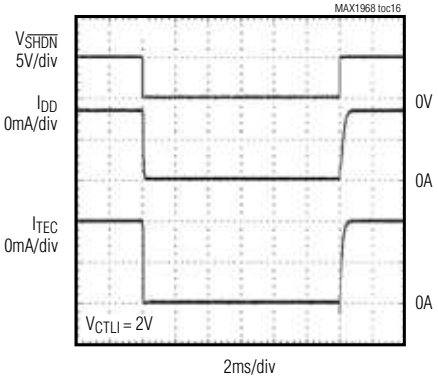
REFERENCE LOAD REGULATION V_{DD} = 3.3V



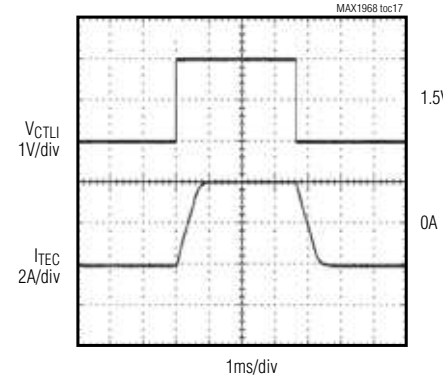
REFERENCE LOAD REGULATION V_{DD} = 5V



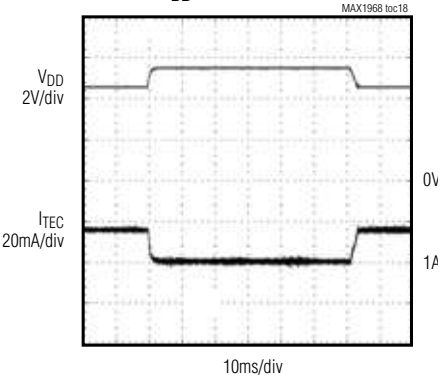
STARTUP AND SHUTDOWN WAVEFORMS



CTLI STEP RESPONSE



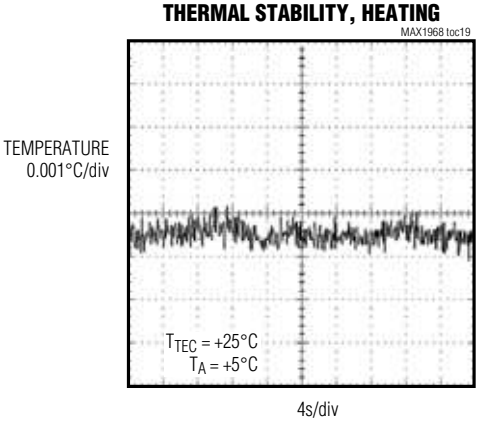
V_{DD} STEP RESPONSE



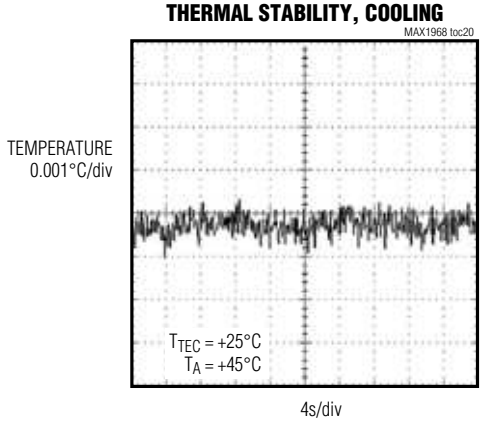
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, R_{LOAD} = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

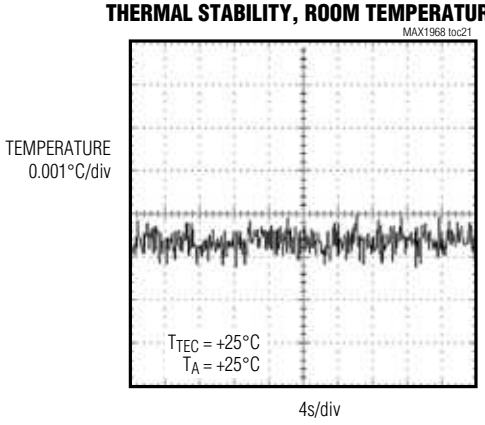
THERMAL STABILITY, HEATING



THERMAL STABILITY, COOLING



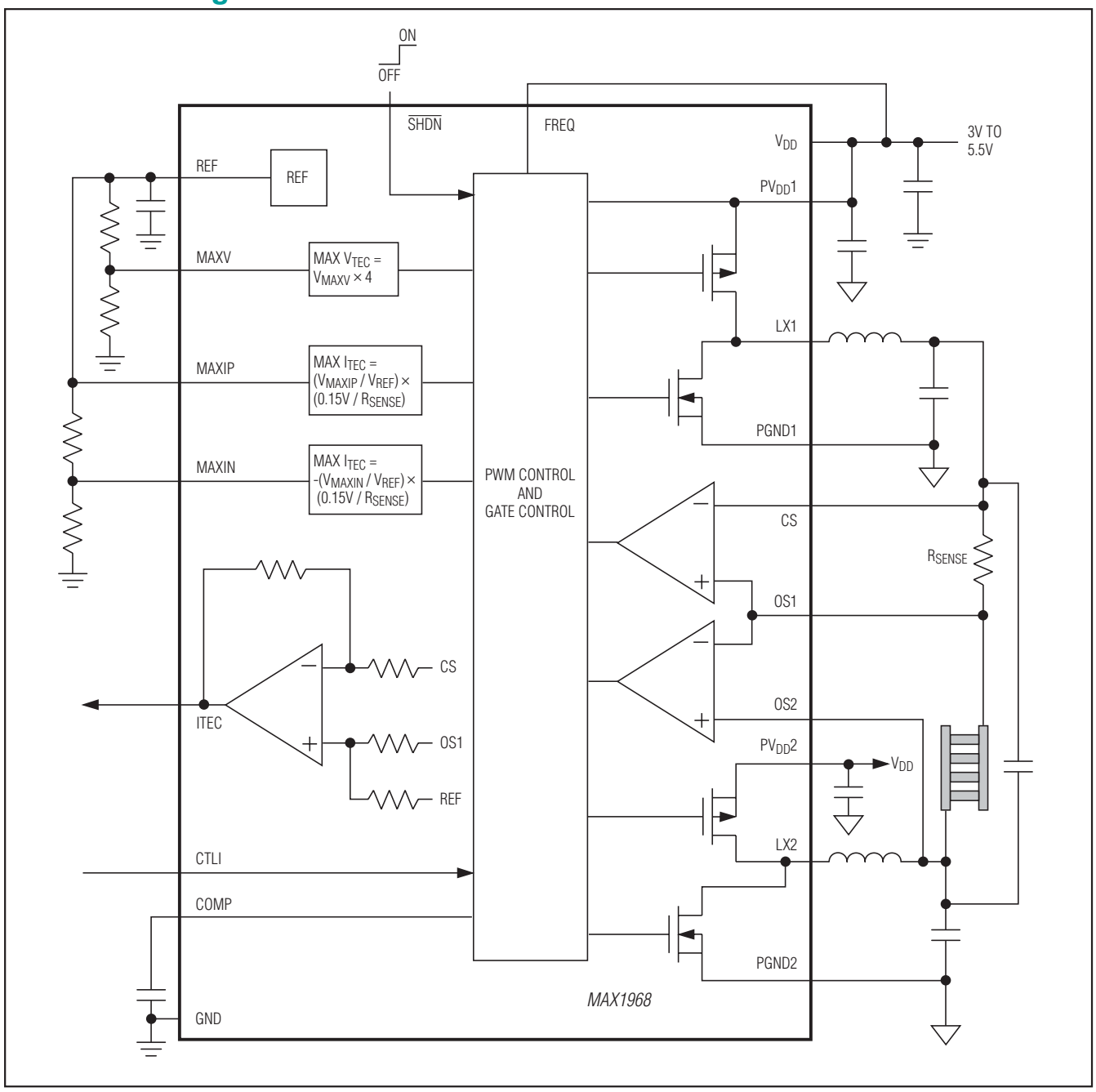
THERMAL STABILITY, ROOM TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Analog Supply Voltage Input
2	GND	Analog Ground
3	CTLI	TEC Current Control Input. Sets differential current into the TEC. Center point is 1.50V (no TEC current). The current is given by: $I_{TEC} = (V_{OS1} - V_{CS}) / R_{SENSE} = (V_{CTLI} - 1.50) / (10 \times R_{SENSE})$. When $(V_{CTLI} - V_{REF}) > 0$, $V_{OS2} > V_{OS1} > V_{CS}$.
4	REF	1.50V Reference Output. Bypass REF to GND with a 1µF ceramic capacitor.
5, 7	PGND2	Power Ground 2. Internal synchronous rectifier ground connections. Connect all PGND pins together at power ground plane.
6, 8, 10	LX2	Inductor Connection. Connect all LX2 pins together. For MAX1969, connect LX1 and LX2 pins together.
9, 11	$PV_{DD}2$	Power 2 Inputs. Must be same voltage as V_{DD}. Connect all $PV_{DD}2$ inputs together at the V_{DD} power plane.
12	FREQ	Switching Frequency Select. High = 1MHz, Low = 500kHz.
13	ITEC	TEC Current Monitor Output. The ITEC output voltage is a function of the voltage across the TEC current-sense resistor. $V_{ITEC} = 1.50V + (V_{OS1} - V_{CS}) \times 8$.
14	OS2	Output Sense 2. OS2 senses one side of the differential TEC voltage. OS2 is a sense point, not a power output. For MAX1969, connect OS2 to GND.
15	OS1	Output Sense 1. OS1 senses one side of the differential TEC voltage. OS1 is a sense point, not a power output.
16	CS	Current-Sense Input. The current through the TEC is monitored between CS and OS1. The maximum TEC current is given by 150mV / R_{SENSE} and is bipolar.
17	$\overline{SHDN}$	Shutdown Control Input. Active-low shutdown control.
18, 20	$PV_{DD}1$	Power 1 Inputs. Must be same voltage as V_{DD}. Connect all $PV_{DD}1$ inputs together at the V_{DD} power plane.
19, 21, 23	LX1	Inductor Connection. Connect all LX1 pins together. For MAX1969, connect all LX1 and LX2 pins together.
22, 24	PGND1	Power Ground 1. Internal synchronous rectifier ground connections. Connect all PGND pins together at power ground plane.
25	COMP	Current Control-Loop Compensation. For most designs connect a 0.01µF capacitor from COMP to GND.
26	MAXIN	Maximum Negative TEC Current. Connect MAXIN to REF to set default negative current limit -150mV / R_{SENSE}. For MAX1969, connect MAXIN to MAXIP.
27	MAXIP	Maximum Positive TEC Current. Connect MAXIP to REF to set default positive current limit +150mV / R_{SENSE}. (See the *Setting Max Positive and Negative TEC Current* section).
28	MAXV	Maximum Bipolar TEC Voltage. Connect an external resistive-divider from REF to GND to set the maximum voltage. The maximum TEC voltage is 4 x V_{MAXV}.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance.

Functional Diagram



Detailed Description

The MAX1968/MAX1969 TEC drivers consist of two switching buck regulators that operate together to directly control TEC current. This configuration creates a differential voltage across the TEC, allowing bidirectional TEC current for controlled cooling and heating. Controlled cooling and heating allow accurate TEC temperature control within the tight tolerances of laser driver specifications. The voltage at CTLI directly sets the TEC current. An external thermal-control loop is typically used to drive CTLI. Figures 1 and 2 show examples of thermal control-loop circuits.

Ripple Cancellation

Switching regulators like those used in the MAX1968/MAX1969 inherently create ripple voltage on the output. The regulators in the MAX1968 switch in phase and provide complementary in-phase duty cycles so ripple waveforms at the TEC are greatly reduced. This feature suppresses ripple currents and electrical noise at the TEC to prevent interference with the laser diode.

Switching Frequency

FREQ sets the switching frequency of the internal oscillator. With FREQ = GND, the oscillator frequency is set to 500kHz. The oscillator frequency is 1MHz when FREQ = V_{DD}.

Voltage and Current-Limit Settings

Both the MAX1968 and MAX1969 provide control of the maximum differential TEC voltage. Applying a voltage to MAXV limits the maximum voltage across the TEC. The MAX1968 provides control of the maximum positive and negative TEC current. The voltage at MAXIP and MAXIN sets the maximum positive and negative current through the TEC. These current limits can be independently controlled. The MAX1969 only controls TEC current in one direction. The maximum TEC current is controlled by MAXIP. Connect MAXIN to GND when using the MAX1969.

Current Monitor Output

ITEC provides a voltage output proportional to the TEC current (I_{TEC}). See the *Functional Diagram* for more detail:

$$V_{ITEC} = 1.5V + 8 \times (V_{OS1} - V_{CS})$$

Reference Output

The MAX1968/MAX1969 include an on-chip voltage reference. The 1.50V reference is accurate to 1% over temperature. Bypass REF with 1µF to GND. REF may be used to bias an external thermistor for temperature sensing as shown in Figures 1 and 2.

Design Procedure

Inductor Selection

Small surface-mount inductors are ideal for use with the MAX1968/MAX1969. 3.3µH inductors are suitable for most applications. Select the output inductors so that the LC resonant frequency of the inductance and the output capacitance is less than 1/5 the selected switching frequency. For example, 3.3µH and 1µF have a resonance at 87.6kHz, which is adequate for 500kHz operation

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where:

f = resonant frequency of output filter.

Capacitor Selection

Filter Capacitors

Decouple each power-supply input (V_{DD}, $PV_{DD}1$, $PV_{DD}2$) with a 1µF ceramic capacitor close to the supply pins. In some applications with long distances between the source supply and the MAX1968/MAX1969, additional bypassing may be needed to stabilize the input supply. In such cases, a low-ESR electrolytic capacitor of 100µF or more at V_{DD} is usually sufficient.

Compensation Capacitor

A compensation capacitor is needed to ensure current control-loop stability. Select the capacitor so that the unity-gain bandwidth of the current control loop is less than or equal to 1/12th the resonant frequency of the output filter:

$$C_{COMP} \geq \left(\frac{g_m}{f_{BW}}\right) \times \left(\frac{24 \times R_{SENSE}}{2\pi \times (R_{SENSE} + R_{TEC})}\right) \text{ (For MAX1968)}$$

$$C_{COMP} \geq \left(\frac{g_m}{f_{BW}}\right) \times \left(\frac{12 \times R_{SENSE}}{2\pi \times (R_{SENSE} + R_{TEC})}\right) \text{ (For MAX1969)}$$

where:

f_{BW} = loop unity gain bandwidth

g_m = loop transconductance, typically 100µA/V

C_{COMP} = value of the compensation capacitor

R_{TEC} = TEC series resistance

R_{SENSE} = sense resistor

Setting Voltage and Current Limits

Certain TEC parameters must be considered to guarantee a robust design. These include maximum positive current, maximum negative current, and the maximum voltage allowed across the TEC. These limits should be used to set the MAXIP, MAXIN, and MAXV voltages.

Setting Max Positive and Negative TEC Current

MAXIP and MAXIN set the maximum positive and negative TEC currents, respectively. The default current limit is ±150mV / R_{SENSE} when MAXIP and MAXIN are connected to REF. To set maximum limits other than the defaults, connect a resistor-divider from REF to GND to set $V_{MAXI_}$. Use resistors in the 10kΩ to 100kΩ range. $V_{MAXI_}$ is related to I_{TEC} by the following equations:

$$V_{MAXIP} = 10(I_{TECP(MAX)} \times R_{SENSE})$$

$$V_{MAXIN} = 10(I_{TECN(MAX)} \times R_{SENSE})$$

where $I_{TECP(MAX)}$ is the maximum positive TEC current and $I_{TECN(MAX)}$ is the negative maximum TEC current.

Positive TEC current occurs when CS is less than OS1:

$$I_{TEC} \times R_{SENSE} = V_{OS1} - V_{CS}$$

when $I_{TEC} > 0$.

$$I_{TEC} \times R_{SENSE} = V_{CS} - V_{OS1}$$

when $I_{TEC} < 0$.

The MAX1969 controls the TEC current in one direction (unipolar current flow from OS1 to CS). Set the maximum unipolar TEC current by applying a voltage to MAXIN. Connect MAXIP to MAXIN. The equation for setting MAXIN is the same for the MAX1968 and MAX1969.

Take care not to exceed the positive or negative current limit on the TEC. Refer to the manufacturer's data sheet for these limits.

Setting MAX TEC Voltage

Apply a voltage to the MAXV pin to control the maximum differential TEC voltage. MAXV can vary from 0 to REF. The voltage across the TEC is four times V_{MAXV} and can be positive or negative:

$$|V_{OS1} - V_{OS2}| = 4 \times V_{MAXV}$$

Set V_{MAXV} with a resistor-divider between REF and GND using resistors from 10kΩ to 100kΩ. V_{MAXV} can vary from 0 to REF.

Control Inputs/Outputs

Output Current Control

The voltage at CTLI directly sets the TEC current. CTLI is typically driven from the output of a temperature control loop. For the purposes of the following equations, it is assumed that positive TEC current is cooling (see Figure 1). The transfer function relating current through the TEC (I_{TEC}) and V_{CTLI} is given by:

$$I_{TEC} = (V_{CTLI} - V_{REF})/(10 \times R_{SENSE})$$

where V_{REF} is 1.50V and:

$$I_{TEC} = (V_{OS1} - V_{CS})/R_{SENSE}$$

CTLI is centered around REF (1.50V). I_{TEC} is zero when CTLI = 1.50V. When VCTLI > 1.50V the MAX1968 is cooling. Current flow is from OS2 to OS1. The voltages on the pins relate as follows:

$$V_{OS2} > V_{OS1} > V_{CS}$$

The opposite applies when heating. When V_{CTLI} < 1.50V current flows from OS1 to OS2:

$$V_{OS2} < V_{OS1} < V_{CS}$$

Shutdown Control

The MAX1968/MAX1969 can be placed in a power-saving shutdown mode by driving $\overline{SHDN}$ low. When the MAX1968/MAX1969 are shut down, the TEC is off (OS1 and OS2 decay to GND) and supply current is reduced to 2mA (typ).

ITEC Output

ITEC is a status output that provides a voltage proportional to the actual TEC current. ITEC = REF when TEC current is zero. The transfer function for the ITEC output is:

$$V_{ITEC} = 1.50 + 8 \times (V_{OS1} - V_{CS})$$

Use ITEC to monitor the cooling or heating current through the TEC. The maximum capacitance that ITEC can drive is 100pF.

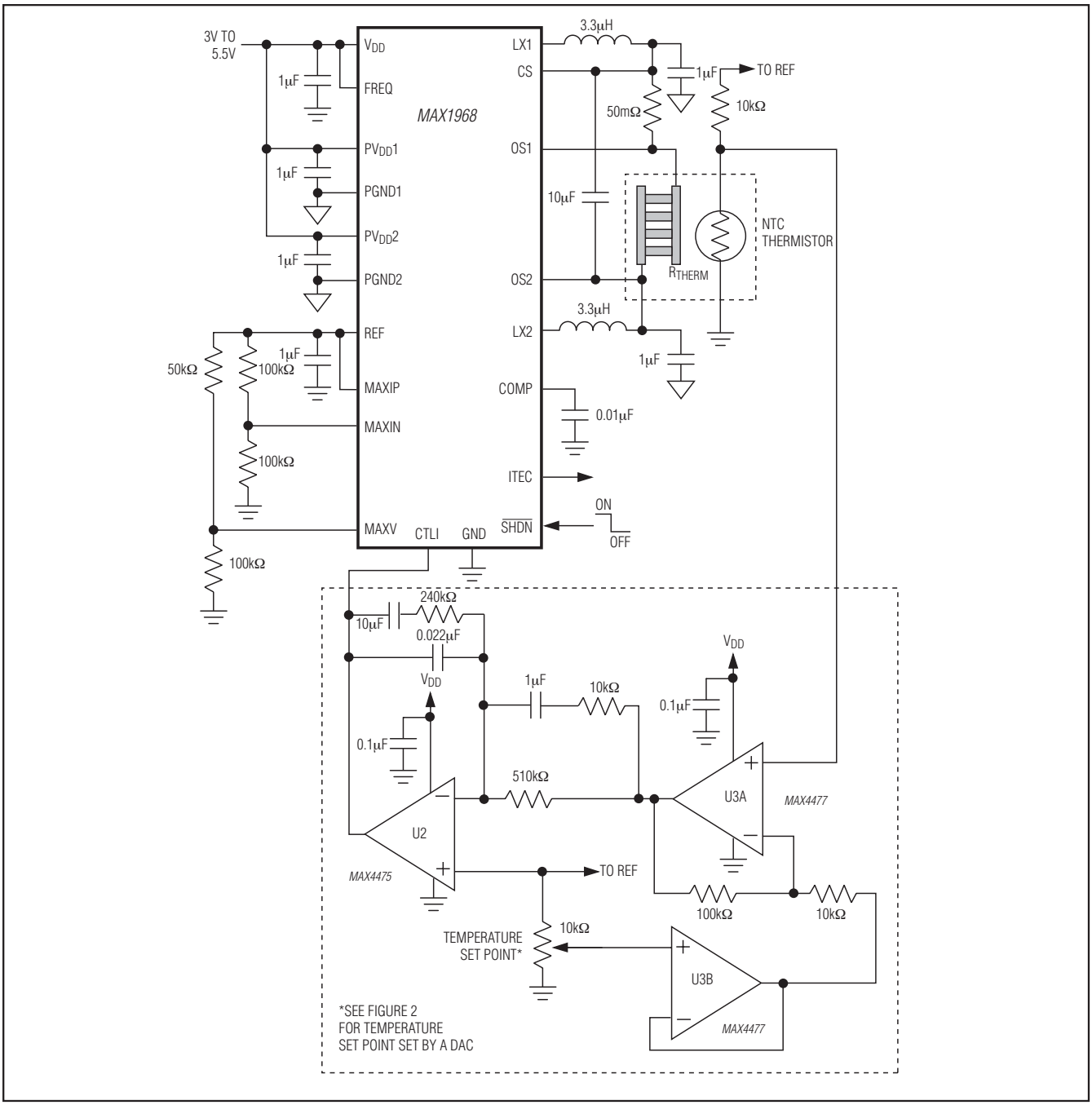


Figure 1. Typical Application Circuit for MAX1968. Circuit is configured for both cooling and heating with an NTC thermistor. Current flowing from OS2 to OS1 is cooling.

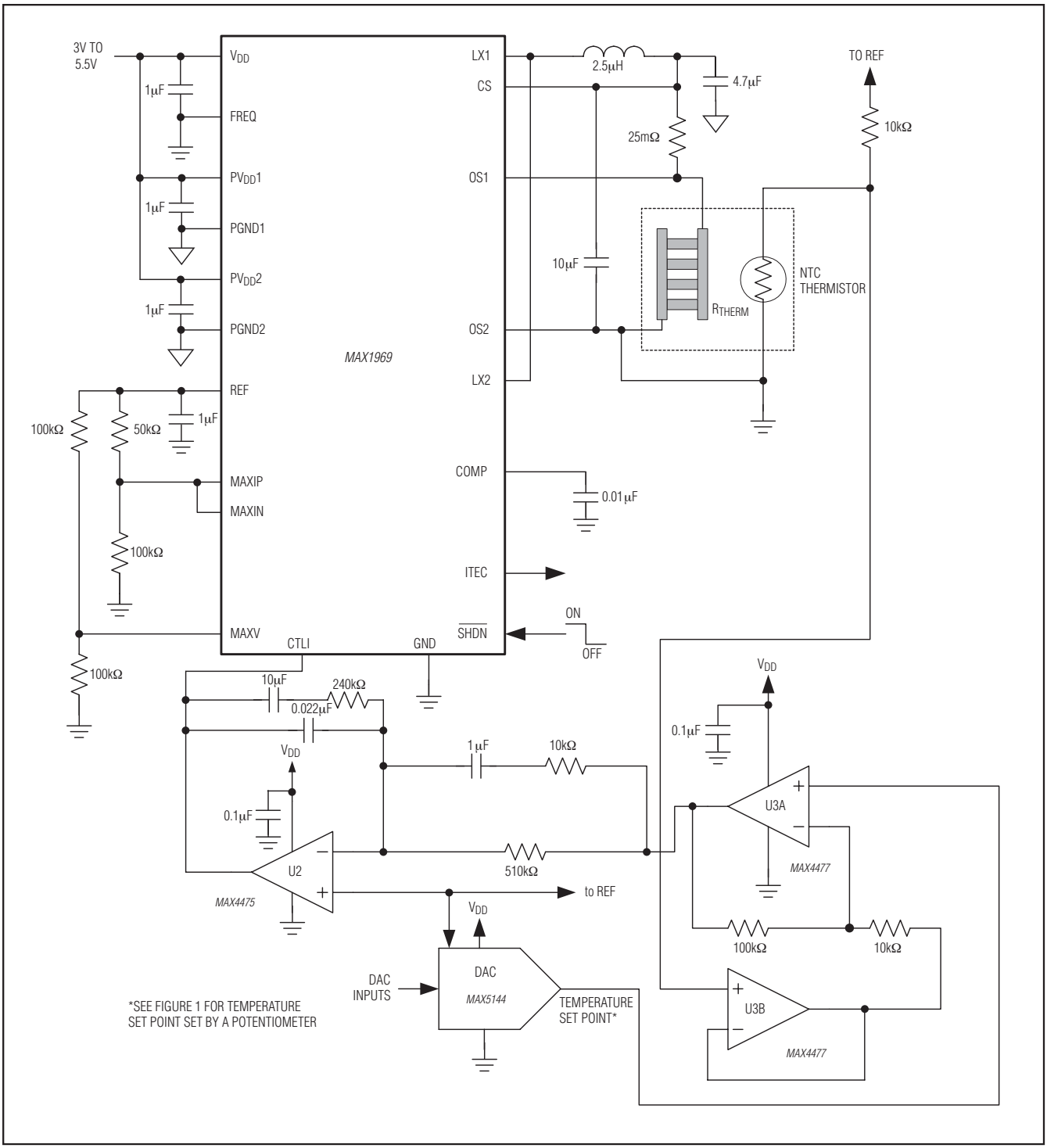


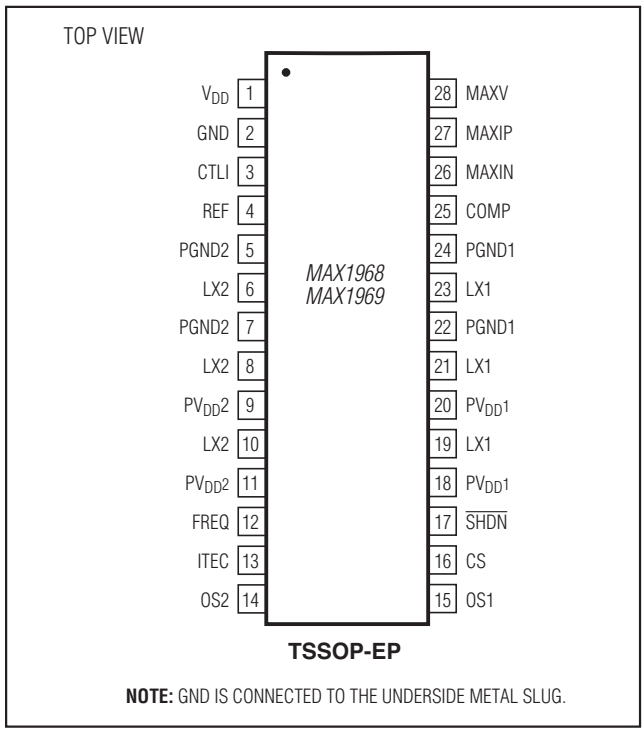
Figure 2. Typical Application Circuit for MAX1969. MAXIN sets the maximum TEC current. Circuit configured for cooling with NTC thermistor. Current always flows from CS to OS2.

Applications Information

The MAX1968/MAX1969 typically drive a thermoelectric cooler inside a thermal control loop. TEC drive polarity and power are regulated based on temperature information read from a thermistor, or other temperature-measuring device to maintain a stable control temperature. Temperature stability of 0.01°C can be achieved with carefully selected external components.

There are numerous ways to implement the thermal loop. Figures 1 and 2 show a design that employs precision op amps, along with a DAC or potentiometer to set the control temperature. The loop may also be implemented digitally, using a precision A/D to read the thermistor or other temperature sensor, a microcontroller to implement the control algorithm, and a DAC (or filtered PWM signal) to send the appropriate signal to the MAX1968/MAX1969 CTLI input. Regardless of the form taken by the thermal control circuitry, all designs are similar in that they read temperature, compare it to a set-point signal, and then send an error-correcting signal to the MAX1968/MAX1969 that moves the temperature in the appropriate direction.

Pin Configuration



NOTE: GND IS CONNECTED TO THE UNDERSIDE METAL SLUG.

Chip Information

TRANSISTOR COUNT: 2959

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TSSOP	U28E4	21-0108	90-0146

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	5/15	Updated *Benefits and Features* section	1

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