19-2297; Rev 1; 2/09

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO



## General Description

The MAX1970/MAX1971/MAX1972 dual-output current-mode PWM buck regulators operate from 2.6V to 5.5V input and deliver a minimum of 750mA on each output. The MAX1970 and MAX1972 operate at a fixed 1.4MHz (MAX1971 operates at 700kHz) to reduce output inductor and capacitor size and cost. Switching the regulators 180° out-of-phase also reduces the input capacitor size and cost. Ceramic capacitors can be used for input and output.

The output voltages are programmable from 1.2V to $V_{IN}$ using external feedback resistors, or can be preset to 1.8V or 3.3V for output 1 and 1.5V or 2.5V for output 2. When one output is higher than 1.2V, the second can be configured down to sub-1V levels. Output accuracy is better than ±1% over variations in load, line, and temperature. Internal soft-start reduces inrush current during startup.

All devices feature power-on reset ($\overline{POR}$). The MAX1971 includes a reset input (RSI), which forces $\overline{POR}$ low for 175ms after RSI goes low. The MAX1970 and MAX1972 include an open-drain power-fail output (PFO) that monitors input voltage and goes high when the input falls below 3.94V. For USB-powered xDSL modems, this output can be used to detect USB power failure. A minimum switching frequency of 1.2MHz ensures operation outside the xDSL band.

## Applications

xDSL Modems

xDSL Routers

Copper Gigabit SFP and GBIC Modules

USB-Powered Devices

Dual LDO Replacement

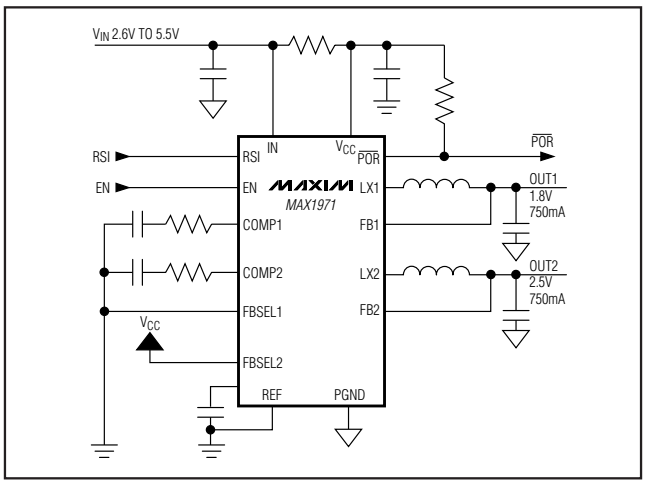
## Features

- **Current-Mode, 1.4MHz Fixed-Frequency PWM Operation**
- **180° Out-of-Phase Operation Reduces Input Capacitor**
- **±1% Output Accuracy Over Load, Line, and Temperature Ranges**
- **750mA Guaranteed Output Current**
- **2.6V to 5.5V Input**
- **Power-On Reset Delay of 16.6ms (MAX1970) or 175ms (MAX1971 and MAX1972)**
- **Power-Fail Output (MAX1970 and MAX1972 Only)**
- **Power-On Reset Input (MAX1971 Only)**
- **Operation Outside xDSL Band**
- **Ultra-Compact Design with Smallest External Components**
- **Outputs Adjustable from 0.8V to $V_{IN}$ or 1.8V/3.3V and 1.5V/2.5V Preset**
- **All-Ceramic Capacitor Application**
- **Soft-Start Reduces Inrush Current**

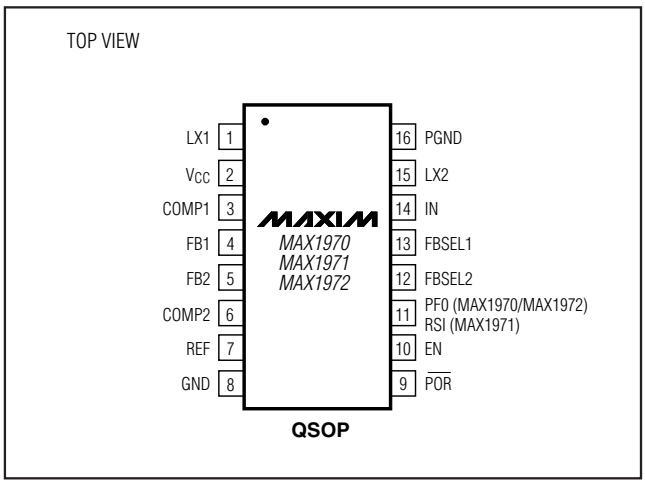
## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX1970**EEE | -40°C to +85°C | 16 QSOP |
| **MAX1971**EEE | -40°C to +85°C | 16 QSOP |
| **MAX1972**EEE | -40°C to +85°C | 16 QSOP |

## Typical Operating Circuit




## Pin Configuration






For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## ABSOLUTE MAXIMUM RATINGS

IN, EN, FBSEL1, FBSEL2, PFO, $\overline{POR}$, RSI, $V_{CC}$ to GND .....-0.3V to +6V
COMP1, COMP2, FB1, FB2, REF to GND .....-0.3V to ($V_{CC}$ + 0.3V)
LX1, LX2 to PGND .....-0.3V to ($V_{IN}$ + 0.3V)
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, $V_{RSI}$ = 0, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **IN AND $V_{CC}$** | | | | | | |
| IN Voltage Range | | | 2.6 | | 5.5 | V |
| IN Supply Current | Switching with no load, $V_{IN}$ = 3.3V | MAX1971 | | 5 | 10 | mA |
| | | MAX1970/MAX1972 | | 10 | 20 | |
| IN Shutdown Current | $V_{IN}$ = 5.5V, $V_{EN}$ = 0 | MAX1970/MAX1972 | | 1 | 100 | µA |
| | | MAX1971 | | 1 | 60 | |
| $V_{CC}$ Undervoltage Lockout Threshold | $V_{CC}$ rising | | | 2.40 | 2.55 | V |
| | $V_{CC}$ falling | | 2.20 | 2.35 | | |
| **REF** | | | | | | |
| REF Voltage | $I_{REF}$ = 0, $V_{IN}$ = 2.6V to 5.5V | | 1.188 | 1.200 | 1.212 | V |
| REF Shutdown Resistance | REF to GND, $V_{EN}$ = 0 | | | 10 | 25 | Ω |
| REF Soft-Start Current | $V_{REF}$ = 1V | | 20 | 25 | 30 | µA |
| **FB1 AND FB2** | | | | | | |
| FB_ Regulation Voltage | FBSEL_ = unconnected, OUT1 = FB1, OUT2 = FB2, $V_{COMP_}$ = 1.20V to 1.80V, $V_{IN}$ = 2.6V to 5.5V | | 1.188 | 1.200 | 1.212 | V |
| OUT_ Voltage Range | FBSEL_ = unconnected | | 1.2 | | $V_{IN}$ | V |
| OUT1 Regulation Voltage | $V_{IN}$ = 2.6V to 5.5V | $V_{COMP1}$ = 1.2V, FBSEL1= GND | 1.782 | 1.800 | 1.818 | V |
| | $V_{IN}$ = 4.5V to 5.5V | $V_{COMP1}$ = 1.2V, FBSEL1 = $V_{CC}$ | 3.2670 | 3.3 | 3.330 | |
| OUT2 Regulation Voltage | $V_{IN}$ = 2.6V to 5.5V | $V_{COMP2}$ = 1.2V, FBSEL2 = GND | 1.485 | 1.5 | 1.150 | V |
| | | $V_{COMP2}$ = 1.2V, FBSEL2 = $V_{CC}$ | 2.475 | 2.5 | 2.525 | |
| Maximum Output Current | Guaranteed by design (Note 1) | | 750 | | | mA |
| FB1 Input Resistance | Measured from FB1 to GND | FBSEL1 = GND | 30 | 60 | 120 | kΩ |
| | | FBSEL1 = $V_{CC}$ | 30 | 60 | 120 | |
| FB2 Input Resistance | Measured from FB2 to GND | FBSEL2 = GND | 22.5 | 45 | 90 | kΩ |
| | | FBSEL2 = $V_{CC}$ | 22.5 | 45 | 90 | |
| FB_ Input Bias Current | FB1 or FB2, FBSEL_ = unconnected, $V_{FB1}$ = $V_{FB2}$ = 1.15V | | | 0.01 | 0.1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, $V_{RSI}$ = 0, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **COMP1 AND COMP2** | | | | | | |
| COMP1 Transconductance | FB1 = COMP1, $V_{COMP1}$ = 1.2V | FBSEL1 = unconnected | 35 | 55 | 85 | µS |
| COMP2 Transconductance | FB2 = COMP2, $V_{COMP2}$ = 1.2V | FBSEL2 = unconnected | 35 | 55 | 85 | µS |
| **LX1 AND LX2** | | | | | | |
| Internal High-Side MOSFET On-Resistance | $I_{LX}$ = -180mA | $V_{IN}$ = 5.0V | | 0.20 | 0.32 | Ω |
| | | $V_{IN}$ = 3.3V | | 0.24 | 0.37 | |
| | | $V_{IN}$ =2.6V | | 0.28 | | |
| Internal Low-Side MOSFET On-Resistance | $I_{LX}$ = 180mA | $V_{IN}$ = 5.0V | | 0.12 | 0.23 | Ω |
| | | $V_{IN}$ = 3.3V | | 0.14 | 0.25 | |
| | | $V_{IN}$ = 2.6V | | 0.16 | | |
| LX_ Current-Sense Transresistance | | | 0.4 | 0.5 | 0.6 | V/A |
| LX_ Current-Limit Threshold | Duty Cycle = 100%, $V_{IN}$ = 2.6V to 5.5V | High side | 0.80 | 1.2 | 1.60 | A |
| | | Low side | -1.6 | -0.85 | -0.40 | |
| LX_ Leakage Current | $V_{IN}$ = 5.5V | $V_{LX1}$ = $V_{LX2}$ = 5.5V | | | 20 | µA |
| | | $V_{LX1}$ = $V_{LX2}$ = 0 | -20 | | | |
| LX_ Switching Frequency | $V_{IN}$ = 2.6V to 5.5V | MAX1970/MAX1972 | 1.2 | 1.4 | 1.6 | MHz |
| | | MAX1971 | 0.60 | 0.70 | 0.80 | |
| LX_ Maximum Duty Cycle | | | | 100 | | % |
| LX_ Minimum Duty Cycle | $V_{IN}$ = 2.6V to 5.5V | MAX1970/MAX1972 | | 15 | 20 | % |
| | | MAX1971 | | 10 | 15 | |
| **$\overline{POR}$** | | | | | | |
| $\overline{POR}$ Thresholds | Percentage of $V_{OUT}$, $V_{IN}$ = 2.6V to 5.5V | $V_{OUT}$ rising | | 92 | 94 | % |
| | | $V_{OUT}$ falling | 87 | 90 | | |
| $\overline{POR}$ Delay Time ($T_D$) | MAX1970 | | 13.3 | 16.6 | 20 | ms |
| | MAX1971/MAX1972 | | 140 | 175 | 210 | |
| $\overline{POR}$ Output Current, High | $V_{\overline{POR}}$ = $V_{IN}$ = 5.5V, $V_{FB1}$ = $V_{FB2}$ = 1.15V | | -1 | | 1 | µA |
| $\overline{POR}$ Output Voltage, Low | $V_{FB1}$ = 1.05V or $V_{FB2}$ = 1.05V or RSI = IN (MAX1971 only), $I_{\overline{POR}}$ = 1mA | | | 0.01 | 0.05 | V |
| $\overline{POR}$ Startup Voltage | FB1 = FB2 = GND, $I_{\overline{POR}}$ = 100µA, $V_{IN}$ = 1.2V | | | 0.01 | 0.05 | V |

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, $V_{RSI}$ = 0, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PFO (MAX1970 and MAX1972 Only)** | | | | | | |
| PFO Trip Threshold | IN = $V_{CC}$ | $V_{CC}$ rising | | 4.04 | 4.12 | V |
| | | $V_{CC}$ falling | 3.86 | 3.94 | | |
| PFO Output Current, High | PFO = IN | | -1 | | 1 | µA |
| PFO Output Voltage, Low | $I_{PFO}$ = 1mA, $V_{IN}$ = 4.3V | | | 0.01 | 0.05 | V |
| **EN AND RSI (MAX1971 Only)** | | | | | | |
| Logic Input Thresholds | IN = 2.6V to 5.5V | $V_{IL}$ | 0.4 | 0.95 | | V |
| | | $V_{IH}$ | | 1.0 | 1.6 | |
| RSI Input Resistance | Internal pullup resistor to IN | | 5 | 10 | 20 | kΩ |
| EN Logic Input Current | Logic input at 0 or 5.5V, $V_{IN}$ = 5.5V | $V_{IL}$ | -1 | | 1 | µA |
| | | $V_{IH}$ | -1 | | 1 | |

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $V_{FB1}$ = $V_{FB2}$ = 1.15V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, RSI = 0, $C_{VCC}$ = 0.1µF, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = -40°C to +85°C.**) (Note 2)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **IN AND $V_{CC}$** | | | | | | |
| IN Voltage Range | | | 2.6 | | 5.5 | V |
| IN Supply Current | Switching with no load $V_{IN}$ = 3.3V | MAX1971 | | | 10 | mA |
| | | MAX1970/MAX1972 | | | 20 | |
| IN Shutdown Current | $V_{IN}$ = 5.5V, $V_{EN}$ = 0 | MAX1970/MAX1972 | | | 20 | µA |
| | | MAX1971 | | | 100 | |
| $V_{CC}$ Undervoltage Lockout Threshold | $V_{CC}$ rising | | | | 2.55 | V |
| | $V_{CC}$ falling | | 2.20 | | | |
| **REF** | | | | | | |
| REF Voltage | $I_{REF}$ = 0, $V_{IN}$ = 2.6V to 5.5V | | 1.185 | | 1.212 | V |
| REF Shutdown Resistance | REF to GND, $V_{EN}$=0 | | | | 25 | Ω |
| REF Soft-Start Current | $V_{REF}$ = 1V | | 20 | | 30 | µA |
| **FB1 AND FB2** | | | | | | |
| FB_ Regulation Voltage | FBSEL_ = unconnected, OUT1 = FB1, OUT2 = FB2, $V_{COMP_}$ = 1.20V to 1.80V, $V_{IN}$ = 2.6V to 5.5V | | 1.185 | | 1.212 | V |
| OUT_ Voltage Range | FBSEL_ = unconnected | | 1.2 | | $V_{IN}$ | V |
| OUT1 Regulation Voltage | $V_{IN}$ = 2.6V to 5.5V | $V_{COMP1}$ = 1.2V, FBSEL1= GND | 1.778 | | 1.818 | V |
| | $V_{IN}$ = 4.5V to 5.5V | $V_{COMP1}$ = 1.2V, FBSEL1 = $V_{CC}$ | 3.259 | | 3.333 | |
| OUT2 Regulation Voltage | $V_{IN}$ = 2.6V to 5.5V | $V_{COMP2}$ = 1.2V, FBSEL2 = GND | 1.481 | | 1.515 | V |
| | | $V_{COMP2}$ = 1.2V, FBSEL2 = $V_{CC}$ | 2.469 | | 2.525 | |
| Maximum Output Current | Guaranteed by design (Note 1) | | 750 | | | mA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $V_{FB1}$ = $V_{FB2}$ = 1.15V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, RSI = 0, $C_{VCC}$ = 0.1µF, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = -40°C to +85°C.**) (Note 2)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| FB1 Input Resistance | Measured from FB1 to GND | FBSEL1 = GND | 30 | | 120 | kΩ |
| | | FBSEL1 = $V_{CC}$ | 30 | | 120 | |
| FB2 Input Resistance | Measured from FB2 to GND | FBSEL2 = GND | 22.5 | | 90 | kΩ |
| | | FBSEL2 = $V_{CC}$ | 22.5 | | 90 | |
| FB_ Input Bias Current | FB1 or FB2, FBSEL_ = unconnected, $V_{FB1}$ = $V_{FB2}$ = 1.15V | | | | 0.1 | µA |
| **COMP1 AND COMP2** | | | | | | |
| COMP1 Transconductance | FB1 = COMP1, $V_{COMP1}$ = 1.2V | FBSEL1 = unconnected | 35 | | 85 | µS |
| COMP2 Transconductance | FB2 = COMP2, $V_{COMP2}$ = 1.2V | FBSEL2 = unconnected | 35 | | 85 | µS |
| **LX1 AND LX2** | | | | | | |
| Internal High-Side MOSFET On-Resistance | $I_{LX}$ = -180mA | $V_{IN}$ = 5.0V | | | 0.32 | Ω |
| | | $V_{IN}$ = 3.3V | | | 0.37 | |
| Internal Low-Side MOSFET On-Resistance | $I_{LX}$ = 180mA | $V_{IN}$ = 5.0V | | | 0.23 | Ω |
| | | $V_{IN}$ = 3.3V | | | 0.25 | |
| LX_ Current-Sense Transresistance | | | 0.4 | | 0.6 | V/A |
| LX_ Current-Limit Threshold | Duty cycle = 100%, $V_{IN}$ = 2.6V to 5.5V | High side | 0.76 | | 1.60 | A |
| | | Low side | -1.6 | | -0.40 | |
| LX_ Leakage Current | $V_{IN}$ = 5.5V | $V_{LX1}$ = $V_{LX2}$ = 5.5V | | | 20 | µA |
| | | $V_{LX1}$ = $V_{LX2}$ = 0 | -20 | | | |
| LX_ Switching Frequency | $V_{IN}$ = 2.6V to 5.5V | MAX1970/MAX1972 | 1.2 | | 1.6 | MHz |
| | | MAX1971 | 0.60 | | 0.80 | |
| LX_ Minimum Duty Cycle | $V_{IN}$ = 2.6V to 5.5V | MAX1970/MAX1972 | | | 20 | % |
| | | MAX1971 | | | 15 | |
| **$\overline{POR}$** | | | | | | |
| $\overline{POR}$ Thresholds | Percentage of $V_{OUT}$, $V_{IN}$ = 2.6V to 5.5V | $V_{OUT}$ rising | | | 94 | % |
| | | $V_{OUT}$ falling | 87 | | | |
| $\overline{POR}$ Delay Time ($T_D$) | MAX1970 | | 13.3 | | 20 | ms |
| | MAX1971/MAX1972 | | 140 | | 210 | |
| $\overline{POR}$ Output Current, High | $V_{\overline{POR}}$ = $V_{IN}$ = 5.5V, $V_{FB1}$ = $V_{FB2}$ = 1.15V | | -1 | | 1 | µA |
| $\overline{POR}$ Output Voltage, Low | $V_{FB1}$ = 1.05V or $V_{FB2}$ = 1.05V or RSI = IN (MAX1971 only), $I_{\overline{POR}}$ = 1mA | | | | 0.05 | V |
| $\overline{POR}$ Start-Up Voltage | FB1 = FB2 = GND, $I_{\overline{POR}}$ = 100µA, $V_{IN}$ = 1.2V | | | | 0.05 | V |

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = $V_{EN}$ = 5V, $V_{FB1}$ = $V_{FB2}$ = 1.15V, $R_{\overline{POR}}$ = 100kΩ to IN, $R_{PFO}$ = 100kΩ to IN, RSI = 0, $C_{VCC}$ = 0.1µF, $C_{REF}$ = 0.1µF, FBSEL1 = unconnected, FBSEL2 = unconnected, **$T_A$ = -40°C to +85°C.**) (Note 2)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PFO (MAX1970 and MAX1972 Only)** | | | | | | |
| PFO Trip Threshold | IN = $V_{CC}$ | $V_{CC}$ rising | | | 4.12 | V |
| | | $V_{CC}$ falling | 3.86 | | | |
| PFO Output Current, High | PFO = IN | | -1 | | 1 | µA |
| PFO Output Voltage, Low | $I_{PFO}$ = 1mA, $V_{IN}$ = 4.3V | | | | 0.05 | V |
| **EN AND RSI (MAX1971 Only)** | | | | | | |
| Logic Input Thresholds | IN = 2.6V to 5.5V | $V_{IL}$ | 0.4 | | | V |
| | | $V_{IH}$ | | | 1.6 | |
| RSI Input Resistance | Internal pullup resistor to IN | | 5 | | 20 | kΩ |
| EN Logic Input Current | Logic Input at 0 or 5.5V, $V_{IN}$ = 5.5V | $V_{IL}$ | -1 | | 1 | µA |
| | | $V_{IH}$ | -1 | | 1 | |

**Note 1:** See the *Output Voltage Selection* section.

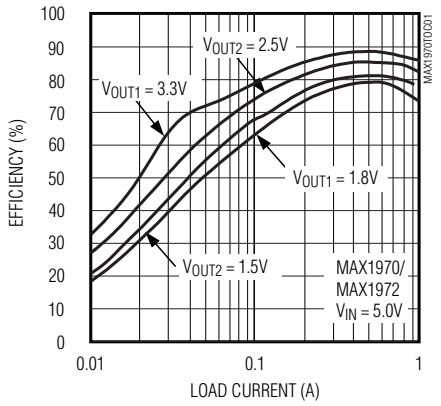
**Note 2:** Specifications to $T_A$ = -40°C are guaranteed by design and not production tested.

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

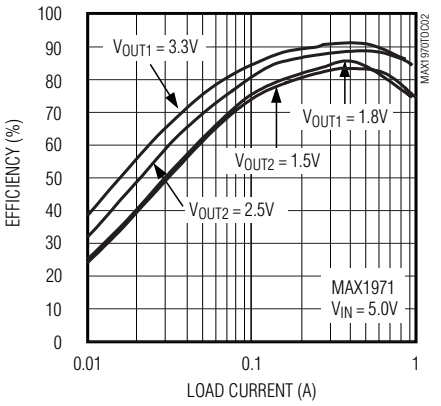
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

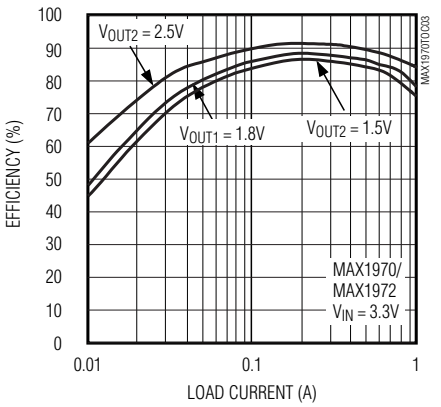
**EFFICIENCY vs. LOAD CURRENT**



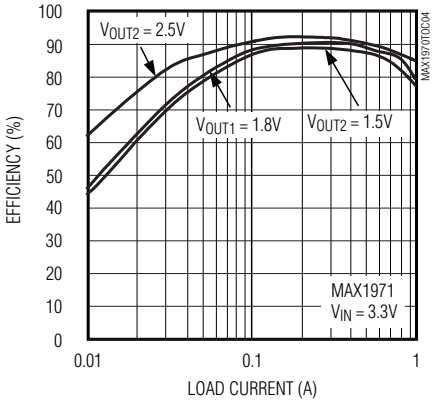

**EFFICIENCY vs. LOAD CURRENT**



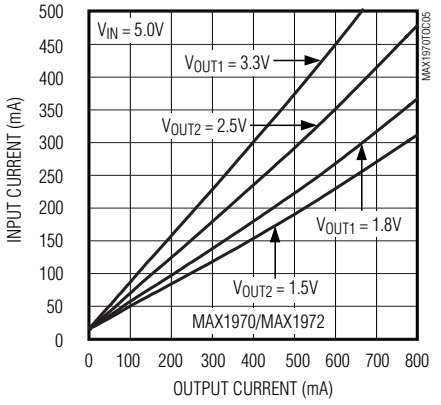

**EFFICIENCY vs. LOAD CURRENT**



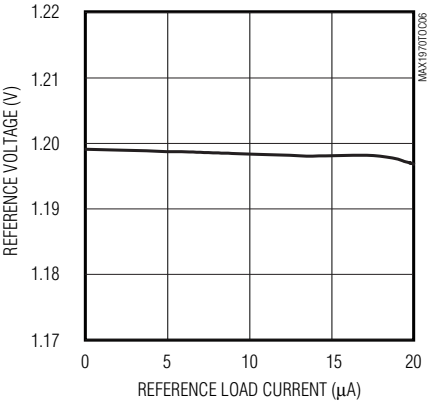

**EFFICIENCY vs. LOAD CURRENT**



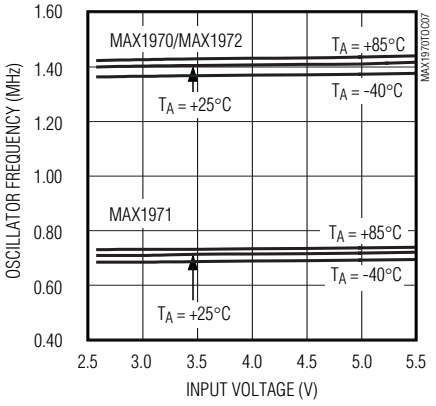

**INPUT CURRENT vs. OUTPUT CURRENT**



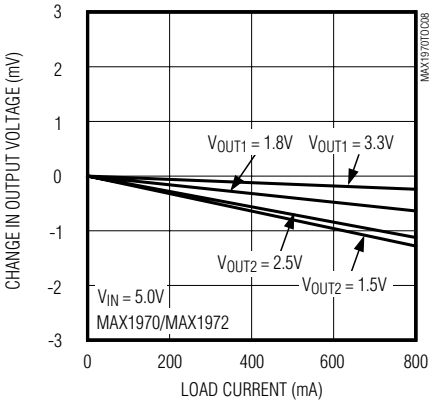

**REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT**




**OSCILLATOR FREQUENCY vs. INPUT VOLTAGE**




**CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT**

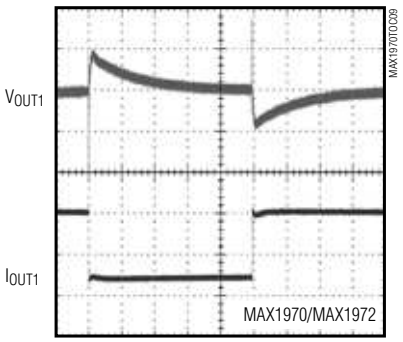


# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## Typical Operating Characteristics (continued)

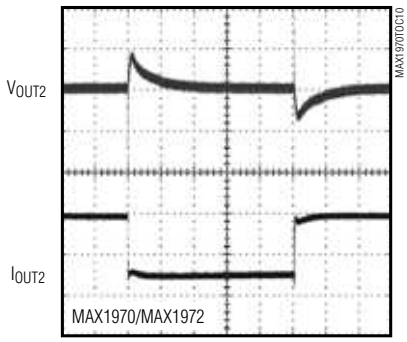
($T_A$ = +25°C, unless otherwise noted.)

**LOAD-TRANSIENT RESPONSE**



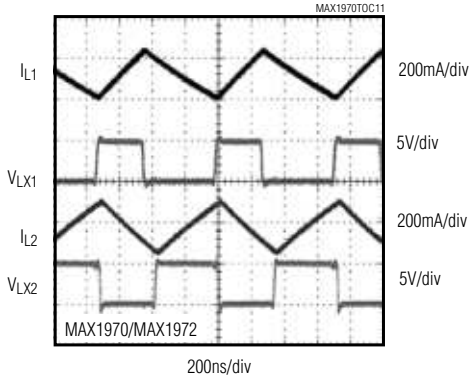

$V_{IN}$ = 5V
$V_{OUT1}$ = 3.3V, 100mV/div
$I_{OUT1}$ = 300mA TO 600mA
$R_{C1}$ = 82kΩ, $C_{C1}$ = 680pF

**LOAD-TRANSIENT RESPONSE**



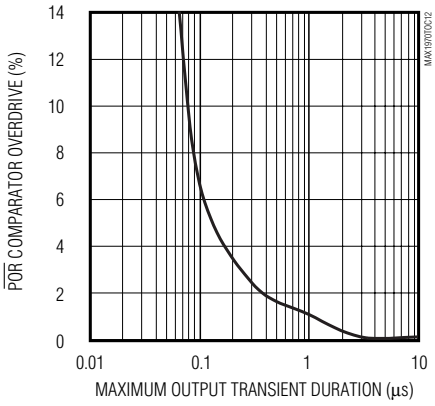

$V_{IN}$ = 5V
$V_{OUT2}$ = 1.5V, 100mV/div
$I_{OUT2}$ = 300mA TO 600mA
$R_{C2}$ = 39kΩ, $C_{C2}$ = 680pF

**SWITCHING WAVEFORMS**




$V_{IN}$ = 5V
$V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 2.5V
$I_{OUT1}$ = 500mA, $I_{OUT2}$ = 500mA

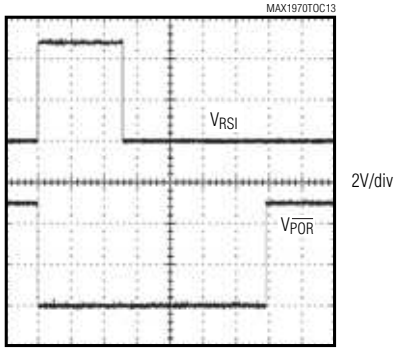
**MAXIMUM OUTPUT TRANSIENT DURATION vs. $\overline{POR}$ COMPARATOR OVERDRIVE**



## Typical Operating Characteristics (continued)

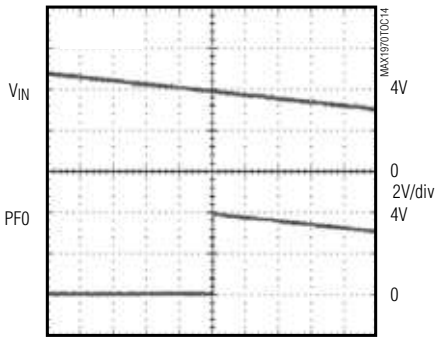
($T_A$ = +25°C, unless otherwise noted.)

**RSI AND $\overline{POR}$ TIMING**



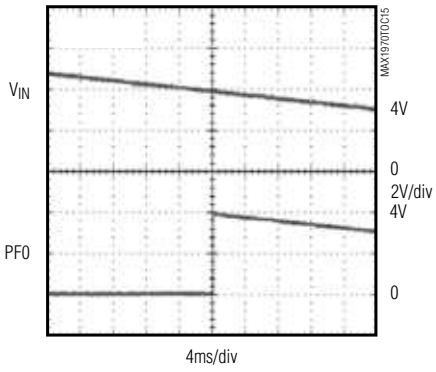

$V_{IN}$ = 5V
$V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 2.5V
$I_{OUT1}$ = 500mA, $I_{OUT2}$ = 500mA

**PFO AND RISING INPUT VOLTAGE**



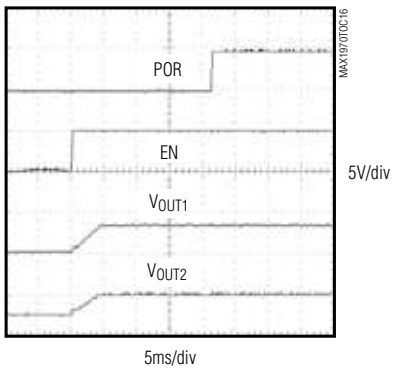

$V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 2.5V

**PFO AND FALLING INPUT VOLTAGE**




$V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 2.5V

**ENABLE RESPONSE**



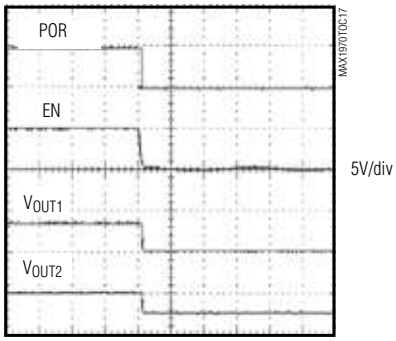

MAX1970
$V_{IN}$ = 5V
$V_{OUT1}$ = 3.3V, $V_{OUT2}$ = 2.5V
$I_{OUT1}$ = 375mA, $I_{OUT2}$ = 375mA

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

**SHUTDOWN RESPONSE**




MAX1970
$V_{IN}$ = 5V
$V_{OUT1}$ = 3.3V, $V_{OUT2}$ = 2.5V
$I_{OUT1}$ = 375mA, $I_{OUT2}$ = 375mA

## Pin Description

| PIN | NAME | | FUNCTION |
|---|---|---|---|
| | MAX1970/MAX1972 | MAX1971 | |
| 1 | LX1 | LX1 | Inductor Connection 1. Connect an inductor between LX1 and OUT1. |
| 2 | $V_{CC}$ | $V_{CC}$ | Analog Supply Voltage. Bypass with 0.1µF to ground. |
| 3 | COMP1 | COMP1 | OUT1 Regulator Compensation. Connect series RC network from COMP1 to GND. COMP1 is pulled to GND when the outputs are shut down. See the *Compensation Design* section for component values. |
| 4 | FB1 | FB1 | OUT1 Feedback. Connected to OUT1 for internal mode (FBSEL1 = GND or $V_{CC}$). Use an external resistor-divider from OUT1 to GND to set the output voltage from 1.2V to $V_{IN}$ for external mode (FBSEL1 = unconnected). See the *Output Voltage Selection* section for <1.2V output. |
| 5 | FB2 | FB2 | OUT2 Feedback. Connected to OUT2 for internal mode (FBSEL2 = GND or $V_{CC}$). Use an external resistor-divider from OUT2 to GND to set the output voltage from 1.2V to $V_{IN}$ for external mode (FBSEL2 = unconnected). See the *Output Voltage Selection* section for <1.2V output. |
| 6 | COMP2 | COMP2 | OUT2 Regulator Compensation. Connect series RC network from COMP2 to GND. COMP2 is pulled to GND when the outputs are shut down. See the *Compensation Design* section for component values. |
| 7 | REF | REF | Reference. Bypass with 0.01µF to 1.0µF capacitor. REF controls the soft-start ramp and is pulled to GND when the outputs are shut down. |
| 8 | GND | GND | Ground |

## Pin Description (continued)

| PIN | NAME | | FUNCTION |
|---|---|---|---|
| | MAX1970/MAX1972 | MAX1971 | |
| 9 | $\overline{POR}$ | $\overline{POR}$ | Active-Low Power-On Reset Output. Open-drain output goes high 16.6ms (MAX1970) or 175ms (MAX1971 or MAX1972) after both outputs reach 92% of nominal value, and RSI (MAX1971 only) is low. |
| 10 | EN | EN | Enable Input. Drive high to turn on both OUT1 and OUT2. Drive low to place the device in shutdown. |
| 11 | PFO | — | Power-Fail Output. Open-drain output goes high when $V_{CC}$ drops below 3.94V. Useful for detecting a valid USB input voltage. |
| | — | RSI | Noninverting Reset Input. Causes $\overline{POR}$ to go low when RSI is high. Allows $\overline{POR}$ to go high 175ms after RSI falls, if outputs are in regulation. |
| 12 | FBSEL2 | FBSEL2 | Regulator 2 Feedback Select. Connect to $V_{CC}$ to set $V_{OUT2}$ to 2.5V. Connect to GND to set $V_{OUT2}$ to 1.5V. Leave unconnected to use external feedback resistors. |
| 13 | FBSEL1 | FBSEL1 | Regulator 1 Feedback Select. Connect to $V_{CC}$ to set $V_{OUT1}$ to 3.3V. Connect to GND to set $V_{OUT1}$ to 1.8V. Leave unconnected to use external feedback resistors. |
| 14 | IN | IN | Power-Supply Voltage. Input range from 2.6V to 5.5V. Bypass with 10µF capacitor to PGND. |
| 15 | LX2 | LX2 | Inductor Connection 2. Connect an inductor between LX2 and OUT2. |
| 16 | PGND | PGND | Power Ground |

## Detailed Description

The MAX1970/MAX1971/MAX1972 are dual-output, fixed-frequency, current-mode, PWM, step-down DC-DC converters. The MAX1970 and MAX1972 switch at 1.4 MHz while the MAX1971 switches at 700kHz. The two converters on each IC switch 180° out of phase with each other to reduce input ripple current. The high-switching frequency allows use of smaller capacitors for filtering and decoupling. Internal synchronous rectifiers improve efficiency and eliminate the typical Schottky freewheeling diode. The on-resistances of the internal MOSFETs are used to sense the switch currents for controlling and protecting the MOSFETs, eliminating current-sensing resistors to further improve efficiency and cost.

The input voltage range is 2.6V to 5.5V. Each converter has a three-mode feedback input. Internally, OUT1 is set to either 3.3V or 1.8V, and OUT2 to 2.5V or 1.5V by connecting FBSEL1 and FBSEL2 to $V_{CC}$ or GND, respectively. When FBSEL1 or FBSEL2 are floating, each output can be set to any voltage between 1.2V and $V_{IN}$ through an external resistive divider. Having an output below 1.2V is also possible (see the *Output Voltage Selection* section).

### DC-DC Controller

The MAX1970/MAX1971/MAX1972 family of step-down converters uses a pulse-width-modulating (PWM) current-mode control scheme. The heart of the current-mode PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on time, current ramps up through the inductor, sourcing current to the output and storing energy in a magnetic field. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (assuming that the inductor value is relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the output LC filter pole, normally found in a voltage-mode PWM, to a higher frequency. To preserve inner loop stability and eliminate inductor stair casing, a slope-compensation ramp is summed into the main PWM comparator. During the second half of the cycle, the internal high-side MOSFET

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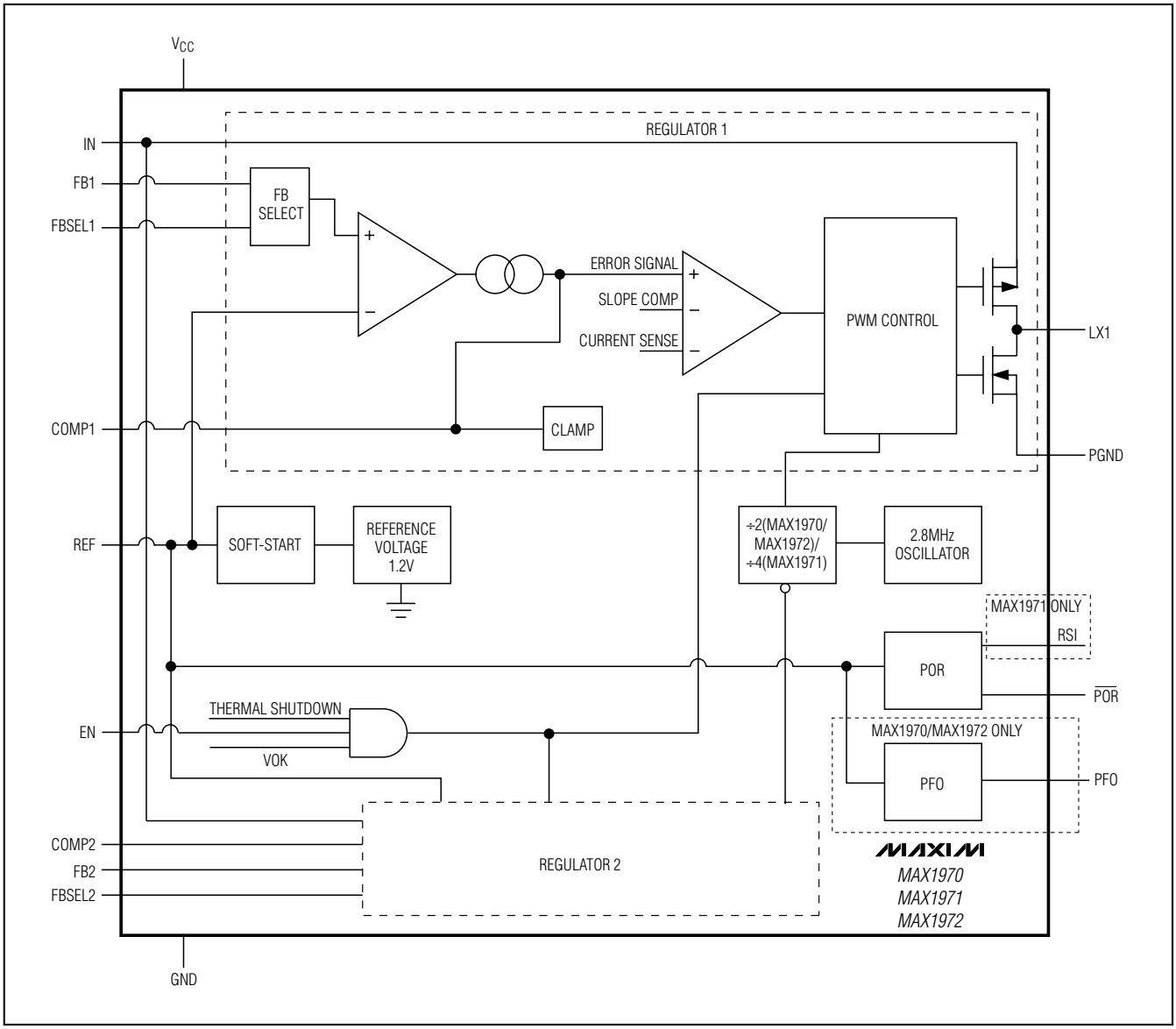



*Figure 1. Functional Diagram*

turns off and the internal low-side n-channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the *Current Limit* section), the high-side MOSFET is not turned on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

### Current Sense

The current-sense circuit amplifies the current-sense voltage generated by the high-side MOSFET's on-resistance and the inductor current ($R_{DS(ON)} \times I_{INDUCTOR}$). This amplified current-sense signal and the internal slope compensation signal are summed together into

the PWM comparator's inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the integrated feedback voltage.

### Current Limit

The internal MOSFET has a current limit of 1.2A (typ). If the current flowing out of LX_ exceeds this maximum, the high-side MOSFET turns off and the synchronous rectifier MOSFET turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. There is also a synchronous rectifier current limit of -0.85A. This is to protect the device from current flowing into LX_. If the negative current limit is exceeded, the synchronous rectifier is turned off, and the inductor current continues to flow through the high-side MOSFET body diode back to the input until the beginning of the next cycle or until the inductor current drops to zero.

### $V_{CC}$ Decoupling

Due to the high-switching frequency and tight output tolerance (±1%), decoupling between IN and $V_{CC}$ is recommended. Connect a 10Ω resistor between IN and $V_{CC}$ and a 0.1µF ceramic capacitor from $V_{CC}$ to GND. Place the resistor and capacitor as close to $V_{CC}$ as possible.

### Startup

To reduce the supply inrush current, soft-start circuitry ramps up the output voltage during startup. This is done by charging the REF capacitor with a current source of 25µA. Once REF reaches 1.2V, the output is in full regulation. The soft-start time is determined from:

$$t_{SS} = \frac{V_{REF}}{I_{REF}} C_{REF} = 4.8 \times 10^4 \times C_{REF}$$

Soft-start occurs when power is first applied, and when EN is pulled high with power already present. The part also goes through soft-start when coming out of undervoltage lockout (UVLO) or thermal shutdown. The range of capacitor values for $C_{REF}$ is from 0.01µF to 1.0µF.

### Undervoltage Lockout

If $V_{CC}$ drops below 2.35V, the MAX1970/MAX1971/MAX1972 assume that the supply voltage is too low to provide a valid output voltage, and the UVLO circuit inhibits switching. Once $V_{CC}$ rises above 2.4V, the UVLO is disabled and the soft-start sequence initiates.

### Enable

A logic-enable input (EN) is provided. For normal operation, drive EN logic high. Driving EN low turns off both outputs, and reduces the input supply current to approximately 1µA.

### Power-Fail Output

The input voltage is sensed for 5V (typical USB applications), and if $V_{CC}$ drops below 3.94V, the power-fail output (PFO) goes high. The time from PFO going high to the outputs going out of regulation depends on the operating output voltage and currents, and the upstream 5V bus storage capacitor value, which is 120µF minimum (per USB specification, version 2.0). The lower the operating voltages and currents, and the higher the storage capacitor, the longer the elapsed time. PFO is an open-drain output, and a 10kΩ to 100kΩ pullup resistor to $V_{CC}$, or either output, is recommended.

### Power-On Reset

Power-on reset ($\overline{POR}$) provides a system reset signal. During power-up, $\overline{POR}$ is held low until both outputs reach 92% of their regulated voltages, $\overline{POR}$ continues to be held low for a delayed period, and then goes high. This delay time ($T_D$) for MAX1970 is 16.6ms. The MAX1971 and MAX1972 have a delay of 175ms. Figure 2 is an example of a timing diagram.

The $\overline{POR}$ comparator is designed to be relatively immune to short-duration negative-going output glitches.The *Typical Operating Characteristics* gives a plot of maximum transient duration vs. $\overline{POR}$ comparator overdrive. The graph was generated using a negative-going pulse applied to an output, starting at 100mV above the actual $\overline{POR}$ threshold, dropping below the $\overline{POR}$ threshold by the percentage indicated as comparator overdrive, and then returning to 100mV above the threshold. The graph indicates the maximum pulse width the output transient can have without causing $\overline{POR}$ to trip low.

### Reset Input

Reset input (RSI) is an input on the MAX1971 that, when driven high, forces the $\overline{POR}$ to go low. When RSI goes low, $\overline{POR}$ goes through a delay time identical to a power-up event. See Figure 2 for timing diagram. RSI allows software to command a system reset. RSI must be high for a minimum period of 1µs in order to initiate the $\overline{POR}$.

### Thermal-Overload Protection

Thermal-overload protection limits total power dissipation. When the IC's junction temperature exceeds $T_J$ = +170°C, a thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by 20°C. This results in a pulsed output during continuous overload conditions.

During a thermal event, $\overline{POR}$ goes low, PFO goes high, and soft-start is reset.

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

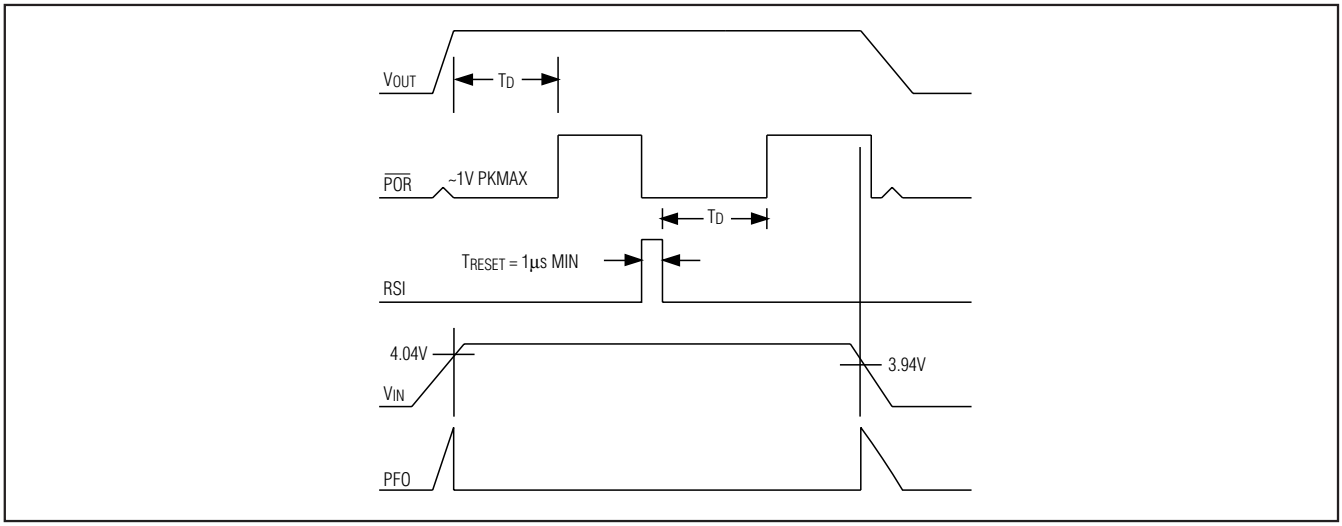



*Figure 2. Timing Diagram*

## Design Procedure

### Output Voltage Selection

Both output voltages can be selected in three different ways as indicated by Table 1. Each output has two preset voltages that can be set using FBSEL_ and it can also be set to any voltage from 0.8V to $V_{IN}$ by using an external resistor voltage-divider.

To use a resistor-divider to set the output voltage to 1.2V or higher (Figure 5), connect a resistor from FB_ to OUT_ ($R_{_a}$), and connect a resistor from FB_ to GND ($R_{_b}$). Select the value of $R_{_b}$, between 10kΩ and 30kΩ. Then $R_{_a}$ is calculated by:

$$R_{_a} = R_{_b} \times \left[ \frac{V_{OUT}}{1.2} - 1 \right]$$

A resistor-divider can also be used to set the voltage of one output from 0.8V to 1.2V. To do this, the other output must be above 1.2V. Figure 6 shows an example of this where OUT1 is set to 1V. To set the output voltage to less than 1.2V, connect a resistor from FB1 to OUT1 (R1), and from FB1 to OUT2 (R2). Select values of R1 and R2 such that current flowing through R1 and R2 is about 100µA and following equation is satisfied:

$$R1 = R2 \frac{V_{OUT1} - 1.2}{1.2 - V_{OUT2}}$$

Each output is capable of continuously sourcing up to 750mA of current as long as the following condition is met:

$$\frac{V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2}}{V_{IN}} \leq 1.05A$$

### Inductor Value

A 3.3µH to 6.8µH inductor with a saturation current of 800mA (min) is recommended for most applications. For best efficiency, the inductor's DC resistance should be less than 100mΩ, and saturation current should be greater than 1A. See Table 2 for recommended inductors and manufacturers.

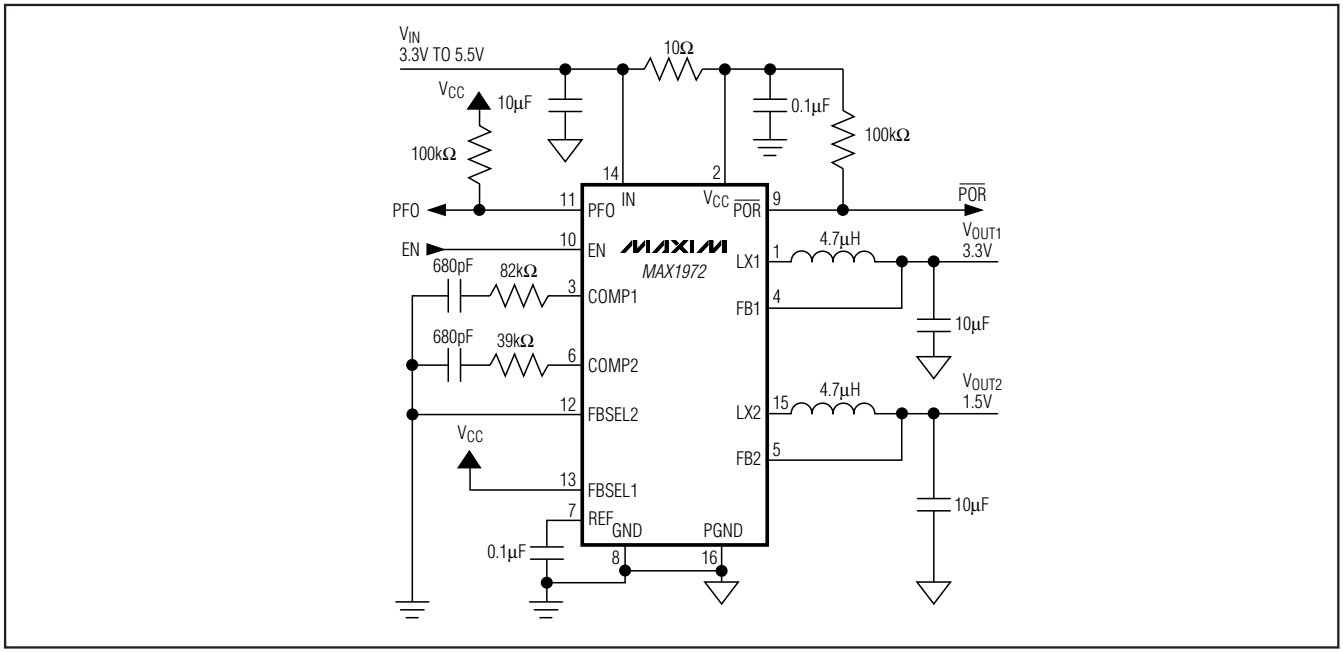



*Figure 3. Typical Application Circuit 1*

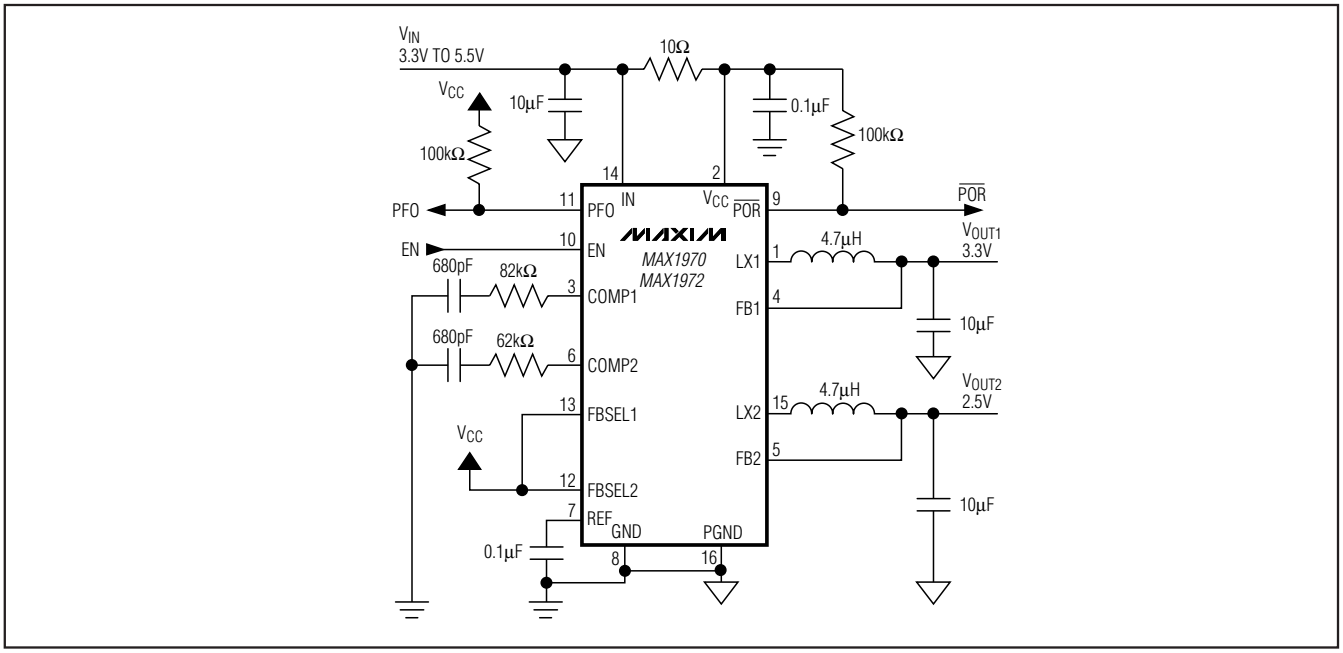



*Figure 4. Typical Application Circuit 2*

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

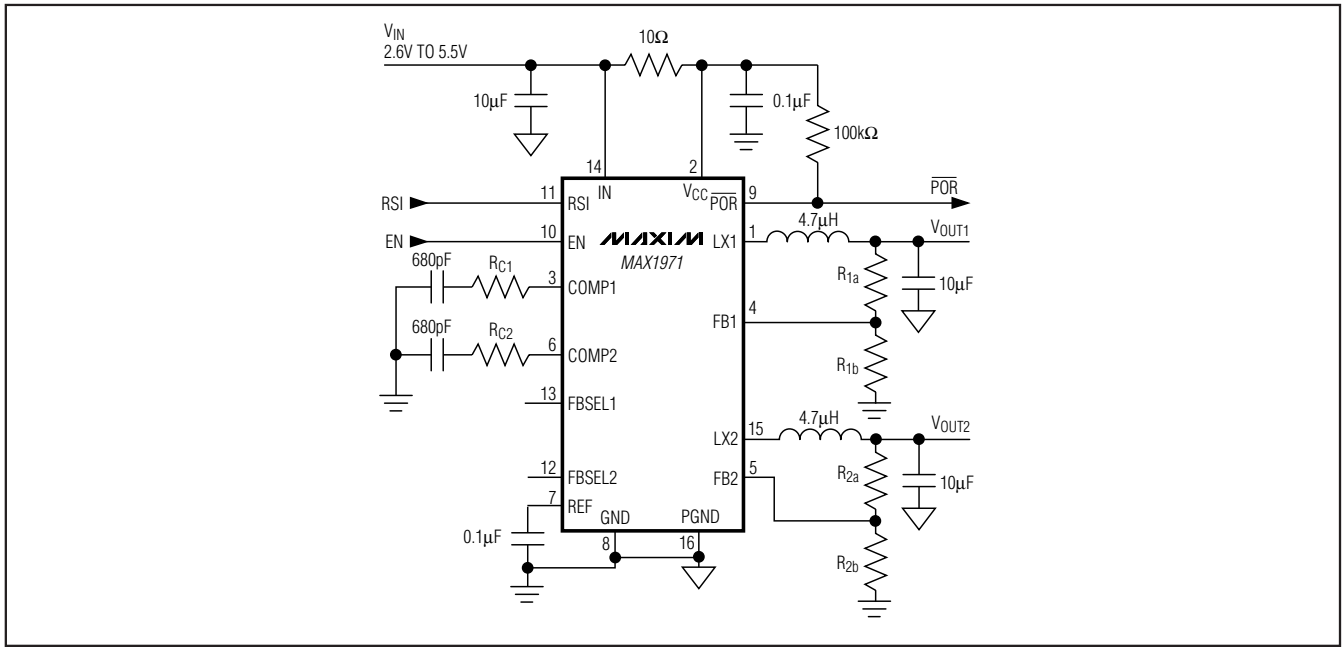



*Figure 5. Setting the Output Voltage with External Resistors*

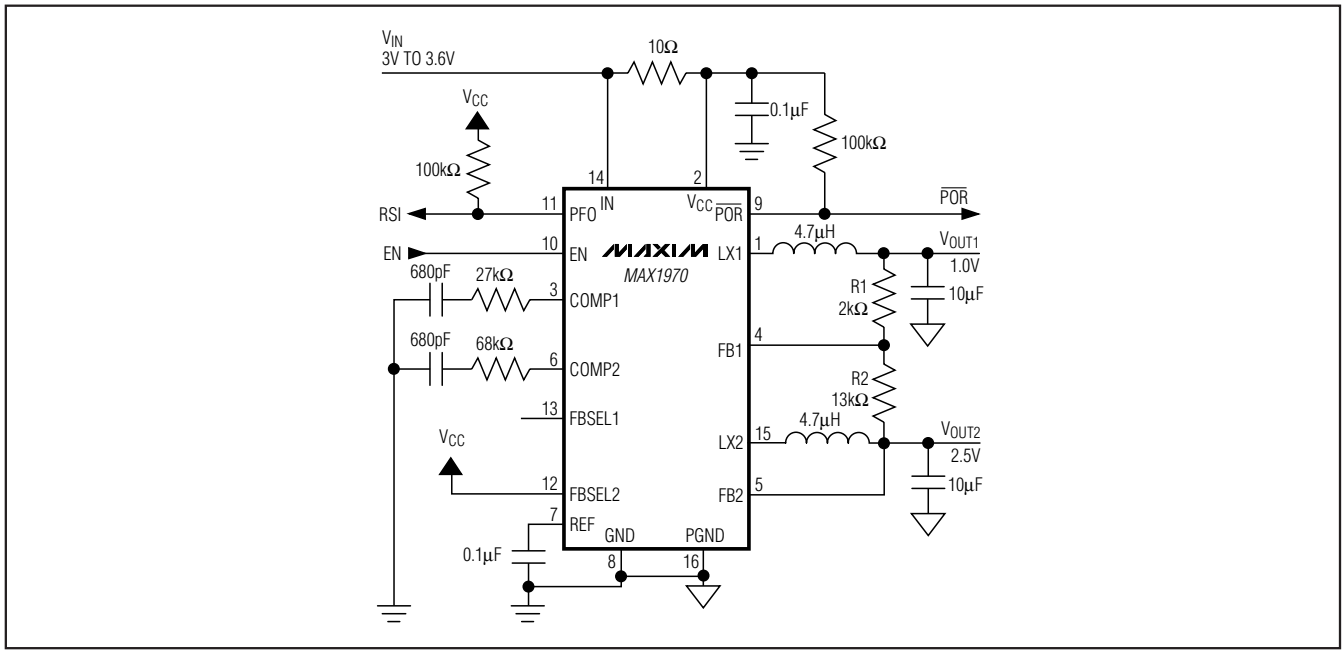



*Figure 6. Setting an Output Below 1.2V*

## Table 1. Output Voltage Settings

| FBSEL1 | OUTPUT 1 | FBSEL2 | OUTPUT 2 |
|---|---|---|---|
| $V_{CC}$ | 3.3V | $V_{CC}$ | 2.5V |
| GND | 1.8V | GND | 1.5V |
| Open | Ext Divider | Open | Ext Divider |

For most designs, a reasonable inductor value ($L_{INIT}$) is derived from the following equation:

$$L_{INIT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{OSC}}$$

Keep the inductor current ripple percentage LIR between 20% and 40% of the maximum load current for best compromise of cost, size, and performance. The maximum inductor current is:

$$I_{L(MAX)} = \left[1 + \frac{LIR}{2}\right] I_{OUT(MAX)}$$

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement ($I_{RMS}$) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{1}{V_{IN}} \sqrt{\begin{array}{l} I_{OUT1}^2 \times V_{OUT1}(V_{IN} - V_{OUT1}) + \\ I_{OUT2}^2 \times V_{OUT2}(V_{IN} - V_{OUT2}) \end{array}}$$

A ceramic capacitor is recommended due to its low equivalent series resistance (ESR), equivalent series inductance (ESL), and lower cost. Choose a capacitor that exhibits less than a 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

### Output Capacitor

The key selection parameters for the output capacitor are its capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter.

The output ripple is due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

The output voltage ripple due to the output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$V_{RIPPLE\ (ESL)} = (I_{P-P}/T_{ON}) \times ESL$ or $(I_{P-P}/T_{OFF}) \times ESL$, whichever is greater.

$I_{P-P}$ is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be set by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Ceramic capacitors are recommended due to their low ESR and ESL at the switching frequency of the converter. For ceramic capacitors, the ripple voltage due to ESL is negligible.

Load transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR × $\Delta I_{LOAD}$. Before the con-

## Table 2. Suggested Inductors

| MANUFACTURER | PART | INDUCTANCE (µH) | ESR (mΩ) | SATURATION CURRENT (A) | DIMENSIONS (mm) |
|---|---|---|---|---|---|
| Coilcraft | DO1606 | 4.7 | 120 | 1.2 | 5.3 × 5.3 × 2 |
| Sumida | CR43-4R7 | 4.7 | 108.7 | 1.15 | 4.5 × 4 × 3.5 |
| Sumida | CDRH3D16-4R7 | 4.7 | 80 | 0.9 | 3.8 × 3.8 × 0.8 |

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

troller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output from deviating further from its regulating value.

### Compensation Design

An internal transconductance error amplifier is used to compensate the control loop. Connect a series resistor and capacitor between COMP and GND to form a pole-zero pair. The external inductor, internal high-side MOSFET, output capacitor, compensation resistor, and compensation capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitor are selected to optimize control-loop stability. The component values shown in the typical application circuits (Figures 3, 4, and 5) yield stable operation over a broad range of input-to-output voltages.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The voltage across the internal high-side MOSFET's on-resistance ($R_{DS(ON)}$) is used to sense the inductor current. Current mode control eliminates the double pole caused by the inductor and output capacitor, which has large phase shift that requires more elaborate error-amplifier compensation. A simple Type 1 compensation with single compensation resistor ($R_C$) and compensation capacitor ($C_C$) is all that is needed to have a stable and high-bandwidth loop.

The basic regulator loop consists of a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain set by gmc x $R_{LOAD}$, with a pole and zero pair set by $R_{LOAD}$, the output capacitor ($C_{OUT}$), and its ESR. Below are equations that define the power modulator:

$$G_{MOD} = gmc \times R_{LOAD}$$

The pole frequency for the modulator is:

$$fp_{MOD} = \frac{1}{2\pi \times C_{OUT} \times (R_{LOAD} + ESR)}$$

The zero frequency for the output capacitor ESR is:

$$fz_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

where, $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, and GMC = 2µS. The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where $V_{FB}$ is equal to 1.2V. The transconductance error amplifier has a DC gain, $G_{EA(DC)}$, of 60dB. A dominant pole is set by the compensation capacitor, $C_C$, the output resistance of the error amplifier ($R_{OEA}$), 20MΩ, and the compensation resistor, $R_C$. A zero is set by $R_C$ and $C_C$.

The pole frequency set by the transconductance amplifier output resistance, and compensation resistor and capacitor is:

$$fp_{EA} = \frac{1}{2\pi \times C_C \times R_{OEA}}$$

The zero frequency set by the compensation capacitor and resistor is:

$$fz_{EA} = \frac{1}{2\pi \times C_C \times R_C}$$

For best stability and response performance, the closed-loop unity-gain frequency must be much higher than the modulator pole frequency. In addition, the closed-loop unity-gain frequency should be approximately 50kHz. The loop gain equation at unity gain frequency then is:

$$G_{EA(fc)} \times G_{MOD(fc)} \times \frac{V_{FB}}{V_O} = 1$$

Where $G_{EA(fc)} = gm_{EA} \times R_C$, and $G_{MOD(fc)} = gmc \times R_{LOAD} \times fp_{MOD}/fc$, where $gm_{EA}$ = 50µS, $R_C$ can be calculated as:

$$R_C = \frac{V_O}{gm_{EA} \times V_{FB} \times G_{MOD(fc)}}$$

The error-amplifier compensation zero formed by $R_C$ and $C_C$ is set at the modulator pole frequency at maximum load. $C_C$ is calculated as follows:

$$C_C = V_{OUT} \times \frac{C_{OUT}}{R_C \times I_{OUT(MAX)}}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly, and the closed-loop unity-gain frequency remains the same. Below is a numerical example to calculate $R_C$ and $C_C$ values of the typical application circuit of Figure 4, where:

$V_{OUT}$ = 2.5V

$I_{OUT(MAX)}$ = 0.6A

$C_{OUT}$ = 10µF

$R_{ESR}$ = 0.010Ω

$gm_{EA}$ = 50µS

$gm_C$ = 2S

$f_{SWITCH}$ = 1.4MHz

$R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$ = 2.5V/0.6A = 4.167Ω

$fp_{MOD} = 1/[2\pi\ C_{OUT}\ (R_{LOAD} + R_{ESR})] = 1/[2\pi \times 10 \times 10^{-6}\ (4.167 + 0.01)]$ = 3.80kHz.

$fz_{ESR} = 1/[2\pi\ C_{OUT}\ R_{ESR}] = 1/[2\pi \times 10 \times 10^{-6} \times 0.01]$ = 1.59MHz.

Pick a closed-loop unity-gain frequency ($f_C$) of 50kHz. The power modulator gain at fc is:

$G_{MOD}(fc) = gmc \times R_{LOAD} \times fp_{MOD}/f_C = 2 \times 4.167 \times 3.80k/50k$ = 0.635

then:

$R_C = V_O/(gm_{EA}\ V_{FB}\ G_{MOD}(fc)) = 2.5/(50 \times 10^{-6} \times 1.2 \times 0.635) \approx 62k\Omega$

$C_C = V_{OUT} \times (C_{OUT}/R_C) \times I_{OUT}(MAX) = 2.5 \times 4.7 \times 10^{-6}/62k \times 0.6 \approx 680pF$

## Applications Information

### PCB Layout

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close to IC pins as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate. Connect the two ground planes together with a single connection from PGND to GND.
2) Input and output capacitors are connected to the power ground plane; all other capacitors are connected to signal ground plane.
3) Keep the high-current paths as short and wide as possible.
4) If possible, connect IN, LX1, LX2, and PGND separately to a large land area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB1, FB2, COMP1, COMP2).

# Dual, 180° Out-of-Phase, 1.4MHz, 750mA Step-Down Regulator with POR and RSI/PFO

## Chip Information

TRANSISTOR COUNT: 5428

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 16 QSOP | E16-5 | **21-0055** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/02 | Initial release | — |
| 1 | 2/09 | Updated formula in the *Output Voltage Selection* section. | 14 |

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