*Click **here** for production status of specific part numbers.*

MAX20078

Synchronous Buck, High-Brightness LED Controller

General Description

The MAX20078 is a high-voltage, synchronous n-channel MOSFET controller for high-current buck LED drivers. The device uses a proprietary average current-mode-control scheme to regulate the inductor current. This control method does not need any control-loop compensation while maintaining nearly constant switching frequency. Inductor current sense is achieved by sensing the current in the bottom synchronous n-channel MOSFET. It does not require any current sense at high voltages. The device operates over a wide 4.5V to 65V input range. The device is designed for high-frequency operation and can operate at switching frequencies as high as 1MHz. The high- and low-side gate drivers have peak source and sink current capability of 2A. The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The device includes both analog and PWM dimming. The device includes a 5V V_{CC} regulator capable of delivering 10mA to external circuitry. The device also includes a current monitor that provides an analog voltage proportional to the inductor current. The device has a fault flag that indicates open and shorts across the output. Protection features include inductor current-limit protection, overvoltage protection, and thermal shutdown. The MAX20078 is available in a space-saving (3mm x 3mm), 16-pin TQFN or a 16-pin TSSOP package and is specified to operate over the -40°C to +125°C automotive temperature range.

***Ordering Information** appears at end of data sheet.*

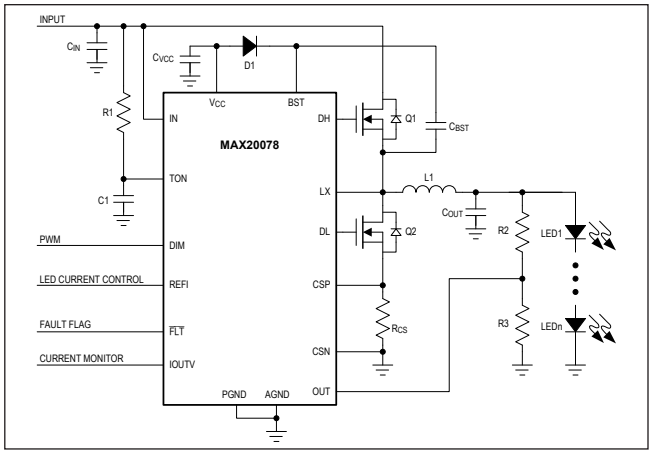
Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Wide Input Voltage Range: 4.5V to 65V
- Easy to Design
  - No Compensation Components
  - Programmable Switching Frequency
- Wide Dimming Ratio Allows High Contrast Ratio
  - Analog Dimming
  - PWM Dimming
- Suitable for Matrix Lighting
  - Maintains Current Regulation While Shorting/Opening Individual LEDs in the String
  - Ultrafast-Response Control Loop Prevents Overshoots and Undershoots
- Fault Detection and Protection
  - Overvoltage Protection
  - Open and Short Detection
  - Thermal Shutdown
  - Inductor Current Monitor
- Low-Power Shutdown Mode

Applications

- Automotive Front Lights
- Automotive Matrix Lights
- Head-Up Displays
- Constant-Current Regulators

Simplified Schematic



maxim integrated™

Absolute Maximum Ratings

IN, DIM, TON to AGND .....-0.3V to +70V
LX to AGND.....-1.0V to +70V
BST to AGND .....-0.3V to +75V
BST, DH to LX.....-0.3V to +6V
DH to AGND.....-0.3V to +75V
DL to AGND.....-0.3V to +V_{CC}
V_{CC} to AGND .....-0.3V to lower of (V_{IN} + 0.3V) and +6V
CSP, CSN to AGND.....-2.5V to +V_{CC}
OUT, $\overline{FLT}$, IOUTV to AGND.....-0.3V to +6V
PGND to AGND.....-0.3V to +0.3V
REFI .....-0.3V to +2.5V
V_{CC} Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C) (Note 1)
16-Pin TQFN-EP
(derate 24.4 mW/°C above +70°C) 1951.2mW
16-Pin TSSOP-EP
(derate 25.6 mW/°C above +70°C) 2051.3mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

16 TQFN-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....7°C/W

16 TSSOP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{DIM} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}		4.5		65	V
		IN connected to V_{CC}	4.5		5.5	
Quiescent Current	I_Q	V_{DIM} = 5V, V_{IN} = 65V		2	4	mA
Shutdown Current	I_{SHDN}	V_{DIM} = 0V, V_{IN} = 12V		8	15	µA
		V_{DIM} = 0V, V_{IN} = 65V		12	30	
V_{CC} REGULATOR						
Output Voltage	V_{CC}	5.5V < V_{IN} < 65V; I_{VCC} = 1mA 6V < V_{IN} < 25V; I_{VCC} = 10mA	4.85	5	5.15	V
Dropout Voltage	$V_{CC\ DROP}$	V_{IN} = 4.5V, I_{VCC} = 5mA		0.07	0.15	V
V_{CC} UVLO Rising	$V_{CC\ UVLOR}$	Rising	3.8	4.1	4.4	V
V_{CC} UVLO Falling	$V_{CC\ UVLOFALL}$	Falling	3.55	3.8	4.0	V
Short-Circuit Current Limit	I_{VCC_SC}	V_{CC} shorted to AGND		80		mA

Electrical Characteristics (continued)

(V_{IN} = V_{DIM} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH and DL DRIVERS						
DH Sourcing Resistance	R_{DH_SRC}	DH = high, T_A = -40°C to +125°C		2.5	5.0	Ω
DH Sinking Resistance	R_{DH_SINK}	DH = low, T_A = -40°C to +125°C		1.0	2.0	Ω
DL Sourcing Resistance	R_{DL_SRC}	DL = low, T_A = -40°C to +125°C		2.5	5.0	Ω
DL Sinking Resistance	R_{DL_SINK}	DL = low, T_A = -40°C to +125°C		1.5	3.0	Ω
DH-to-DL Dead Time		DH fall to DL rise		20		ns
DL-to-DH Dead Time		DL fall to DH rise		20		ns
ON-TIME CONTROL/OVERVOLTAGE PROTECTION/SHORT-FAULT INDICATOR						
Minimum On-Time	t_{ON_MIN}			80	110	ns
Programmed On-Time		V_{OUT} = 1V, R1 = 50kΩ, C1 = 1nF		4.55		µs
Maximum On-Time	t_{ON_MAX}	t_{ON} = AGND, V_{OUT} = 1V		24		µs
TON Pulldown Resistance		V_{IN} = 65V, R1 > 20kΩ		15	30	Ω
TON Threshold to DH Falling Delay	$t_{D\text{-}ON}$			65		ns
OUT Overvoltage Threshold	V_{TH_OVP}	OUT rising	2.9	3.0	3.1	V
OUT Overvoltage Hysteresis		OUT falling		0.02		V
Short-Fault Threshold	OUT_{V_SHF}	Output falling, V_{OUT} is lower than threshold		50		mV
OFF-TIME CONTROL						
Minimum Off-Time		CS = 0V		200		ns
CS Comparator Propagation Delay				65		ns
Linear Range of Pulse Doubler			0		5	µs
Maximum Off-Time				42		µs
ANALOG DIMMING INPUT						
REFI Input Voltage Range	$REFI_{RNG}$		0.2		1.2	V
REFI Zero-Current Threshold	$REFI_{ZC_VTH}$	V_{CS} < 5mV	0.165	0.18	0.195	V
REFI Clamp Voltage	$REFI_{CLMP}$	I_{REFI} sink = 1µA	1.274	1.3	1.326	V
REFI Input Bias Current	$REFI_{IN}$	V_{REFI} = 0 to 2V	0	20	200	nA
CURRENT-SENSE AMPLIFIER						
Current-Sense Amplifier Offset			0.18	0.2	0.22	V
Current-Sense Gain			4.9	5.0	5.05	V/V

Electrical Characteristics (continued)

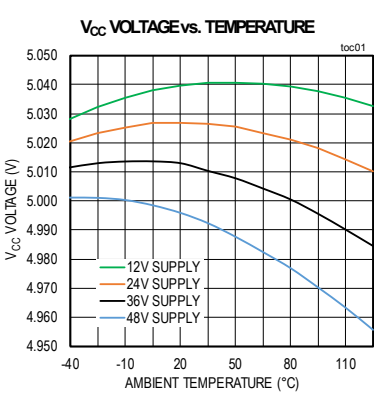
(V_{IN} = V_{DIM} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

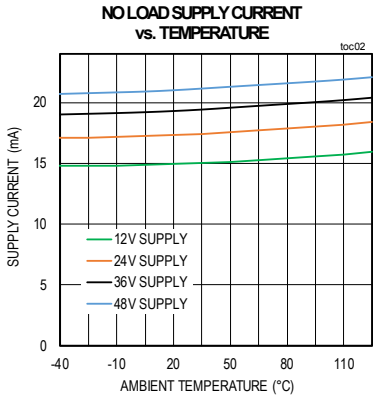
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM DIMMING						
DIM Rising Threshold	DIM_{VTHR}	DIM rising	2.0			V
DIM Falling Threshold	DIM_{VTHF}	DIM falling			0.8	V
DIM Rising-to-DL Rising Delay	t_{DIM_RIS}	DIM rising		40		ns
DIM Shutdown Detect Timer	t_{SHDW}	DIM low duration to enter shutdown mode	180	200	220	ms
CURRENT MONITOR						
Current Monitor Amplifier Gain		$V_{(CSP - CSN)}$ < 200mV		5		V/V
Offset Voltage	V_{THDIML}			0.2		V
FAULT FLAG						
$\overline{FLT}$ Output Voltage	$\overline{FLT}_V$	I_{SINK} is 1mA after fault		0.05	0.3	V
$\overline{FLT}$ Leakage Current	$\overline{FLT}_{LGK}$	$V_{\overline{FLT}}$ = 5.5V			1	µA
LED Open-Fault REFI Range	LOF_{REFI_RNG}		300	325	350	mV
LED Open-Fault Threshold	LOF_{TH}	V_{IOUTV} is lower than the threshold when DIM is high	10	25	40	%
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	$T_{SHUTDOWN}$	Temperature rising		165		°C
Thermal-Shutdown Hysteresis	T_{HYS}			15		°C

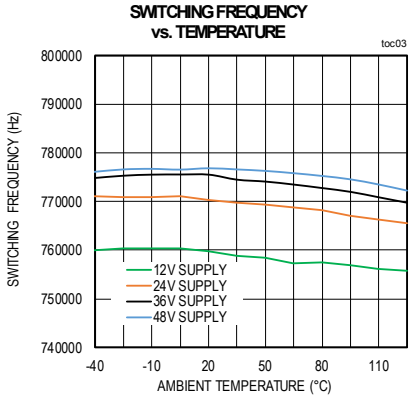
Note 2: Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

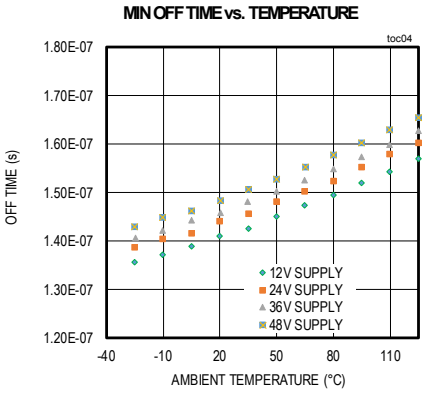
Typical Operating Characteristics

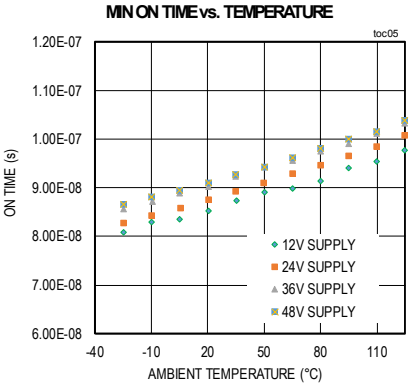
Data taken on Typical Operating Circuit

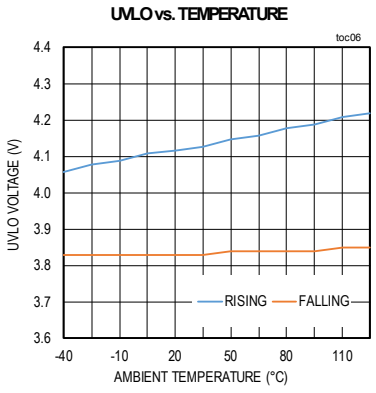


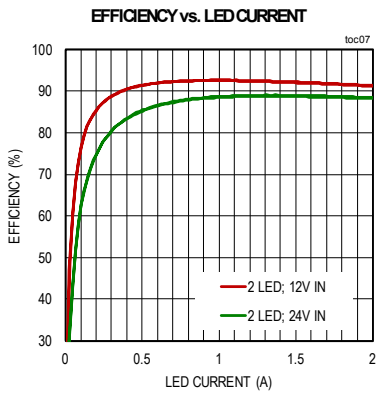








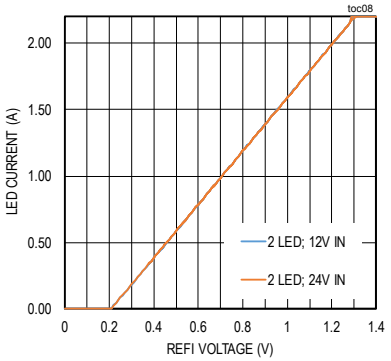




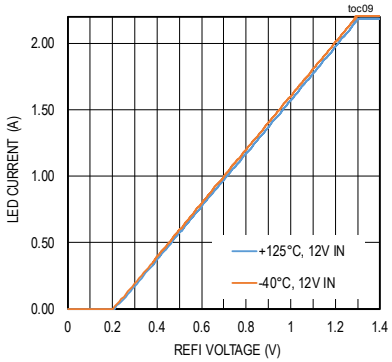
Typical Operating Characteristics (continued)

Data taken on Typical Operating Circuit

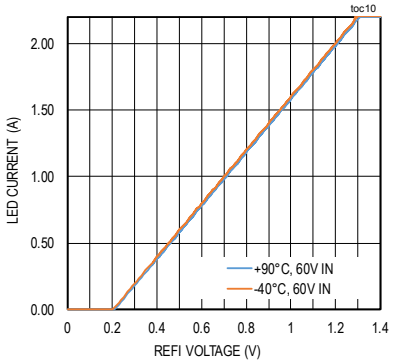
LED CURRENT vs. REFI VOLTAGE



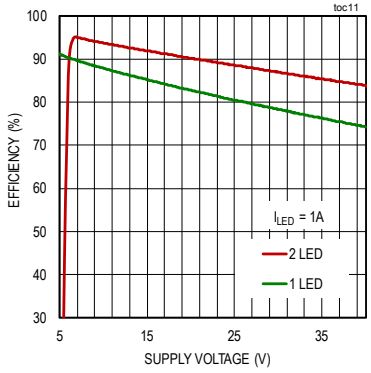
LED CURRENT vs. REFI VOLTAGE



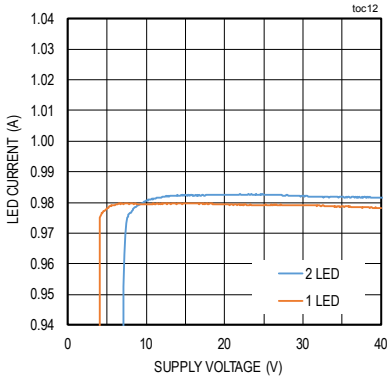
LED CURRENT vs. REFI VOLTAGE



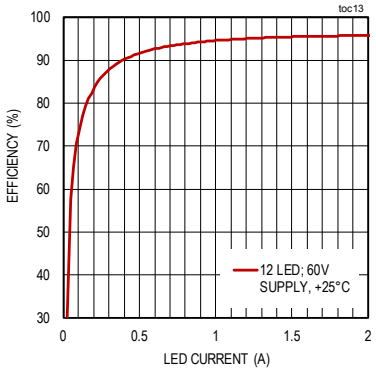
EFFICIENCY vs. SUPPLY VOLTAGE



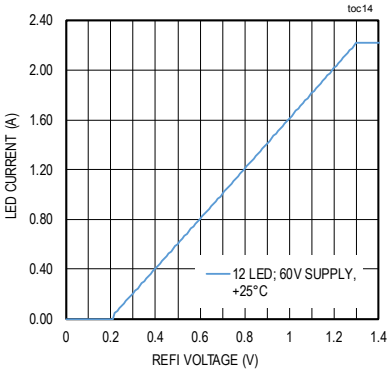
LED CURRENT vs. SUPPLY VOLTAGE



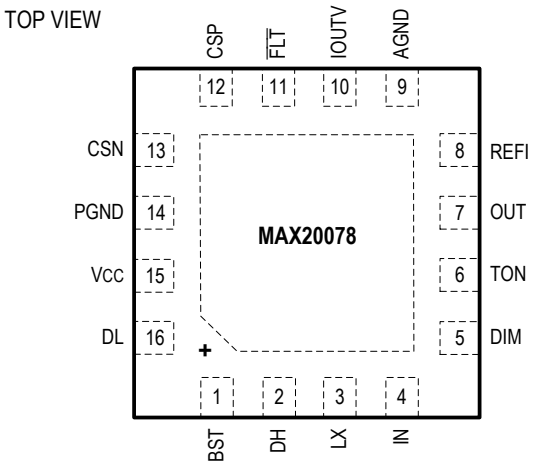
EFFICIENCY vs. LED CURRENT



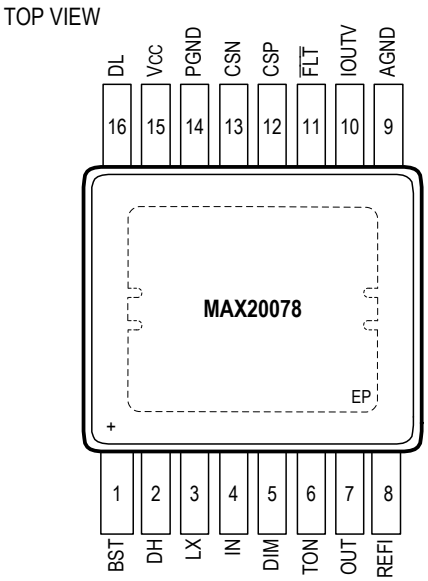
LED CURRENT vs. REFI VOLTAGE



Pin Configurations



TQFN-EP/TQFN-EP (SW)
3mm x 3mm

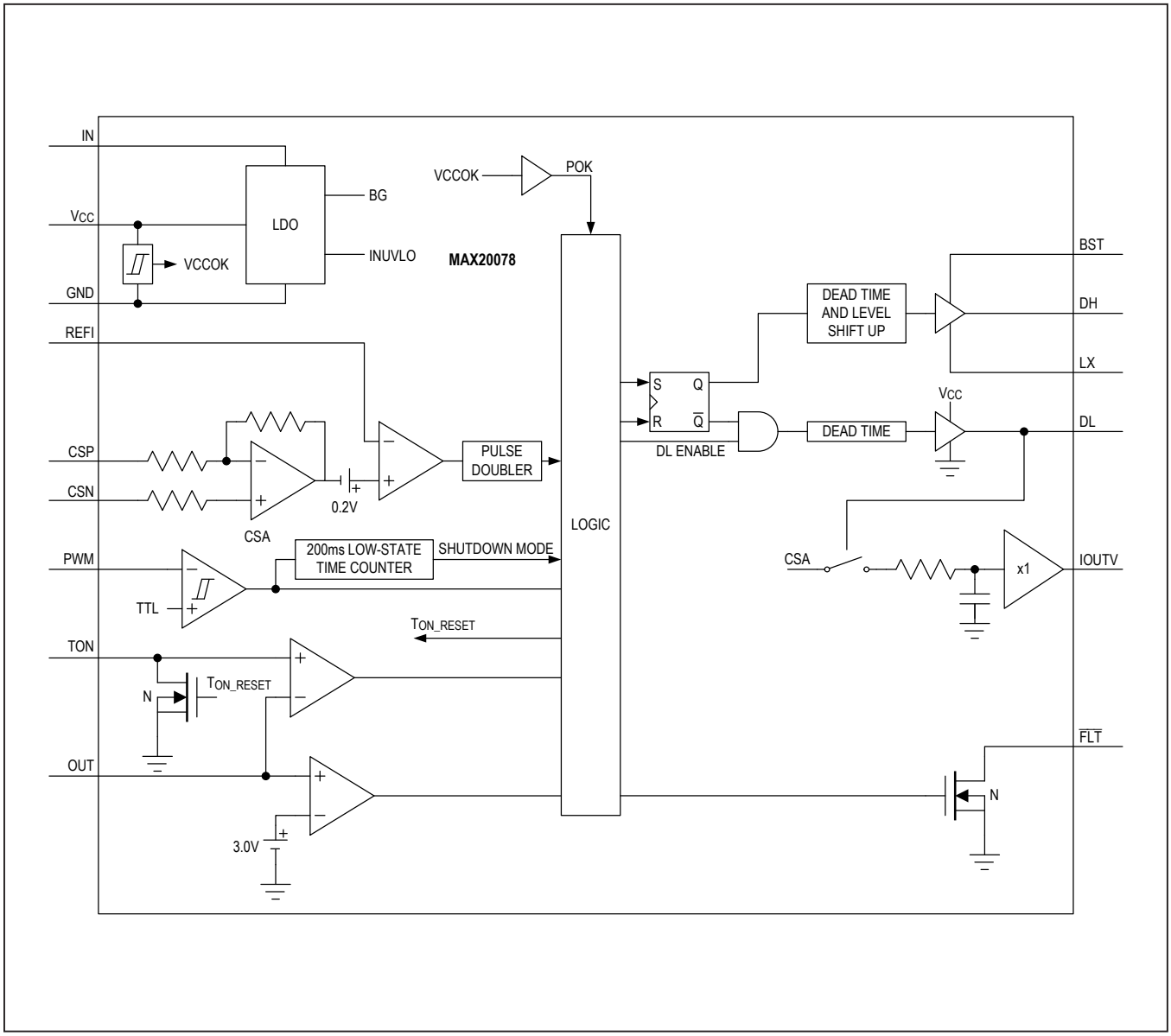


TSSOP-EP

Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	1	BST	High-Side Power Supply for High-Side Gate Drive. Connect a 0.1µF ceramic capacitor from BST to LX.
2	2	DH	Connect to Gate of High-Side n-Channel MOSFET of Buck LED Driver. Use series resistor to limit current slew rate and mitigate EMI noise if required.
3	3	LX	Switching Node of Buck LED Driver. Connect to one end of output inductor.
4	4	IN	Bias Supply Input. Connect a 4.5V to 65V supply to IN. Bypass to ground with a 2.2µF ceramic capacitor.
5	5	DIM	Connect DIM to an External PWM Signal for PWM Dimming
6	6	TON	Connect a Resistor to the Input Supply and Capacitor to AGND to Set Switching Frequency
7	7	OUT	Connect a Resistor-Divider from OUT to the Output Voltage. This pin has the scaled-down measurement of the output voltage.
8	8	REFI	Analog Dimming-Control Input. Connect an analog voltage from 0 to 1.2V for analog dimming of LED current.
9	9	AGND	Analog Ground Connection
10	10	IOUTV	Analog Voltage Indication of Inductor Current. Bypass to ground with a 1µF ceramic capacitor.
11	11	$\overline{FLT}$	Open-Drain Fault Output. See the *Fault Indicator (FLT)* section for information.
12	12	CSP	Connect to source of external MOSFET that is driven by DL. Connect a resistor from this pin to CSN to sense the current in the MOSFET.
13	13	CSN	Connect Directly to the Other End of the Current-Sense Resistor. This end is also connected to the power-ground plane.
14	14	PGND	Power-Ground Connection
15	15	V_{CC}	5V Regulator Output. Connect a 2.2µF ceramic capacitor to AGND from V_{CC} for stable operation.
16	16	DL	Connect to Gate of Low-Side n-Channel MOSFET of Buck LED Driver. Use series resistor to limit current slew rate and mitigate EMI noise if required.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous-copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP **must** be connected to AGND.

Block Diagram



Detailed Description

The MAX20078 is a high-voltage, synchronous n-channel MOSFET controller for high-current buck LED drivers. The device uses a proprietary average current-mode-control scheme to regulate the inductor current. This control method does not need any control-loop compensation while maintaining nearly constant switching frequency. Inductor current sense is achieved by sensing the current in the bottom synchronous n-channel MOSFET. It does not require any current sense at high voltages. The device operates over a wide 4.5V to 65V input range. The device is designed for high-frequency operation and can operate at switching frequencies as high as 1MHz. The high- and low-side gate drivers have peak source and sink current capability of 2A. The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The device includes both analog and PWM dimming. The device includes a 5V V_{CC} regulator capable of delivering 10mA to external circuitry. The device also includes a current monitor that provides an analog voltage proportional to the inductor current. The device has a fault flag that indicates open and shorts across the output. Protection features include inductor current-limit protection, over-voltage protection, and thermal shutdown. The MAX20078 is available in a space-saving (3mm x 3mm), 16-pin TQFN or a 16-pin TSSOP package and is specified to operate over the -40°C to +125°C automotive temperature range.

New Average Current-Mode-Controlled Architecture

The device uses a new average current-mode-control scheme to regulate the current in the output inductor of the buck LED driver. The inductor current is not directly sensed. The device senses the current in the bottom synchronous switch. See Figure 1 for the location of the current-sense resistor (R_{CS}). In a buck converter, operating in continuous-conduction mode, when the top switch is turned off the current in the inductor also flows in

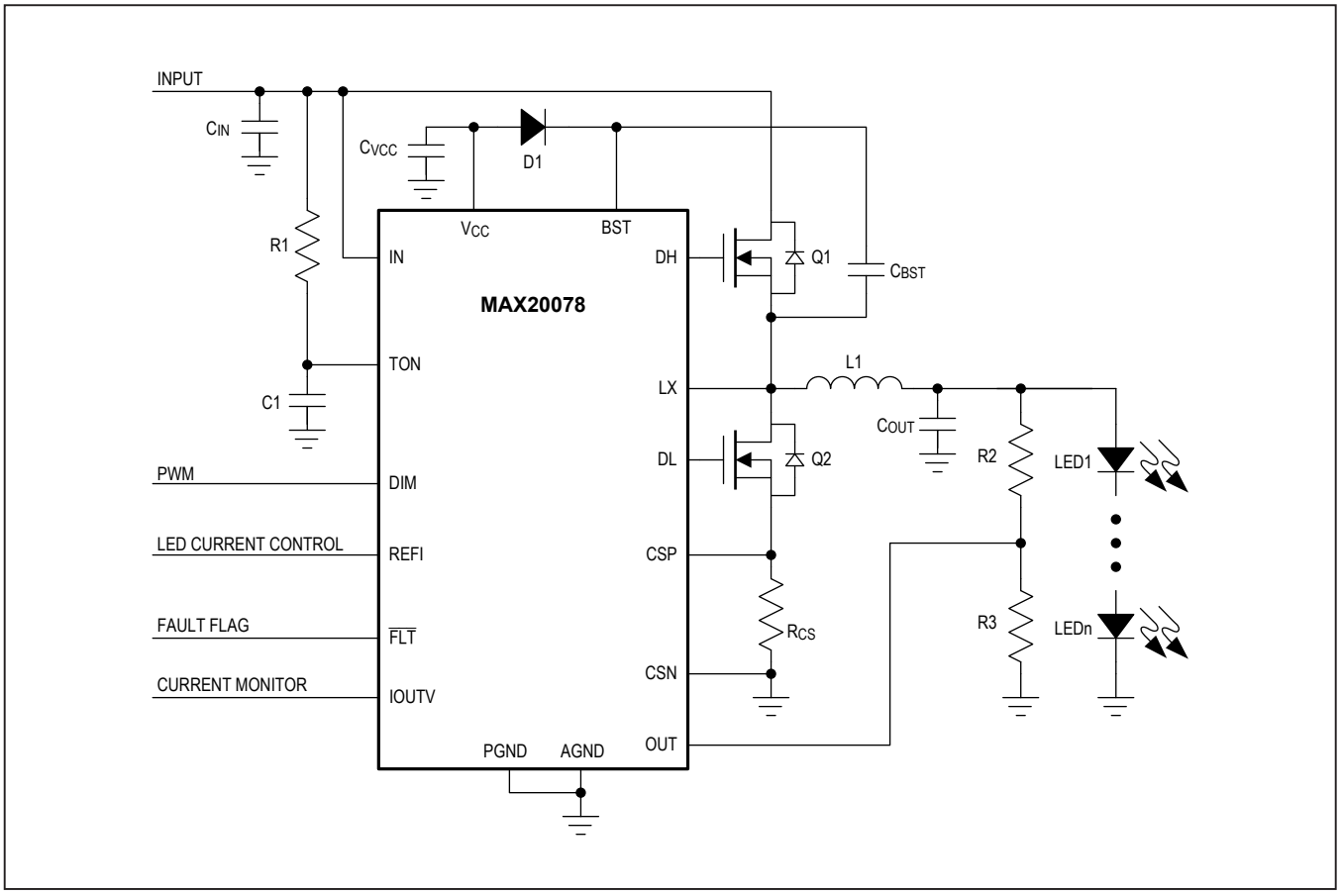


Figure 1. Application Circuit Using the MAX20078

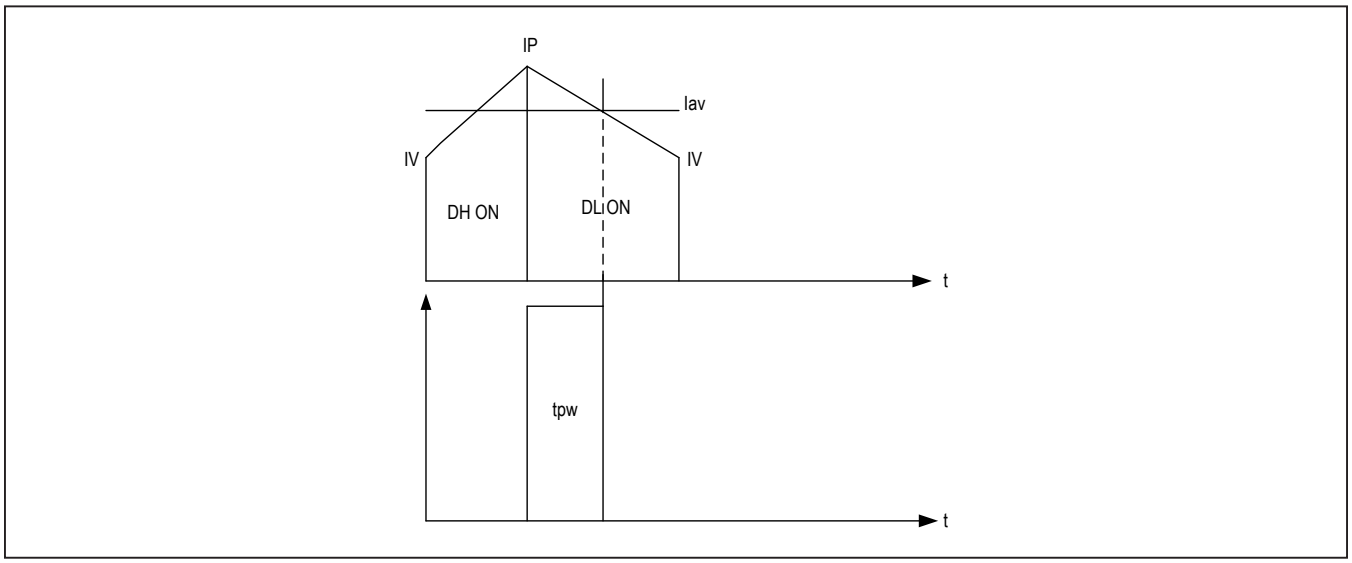


Figure 2. Inductor Current Waveform in One Full Switching Cycle

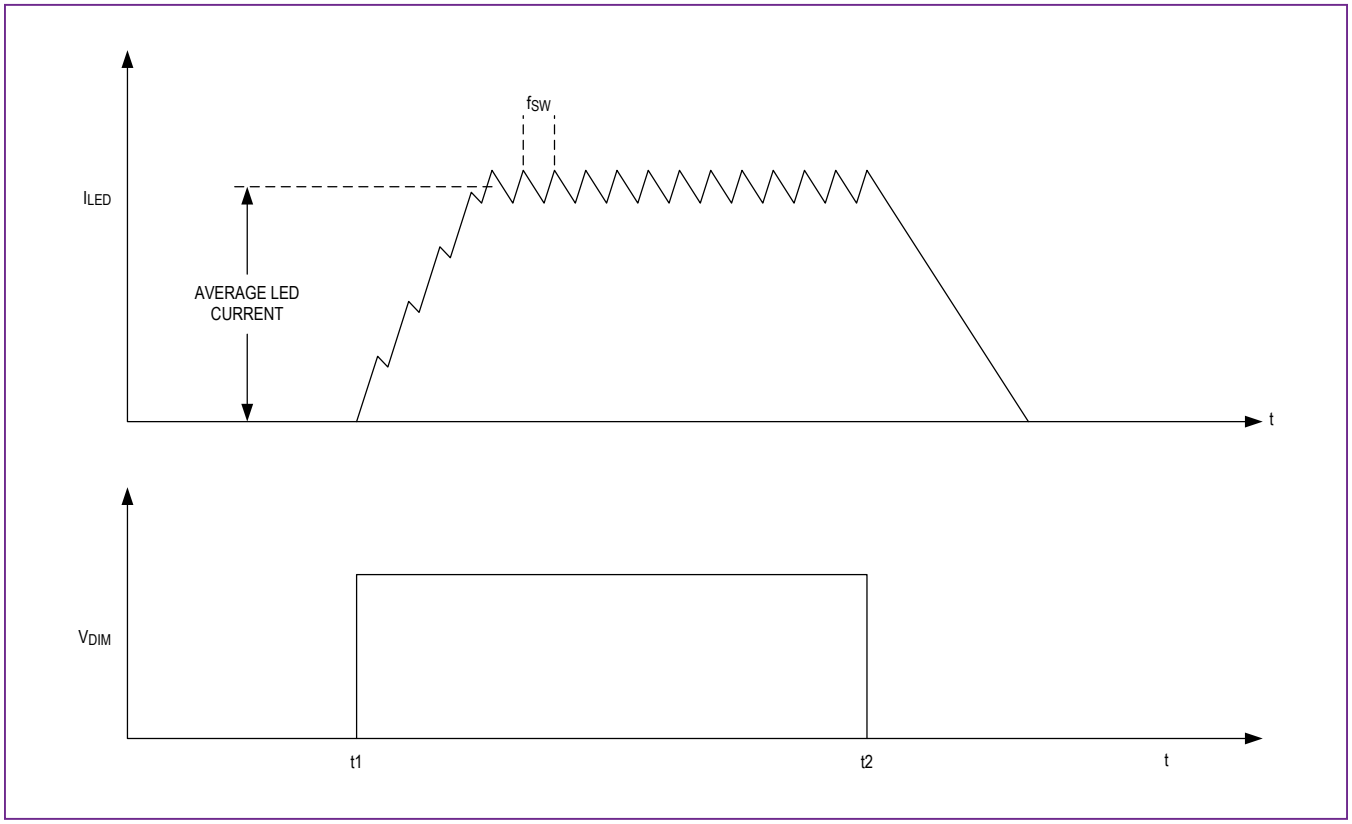


Figure 3. Operation During PWM Dimming When PWM Signal is Applied at PWM Pin

the bottom switch or diode. This peak current is Ip. When the bottom switch is turned off and the top switch is then turned on the current in the switch is the same as the current in the inductor, and it is Iv. The average current in the inductor is given by Iav = 0.5(Ip + Iv). Iav is the same as the output current, Io. If the bottom switch current is sensed at exactly half of the bottom switch period, the current in the switch would be Iav. A pulse doubler is used to determine the on-time of the bottom switch:

$$t_{OFF} = 2 \times t_{PW}$$

where t_{PW} is the high-state pulse width of the internal comparator in the device.

The on-time is determined based on the external resistor (R1) connected between TON and the input voltage, in combination with a capacitor (C1) between R1 and AGND/PGND pins. The input voltage and the R1 resistor set the current sourced into the capacitor (C1), which governs the ramp speed. The ramp threshold is proportional to scaled-down feedback of the output voltage at the OUT pin. The proportionality of V_{OUT} is set by an external resistor-divider (R2, R3) from V_{OUT}.

$$t_{ON}V_{IN}/R1 = C1\ (V_{OUT} \times R3/(R3 + R2))$$

$$t_{ON} = KV_{OUT}/V_{IN}$$

where K = C1R3R1/(R3 + R2)

In the case of a buck converter $t_{ON}V_{IN}$ is also given by:

$$t_{ON} = V_{OUT}/V_{IN}f_{SW}$$

where f_{SW} is the switching frequency.

Based on that, the switching frequency in case of the new average current-mode-controlled architecture is given by:

$$f_{SW} = 1/K \text{ or } f_{SW} = (R3 + R2)/(C1R3R1)$$

In the actual application, there are slight variations in switching frequency due to the voltage drops in the switches and the inductor, the propagation delay from the TON input to the LX switching node, and the nonlinear current charging the TON capacitor. These effects have been ignored in the calculations for switching frequency.

Analog Dimming

The device has an analog dimming-control input (REFI). The voltage at REFI sets the LED current level when $V_{REFI} \le 1.2V$. For $V_{REFI} > 1.3V$, REFI is clamped to 1.3V (typ). The maximum withstand voltage of this input is 2V. The LED current is guaranteed to be at zero when the REFI voltage is at or below 0.18V. The LED current can be linearly adjusted from zero to full scale for the REFI voltage in the range of 0.2V to 1.2V.

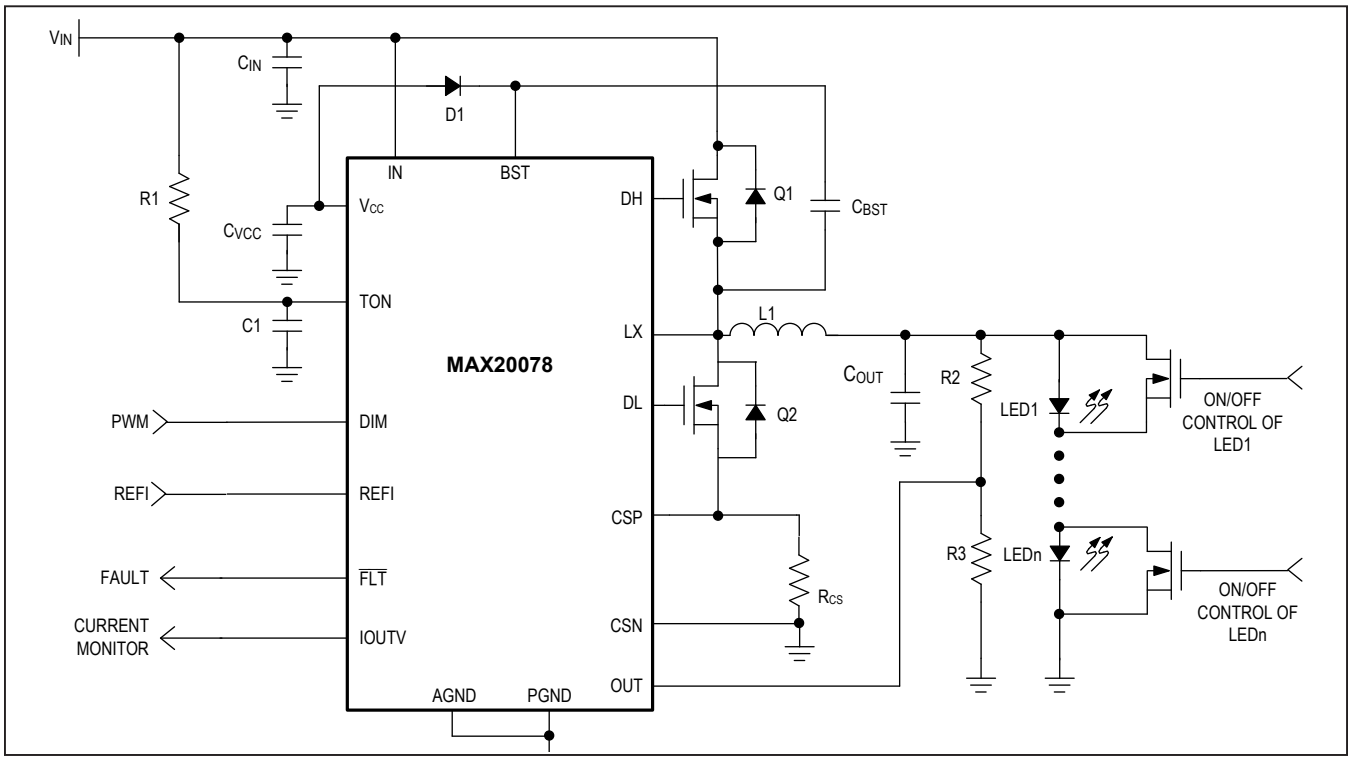


Figure 4. Dimming of Individual LEDs in the Entire String

PWM Dimming

The DIM pin functions as the PWM dimming input of the LEDs. The DIM pin can be driven with a PWM signal that controls the dimming operation of the device. When the DIM signal is high, the switching of the synchronous MOSFETs in the buck LED driver is enabled, but when DIM goes low, both the high- and low-side MOSFETs are turned off. The LED current waveform is shown in Figure 3. The device goes into shutdown mode if the DIM input is below the ON threshold minus the hysteresis for 210ms. In shutdown mode, the input current is less than 5µA (typ).

Dimming by Shorting Individual LEDs in the String

Extremely fast dimming of individual LEDs in the string can be done by applying a shorting FET across each LED, as shown in Figure 4. This application is used in matrix lighting where individual LEDs in the string are controlled by a shorting MOSFET across each LED. Each LED in the string can be turned on and off without any impact on the brightness of the other LEDs in the string by this method. If required, the entire string can be shorted at the same time while still maintaining current regulation in the inductor with minimal overshoot or undershoot. The rise and fall times of the currents in each LED are extremely fast. With this method, only the speed of the parallel-shunt MOSFET limits the dimming frequency and dimming duty cycle. Minimize the output capacitor (C_{OUT}) to minimize current spikes due to the discharge of this capacitor into the LEDs when the shorting FETs are turned on. In some applications, this capacitor can be completely eliminated.

5V Regulator

A regulated 5V output is provided for driving the gates of the external MOSFETs and other external circuitry with a current up to 10mA. Bypass V_{CC} to AGND/PGND with a minimum of 2.2µF ceramic capacitor, positioned as close as possible to the device. In certain applications when an external regulated 5V supply is available, the IN and V_{CC} pins can be connected together and the regulated 5V can be applied directly to V_{CC} saving the power dissipation in the internal regulator of the device.

Overvoltage Protection

The device has programmable overvoltage protection by using the resistor-divider at the OUT pin. The overvoltage setpoint is defined by:

$$V_{OVP_ON} = \frac{3.0\ (R2 + R3)}{R3}$$

If the output voltage reaches V_{OVP_ON}, the DH and DL pins are pulled low to prevent damage to the LEDs or the rest of the circuit. The OVP circuit has a fixed hysteresis of 20mV before the driver attempts to switch again.

High-Side Gate-Drive Supply

The high-side MOSFET is turned on by closing an internal switch between BST and DH and transferring the bootstrap capacitor's (at BST) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor. The selected n-channel high-side MOSFET determines the appropriate boost capacitance values (C_{BST} in the *Typical Operating Circuit*), according to the following equation:

$$C_{BST} = Q_G/\Delta V_{BST}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV to 300mV) when determining C_{BST}. Use a Schottky diode when efficiency is most important, as this maximizes the gate-drive voltage. If the quiescent current at high temperature is important, it may be necessary to use a low-leakage switching diode. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases. A minimum value of 220nF is recommended when using a Schottky diode.

Current Monitor

The device includes a current monitor on the IOUTV pin. The IOUTV voltage is an analog voltage indication of the inductor current when DIM is high. The current-sense signal on the bottom MOSFET across R_{CS} is inverted and amplified by a factor of 5 by an inverting amplifier inside the device. An added offset voltage of 0.2V is also added to this voltage. This amplified signal goes through a sample and hold switch. The sample and hold switch is controlled by the DL signal. The sample and hold switch is turned on only when DL is high and is off when DL is low. This provides a signal on the output of the sample and hold that is a true representation of the inductor current when DIM is high. The sample and hold signal passes through an RC filter and then the buffered output is available on the IOUTV pin. The voltage on the IOUTV pin is given by:

$$V_{IOUTV} = I_{LED} \times R_{CS} \times 5 + 0.2V$$

where I_{LED} is the LED current, which is the same as the average inductor current when DIM is high. V_{IOUTV} indicates the same voltage when DIM goes low that was indicated by V_{IOUTV} when DIM was high prior to it going low.

Thermal Shutdown

Internal thermal-shutdown circuitry is provided to protect the device in the event the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with a 15°C hysteresis (both values typical). During thermal shutdown, the low- and high-side gate drivers are disabled.

Fault Indicator ($\overline{FLT}$)

The device features an active-low, open-drain fault indicator ($\overline{FLT}$). The $\overline{FLT}$ pin goes low under the following conditions.

Short-Circuit Condition Across the LED String

When the LED string is shorted and the OUT pin voltage goes below the short threshold of 50mV for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the short detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once the $\overline{FLT}$ is asserted when the DIM is high, it stays asserted until the fault condition is removed.

Open LED Detection

When the LED string is opened and the IOUTV pin voltage drops to lower than 75% of the targeted voltage for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the open detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once the $\overline{FLT}$ is asserted when the DIM is high, it stays asserted until the fault condition is removed. The LED open detection works only when the REFI pin is greater than 325mV.

Overvoltage Detection

When the voltage on the OUT pin exceeds the over-voltage threshold of 3V for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the over-voltage detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once the $\overline{FLT}$ is asserted when the DIM is high, it stays asserted till the fault condition is removed.

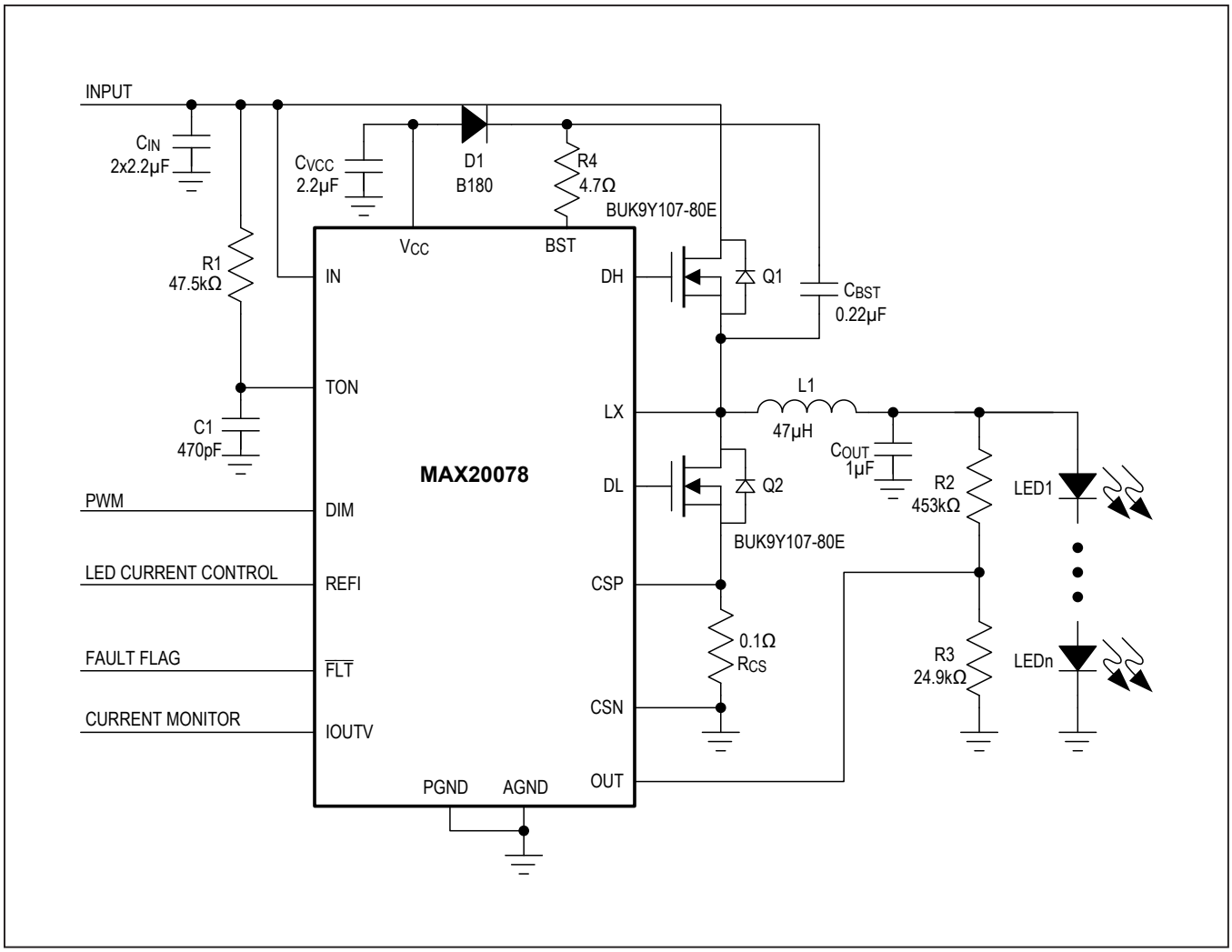
Thermal Shutdown

When the junction temperature of the IC exceeds the thermal shutdown threshold of 165°C, the $\overline{FLT}$ pin goes low.

Shutdown Mode

When DIM pin is pulled low for more than 200ms, the linear regulator generating the 5V on the V_{CC} pin is turned off for low power consumption. The $\overline{FLT}$ pin is also pulled low in this condition.

Typical Operating Circuit



Applications Information

Switching Frequency

Switching frequency is selected based on the trade-offs between efficiency, solution size/cost, and the range of output voltage that can be regulated. Many applications place limits on switching frequency due to EMI sensitivity. The on-time of the MAX20078 can be programmed for switching frequencies ranging from 100kHz up to 1MHz. This on-time varies in proportion to both input voltage and output voltage, as described in the *New Average Current-Mode-Controlled Architecture* section. However, in practice, the switching frequency shifts in response to large swings in input or output voltage. The maximum switching frequency is limited only by the minimum on-time and minimum off-time requirements. The switching frequency (f_{SW}) is given by:

$$f_{SW} = (R3 + R2)/(C1R3R1)$$

Programming the LED Current

The LED current can be programmed using the voltage on REFI when $V_{REFI} \leq 1.2V$ (analog dimming). The current is given by:

$$I_{LED} = (V_{REFI} - 0.2)/(5 \times RCS)$$

Inductor Selection

The peak inductor current, selected switching frequency, and the allowable inductor current ripple determine the value and size of the output inductor. Selecting a higher switching frequency reduces the inductance requirements, but at the cost of efficiency. The charge/discharge cycle of the gate capacitance of the external switching MOSFET's gate and drain capacitance create switching losses, which worsen at higher input voltages since the switching losses are proportional to the square of the input voltage. Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. High inductor ripple current causes large peak-to peak flux excursion, increasing the core losses at higher frequencies.

The peak-to-peak current-ripple values typically range from ±10% to ±40% of DC current (I_{LED}). Based on the LED current-ripple specification and desired switching frequency, the inductor value can be calculated as follows:

$$L = (V_{IN} - V_{OUT})\, t_{ON}/\Delta I_{LED}$$

where ΔI_{LED} is the peak-to-peak inductor ripple.

It is important to ensure that the rated inductor saturation current is greater than the worst-case operating current ($I_{LED}+\Delta I_{LED}/2$) under the wide operating temperature range.

Input Capacitor

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. A good starting point for selection of C_{IN} is to use an input-voltage ripple of 2% to 10% of V_{IN}. C_{IN_MIN} can be selected as follows:

$$C_{IN_MIN} = 2(I_{LED} \times t_{ON})/\Delta V_{IN}$$

where t_{ON} is the on-time pulse width per switching cycle.

When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose one-half or more of their capacitance at their rated DC-voltage bias and also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature.

Switching MOSFET Selection

The device requires two external n-channel MOSFETs for the switching regulator. The MOSFETs should have a voltage rating at least 20% higher than the maximum input voltage to ensure safe operation during the ringing of the

switch node. In practice, all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The MOSFETs should also have a current rating at least 50% higher than the average switch current. The total losses of the power MOSFETs in both high- and low-side MOSFETs should be estimated once the MOSFETs are chosen. Both n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. The conduction losses at minimum input voltage should not exceed MOSFET package thermal limits or violate the overall thermal budget. Also, ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget. In particular, check that the dV/dt caused by DH turning on does not pull up the DL gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, the power dissipation in the device due to drive losses must be checked. Both MOSFETs must be selected so that their total gate charge is low enough; such that the IC can power both drivers without overheating the device. The total power dissipated in the internal gate drivers of the device is given by:

$$P_{DRIVE} = V_{CC} \times (Q_{GTOTH} + Q_{GTOTL}) \times f_{SW}$$

where Q_{GTOTL} is the low-side MOSFET total gate charge and Q_{GTOTH} is the high-side MOSFET total gate charge. The power dissipated in the 5V regulator in the device due to the gate drivers is given by:

$$P_{LG} = (V_{IN} - V_{CC}) \times (Q_{GTOTH} + Q_{GTOTL}) \times f_{SW}$$

Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance.

The output capacitance (C_{OUT}) is calculated using the following equation:

$$C_{OUT} = \frac{((V_{IN_MAX} - V_{LED}) \times V_{LED})}{(\Delta V_R \times 8 \times L \times V_{IN_MAX} \times fsw^2)}$$

where ΔV_R is the maximum allowable voltage ripple.

PCB Layout

For proper operation and minimum EMI, PCB layout should follow the guidelines below:

1) Large switched currents flow in the IN and AGND/PGND pins and the input capacitor (C_{IN}) of Figure 3. The loop formed by the input capacitor should be as small as possible by placing this capacitor as close as possible to the IN and AGND/PGND pins. The input capacitor, device, output inductor, and output capacitor should be placed on the same side of the PCB, with the connections made on the same layer.
2) Place an unbroken ground plane on the layer closest to the surface layer with the inductor, device, and the input and output capacitors.
3) The surface area of the LX and BST nodes should be as small as possible to minimize emissions.
4) The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heatsink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the device to additional ground planes within the circuit board.
5) In a synchronous rectifier, the high-speed gate-drive signals can generate significant conducted and radiated EMI. This noise can couple with high-impedance nodes of the IC and result in undesirable operation. A small amount (4−10) of resistors (R_{DH} and R_{DL}), in series with the gate-drive signals are recommended to slow the slew rate of the LX node and reduce the noise signature. They also improve the robustness of the circuit by reducing the noise coupling into sensitive nodes.
6) The parasitic capacitance between switching node and ground node should be minimized to reduce common-mode noise. Other common layout techniques, such as star ground and noise suppression using local bypass capacitors, should be followed to maximize noise rejection and minimize EMI within the circuit.
7) Place a capacitor (C_{BST}) as close as possible to the BST and LX pins.

Typical Application Circuits

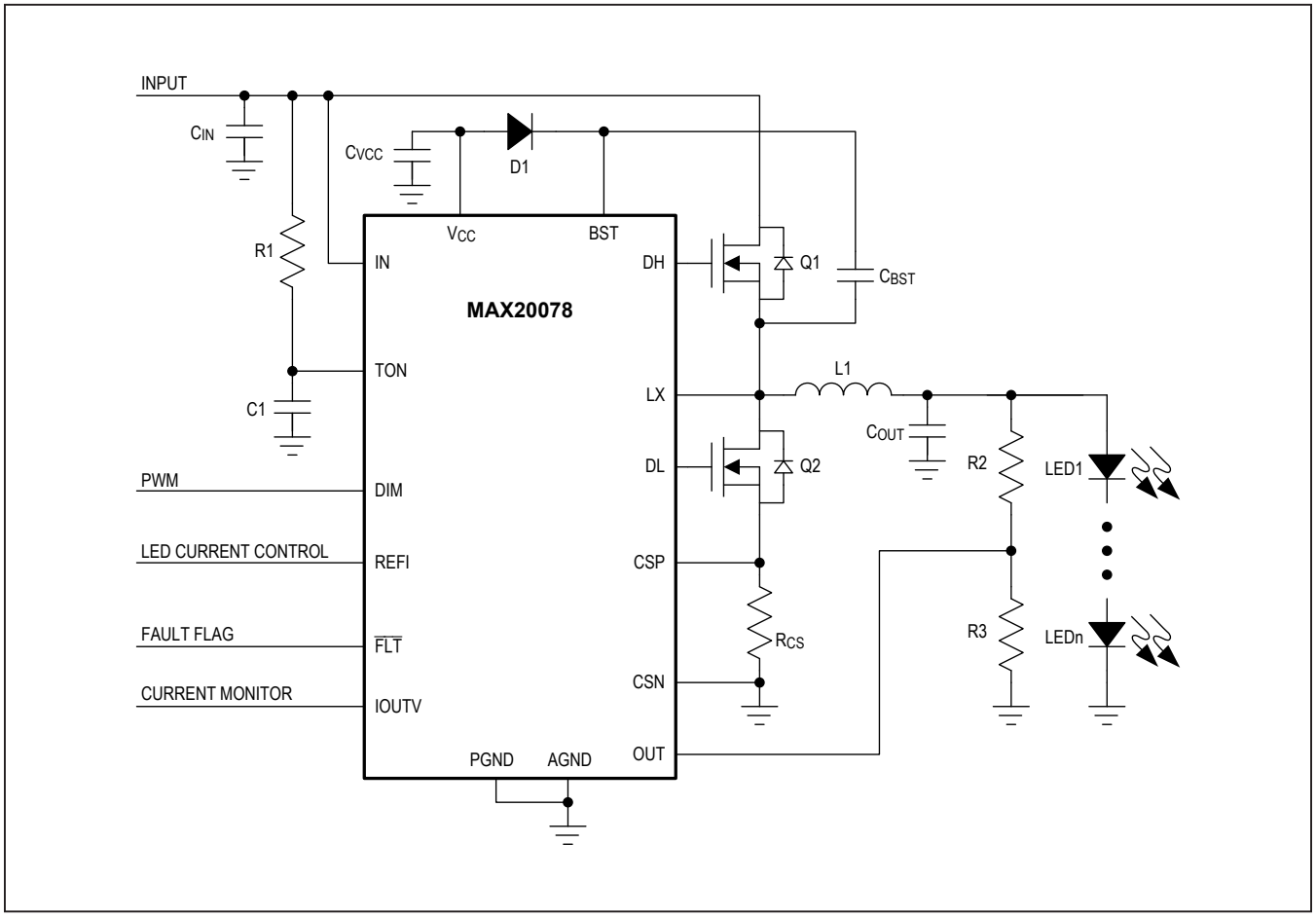


Figure 5. Typical Application Circuit for High-Beam, Low-Beam, Daytime-Running Lights, and Turn Indicators

Typical Application Circuits (continued)

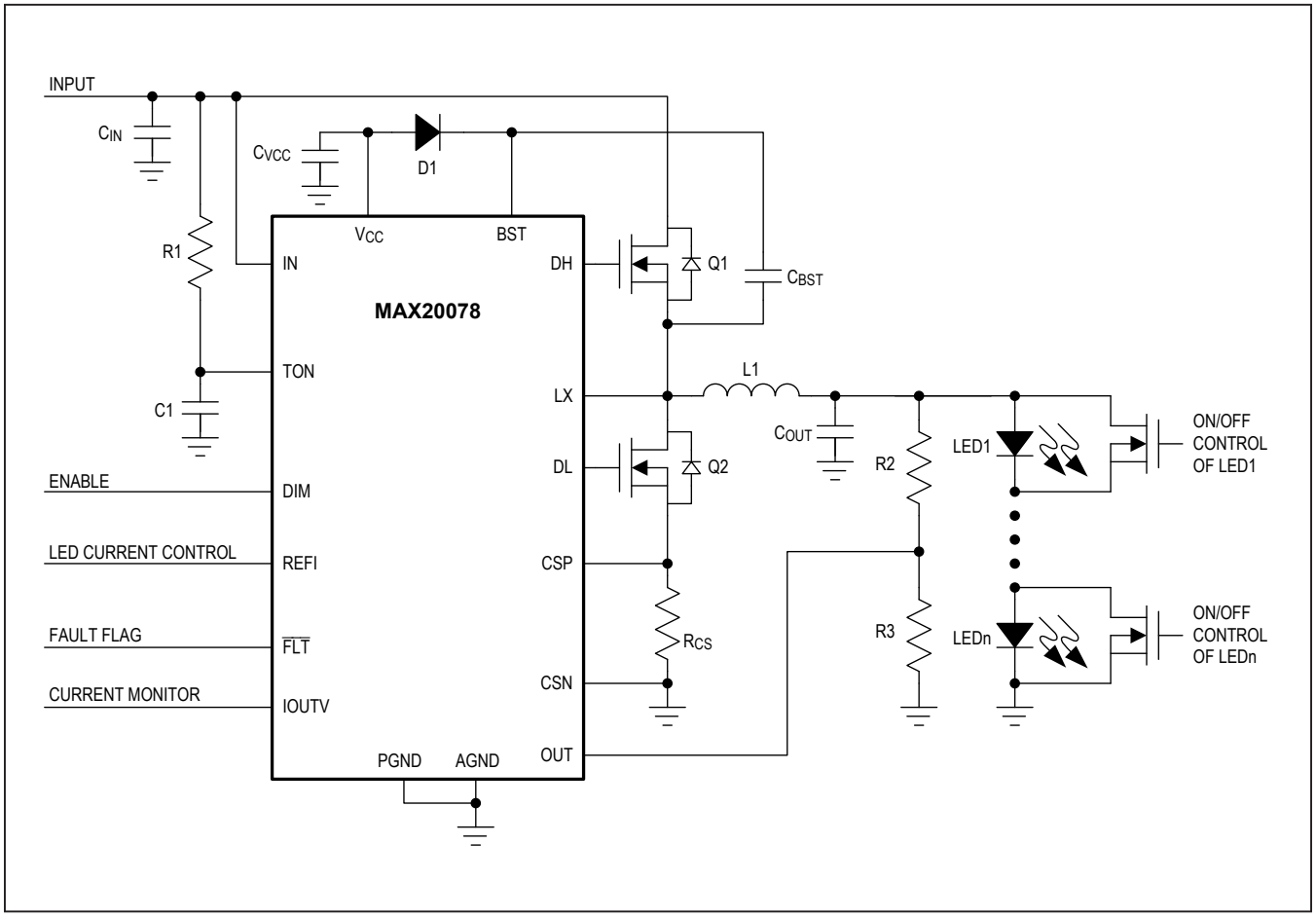


Figure 6. Typical Application Circuit for Automotive Matrix Lighting

Typical Application Circuits (continued)

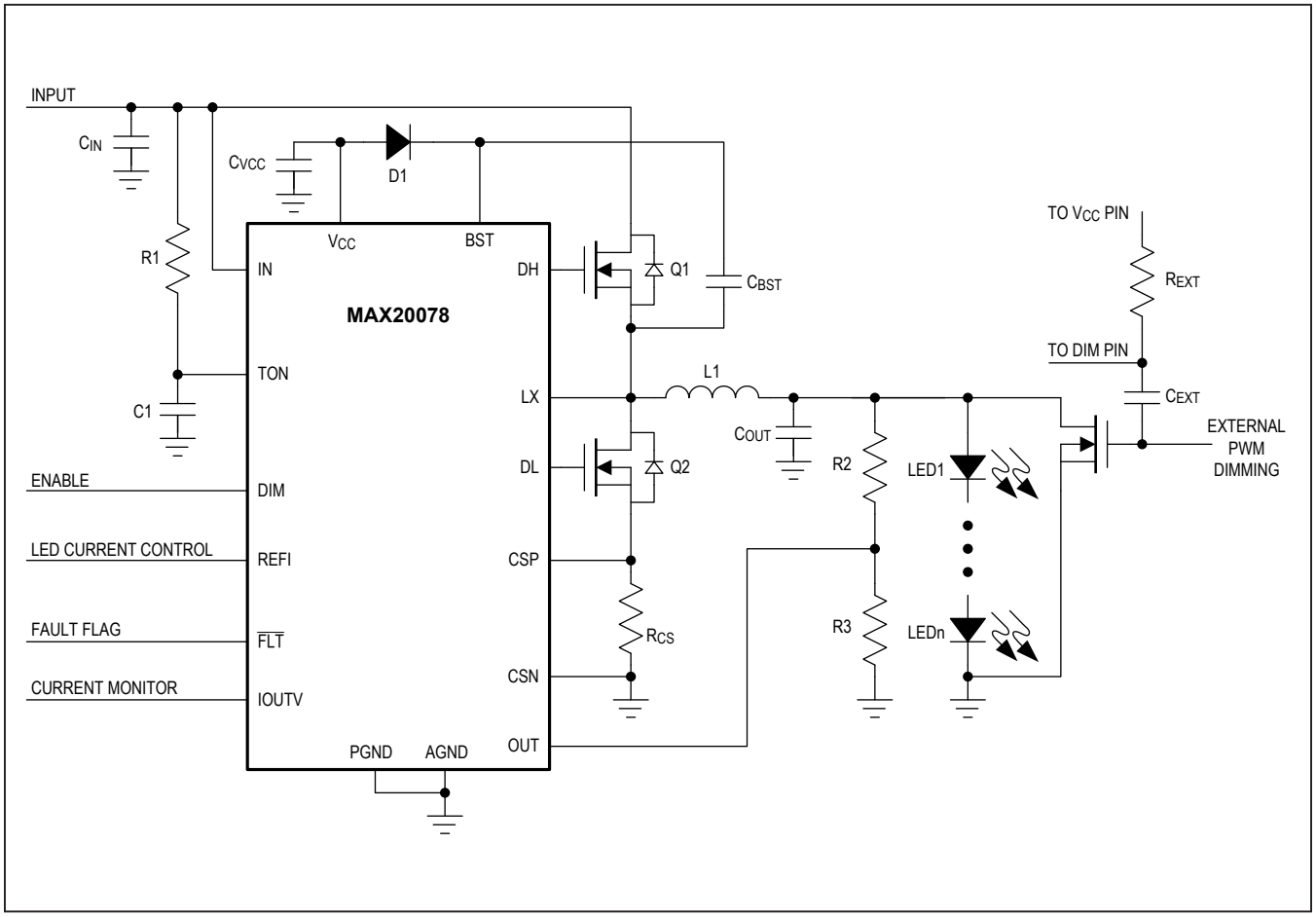


Figure 7. Typical Application Circuit For Head-Up Displays

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20078ATE+	-40ºC to +125ºC	16 TQFN-EP*
MAX20078ATE/V+	-40ºC to +125ºC	16 TQFN-EP*
MAX20078ATEY+	-40ºC to +125ºC	16 TQFN-EP* (SW)
MAX20078ATE/VY+	-40ºC to +125ºC	16 TQFN-EP* (SW)
MAX20078AUE+	-40ºC to +125ºC	16 TSSOP-EP*
MAX20078AUE/V+	-40ºC to +125ºC	16 TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
(SW) = Side wettable.
**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
TQFN-EP	T1633+4C	**21-0136**	**90-0031**
TQFN-EP (SW)	T1633Y+4C	**21-100108**	**90-100046**
TSSOP-EP	U16E+4C	**21-0108**	**90-0446**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/17	Initial release	—
1	6/17	Changed data sheet title from “Synchronous Buck Controller for High-Power HB LED Drivers” to “Synchronous Buck, High-Brightness LED Controller”	1–23
2	9/17	Updated *Benefits and Features*, REFI in *Absolute Maximum Ratings*, *Package Thermal Characteristics*, Shutdown Current and DIM Rising-to-DL Rising Delay in *Electrical Characteristics*, TOC11 in *Typical Operating Characteristics*, total list of steps in *PCB Layout section;* added one new variant (MAX20078ATE+) and deleted three (MAX20078ATEV+T, MAX20078ATE/VY+T, MAX20078AUE/V+T**) in *Ordering Information*; and updated POD and LPN in *Package Information*	1, 2, 4, 6, 16, 20
3	1/18	Removed future product status from MAX20078AUE/V+ in *Ordering Information*	20
4	7/18	Added MAX20078ATEY+ and MAX20078ATUE+ to *Ordering Information*	20
5	4/19	Updated *General Description* and *New Average Current-Mode-Controlled Architecture* and *Fault Indicator (FLT)* sections	1, 12, 14

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