Click here for production status of specific part numbers.

MAX20332

USB Charger Detection with Integrated Overvoltage Protector

General Description

The MAX20332 is a USB charger detector compliant with USB Battery Charging Specification Revision 1.2. The USB charger detection circuitry detects USB standard downstream ports (SDPs), USB charging downstream ports (CDPs), or dedicated charger ports (DCPs), and controls an external lithium-ion (Li+) battery charger.

The device implements USB Battery Charging Specification Revision 1.2-compliant detection logic. The device also includes Apple® charger detection that allows identification of resistor-divider networks on D+/D-.

The internal double-pole double-throw (DPDT) USB switch is compliant to Hi-Speed USB, full-speed USB, low-speed USB, and UART signals. The device's internal switch features low on-resistance, low on-resistance flatness, and very low capacitance. The ID pin controls the DPDT switch position. The MAX20332 features high-ESD protection up to ±15kV Human Body Model (HBM)on CD+, CD-, and ID pins.

The MAX20332 is available in a 16-bump, 0.4mm pitch, 1.8mm x 1.9mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- DSCs and Camcorders
- Tablet PCs
- Smartphones
- e-Readers

Benefits and Features

- Consumes Less Power
  - Low Battery Standby Current 5µA (typ)
- Delivers USB Compliance and Flexibility
  - Compliant to USB Battery Charging Specification Revision 1.2
  - Data Contact Detection for Foolproof Connector Insertion Detection
  - Dedicated Charger Detection
  - Standard Downstream Port Detection
  - Charging Downstream Port Detection
  - Apple Charger Detection
- Facilitates System Design
  - Integrated Precision 1.5A Overvoltage Protection (OVP)
  - Negative Audio Capable DPDT Hi-Speed USB Switches
  - Automatic Switch and Charger Interface Control
  - Full Control by I^2C Interface
  - Interrupt for Device Status Change
- Saves Board Space
  - V_{BUS} Connection Capable of 36V
  - ±15kV HBM ESD Protection
  - 1.8mm x 1.9mm WLP Package

***Ordering Information* and *Typical Operating Circuit* appears at end of data sheet.**

**Contact factory for the list of compatible chargers.*

Apple is a registered trademark of Apple, Inc.
Sony is a registered trademark and registered service mark of Kabushiki Kaisha TA Sony Corporation.

19-100282; Rev 0; 3/18

maxim integrated™

Absolute Maximum Ratings

(Voltages referenced to GND.)
BAT, $\overline{INT}$, SDA, SCL, $\overline{CE}$, ID, $\overline{DB}$ ..... -0.3V to +6.0V
OUT ..... -0.3V to min (V_B + 0.3V, +6.0V)
V_B ..... -0.3V to +40V
CP_EN = 1 (Note 1)
  $\overline{CD}$+, CD-, UT, UR ..... -2.1V to (V_{SWPOS} + 0.3V)
  TD+, TD- ..... -0.3V to (V_{SWPOS} + 0.3V)
CP_EN = 0 (Note 2)
  $\overline{CD}$+, CD-, TD+, TD-, UT, UR ..... -0.3V to (V_{CCINT} + 0.3V)

Continuous Current into V_B, OUT ..... ±1.5A
Continuous Current into Any Other Terminal ..... ±50mA
Continuous Power Dissipation (T_A = +70ºC)
  WLP (derate 17.2mW/ºC above +70ºC) 1376mW
Operating Temperature Range ..... -40ºC to +85ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150ºC
Soldering Temperature (reflow) ..... +260ºC

Note 1: V_{SWPOS} = min (V_{CCINT} or 3.3V).
Note 2: V_{CCINT} = max (V_{BAT} or min (V_B or 3.7V)).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
  Junction-to-Ambient Thermal Resistance (θ_{JA}) 58ºC/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +36V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage Range	V_{BAT}		2.8		5.5	V
	V_B		3.5		36	
Internal Positive Switch Regulator	V_{SWPOS}		3.3	3.4	3.5	V
Internal Negative Switch Regulator	V_{SWNEG}		-2.08	-1.97	-1.8	V
POR	V_{CCINT}	Rising edge	0.5	1.6	2.6	V
		Falling edge			2.35	
BAT Supply Current	I_{BAT}	V_{BAT} = 4.2V, V_B = 0V, CP_EN = 0, USB_SWC = 00, ADC_EN = 0, V_{SDA} = V_{SCL} = 0.4V		5	7.5	µA
		V_{BAT} = 4.2V, V_B = 0V, CP_EN = 1, USB_SWC = 11, ADC_EN = 1, V_{SDA} = V_{SCL} = 1.8V		49	80	
V_B Supply Current	I_{VB}	V_B = 5.5V, CP_EN = 1, USB_SWC = 00		200	360	µA

Electrical Characteristics (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +36V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION							
Switch On-Resistance	R_{ON}	V_B = 5V, I_{OUT} = -80mA			60	130	mΩ
Overvoltage Lockout Cutoff Threshold	V_{OVLO}	Rising edge of V_B		5.75	5.875	6.0	V
Overvoltage Lockout Hysteresis		Falling edge of V_B		5.50			V
OUT Load Capacitance		I_{OUT} up to 1.5A		1			µF
Thermal Shutdown Threshold					+150		ºC
Thermal Shutdown Hysteresis					20		ºC
CHARGER DETECTION							
V_{DAT_SRC} Voltage	V_{DP_SRC}	With I_{DP_SRC} = 0 to 200µA		0.5		0.7	V
V_{DAT_REF} Voltage	V_{DAT_REF}			0.25		0.4	V
V_{LGC} Voltage	V_{LGC}			1		1.5	V
I_{DP_SRC} Current	I_{DP_SRC}	0 to 2.5V		6		11	µA
R_{DM} Pulldown Resistor	R_{DM_DWN}			14.25		24.8	kΩ
CD+ and CD- Sink Current	I_{CD+_SINK}, I_{CD-_SINK}	150mV to 3.6V		50		150	µA
Charger Detection Weak Sink	I_{WEAK}	V_{CD-} = 3.6V				0.3	µA
V_{BUS25} Ratio	V_{BUS25}	Reference ratio for special charger as a percentage of V_{BUS} voltage, V_B = 5V		22.5	25	27.5	%
V_{BUS47} Ratio	V_{BUS47}	Reference ratio for special charger as a percentage of V_{BUS} voltage, V_B = 5V		42.3	47	51.7	%
V_{BUS60} Ratio	V_{BUS60}	Reference ratio for special charger as a percentage of V_{BUS} voltage, V_B = 5V		57	60	63	%
Charger Detect Source Time	$t_{DP_SRC_ON}$			40			ms
Charger Detect Type Detection Time	$t_{DP_RES_ON}$	From V_B > V_{VBDET} to detection completed		120			ms
Charger Detect Delay Time	$t_{DP_SRC_HICRNT}$			40		80	ms
V_B Attach to $\overline{CE}$ Output Time	t_{VBSW}	From V_B > V_{VBDET} or CHG_TYP_M = 1 to $\overline{CE}$ change				520	ms
V_B Detect Threshold	V_{VBDET}	Rising edge		3.3	3.4	3.5	V
V_B Detect Hysteresis	V_{VBDET_HYS}				400		mV
DCD Delay Time	t_{DCD}	From VB attach until DCD fail		730	810	900	ms
USB ANALOG SWITCHES (CD+, CD-)							
Analog Signal Range	V_{CD+}, V_{CD-}	CP_EN = 0		0		V_{CCINT}	V
		CP_EN = 1	TD+, TD-	0		V_{SWPOS}	
			UR, UT	V_{SWNEG}		V_{SWPOS}	

Electrical Characteristics (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +36V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Resistance	R_{ONUSB}	V_{BAT} = 3.0V, I_{CD+} or I_{CD-} = 10mA, V_{CD+} or V_{CD-} = 0 to 3.0V			3	6	Ω
On-Resistance Match Between Channels	DR_{ONUSB}	V_{BAT} = 3.0V, I_{CD+} or I_{CD-} = 10mA, V_{CD+} or V_{CD-} = 400mV				0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	V_{BAT} = 3.0V, I_{CD+} or I_{CD-} = 10mA, V_{CD+} or V_{CD-} = 0 to 3.3V			0.06	0.2	Ω
Off-Leakage Current	$I_{LUSB(OFF)}$	V_{BAT} = 4.2V, switch open; V_{UT}, V_{UR}, V_{TD-}, or V_{TD+} = 0.3V, 2.5V; V_{CD+} or V_{CD-} = 2.5V, 0.3V		-360		+360	nA
On-Leakage Current	$I_{LUSB(ON)}$	V_{BAT} = 4.2V, switch closed; V_{CD-} or V_{CD+} = 0.3V, 2.5V		-360		+360	nA
ANALOG INPUT (ID) (Note 5)							
ADC Detection Resistors (Use ±1% Resistors for R1 to R30)	R_{ADC}	00000	GND			1.5	kΩ
		00001	R1		2.21		
		00010	R2		2.8		
		00011	R3		3.48		
		00100	R4		4.22		
		00101	R5		5.11		
		00110	R6		6.04		
		00111	R7		7.87		
		01000	R8		10.02		
		01001	R9		12.1		
		01010	R10		14.7		
		01011	R11		17.8		
		01100	R12		21.5		
		01101	R13		25.5		
		01110	R14		30.1		
		01111	R15		36.5		
		10000	R16		45.3		
		10001	R17		53.6		
		10010	R18		64.9		
		10011	R19		80.06		
		10100	R20		102		
		10101	R21		121		
		10110	R22		150		
		10111	R23	175	200	202	
		11000	R24		232		
		11001	R25		267		
		11010	R26		309		
		11011	R27		365		
		11100	R28		422		
		11101	R29		491		
		11110	R30		576		
		11111	Open	750			

Electrical Characteristics (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +36V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SIGNALS ($\overline{INT}$, $\overline{CE}$, SCL, SDA)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current	I_{INLEAK}		-1		+1	µA
Output Leakage Current	I_{LEAK}	V_{IO} = 3.3V			1	µA
Output Logic-Low Voltage (INT, CE)	V_{OL}	I_{SINK} = 1mA			0.2	V
DIGITAL OUTPUT ($\overline{DB}$)						
Output Logic-High		V_{OUT} = 5.5V, I_{SOURCE} = 1mA	V_{OUT} - 0.4			V
Output Logic-Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Output Logic-High Impedance	I_{LEAK}		-1		+1	µA
DYNAMIC PERFORMANCE						
Analog-Switch Turn-On Time	t_{ON}	I²C stop to switch on, R_L = 50Ω		0.02	1	ms
Analog-Switch Turn-Off Time	t_{OFF}	I²C stop to switch off, R_L = 50Ω		0.02	0.1	ms
Debounce Time	t_{MDEB}	Main debounce, all comparators	20	30	40	ms
Off-Capacitance	C_{OFF}	TD-, TD+ applied voltage is $0.5V_{P-P}$, DC bias = 0V, f = 240MHz		2		pF
On-Capacitance	C_{ON}	TD-, TD+ applied voltage is $0.5V_{P-P}$, DC bias = 0V, f = 240MHz, CD- connected to TD-, CD+ connected to TD+		7		pF
-3dB Bandwidth	BW			1		GHz
Crosstalk		R_L = 50Ω, f = 20kHz, $V_{CD_}$ = $0.5V_{P-P}$		-80		dB
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 20kHz, $V_{CD_}$ = $0.5V_{P-P}$		-60		dB
I²C TIMING SPECIFICATIONS (Figure 4)						
I²C Maximum Clock	f_{I2C_CLK}			400		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Setup Time			0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$	90% to 90%	0.6			µs
START Condition Hold Time	$t_{HD:STA}$	10% of SDA to 90% of SCL	0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	0.6			µs
Clock Low Period	t_{LOW}	10% to 10%	1.3			µs
Clock High Period	t_{HIGH}	90% to 90%	0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time	100			µs
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time			0	µs

Electrical Characteristics (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +36V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

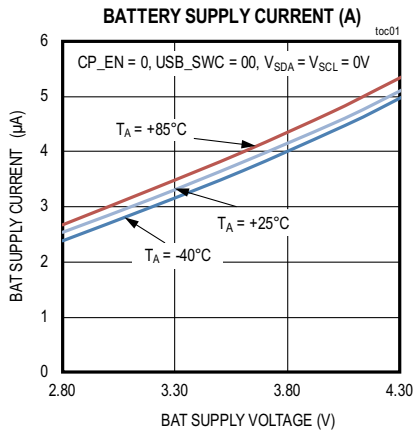
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
CD+, CD-, ID		Human Body Model		±15		kV
All Other Pins		Human Body Model		±2		kV

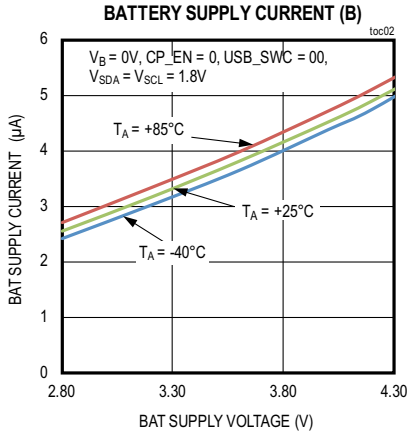
Note 4: All devices are 100% production tested at T_A = +25ºC. Limits over the operating temperature range are guaranteed by design and not production tested.

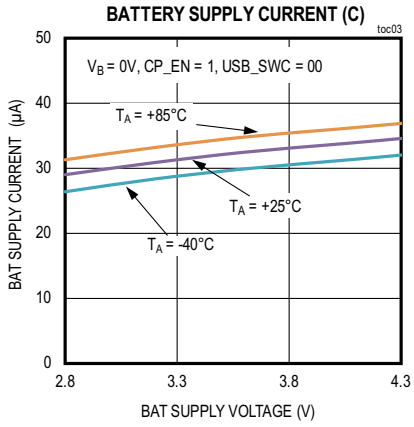
Note 5: All resistor values guaranteed to be detected within ±1% range.

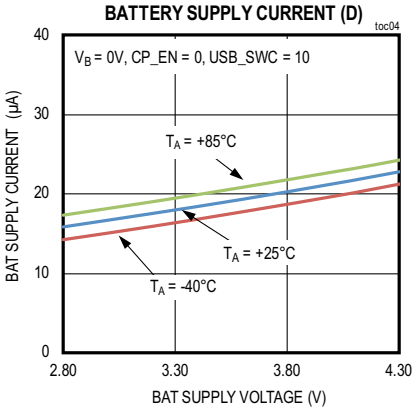
Typical Operating Characteristics

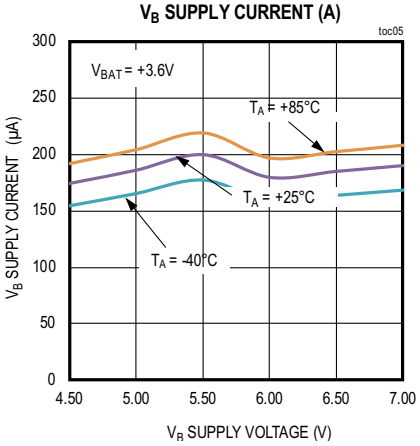
(T_A = +25°C, unless otherwise noted.)

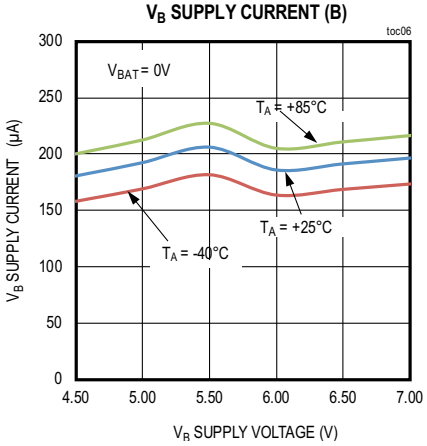








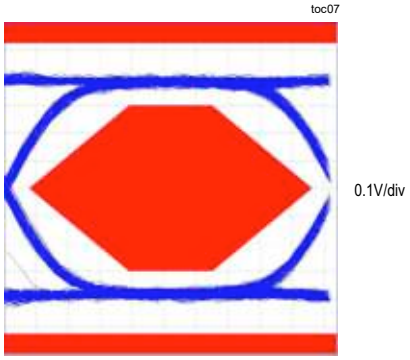




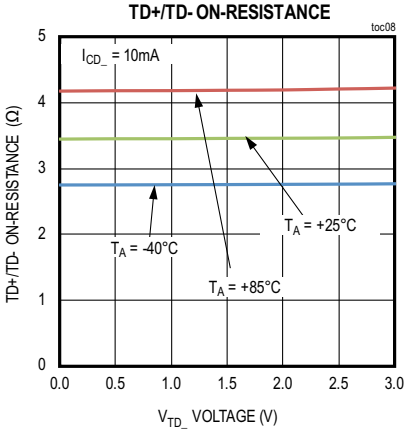
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

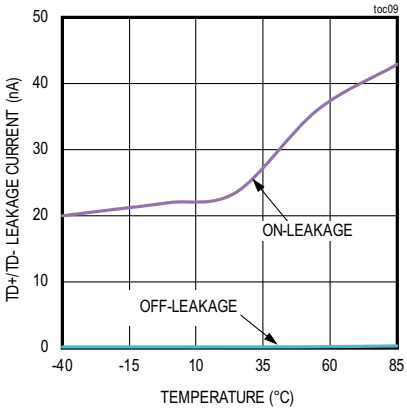
TD+/TD- CHANNEL EYE DIAGRAM



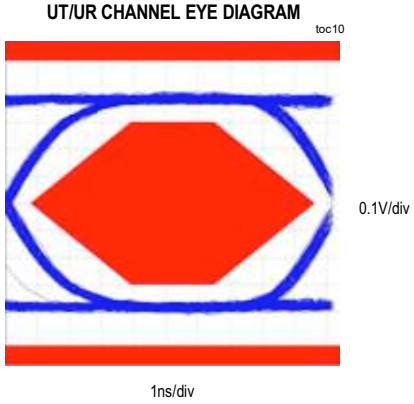
TD+/TD- ON-RESISTANCE



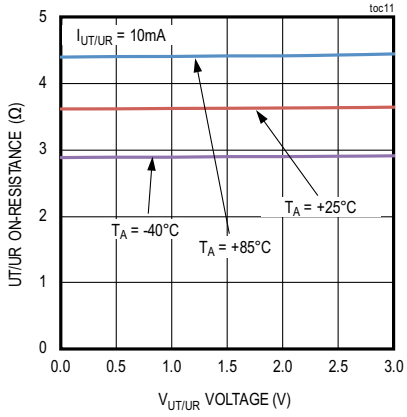
TD+/TD- LEAKAGE CURRENT vs TEMPERATURE



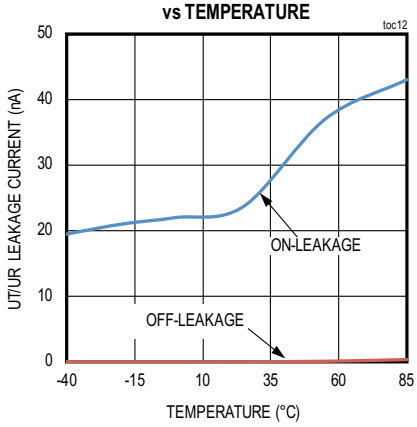
UT/UR CHANNEL EYE DIAGRAM



UT/UR ON-RESISTANCE



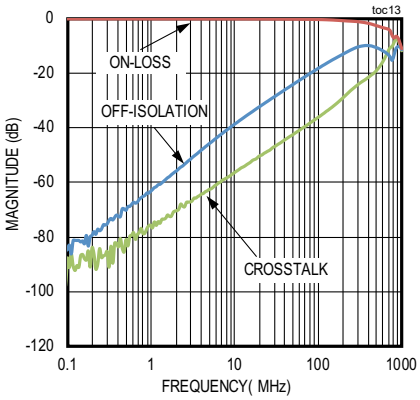
UT/UR LEAKAGE CURRENT vs TEMPERATURE



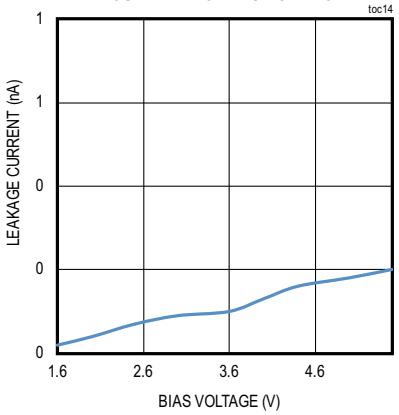
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

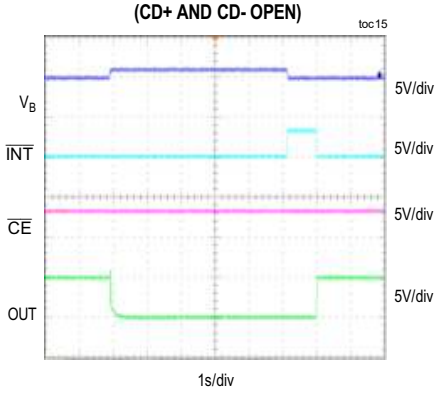
FREQUENCY RESPONSE



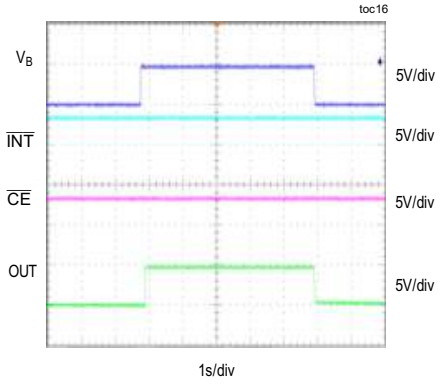
LOGIC OUTPUT LEAKAGE CURRENT vs. BIAS VOLTAGE



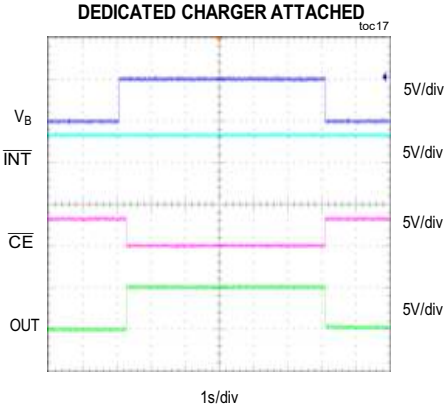
V_B OVERVOLTAGE PROTECTION (CD+ AND CD- OPEN)



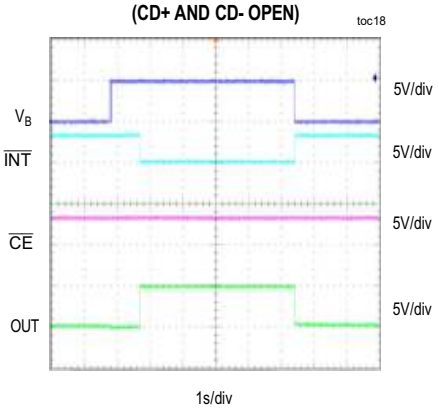
STANDARD DOWNSTREAM PORT ATTACHED



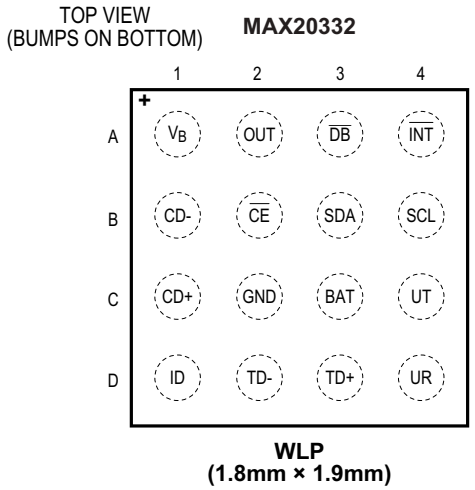
DEDICATED CHARGER ATTACHED



POWER ONLY ATTACHED (CD+ AND CD- OPEN)



Bump Configuration



WLP
(1.8mm × 1.9mm)

Bump Description

BUMP	NAME	FUNCTION
A1	V_B	USB Connector V_{BUS} Connection. Bypass V_B with a 1µF capacitor to GND.
A2	OUT	Overvoltage-Protected USB Transceiver V_{BUS} Power Output. Bypass OUT with a 1µF capacitor to GND.
A3	$\overline{DB}$	Active-Low, Open-Drain. Driven low in response to a 80K resistor connect to ID. See Table 4.
A4	$\overline{INT}$	Active-Low, Open-Drain, Interrupt Request Fault Output. Connect $\overline{INT}$ to an external pullup resistor.
B1	CD-	USB Connector D- Connection
B2	$\overline{CE}$	Active-Low, Open-Drain, Charger Control Enable Output. Connect $\overline{CE}$ to an external pullup resistor.
B3	SDA	I^2C Serial-Data Input/Output. Connect SDA to an external pullup resistor.
B4	SCL	I^2C Serial-Clock Input. Connect SCL to an external pullup resistor.
C1	CD+	USB Connector D+ Connection
C2	GND	Ground
C3	BAT	Battery Connection Input. Bypass BAT with a 1µF capacitor to GND.
C4	UT	UART Tx Line from Device
D1	ID	USB Connector ID Connection. Bypass ID with a 1nF (max) capacitor to GND.
D2	TD-	USB Transceiver D- Connection
D3	TD+	USB Transceiver D+ Connection
D4	UR	UART Rx Line from Device

Functional Diagram

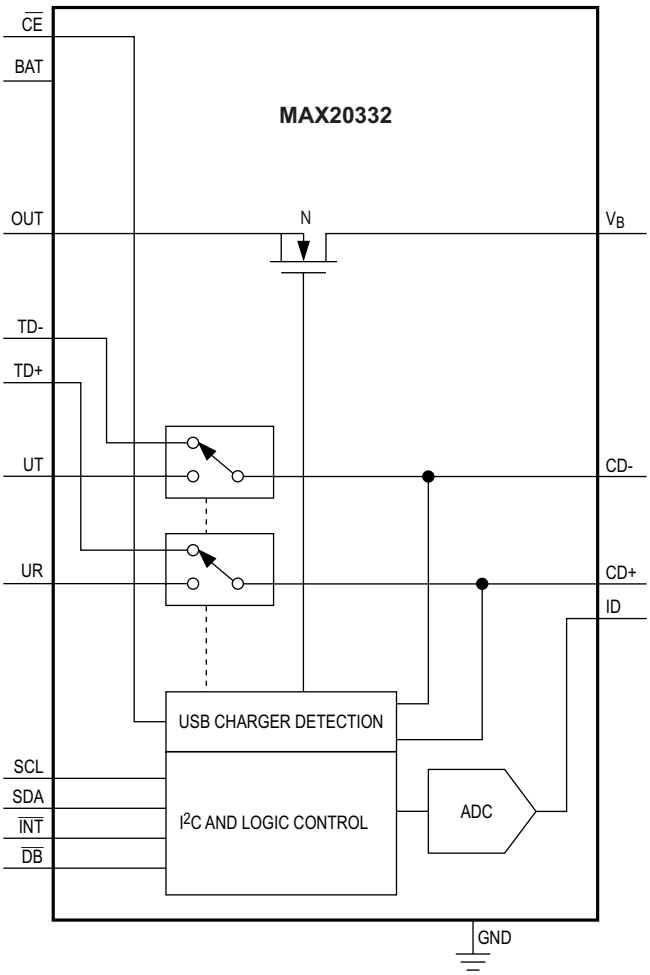


Table 1. Register Map

ADDRESS	NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x00	DEVICE ID	VENDOR_ID				CHIP_REV			
0x01	INTERRUPT 1	DCD_TMR	CHG_DET_START	CHG_DET_STOP	RFU		OVP	VB_VALID	CHG_TYP
0x02	INTERRUPT 2	ADC_ERROR	RFU						ADC
0x03	STATUS 1	DCD_TMR_S	CHG_DET_RUN_S	OVP_S	VB_VALID_S	CHG_TYP_S			
0x04	STATUS 2	ADC_ERROR_S	RFU		ADC_S				
0x05	INTMASK 1	DCD_TMR_M	CHG_DET_START_M	CHG_DET_STOP_M	RFU		OVP_M	VB_VALID_M	CHG_TYP_M
0x06	INTMASK 2	ADC_ERROR_M	RFU						ADC_M
0x07	CONTROL 1	INT_TYP	INT_DLY	INT_POL	INT_EN	USB_SWC		CP_EN	LOW_PWR
0x08	CONTROL 2	APPL_NXT	CE_FRC	CE	ADC_DEB		USB_CPL	ID_AUTO_SWC	ADC_EN
0x09	CONTROL 3	OVP_EN		RFU	RFU	DCD_2S_CT	DCD_EN	CHG_TYP_MAN	CHG_DET_EN

Table 2. Detailed Register Map

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
DEVICE ID (0x00)				
VENDOR_ID	Read only	[7:4]	0010	Vendor Identification
CHIP_REV	Read only	[3:0]	1111	Chip Revision
INTERRUPT 1 (0x01)				
DCD_TMR	Read only	[7]	0	Data Contact Detection Timer Interrupt 0 = No interrupt 1 = Interrupt
CHG_DET_START	Read only	[6]	0	Charger Detection Start Transition Interrupt 0 = No interrupt 1 = Interrupt
CHG_DET_STOP	Read only	[5]	0	Charger Detection Stop Transition Interrupt 0 = No interrupt 1 = Interrupt
RFU	Read only	[4:3]	00	Reserved
OVP	Read only	[2]	0	Overvoltage Protection Interrupt. When V_B is greater than V_{OVLO}, the interrupt is triggered. 0 = No interrupt 1 = Interrupt
VB_VALID	Read only	[1]	0	V_{BUS} Valid Interrupt. Any change in the VB_VALID_S bit triggers an interrupt. 0 = No interrupt 1 = Interrupt
CHG_TYP	Read only	[0]	0	Charger Type Interrupt 0 = No interrupt 1 = Interrupt
INTERRUPT 2 (0x02)				
ADC_ERROR	Read only	[7]	0	ADC Error Interrupt 0 = No interrupt 1 = Interrupt

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
RFU	Read only	[6:1]	000000	Reserved
ADC	Read only	[0]	0	ADC Change Interrupt 0 = No interrupt 1 = Interrupt
STATUS 1 (0x03)				
DCD_TMR_S	Read only	[7]	0	Data Contact Detection Timer Wait Status 0 = Data contact detection timer not expired or not running 1 = Data contact detection running for greater than 900ms (typ)
CHG_DET_RUN_S	Read only	[6]	0	Charger Detection State Machine Running Status 0 = Not running 1 = Running
OVP_S	Read only	[5]	0	V_B Overvoltage Protection Trip Level Indication 0 = V_B is less than or equal to the overvoltage trip level 1 = V_B is greater than the overvoltage trip level
VB_VALID_S	Read only	[4]	0	V_{BUS} Valid Status 0 = V_B is less than V_{VBDET} or V_B is greater than the overvoltage trip level (OVP_S = 1) 1 = V_B is greater than or equal to the V_{VBDET} and V_B is less than or equal to overvoltage trip level (OVP_S = 0)
CHG_TYP_S	Read only	[3:0]	0000	USB Charger Detection Output 0000 = Nothing attached 0001 = Standard downstream port (SDP) 0010 = Charging downstream port (CDP) 0011 = Dedicated charger port (DCP) 0100 = Apple 500mA (max) charger 0101 = Apple 1A (max) charger 0110 = Apple 2A (max) charger 0111 = Special 500mA charger 1100 = Apple RFU Other conditions are reserved for future use.
STATUS 2 (0x04)				
ADC_ERROR_S	Read only	[7]	0	ADC Error Status 0 = No ADC error 1 = ADC error
RFU	Read only	[6:5]	00	Reserved
ADC_S	Read only	[4:0]	11111	ADC Output. See the ADC Detection Resistors specifications in the Electrical Characteristics table.
INTMASK 1 (0x05)				
DCD_TMR_M	Read/write	[7]	0	Data Contact Detection Timer Interrupt Mask 0 = Mask 1 = Not masked
CHG_DET_START_M	Read/write	[6]	0	Charger Detection Run Rising Transition Interrupt Mask 0 = Mask 1 = Not masked

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CHG_DET_STOP_M	Read/write	[5]	0	Charger Detection Run Falling Transition Interrupt Mask 0 = Mask 1 = Not masked
RFU	Read/write	[4:3]	00	Reserved
OVP_M	Read/write	[2]	0	Overvoltage Protection Interrupt Mask 0 = Mask 1 = Not masked
VB_VALID_M	Read/write	[1]	0	V_B Valid Interrupt Mask 0 = Mask 1 = Not masked
CHG_TYP_M	Read/write	[0]	0	Charge Type Interrupt Mask 0 = Mask 1 = Not masked
INTMASK 2 (0x06)				
ADC_ERROR_M	Read/write	[7]	0	ADC Error Interrupt Mask 0 = Mask 1 = Not masked
RFU	Read/write	[6:1]	000000	Reserved
ADC_M	Read/write	[0]	0	ADC Change Interrupt Mask 0 = Mask 1 = Not masked
CONTROL 1 (0x07)				
INT_TYP	Read/write	[7]	0	This bit sets the interrupt type. See the Interrupts section for details. 0 = Interrupt is level triggered 1 = Interrupt is edge triggered
INT_DLY	Read/write	[6]	0	This bit sets the interrupt pulse width in case of trains of interrupt requests. This bit is valid only if INT_TYP = 1. 0 = 2 x 60kHz clock ticks 1 = 4 x 60kHz clock ticks
INT_POL	Read/write	[5]	0	This bit sets the interrupt polarity. See the Interrupts section for details. 0 = Active-low 1 = Active-high
INT_EN	Read/write	[4]	0	This bit enables interrupt generation. When INT_EN = 0, pending interrupts are not cleared and the INT pin acts as a FLAG per Table 4. INT_EN is a global setting to mask all interrupts. 0 = Disable interrupt 1 = Enable interrupt

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
USB_SWC	Read/write	[3:2]	11	USB Switch Control 00 = All switches open 01 = USB switches connected to UT/UR position 10 = USB switches connected to TD+/TD- position 11 = Follow the detection finite state machine
CP_EN	Read/write	[1]	0	Charge Pump Enable. To pass a negative signal to UR/UT, this bit must be set high. 0 = Charge pump disabled 1 = Charge pump enabled
LOW_PWR	Read/write	[0]	1	Low-Power Mode Enable 0 = Low-power mode disable. The oscillator and bandgap are always on. 1 = Low-power mode enable. The oscillator and bandgap are turned off when V_{BUS} is not valid, USB_SWC = 00, CP_EN = 0, and ADC_S = 11111.
CONTROL 2 (0x08)				
APPL_NXT	Read/write	[7]	1	Enable Next Possible Apple Charger (CHG_TYP = 1100) 0 = CHG_TYP = 1100 cannot be detected 1 = CHG_TYP = 1100 can be detected
CE_FRC	Read/write	[6]	0	Enable Force $\overline{CE}$ Outputs 0 = $\overline{CE}$ output follow the charger detection finite state machine as per Table 3. 1 = $\overline{CE}$ output forced as per CE bit configuration
CE	Read/write	[5]	0	$\overline{CE}$ Output Forced Value. Valid only with CE_FRC = 1. 1 = $\overline{CE}$ output forced low 0 = $\overline{CE}$ output forced high impedance
ADC_DEB	Read/write	[4:3]	01	These bits set the ADC debounce time setting. 00 = 0.5ms (typ) 01 = 10ms (typ) 10 = 25ms (typ) 11 = 38.6ms (typ)
USB_CPL	Read/write	[2]	1	USB Compliant Bit 0 = Device is not USB compliant 1 = Device is USB compliant
ID_AUTO_SWC	Read/write	[1]	1	ID Auto Switch Control. ID resistor change during valid V_B enables the auto switch configuration based on Table 3. 0 = No auto-switch configuration after the first auto configuration from initial valid V_B. 1 = Allow auto switch configuration based on ID while V_B is valid.

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
ADC_EN	Read/write	[0]	0	ADC Enable. When ADC_EN is set low, the ADC is automatically enabled when valid V_B is present and disabled when V_B becomes invalid. When ADC_EN is set high, the ADC is always enabled regardless of V_B. The device draws more quiescent current when ADC_EN is set high. 0 = ADC disable with battery power only, and active only with valid V_B. 1 = ADC always active
CONTROL 3 (0x09)				
OVP_EN	Read/write	[7:6]	10	Manual Overvoltage Protection Control 00 = Force OVP open 01 = Force OVP closed $V_B > V_{VBDET}$ 10 = OVP controlled by logic (closed after V_{BUS} attach based on Table 4). 11 = Reserved for future use.
RFU	Read/write	[5]	0	Reserved
RFU	Read/write	[4]	0	Reserved
DCD_2S_CT	Read/write	[3]	1	Data Contact Detection Exit Method 0 = Stay in DCD until normal exit 1 = Exit DCD when 900ms (max) interrupt asserts
DCD_EN	Read/write	[2]	1	Data Contact Detection State Machine Enable. If DCD is enabled, then before D+/D- is tested for a short, DCD must pass. If DCD is disabled, the DCD is skipped and D+/D- short detection begins. If DCD state machine is running for more than 900ms (max), the DCD timer interrupt is set high (DCD_TMR = 1). 0 = Disable 1 = Enable
CHG_TYP_MAN	Read/write	[1]	0	Charger Type Manual Detection. This bit forces the internal logic to open the USB switches and perform charger type detection when set high. After the detection state machine completes, this bit self-resets. 0 = Disabled 1 = Enable charger detection
CHG_DET_EN	Read/write	[0]	1	USB Charger Detection Enable 0 = Disable charger detection 1 = Enable charger detection

Detailed Description

The MAX20332 is a USB charger detector compliant with USB Battery Charging Specification Revision 1.2. The IC features internal detection logic for determining the device connected and is controlled through the I²C interface. The device is a complete solution for multiplexing a USB and UART signal on a single USB connector with a Li+ battery charger.

USB Charger Detection

The MAX20332 includes internal logic to detect if a valid USB charger is connected. When a valid V_{BUS} voltage is applied to V_B or when CHG_TYP_MAN in the CONTROL 3 (0x09) register is set to 1, the device begins the charger type detection sequence. During the charger type detection sequence, the CD- and CD+ switches are open, and once the sequence completes, the switches return to their previous state. When the MAX20332 detects the charger, it sets the $\overline{CE}$ output based on the charger found (Table 3). Figure 1 shows a timing diagram for an example charger type detection sequence. Figure 2 shows D+/D- termination for a standard USB host charging downstream port, Apple charger, Sony charger, and a dedicated charger.

When a USB DCP is detected, 0.6V is driven on CD+ as required by USB BC1.2.

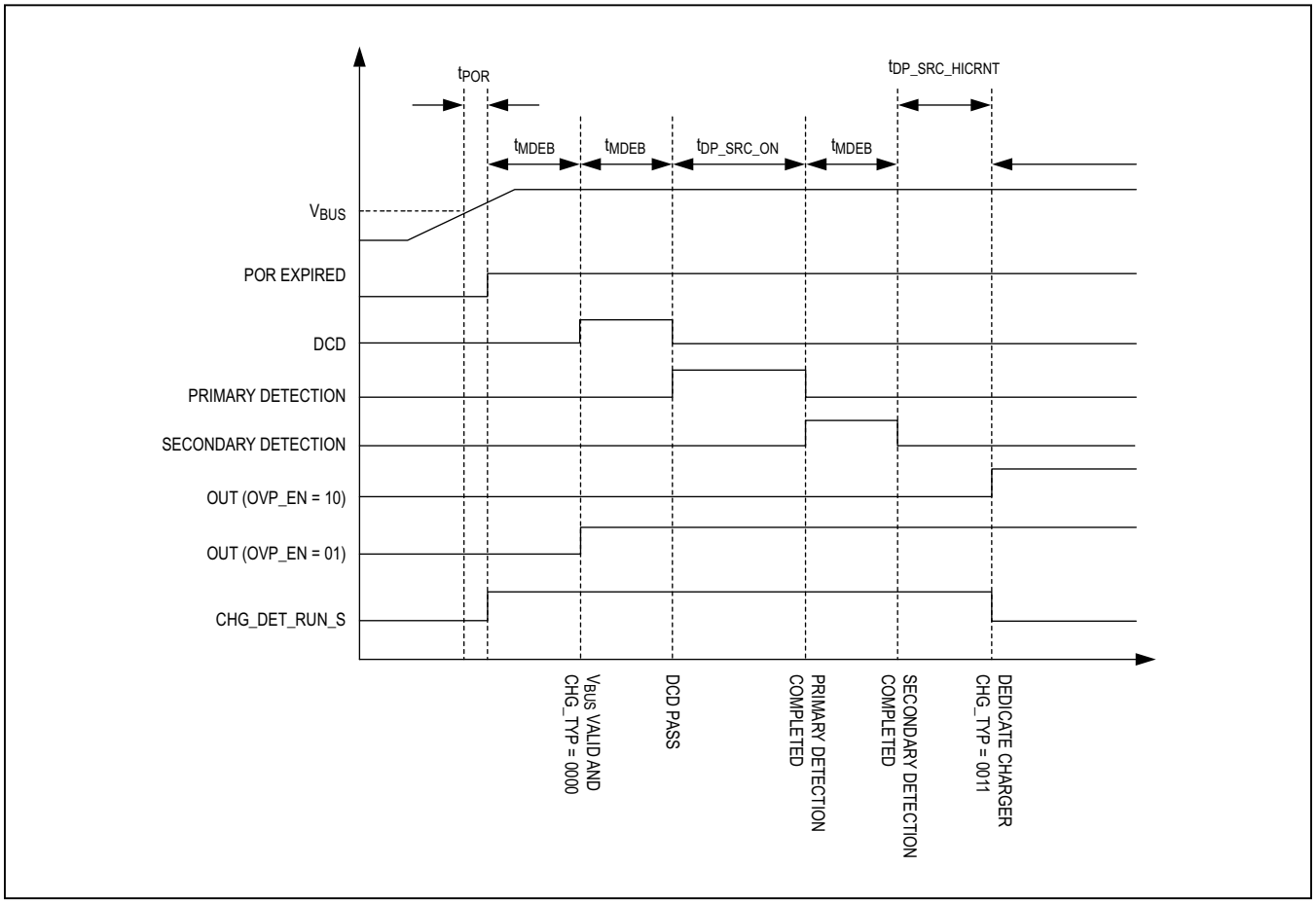


Figure 1. Charger Detection Timing.

Table 3. Charger Control Output Status

CHG_TYP	CHARGER DETECTED	$\overline{CE}$ OUTPUT	
		USB_CPL = 0	USB_CPL = 1
0000	Off	1	1
0001	Standard downstream port	0	1
0010	Charging downstream port	0	0
0011	Dedicated charger port	0	0
0100	Apple 0.5A (max) charger	0	0
0101	Apple 1A (max) charger	0	0
0110	Apple 2A (max) charger	0	0
0111	Special 500mA charger	0	0
1100	Reserved	0	0

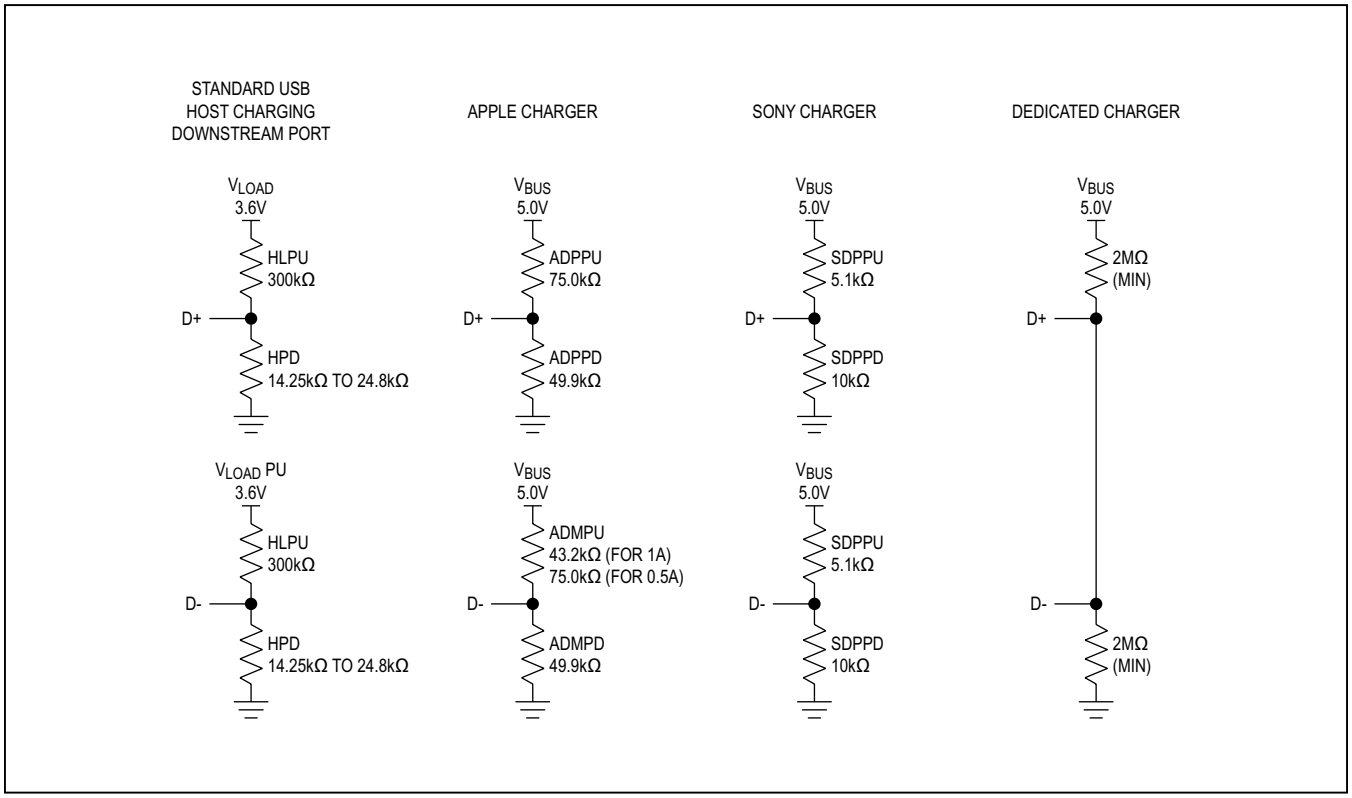


Figure 2. Standard USB Host Charging Downstream Port, Apple Charger, Sony Charger, and Dedicated Charger.

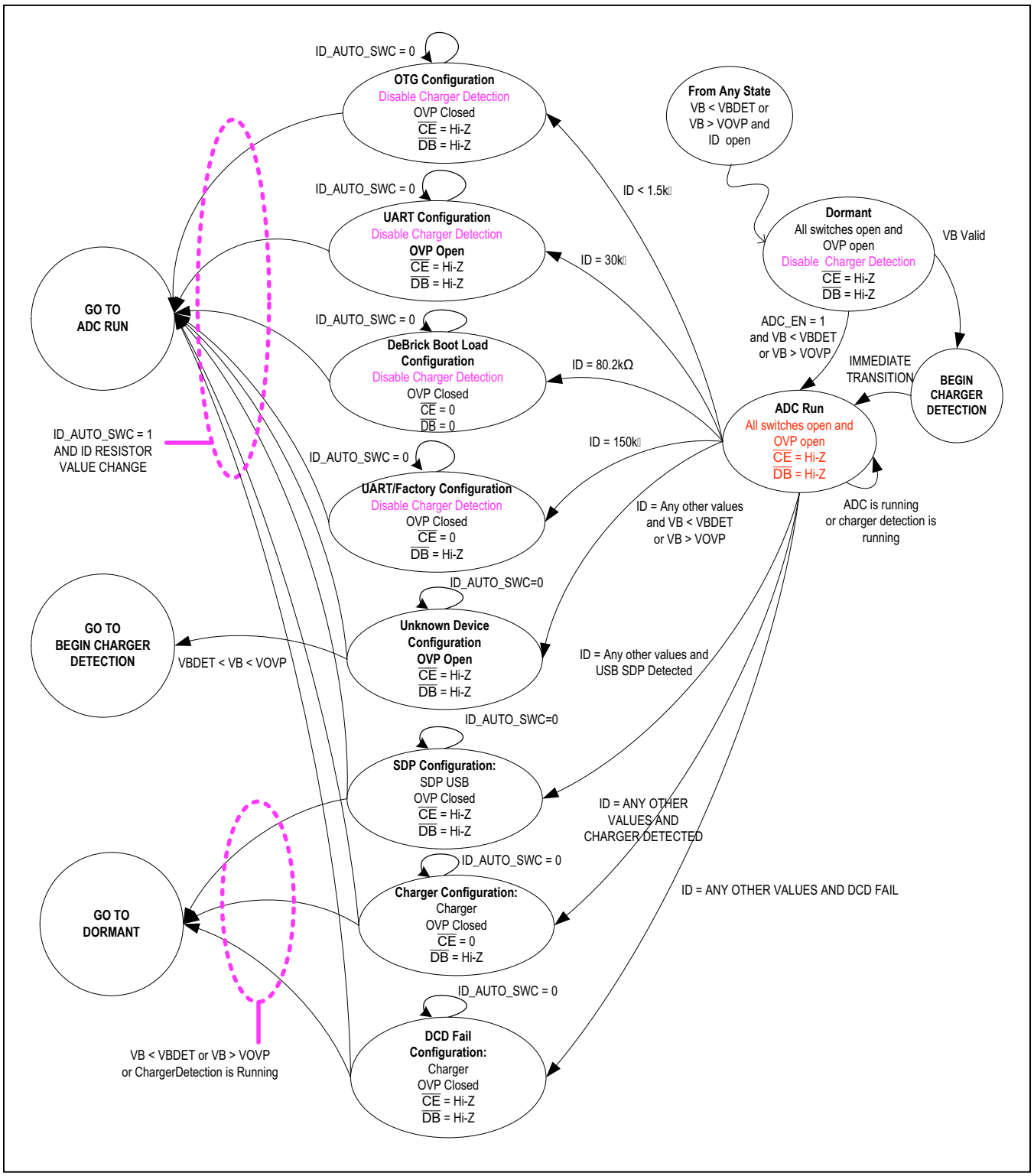


Figure 3. Operation State Diagram.

Detection Debounce

To avoid multiple interrupts at the insertion of an accessory, as well as for added noise/disturbance protection, a debounce timer 30ms (typ) is present that requires an inserted or removed state hold for the debounce time before it sends an interrupt.

USB Switch (CD+, CD-)

The device supports high-speed, full-speed, and low-speed USB signal levels. The USB channel is bidirectional and has low 3Ω (typ) on-resistance and 7pF (typ) on-capacitance. The low on-resistance is stable as the analog input signals are swept from ground to V_{SWPOS} for low signal distortion. This channel can pass negative audio signal without distortion when CP_EN = 1.

USB Switch (UT, UR)

The IC supports standard single-supply UART signals. The UART channel supports high-speed signals. The UART channel is bidirectional and has low 2.4Ω (typ) on-resistance. This channel can pass negative audio signal without distortion when CP_EN = 1.

Overvoltage Protection

The device features overvoltage protection up to +36V (max) on the V_{BUS} line. If the input voltage exceeds the overvoltage lockout cutoff threshold (V_{OVLO}), the internal FET with low 60mΩ (typ) on-resistance disconnects the input from the output and protects low-voltage systems against voltage faults. The device features soft-start capability to minimize inrush current by slowly turning the internal FET on when the V_B voltage is valid for a period longer than the debounce time (t_{MDEB}). When the overvoltage event occurs, the fault flag or interrupt is asserted depending on the INT_EN configuration in the CONTROL 1 (0x07) register.

Thermal Shutdown

The MAX20332 features thermal shutdown protection to protect the device from fault conditions. When the die temperature is +150°C, the device enters thermal shutdown mode and the fault flag or interrupt is asserted depending on INT_EN configuration in the CONTROL 1 (0x07) register. When the die temperature drops by 20°C, the device automatically resumes operation and the fault flag or interrupt is cleared.

Supply Voltage Selector

The MAX20332's supply voltage selector chooses between V_B and BAT inputs to power the internal blocks. If V_B is not present V_{CCINT} is supplied from BAT. A typical 100µs POR is provided at the rising edge of V_{CCINT}.

Interrupts

The MAX20332 generates an interrupt for any change in VB_VALID_S, when DCD_TMR_S transitions from 0 to 1, and when an overvoltage and thermal shutdown events occur. The INT_EN bit in the CONTROL 1 register (0x07) enables interrupt output. When INT_EN sets to disable, all interrupts are masked but not cleared. A read to the INTERRUPT 1 register (0x01) and INTERRUPT 2 register (0x02) is required to clear the interrupts. The $\overline{INT}$ pin is defaulted as a $\overline{FLAG}$ function when the interrupt is disabled (INT_EN = 0). The $\overline{INT}$ pin is pulled low when an invalid or an unknown charger is inserted or when a UART factory cable is detected.

Level-Triggered Interrupt

Set the INT_TYP bit in the CONTROL 1 (0x07) register low to select a level-triggered interrupt. Any unmasked interrupt event drives the $\overline{INT}$ line to its active level, and then holds it at that level until the interrupt register is read or cleared. Set the INT_POL bit in the CONTROL 1 (0x07) register to configure the active level of the $\overline{INT}$ line. Since multiple events share a level-triggered interrupt line, upon detecting assertion of the interrupt line, the host must read the entire interrupt registers. After servicing the interrupt, the host rechecks the interrupt line status to determine if an interrupt is pending.

Edge-Triggered Interrupt

Set the INT_TYP bit in the CONTROL 1 (0x07) register high to select an edge-triggered interrupt. Any unmasked interrupt event toggles the $\overline{INT}$ line to its active level with a pulse width set by the INT_DLY bit in the CONTROL 1 (0x07) register. Set the INT_POL bit in the CONTROL 1 (0x07) register to configure the active level of the $\overline{INT}$ line. If another interrupt occurs before the toggle is not over, the new interrupt event extends the toggle time by the period set by the INT_DLY bit in the CONTROL 1 (0x07) register.

Low-Power Modes

The MAX20332 has CP_EN and LOW_PWR bits in the CONTROL 1 register (0x07) dedicated to low-power operation. CP_EN controls the charge pump required for proper operation of the analog switches. When set to disable, no negative rail voltage can be applied.

The LOW_PWR bit sets low-power mode. In low-power mode, the internal oscillator is turned off under the following conditions: no V_{BUS}, USB_SWC = 00, CP_EN = 0, and ADC_S = 1111. When low-power mode is enabled, all switches are high-impedance. Note that no negative rail voltage can be applied.

When low-power mode is disabled, the oscillator and bandgap are always on. If V_{BUS} is not present, the low-power mode can be disabled, the switches can be closed, and the battery power mode can be enabled using I²C commands.

Digital Inputs

The digital inputs must be designed to be compatible with 1.8V logic.

Digital Outputs

The digital outputs are open drain and output is based on the ID resistor value. Table 4 shows the output status with different ID resistor settings.

Micro-USB ID Input

The resistor to GND at the ID pin of the USB connector determines the factory operating mode as defined in Table 3 and *Ordering Information* table.

Debrick/Boot Load

When ID resistor value is 80kΩ, the device enters Debrick/Boot Load operating mode. In this mode, $\overline{DB}$ output is low and can be used to put system micro into its Boot Loader mode allowing new firmware to be flashed.

I²C Serial Interface

Serial Addressing

The IC operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically, a microcontroller) initiates all data transfers to and from the IC and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START (S) condition (Figure 5) sent by a master, followed by the MAX14592 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP (P) condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 5.) When the master has

Table 4. Output Status*

STATUS									
MAX20332	**RESET**	**INVALID*** **	**OTG**	**UART**	**USB DEBRICK/ BOOT LOAD**	**UART/ FACTORY**	**KNOWN CHARGER**	**USB DCP CHARGER**	**USB DEVICE**
V_B	0V	Not Connected	Connected	Connected	Connected	Connected	Connected	Connected	Connected
ID	—	—	< 1.5kΩ	30kΩ	80kΩ	150kΩ	Undefined**	Undefined**	Undefined**
CD+	—	—	TD+	UR	TD+	UR	TD+	VDP_SRC	TD+
CD-	—	—	TD-	UT	TD-	UT	TD-	OPEN	TD-
OUT	High-Z	High-Z	V_B	High-Z	V_B	V_B	V_B	V_B	V_B
$\overline{CE}$	High-Z	High-Z	High-Z	High-Z	Low	Low	Low	Low	High-Z
$\overline{DB}$	High-Z	High-Z	High-Z	High-Z	Low	High-Z	High-Z	High-Z	High-Z
UR	High-Z	High-Z	High-Z	CD+	High-Z	CD+	High-Z	High-Z	High-Z
UT	High-Z	High-Z	High-Z	CD-	High-Z	CD-	High-Z	High-Z	High-Z
TD+	High-Z	High-Z	CD+	High-Z	CD+	High-Z	CD+	High-Z	CD+
TD-	High-Z	High-Z	CD-	High-Z	CD-	High-Z	CD-	High-Z	CD-
$\overline{INT}$	High-Z	Low	High-Z	Low	High-Z	High-Z	High-Z	High-Z	High-Z

**Table 4 is true when the I²C registers are set at default.*

***Undefined is any resistor value not specifically called out in this table.*

****ADC_EN = 1*

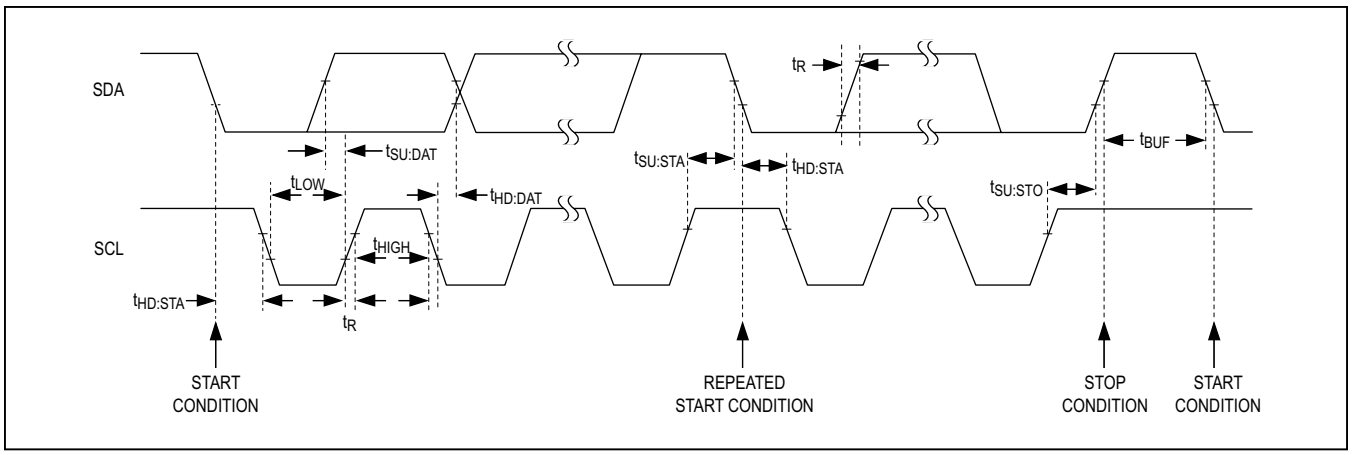


Figure 4. I²C Interface Timing

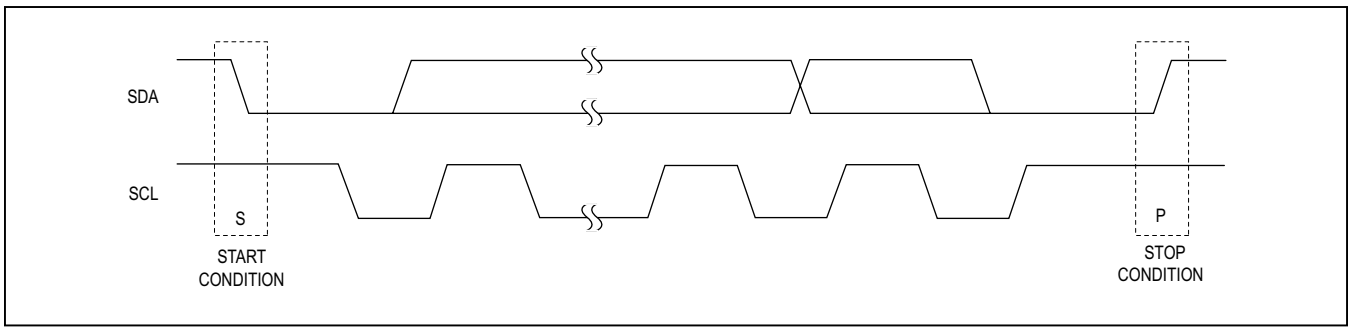


Figure 5. START and STOP Conditions

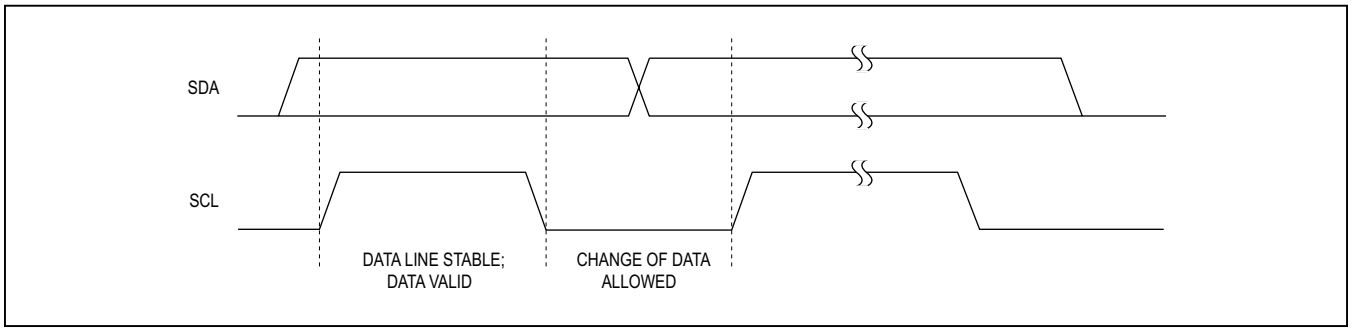


Figure 6. Bit Transfer

finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 6). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 7) that the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the IC, the IC generates the acknowledge bit because the IC is the recipient. When the IC is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The IC has a 7-bit long slave address (0110101b). The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 01101011 for read commands and 01101010 for write commands (Figure 8).

Bus Reset

The IC resets the bus with the I^2C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the IC transmits data to the master, thus the master is reading from the devices.

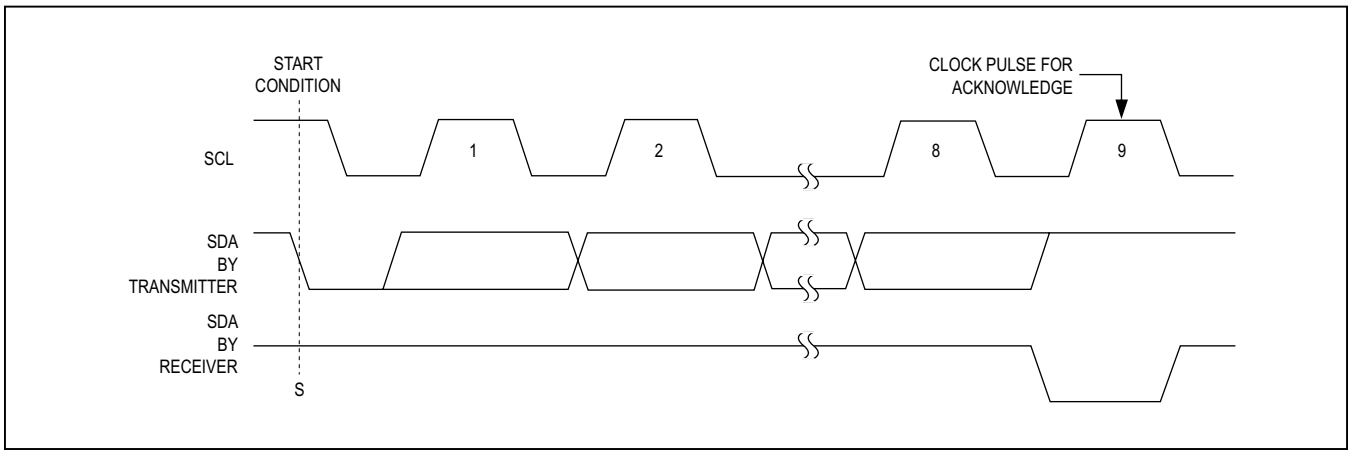


Figure 7. Acknowledge

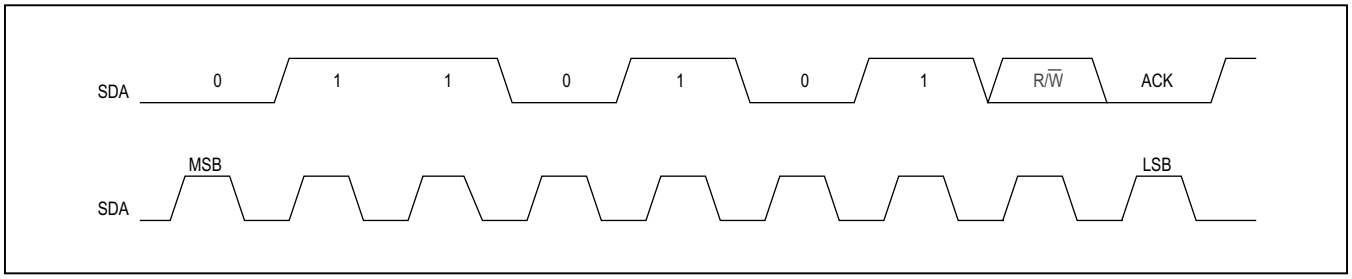


Figure 8. Slave Address

Format for Writing

A write to the IC comprises the transmission of the slave address with the R/$\overline{W}$ bit set to 0, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the IC is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the IC takes no further action beyond storing the register address (Figure 9). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 10). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement.

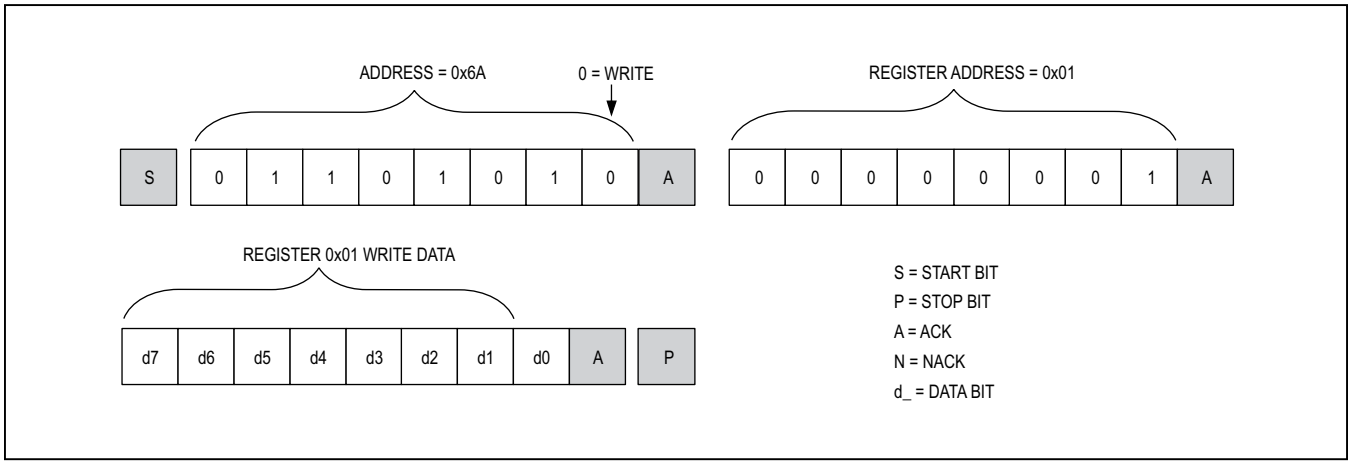


Figure 9. Format for I²C Write

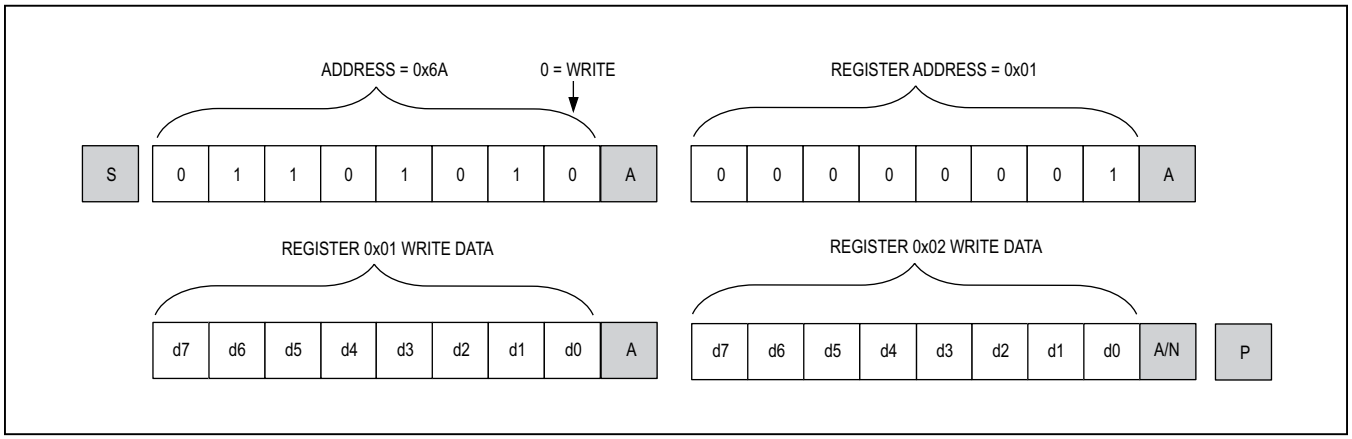


Figure 10. Format for Writing to Multiple Registers

Format for Reading

The IC is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Therefore, a read is initiated by first configuring the register address by performing a write (Figure 11). The master can now read consecutive bytes from the IC, with the first data byte being read from the register address pointed to by the previously written register address. Once the master sends a NACK, the IC stops sending valid data.

Applications Information

Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended/90Ω differential controlled-impedance matched traces of equal lengths.

Power-Supply Bypassing

Bypass V_B and BAT with 1µF ceramic capacitors to GND as close as possible to the device.

Power-On Reset (POR)

The MAX20332 provides secure operation with the power-on-reset circuits. When the power supply for the device exceeds the POR rising value 1.6V (typ) and stays above the maximum falling edge, the internal logic is in a known state for safe operation. However, the *Electrical Characteristics* table parameters are not guaranteed until the V_B and BAT voltages meet the specified global conditions.

Choosing I²C Pullup Resistors

I²C requires pullup resistors to provide a logic-high level to data and clock lines. There are trade-offs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when device is not in operation. I²C specifies 300ns rise time to go from low to high (30% to 70%) for fast mode, which is defined for a clock frequency up to 400kHz (see the I²C specifications in the *Electrical Characteristics* table for details).

To meet the rise time requirement, choose pullup resistors so that the rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. If the transition time becomes too slow, the setup and hold times might not be met and waveforms might not be recognized.

Resetting I²C from Suspend

If the I²C bus is suspendered due to weak or dead battery, an I²C STOP command needs to be performed after enabling the I²C buffers and pullup bias. The I²C STOP command is necessary before restarting the I²C traffic.

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. The CD-, CD+, and ID pins are further protected against ESD up to ±15kV (HBM) without damage. The V_B input withstands up to ±15kV (HBM) if bypassed with a 1µF ceramic capacitor close to the pin. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the IC continues to function without latchup.

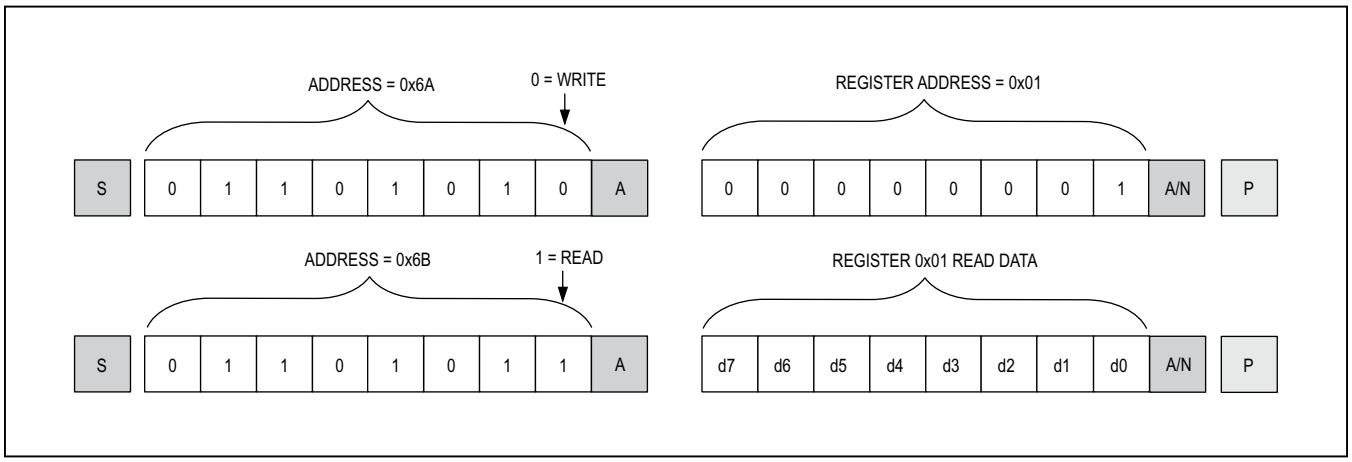


Figure 11. Format for Reads (Repeated START)

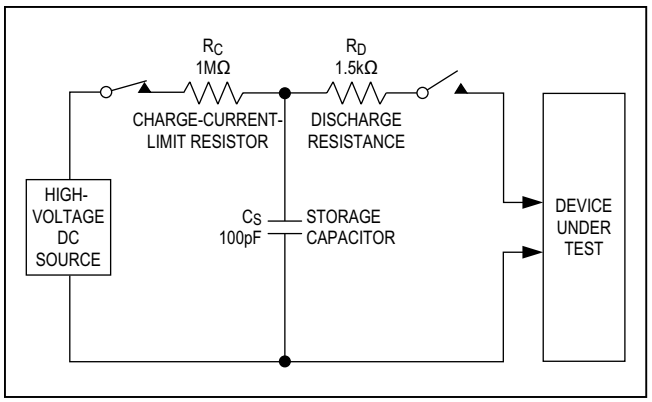


Figure 12. Human Body ESD Test Model

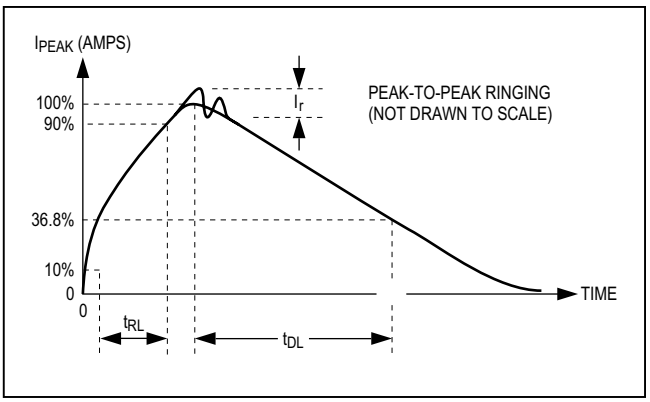


Figure 13. Human Body Current Waveform

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 12 shows the Human Body Model, while Figure 13 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX20332EWE+T	-40°C to +85°C	16 WLP	AAL

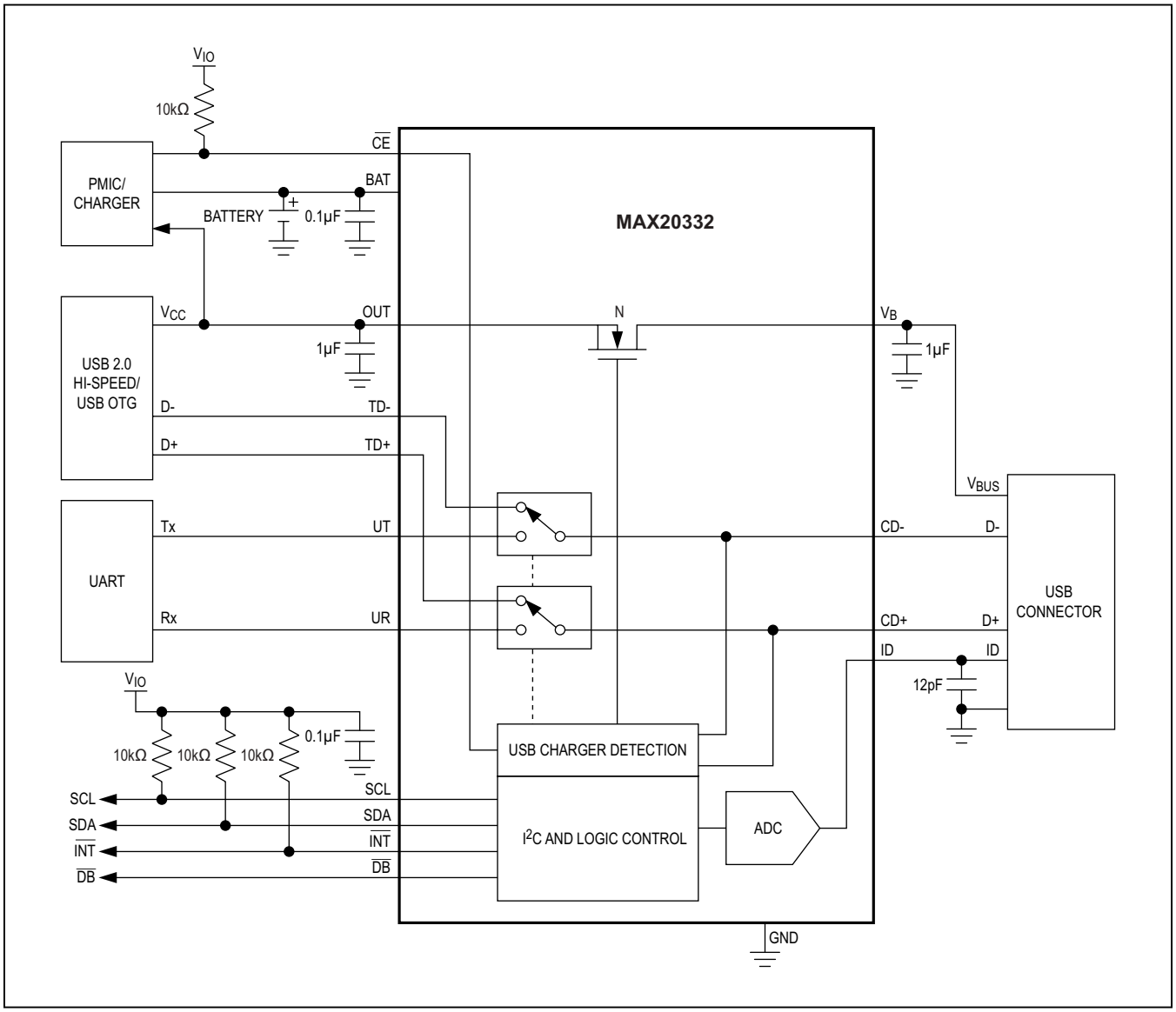
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W161C1+2	**21-100246**	Refer to **Application Note 1891**

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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