MAX20766

Smart Slave IC with Integrated Current and Temperature Sensors

General Description

The MAX20766 is a feature-rich smart slave IC designed to work with Maxim's seventh-generation controller to implement a high-density multiphase voltage regulator. Up to six smart slave ICs, plus a controller IC, provide a compact synchronous buck converter that includes accurate individual phase-current and temperature reporting through SMBus/PMBus™. This smart slave device includes protection circuits for overtemperature, VX short, and all power-supply UVLO faults. If a fault is detected, the slave IC immediately shuts down and sends a fault signal to the controller IC.

Monolithic integration and advanced packaging technologies allow practical per-phase, high-switching frequencies with significantly lower losses than alternative implementations. Smart slave ICs are designed to support phase shedding and DCM modes for efficiency optimization over a wide range of load currents. High per-phase current-capability designs with low C_{OUT} enable a design with fewer phases and a smaller footprint.

The MAX20766 is available in a 16-pin FCQFN package with exposed top-side thermal pads. Top-side cooling improves heat transfer to ambient and reduces PCB and component temperatures.

Applications

- Communication and Networking Equipment
- Servers and Storage Equipment
- High-Current Voltage Regulators
  - Networking ASICs
  - FPGAs
  - Microprocessor Chipsets
  - Memory

DEVICE TYPE	OPERATING CURRENT (A)	INPUT VOLTAGE (V)
Electrical	55 per phase	6.5 to 16.0
85°C, No Airflow	24 per phase, two-phase application	

Note: *For specific operating conditions, see the SOA curves in the Typical Operating Characteristics section. Thermal rating based on 2-phase data.*

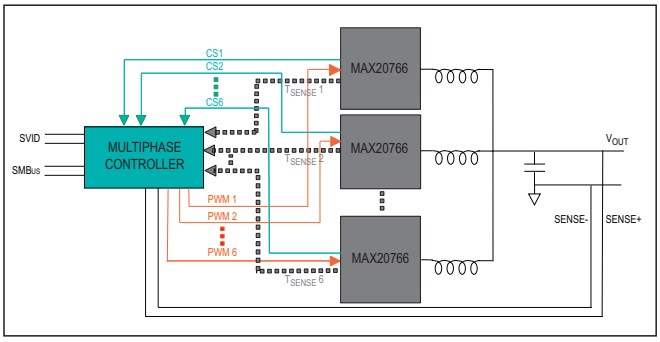
Benefits and Features

- Increased Power Density with Fewer External Components
  - Monolithic Integration for Reduced Parasitics
  - Scalable Architecture Compatible with Coupled Inductors
  - 94% Peak Efficiency
  - Top-Side Cooling for Improved Heat Transfer to Ambient
- Accurate Real-Time Telemetry of Critical Parameters
  - PMBus-Compliant Interface through the Controller IC for Telemetry and Power Management
  - Junction Temperature Monitoring and Reporting
  - Per-Phase Current Reporting
- Advanced Self-Protection Features for the System and IC
  - Overcurrent Protection
  - Overtemperature Protection
  - Boost Voltage UVLO
  - VX Short Protection

***Ordering Information** appears at end of data sheet.*

PMBus is a trademark of SMIF, Inc.

Typical Application Circuit



19-8577; Rev 1; 12/17

maxim integrated™

Absolute Maximum Ratings

Supply Voltage V_{DDH} ..... -0.3V to +18V
Supply and Input Pin Voltages V_{CC}, V_{DD} ..... -0.3V to +2.5V
Switching-Node Voltage (VX) DC ..... -0.3V to +18V
Switching-Node Voltage (VX) 25ns (Note 1) ..... -10V to +23V
V_{DDH} Pin to VX Pin Differential 25ns (Note 2) ..... -10V to +23V
BST Pin (BST) DC ..... -0.3V to +20.5V
BST Pin (BST) 25ns ..... -6.0V to +27V
BST Pin to VX Pin Differential ..... +2.5V
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Peak Reflow Temperature ..... +260°C
CS ..... -0.3V to +2.5V
$\overline{TS_FAULT}$ ..... -0.3V to V_{DD} + 0.3V
PWM ..... -0.3V to +2.5V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

V_{DD}, V_{CC} ..... +1.71V to +1.98V
12V Supply (V_{DDH}) ..... +6.5V to +16.0V
Frequency (f_{SW}) ..... 300kHz to 1.3MHz

Note 1: The 25ns rating is the allowable voltage that the VX node may exceed the -0.3V to +18V ratings in either positive or negative direction for up to 25ns per cycle.

Note 2: A high-frequency input bypass capacitor must be located less than 60mils (1.524mm) from the V_{DDH} and V_{SS} pins.

Package Information

PACKAGE TYPE: 16 FCQFN	
Package Code	P163A6F+2
Outline Number	**21-0986**
Land Pattern Number	**90-0490**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Case (θ_{JC})	+0.42°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = V_{CC} = +1.8V, V_{DDH} = +12V, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES, SUPPLY CURRENT						
Bias Supply Voltage	V_{DD}, V_{CC}		1.71		1.98	V
Powertrain Input Voltage	V_{DDH}		6.5	12.0	16.0	V
1.8V Bias Supply Current	I_{VCC} + I_{VDD}	Shutdown (Note 3)		0.5	2	µA
		Inactive, no switching (Note 4)		3.2	5.0	mA
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 1.3MHz (Note 5)		43	61	mA
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 300kHz (Note 5)		14	20	mA
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 600kHz (Note 5)		29	41	mA
12V Bias Supply Current	I_{VDDH}	Shutdown (Note 3)		1.3	10	µA
		Inactive, no switching (Note 4)		6.5	20	µA
I_{RECON} SPECIFICATION						
Current Gain (I_L to CS)	AI	-35A < I_L < +50A (Note 5)	95,000	100,000	105,000	A/A
TEMPERATURE SENSOR SPECIFICATIONS						
Temperature Sensor Gain	A_{TEMP}			3.01		mV/°C
Temperature Sensor Voltage	—	T_J = 0°C		832		mV
PROTECTION FEATURES						
V_{DD} UVLO Threshold (Rising)	V_{DD_UVLO}		1.47	1.57	1.64	V
V_{DD} UVLO Threshold (Falling)			1.41	1.5	1.58	V
V_{DDH} UVLO Threshold (Rising)	V_{DDH_UVLO}		4.05	4.27	4.44	V
V_{DDH} UVLO Threshold (Falling)			3.90	4.09	4.30	V
BST UVLO Threshold (Rising)	V_{BST_UVLO}	(Note 6)	1.39	1.52	1.66	V
BST UVLO Threshold (Falling)			1.29	1.45	1.58	V
Peak Positive-OCP Clamp Level	I_{OCP_CLAMP}	(Note 5, 8)	64	72	80	A
Peak Positive-OCP Clamp Delay (Note 7)	$I_{OCP_CLAMP_DELAY}$			13		ns
Peak Positive-OCP Falling Level	I_{OCP_FALL}		45.7	54.9	64.2	A
Peak Negative-OCP Clamp Level	I_{NOCP_CLAMP}		-79.1	-71.9	-64.7	A
Peak Negative-OCP Delay (Note 9)	$I_{NOCP_CLAMP_DELAY}$			68.5		ns
Overtemperature Shutdown	OTP	Rising threshold	148	160	172	°C

Electrical Characteristics (continued)

(V_{DD} = V_{CC} = +1.8V, V_{DDH} = +12V, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM INPUT						
Input Voltage, High State	V_{IH}		V_{DD} - 0.20			V
Input Voltage, Low State	V_{IL}				0.20	V
Tristate Control Threshold (PWM Input Rising)	—			0.63		V
$\overline{\text{TS_FAULT}}$ INPUT						
$\overline{\text{TS_FAULT}}$ Digital Threshold V_{IH}	V_{IH}		0.41			V
$\overline{\text{TS_FAULT}}$ Digital Threshold V_{IL}	V_{IL}				0.17	V

Note 3: T_{SENSE}, PWM, and CS pins of the slave are pulled low by the controller. The slave is in this state before the controller is enabled.

Note 4: Inactive, no switching: PWM signal is three stated by the controller. The slave is in this mode when the controller sheds a phase (temporarily disabling this slave) to save power at lighter loads.

Note 5: Design guaranteed by bench characterization. Limits are not production tested.

Note 6: BST UVLO is measured with respect to VX and not from ground.

Note 7: Delay is defined as the time input threshold is crossed to the time FET turns off. V_{DD} = V_{CC} = 1.8V, V_{DDH} = 12V, inductor = 50nH

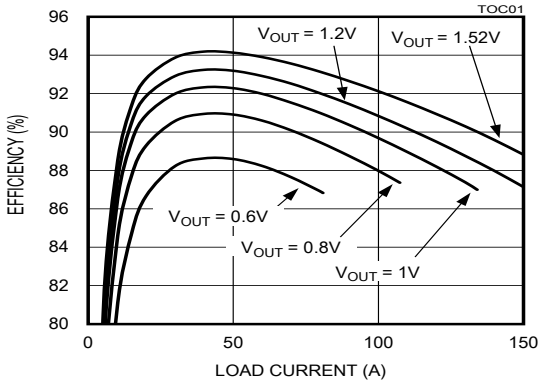
Note 8: Limits are ±4σ about the mean.

Note 9: Delay is defined as the time input threshold is crossed to the time comparator output toggles. V_{DD} = V_{CC} = 1.8V, V_{DDH} = 12V, inductor = 50nH

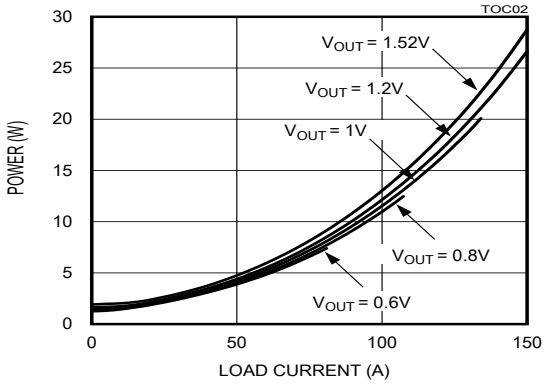
Typical Operating Characteristics

(**Controller: T_A = +25°C**; f_{SW} = 500kHz, unless otherwise noted.)

EFFICIENCY vs. LOAD CURRENT 4X MAX20766

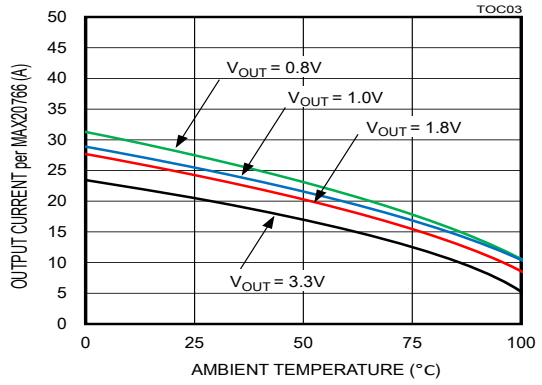


SYSTEM POWER DISSIPATION vs. LOAD CURRENT 4X MAX20766

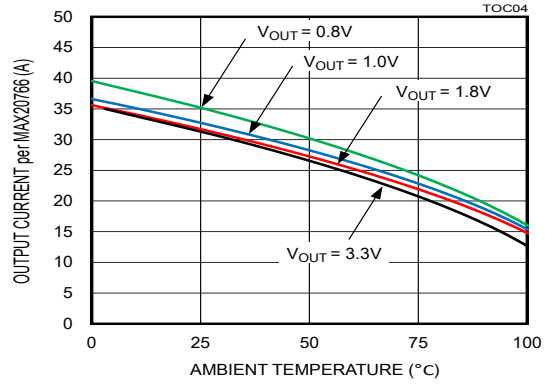


(**Thermal parameters are taken from an evaluation board with 4xMAX20766 and MAX20751 controller at V_{IN} = 12V,** f_{SW} = 500kHz, unless otherwise noted.)

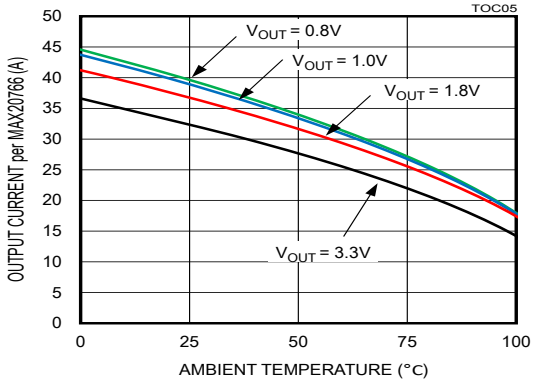
SAFE OPERATING AREA (SOA) NO AIR FLOW, NO HEATSINK



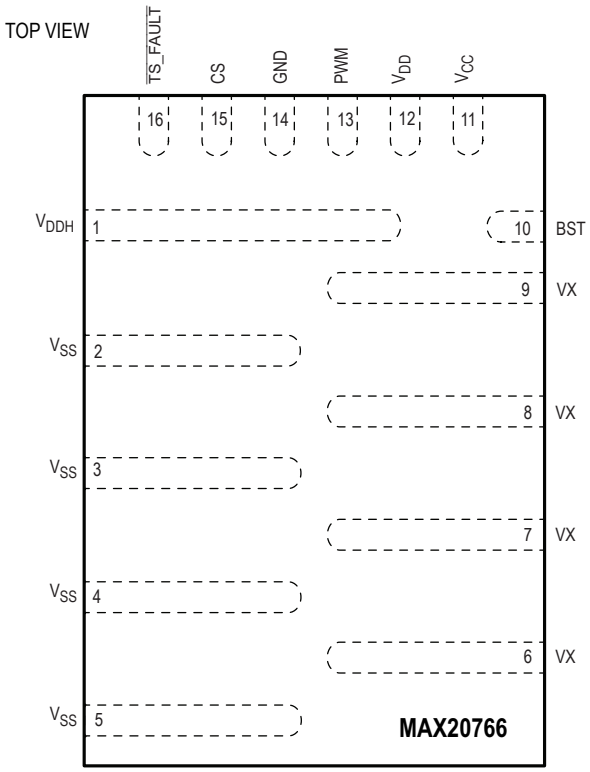
SAFE OPERATING AREA (SOA) 200LFM AIR FLOW, NO HEATSINK



SAFE OPERATING AREA (SOA) 400LFM AIR FLOW, NO HEATSINK



Pin Configuration

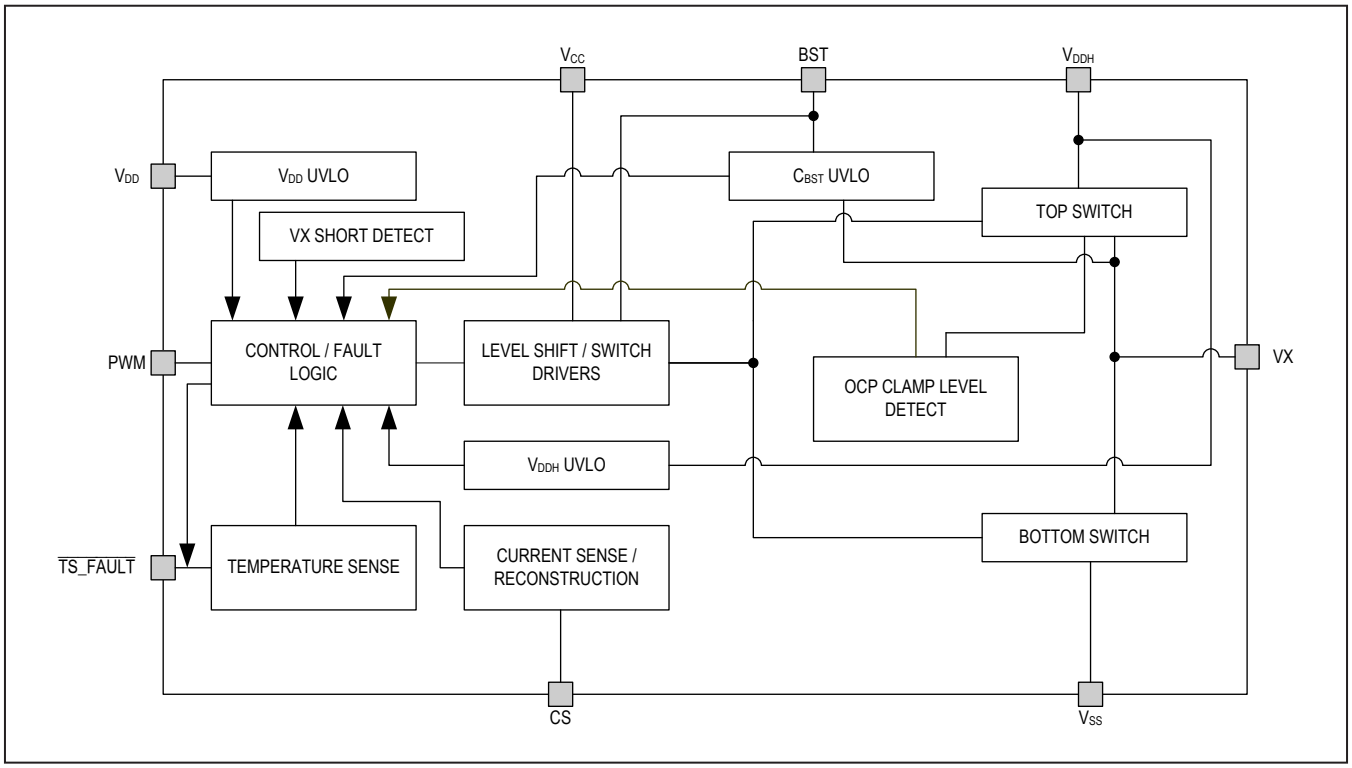


16-PIN FCQFN

Pin Description

PIN	NAME	FUNCTION
1	V_{DDH}	12V Input Supply Voltage Node. This node connects to the 12V input power source. High-frequency decoupling capacitors must be placed in close proximity to the slave IC on the same side as the MAX20766 (see Table 2).
2–5	V_{SS}	Power-Switch Ground Node. These nodes normally connect directly to the ground plane.
6–9	VX	Switching Node. These nodes connect the switching node of the power devices to the output inductor.
10	BST	Bootstrap Supply for High-Side Drivers. Decouple this pin with 0.22µF capacitor (see Table 2).
11	V_{CC}	1.8V Supply for Low-Side Drivers. Decouple this pin with a 1µF capacitor (see Table 2).
12	V_{DD}	1.8V Supply for Control Circuits. Decouple this pin with a 0.1µF capacitor (see Table 2).
13	PWM	PWM Input Node. Connect this node to the PWM output pin from the master.
14	GND	Ground for Control Circuits
15	I_{SENSE}	Current-Sense Output Node. Connect this node to the current-sense input of the master through a simple passive filter (3.01kΩ, add 22pF capacitor if excessive board noise is present).
16	$\overline{TS_FAULT}$	Temperature-Sense and Fault Output Node. Connect this node to the temperature-sense pin of the master through a simple passive filter (4.7Ω + 100pF).

Block Diagram



Detailed Description

Voltage Regulation

Maxim smart slave ICs provide the control logic, drivers, monitoring circuits, and power semiconductors for a synchronous buck converter. Precision measurement circuitry enables fault protection, status monitoring, and accurate lossless current sensing. Phases are controlled by the controller IC independently by separate pulse-width modulation (PWM) control signals.

Power-Switch Control and Drivers

The smart slave ICs operate in conjunction with a Maxim controller IC. The controller configures the voltage regulator through pin strapping and the number of populated phases. The smart slave IC's switching is controlled by the proprietary command signals on the PWM signals. The PWM control signal has three defined states: high, low, and three state. The three-state signal is used for phase shedding and DCM modes.

An external boost capacitor (0.22µF) is required to supply the voltage for the high-side switch driver. V_{DD} and V_{CC} are brought out separately to allow separate decoupling to improve noise immunity on the V_{DD} rail. The V_{DD} pin requires a 0.1µF decoupling capacitor. The V_{CC} pin requires 1µF decoupling capacitor. A 10Ω filter resistor is required between the V_{DD} and V_{CC} pins of each smart slave IC.

Current-Sense Output

The integrated lossless current sense (or "current reconstruction") produces a precise ratiometric current-sense signal (CS) for both positive and negative currents. CS connects to the controller as an analog current signal. This current-sense technology provides accurate current information over load and temperature not affected by tolerances of passive elements such as the output inductor, resistors, and capacitors.

Phase Configuration

The ability for the controller to dynamically disable and re-enable a phase is an integral part of the Maxim controller/slave architecture. The controller sets the phase control signal to three state to disable a phase; the same state is used to control DCM operation. When using a coupled-inductor mode, a proprietary mode can be set by the controller, communicated to the smart slave through PWM to minimize losses due to coupled currents in inactive phases.

Protection Circuits

Overcurrent Protection

The smart slave ICs incorporate instantaneous overcurrent-fault protection using the lossless current sense. This overcurrent protection is separate from the system overcurrent protection, and is intended to operate only in extreme fault conditions to protect the IC and other components.

The system overcurrent protection set by the controller should be set with sufficient margin below the individual slave's threshold to ensure correct system operation. For current-sourcing operation, if the instantaneous current in the top switch exceeds the overcurrent-protection threshold listed in the *Electrical Characteristics* table, the slave truncates the top-side switch to keep its peak current at a safe level. The overcurrent-protection mechanism is shown in Figure 1. The protection threshold is set to ensure that the IC's maximum allowable peak current is not exceeded when using the recommended inductors. Limiting the current sourcing is not considered a hard fault condition for the slave; therefore, $\overline{TS_FAULT}$ is not asserted. Since clamping is based on instantaneous reconstructed current, the ripple current must be considered when calculating the maximum average current per slave. The maximum average current before clamping can be calculated using Equation 1. Limits shown in the *Electrical Characteristics* table reflect expected variations in application conditions and external component characteristics. Also note that the controller (i.e., the system) overcurrent protection should be set lower than the corresponding slave's maximum operating current, as stated above.

Equation 1:

$$I_{SDCA} = I_{OCP_CLAMP} - \frac{I_{RIPPLE}}{2}$$

where:

I_{SDCA} = Maximum average DC slave current (A)

I_{OCP_CLAMP} = Peak OCP clamp level (A)

I_{RIPPLE} = Peak-to-peak inductor ripple current (A)

The MAX20766 also includes a negative current limit. If the negative protection limit is reached, the slave limits the FET off-time and $\overline{TS_FAULT}$ is not asserted.

V_{DD} and BST Undervoltage Lockout (UVLO)

The smart slave ICs include UVLO circuits on the V_{DD} and BST inputs. For power-sequencing guidelines and operation with separate bias rails for controller and slaves, refer to the data sheet of the controller used to drive the MAX20766. BST UVLO is active at all times after the initial system startup. It is not active during the initial system power-on state (before regulation is enabled), and is activated approximately 20µs after initial startup. If either of these UVLO circuits is tripped during operation, the smart slave stops switching and $\overline{TS_FAULT}$ is pulled low.

V_{IN} (V_{DDH}) Undervoltage Lockout

The smart slave ICs include a protection circuit that shuts down the slave and asserts $\overline{TS_FAULT}$ if V_{DDH} is below V_{DDH_UVLO}. If this circuit is tripped during operation, the slave stops switching, and $\overline{TS_FAULT}$ is pulled low.

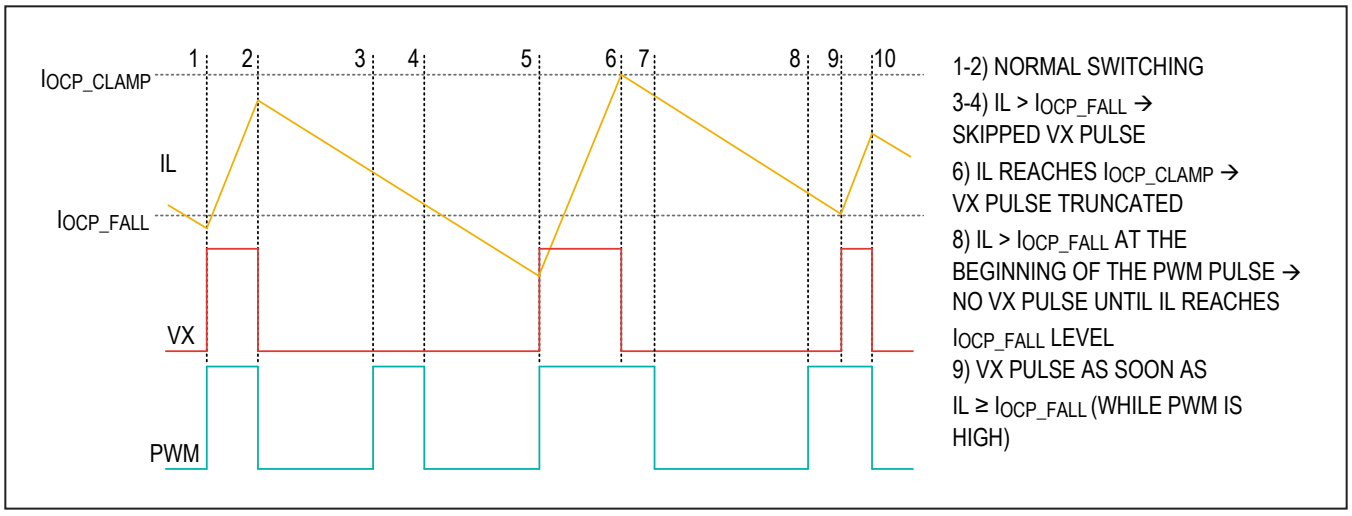


Figure 1. Overcurrent Protection Behavior

Temperature Sensing and Overtemperature Protection

Each smart slave IC incorporates an accurate die temperature sensor. The temperature-sense signal is sent to the controller as an analog signal through the temperature-sense pin. The actual temperature of each smart slave IC is then made available through the SMBus of the controller. The smart slave IC also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the controller through the $\overline{TS_FAULT}$ pin.

VX Short Protection

The smart slave ICs include a VX short detection during switching to detect a local short circuit from the VX node to either V_{DDH} or ground. If such a fault is detected, the slave shuts down and communicates a fault to the controller through the $\overline{TS_FAULT}$ pin.

$\overline{TS_FAULT}$ Signal

If a fault is detected, the smart slave IC sends a signal to the controller by pulling the $\overline{TS_FAULT}$ pin low. Under normal conditions, this pin is used to send an accurate analog voltage representation of the slave's temperature. If a fault is detected, this pin is asserted low. Table 1 summarizes the faults and the slave's exact response. For a latching fault, the fault must be cleared by power cycling V_{DD}.

Design Considerations

Phase-Current Sharing and Steering Control

Maxim controller/slave chipsets offer options for thermal balancing in applications where one or more phases have different thermal characteristics. The current-sense and chipset regulation system offer the potential for current steering, where a percentage of current can be steered away from any phase, allowing that phase to operate at a different current than the other phases. This allows a precise scaling of current in any slave or slaves to achieve proper thermal balance. For more information about how to program this feature, refer to the data sheet of the controller used to drive the MAX20766.

Thermal Path and PCB Design

The smart slave IC has a package that exposes the top side of the die. The top side of the die is electrically connected to GND/V_{SS}, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results in a low junction-to-ambient thermal impedance, and hence lower junction temperature. This method provides an additional thermal path to the heat flow from the die-to-PCB-to-ambient temperature, and also reduces the temperature of the PCB. Use a pad and an insulator that electrically insulates the top side of the die from the heatsink if a heatsink is used. Thermal performance is presented for various thermal conditions and airflow rates in the safe operating area (SOA) plots in the *Typical Operating Characteristics* section.

Table 1. Fault-Detection and Protection Circuits

FAULT	DESCRIPTION	TYPE	FAULT FLAG ($\overline{TS_FAULT}$)
BST UVLO	Undervoltage Lockout on Boost Supply	Shutdown (Note 1)	Asserted
$V_{DDH\ UVLO}$	Undervoltage Lockout on V_{DDH}	Shutdown (Note 1)	Asserted
$V_{DD\ UVLO}$	Undervoltage Lockout Signal on V_{DD}	Shutdown (Note 1)	Asserted
VX Short	VX Short-to-Ground or V_{DDH}	Shutdown (Note 2)	Asserted
POCP (Sourcing)	Positive (Sourcing) Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
NOCP (Sinking)	Negative (Sinking) Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
OTP	Overtemperature Protection	Shutdown (Note 2)	Asserted

Note 1: *V_{DDH} UVLO, BST UVLO, and V_{DD} UVLO are nonlatching faults. If the slave detects a nonlatching fault, it asserts the $\overline{TS_FAULT}$ signal low and stops switching. The slave resumes switching and deasserts $\overline{TS_FAULT}$ approximately 37µs from when the fault condition is removed. For the controller response to $\overline{TS_FAULT}$ being asserted low by the slave device, refer to the data sheet of the controller used to drive the MAX20766.*

Note 2: *VX Short and OTP are latching faults and must be reset by power cycling V_{DD}.*

PCB Layout Guidelines

The PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input capacitors and the output inductor, which should be placed close to the IC. The VX traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces not only be kept short, but also be shielded with a ground plane immediately beneath. Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Contact Maxim to obtain QFN layout guidelines for optimal design.

Table 2. Typical Boost, Filtering, and Decoupling Capacitor Requirements

DESCRIPTION	VALUE	TYPE	PACKAGE	QTY
V_{DD} Capacitor	0.1µF/6.3V	X7R	0603	1
V_{CC} Capacitor	1µF/6.3V	X7R	0603	1
BST Capacitor	0.22µF/6.3V	X7R	0402	1
V_{DD} R_{FILTER}	10Ω	1/16W 1%	0402	1
V_{DDH} HF Capacitor (Note 1)	1µF/25V	X7R	0603	2
V_{DDH} HF Capacitor (Note 2)	4.7µF/25V	X7R	0402	2
V_{DDH} Bulk Capacitor (Note 3)	10µF/25V	X5R	0805/1206	2

Note 1: *All V_{DDH} high-frequency capacitors must be placed in close proximity to the slave IC and on the same side of the PCB as the slave IC. Refer to the PCB Layout Guidelines section for component placement requirements and recommendations.*

Note 2: *For operation below 10.8V, two 22µF bulk capacitors are recommended instead of two 10µF capacitors.*

Note 3: *V_{CC} should be directly connected to the bias supply.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20766EPE+T	-40°C to +85°C	16 FCQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	12/17	Updated table on first page	1

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