19-3104; Rev 2; 10/09

EVALUATION KIT AVAILABLE

ISDB-T 1-Segment Tuner

MAX2163

General Description

The MAX2163 low-IF tuner IC is designed for use in 1-segment ISDB-T applications. The MAX2163 directly converts UHF band signals to a low-IF using a broadband I/Q downconverter. The operating frequency range covers the UHF band from 470MHz to 806MHz.

The MAX2163 includes LNAs, RF variable gain amplifiers, I and Q downconverting mixers, a baseband variable gain amplifier, and a low-IF filter. The MAX2163's variable gain amplifiers provide in excess of 100dB of control range.

The MAX2163 also includes fully monolithic VCOs as well as a complete frequency synthesizer including an on-chip crystal oscillator and output buffer. The device operates with a crystal from 32MHz to 36MHz.

The MAX2163 features a 2-wire I²C-compatible serial-control interface. A low-power standby mode is available that shuts down the signal path leaving the control interface and register circuits active. Additionally, an external pin can shut down the entire device.

The MAX2163 is specified for operation in the extended -40°C to +85°C temperature range and is available in a 5mm x 5mm x 0.8mm, 28-pin thin QFN, lead-free plastic package with exposed paddle (EP).

Applications

Cell Phone Mobile TV

Personal Digital Assistants (PDAs)

Game Consoles

Portable TV Devices

Portable Audio Devices

Automotive

Home Audio

Typical Application Circuit appears at end of data sheet.

Features

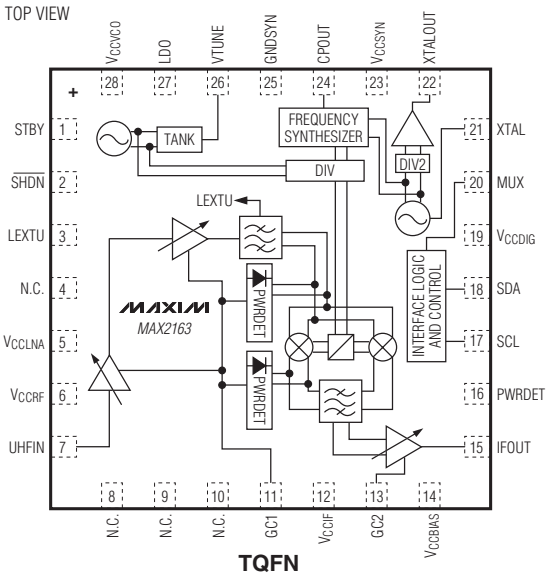
- **Frequency Range**
  UHF: 470MHz to 806MHz (UHFIN)
- **Low Noise Figure: 3.2dB (typ)**
- **High Dynamic Range: -99dBm to 0dBm**
- **Optional UHF Tracking Filter**
- **Integrated VCO and Frequency Synthesizer**
- **Low LO Phase Noise: -87dBc/Hz at 10kHz**
- **Integrated Variable BW Low-IF Filters**
- **Greater Than 40dB Image Rejection**
- **Single +2.4V to +3.47V Supply**
- **Low Power: 80mW (typ) at +2.5V**
- **2-Wire I²C Serial-Control Interface**
- **Low-Power Shutdown and Standby Modes**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2163ETI+	-40°C to +85°C	28 TQFN-EP*
MAX2163ETI/V+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Pin Configuration/ Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ISDB-T 1-Segment Tuner

ABSOLUTE MAXIMUM RATINGS

All $V_{CC_}$ Pins to GND .....-0.3V to +3.6V
UHFIN to GND .....-0.3V to +0.9V
IFOUT to GND .....-0.3V to (V_{CC} + 0.3V)
GC1, GC2, VTUNE, XTALOUT, XTAL to GND .....-0.3V to (V_{CC} + 0.3V)
CPOUT, XTLOUT, PWRDET to GND .....-0.3V to (V_{CC} + 0.3V)
SDA, SCL, $\overline{SHDN}$, STBY to GND .....-0.3V to (V_{CC} + 0.3V)
MUX, LEXTU, LDO to GND .....-0.3V to (V_{CC} + 0.3V)
Maximum RF Input Signal UHFIN .....+10dBm
Short-Circuit Duration IFOUT, CPOUT, XTALOUT, PWRDET, SDA, MUX 10s
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2163 Evaluation Kit, V_{CC} = +2.4V to +3.47V, V_{GC1} = V_{GC2} = 0.3V (maximum gain), no RF input signal at UHFIN. IFOUT is open circuited and the VCO is active with f_{LO} = 557.714MHz, default register settings, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A =+25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND SUPPLY CURRENT					
Supply Voltage		2.4	2.5	3.47	V
Supply Current Normal Mode			30.4	40	mA
Supply Current High-Linearity Mode	RFVGA = 1; MXR = 1		35	44	mA
Supply Current HW or SW Standby Mode			1.1	2.0	mA
Supply Current Shutdown Mode			1	20	µA
ANALOG GAIN-CONTROL INPUTS (GC1, GC2)					
Voltage Range	Maximum gain = 0.3V	0.3		2.1	V
Input Bias Current		-15		+15	µA
POWER DETECTOR OUTPUT BUFFER (PWRDET)					
Output Voltage Range	Load impedance = 2kΩ||10pF	0.3		2.1	V
Output Impedance			25		Ω
VCO TUNING VOLTAGE INPUT (VTUNE)					
Voltage Range		0.35		2.05	V
DIGITAL CONTROLS ($\overline{SHDN}$, STBY)					
Input Logic-Level High		0.7 x V_{CC}			V
Input Logic-Level Low				0.3 x V_{CC}	V
2-WIRE SERIAL I^2C DIGITAL INPUTS (SCL, SDA)					
Clock Frequency				400	kHz
Input Logic-Level High		0.7 x V_{CC}			V
Input Logic-Level Low				0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2163 Evaluation Kit, V_{CC} = +2.4V to +3.47V, V_{GC1} = V_{GC2} = 0.3V (maximum gain), no RF input signal at UHFIN. IFOUT is open circuited and the VCO is active with f_{LO} = 557.714MHz, default register settings, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A =+25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE SERIAL I²C DIGITAL OUTPUT (SDA)					
Output Logic-Level Low				0.4	V
MUX DIGITAL OUTPUT					
Output Logic-Level Low				0.3 x V_{CC}	V
Output Logic-Level High		0.7 x V_{CC}			V

AC ELECTRICAL CHARACTERISTICS

(MAX2163 Evaluation Kit, V_{CC} = +2.4V to +3.47V, f_{RF} = 557.143MHz, f_{LO} = 557.714MHz, f_{IF} = 571kHz, f_{XTAL} = 36MHz, V_{GC1} = V_{GC2} = 0.3V (maximum gain), default register settings, RF input signals as specified, IF output load as specified, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, $\overline{SHDN}$ = V_{CC}, STBY = GND, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SIGNAL PATH PERFORMANCE					
Receive Input Frequency Range	UHFIN (Note 2)	470		806	MHz
Maximum Voltage Gain	-100dBm CW tone, V_{GC1} = V_{GC2} = 0.3V V_{IFOUT} = 0.225V_{P-P}	96			dB
Minimum Voltage Gain	0dBm CW tone, V_{GC1} = V_{GC2} = 2.1V V_{IFOUT} = 0.1V_{P-P}			-2	dB
RF Gain Control Range (GC1)		40	52		dB
Analog IF Gain Control Range (GC2)		60	76		dB
In-Band IM3	(Note 3)		-40		dBc
Out-of-Band IIP3	(Note 4)		30		dBm
Input P_{1dB}	In-band CW tone, V_{GC1} = V_{GC2} = 2.1V		0		dBm
Image Rejection	T_A = +25°C, +85°C	40	49		dB
Noise Figure	T_A = +25°C, 470MHz < f_{RF} < 806MHz		3.2	5.3	dB
OPTIONAL UHF TRACKING FILTER					
Center Frequency			640		MHz
Nominal 3dB Bandwidth	LEXTU = 18nH, Q_{MIN} = 35		320		MHz
WIDEBAND RF OVERLOAD DETECTOR					
Typical RF Attack Point	Relative to RFAGC attack point		+28		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2163 Evaluation Kit, V_{CC} = +2.4V to +3.47V, f_{RF} = 557.143MHz, f_{LO} = 557.714MHz, f_{IF} = 571kHz, f_{XTAL} = 36MHz, V_{GC1} = V_{GC2} = 0.3V (maximum gain), default register settings, RF input signals as specified, IF output load as specified, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, $\overline{SHDN}$ = V_{CC}, STBY = GND, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF POWER DETECTOR					
Minimum Attack Point			-66		dBm
Maximum Attack Point			-52		dBm
Detector Accuracy			1.5		dB
3dB Frequency Response	PDBW[1:0]=00		43		MHz
	PDBW[1:0]=01		26		
	PDBW[1:0]=10		17		
	PDBW[1:0]=11		13		
LOW-IF FILTER RESPONSE					
Center Frequency			571		kHz
1-Segment Mode Frequency Response	±219kHz offset from center frequency	-2.8		+2.8	dB
	1MHz offset from center frequency		-80		
LOW-IF OUTPUT CHARACTERISTICS					
Nominal Output-Voltage Swing	R_{LOAD} = 10kΩ||10pF		225		mV_{P-P}
Output Impedance	Single-ended, real		31		Ω
FREQUENCY SYNTHESIZER					
N-Divider Frequency Range		90		804	MHz
N-Divider Range		256		4095	—
Reference Divider Frequency Range		32		36	MHz
Reference Divider Range (R)		112		280	—
Phase Detector Comparison Frequency		1/7		2/7	MHz
PLL Referred Phase Noise Floor	f_{COMP} = 2/7MHz		-153		dBc/Hz
Spurious Products	f_{COMP} spurious		-70		dBc
Charge-Pump Output Current	CP bits = 00	1.0	1.5	2.0	mA
	CP bits = 01	1.4	2.0	2.6	
	CP bits = 10	1.8	2.5	3.3	
	CP bits = 11	2.1	3.0	3.9	
VOLTAGE-CONTROLLED OSCILLATOR AND LO GEN					
Guaranteed VCO Frequency Range		1890		3216	MHz
Guaranteed LO Frequency Range		472.5		804.0	MHz
LO Phase Noise	f_{OFFSET} = 1kHz		-82		dBc/Hz
	f_{OFFSET} = 10kHz		-87		
	f_{OFFSET} = 100kHz		-108		
	f_{OFFSET} = 1MHz		-128		
	f_{OFFSET} > 10MHz		-140		

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2163 Evaluation Kit, V_{CC} = +2.4V to +3.47V, f_{RF} = 557.143MHz, f_{LO} = 557.714MHz, f_{IF} = 571kHz, f_{XTAL} = 36MHz, V_{GC1} = V_{GC2} = 0.3V (maximum gain), default register settings, RF input signals as specified, IF output load as specified, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, $\overline{SHDN}$ = V_{CC}, STBY = GND, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR INPUT (XTAL)					
Frequency Range		32		36	MHz
Input Capacitance	Crystal load capacitance		8		pF
Input Overdrive Level	AC-coupled sine wave input	0.5		1.5	V_{P-P}
Input Negative Resistance	f_{XTAL} = 36MHz		575		Ω
REFERENCE OSCILLATOR BUFFER OUTPUT (XTALOUT)					
Output Frequency Range		16		18	MHz
Output Voltage Swing	Z_L = 4kΩ‖10pF	0.5		1.0	V_{P-P}
Output Buffer Divide Range		2		2	—
Output Duty Cycle		45		55	%
Output Turn-On Time	XTAL amplitude > $0.5V_{P-P}$			4	ms

Note 1: Min and max values are production tested at T_A = +85°C. Min and max limits at T_A = -40°C and +25°C are guaranteed by design and characterization.

Note 2: IFOUT output voltage level met over this range.

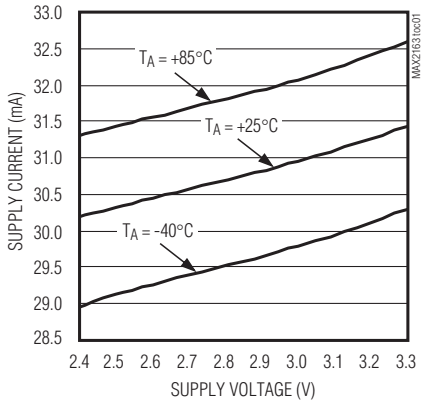
Note 3: In-band IM3 is measured with two tones at f_{LO} - 450kHz and f_{LO} - 550kHz. The RFAGC is engaged and set for the default attack point of -58dBm. IFL[1:0] = 01, RFVGA = MXR = 1. V_{GC2} is adjusted to maintain $225mV_{P-P}$ at IF_{OUT}. Input power levels (tone 1 plus tone 2) up to -10dBm and > 30dBc for levels from -10dBm to 0dBm.

Note 4: V_{GC1} is set for maximum attenuation (2.1V) and V_{GC2} is adjusted to maintain $225mV_{P-P}$ at I_{FOUT} for an equivalent 0dBm input desired level. Closed loop, attack point at -58dBm, f_{RF} = 767.143MHz, f_{LO} = 767.714MHz, f_{RF1} = f_{RF} + 4.25MHz, f_{RF2} = f_{RF} + 8MHz, -10dBm/tone. RFGR = 1, RFVGA = 1, and MXR = 1.

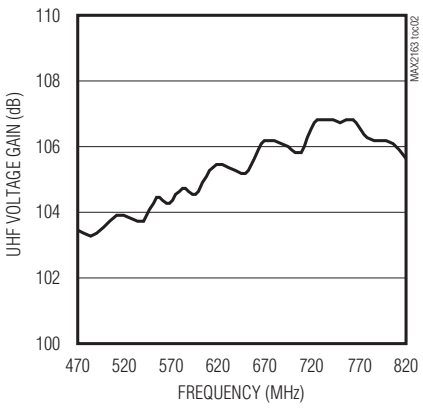
Typical Operating Characteristics

(MAX2163 Evaluation Kit, V_{CC} = +2.5V, default register settings, V_{GC1} = V_{CG2} = 0.3V, V_{IFOUT} = 225mV_{P-P}, f_{LO} = 557.714MHz, T_A = +25°C, unless otherwise noted.)

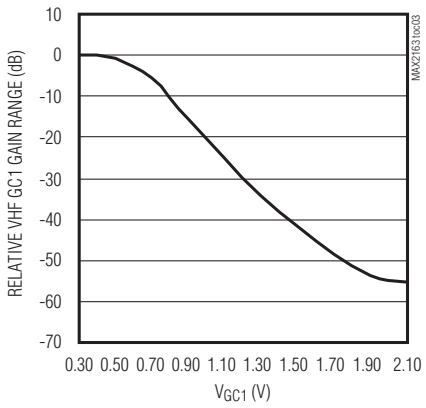
NORMAL MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



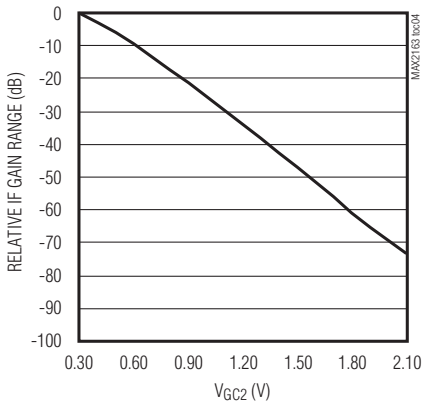
UHF VOLTAGE GAIN vs. FREQUENCY



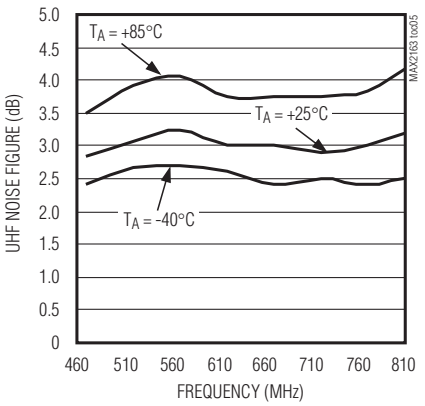
RELATIVE UHF GAIN RANGE vs. V_{GC1}



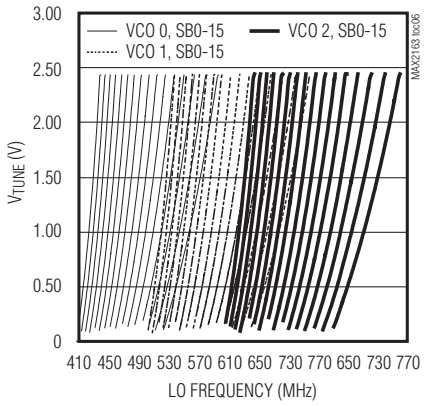
RELATIVE IF GAIN RANGE vs. GC2



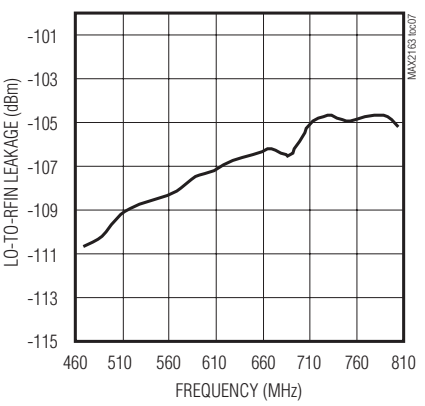
UHF NOISE FIGURE vs. FREQUENCY



UHF V_{TUNE} vs. LO FREQUENCY



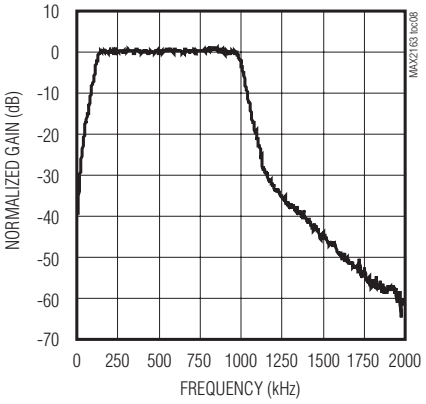
UHF LO-TO-RFIN LEAKAGE vs. FREQUENCY



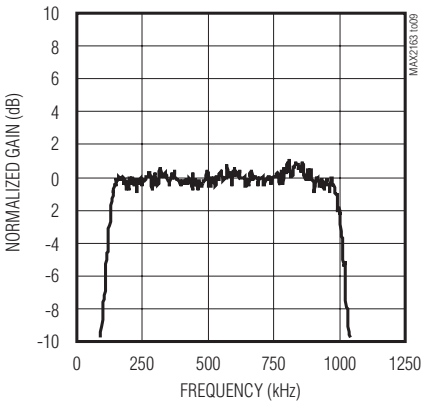
Typical Operating Characteristics (continued)

(MAX2163 Evaluation Kit, V_{CC} = +2.5V, default register settings, V_{GC1} = V_{CG2} = 0.3V, V_{IFOUT} = 225mV_{P-P}, f_{LO} = 557.714MHz, T_A = +25°C, unless otherwise noted.)

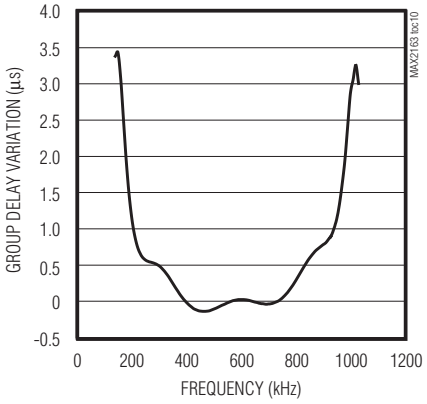
1-SEGMENT BASEBAND FILTER FREQUENCY RESPONSE



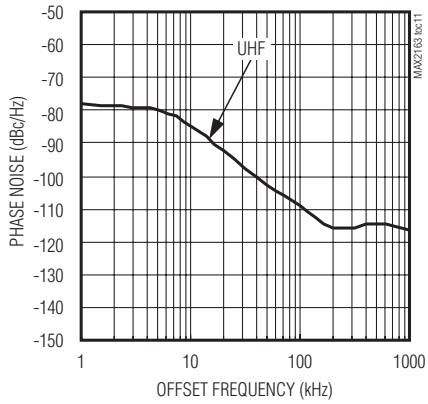
1-SEGMENT BASEBAND FILTER FREQUENCY RESPONSE



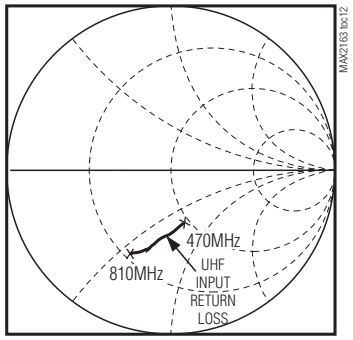
1-SEGMENT GROUP DELAY VARIATION vs. BASEBAND FREQUENCY



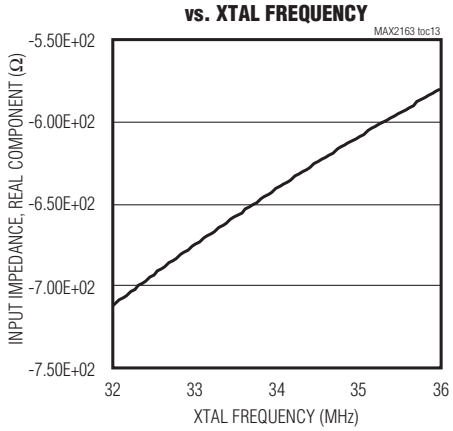
PHASE NOISE vs. OFFSET FREQUENCY



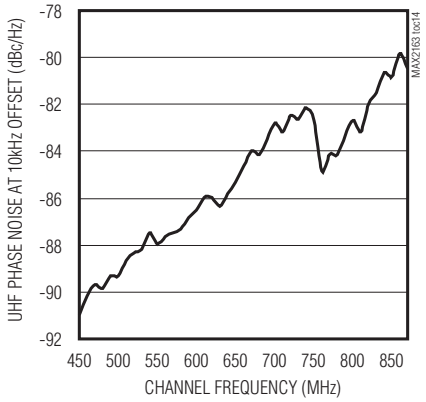
UHF INPUT RETURN LOSS vs. RF FREQUENCY



XTAL PORT INPUT IMPEDANCE vs. XTAL FREQUENCY



UHF LO PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY



Pin Description

PIN	NAME	DESCRIPTION
1	STBY	Device Standby. Connect to logic-high to place the device in standby mode. Connect to logic-low for normal operation. This pin is logically ORed to the STBY bit.
2	$\overline{SHDN}$	Device Shutdown. Connect to logic-low to place the device in shutdown mode.
3	LEXTU	Optional UHF Tracking Filter Inductor. Connect an 18nH inductor from this pin to ground.
4, 8, 9, 10	N.C.	No Connection. Connect to the PCB ground plane.
5	V_{CCLNA}	DC Power Supply for LNA. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
6	V_{CCRF}	DC Power Supply for RF Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
7	UHFIN	UHF 50Ω RF Input. Incorporates an internal DC-blocking capacitor.
11	GC1	RF Gain Control Input. In closed-loop RFAGC mode (PDBM[1:0] = 11), connecting a capacitor from GC1 to ground sets the AGC response time. In open-loop RFAGC mode (PDBM[1:0] = 10), GC1 is a high-impedance analog input that controls the RFAGC.
12	V_{CCIF}	DC Power Supply for IF Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
13	GC2	IF Gain Control Input. High-impedance analog input.
14	V_{CCBIAS}	DC Power Supply for Bias Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
15	IFOUT	Low-IF Output. Requires a DC-blocking capacitor.
16	PWRDET	Low-Impedance Power Detector Output Buffer. Bits PDBM[1:0] control the function of this output pin. See Table 6.
17	SCL	2-Wire Serial-Clock Interface. Requires a pullup resistor to V_{CCDIG}.
18	SDA	2-Wire Serial-Data Interface. Requires a pullup resistor to V_{CCDIG}.

Pin Description (continued)

PIN	NAME	DESCRIPTION
19	V_{CCDIG}	DC Power Supply for Digital Logic Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
20	MUX	Device TEST. See Table 14 for details.
21	XTAL	Base Contact of Internal Colpitts Oscillator. See the *Typical Application Circuit* for details.
22	XTALOUT	Crystal Oscillator Buffer Output. A DC-blocking capacitor must be used when driving external circuitry.
23	V_{CCSYN}	DC Power Supply for Synthesizer Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
24	CPOUT	Charge-Pump Output. Connect this output to the PLL loop filter input with the shortest connection possible.
25	GNDSYN	Synthesizer Ground. Connect to the PCB ground plane. Do not share ground vias with other ground connections.
26	VTUNE	High-Impedance VCO Tune Input. Connect the PLL loop filter output directly to this pin with as short as possible of a connection.
27	LDO	Internal LDO Bypass. Bypass to GND with a 470nF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
28	V_{CCVCO}	DC Power Supply for VCO Circuits. Connect to a +2.5V low-noise supply. Bypass to GND with a 0.1µF capacitor placed as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
—	EP	Exposed Paddle. Solder evenly to the board's ground plane for proper RF performance and enhanced thermal dissipation. Not intended as an electrical connection point.

Detailed Description

Register Descriptions

The MAX2163 includes 16 programmable registers and 2 read-only registers. **Note:** All programmable registers must be written no earlier than 100µs after device power-up or recovery from a brownout event (i.e., when V_{CC} drops below 1V). Follow up by rewriting the registers needed for channel/frequency programming (i.e., registers 00–08) or simply rewrite all registers. The default values listed in Tables 1–15 are provided for informational purposes only. The user must write all required register values, including "factory use only" values.

Table 1. I²C and 4-Wire Register Configuration

REGISTER NUMBER	REGISTER NAME	READ/ WRITE	REGISTER ADDRESS	MSB DATA BYTE							
				D7	D6	D5	D4	D3	D2	D1	D0
00	IF Filter	Read/ Write	0x00	TUN2	TUN1	TUN0	FLTS	IFL1	IFL0	PDBW1	PDBW0
01	VAS	Read/ Write	0x01	1	VASS	VAS	CPS	ADL	ADE	LTC1	LTC0
02	VCO	Read/ Write	0x02	0	VCO1	VCO0	VSB3	VSB2	VSB1	VSB0	VCOB
03	PDET/ RF-FILT	Read/ Write	0x03	PDBM1	PDBM0	PDET2	PDET1	PDET0	RFLT2	RFLT1	RFLT0
04	MODE	Read/ Write	0x04	RFVB	RFFB	HSLS	0	0	0	0	0
05	R-Divider MSB	Read/ Write	0x05	R8	R7	R6	R5	R4	R3	R2	R1
06	R-Divider LSB/CP	Read/ Write	0x06	CP1	CP0	0	DRFD	RFDA1	RFDA0	1	R0
07	N-Divider MSB	Read/ Write	0x07	N11	N10	N9	N8	N7	N6	N5	N4
08	N-Divider LSB/LIN	Read/ Write	0x08	N3	N2	N1	N0	0	MIX	RFVGA	STBY
09	STATUS	Read Only	0X09	X	X	ADC2	ADC1	ADC0	VCP1	VCP0	PWR
0A	VAS STATUS	Read Only	0x0A	VVCO1	VVCO0	VVSB3	VVSB2	VVSB1	VVSB0	VASA	VASE
0B–11	Factory Use Only	Read/ Write	0x0B–0x11	0	0	0	0	0	0	0	0

I²C Read/Write Addresses

The MAX2163 I²C read/write addresses are C1/C0. See Table 2 for details.

Table 2. MAX2163 I²C Write Addresses

DEVICE ADDRESS	ADDRESS TYPE	D7	D6	D5	D4	D3	D2	D1	D0
C0	WRITE	1	1	0	0	0	0	0	0
C1	READ	1	1	0	0	0	0	0	1

Table 3. IF Filter Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
TUN[2:0]	7, 6, 5	011	Sets the IF filter center frequency. This filter's center frequency is trimmed at the factory, but can be manually adjusted by setting the FLTS bit and programming the TUN[2:0] bits as follows: 000 - 0.75 x f_{IF} (Not factory tested.) 001 - 0.84 x f_{IF} (Not factory tested.) 010 - 0.92 x f_{IF} (Not factory tested.) 011 - f_{IF} (571kHz) 100 - 1.08 x f_{IF} (Not factory tested.) 101 - 1.16 x f_{IF} (Not factory tested.) 110 - 1.25 x f_{IF} (Not factory tested.) 111 - 1.33 x f_{IF} (Not factory tested.)
FLTS	4	0	Selects which registers set low-IF bandpass filter center frequency and bandwidth. 0 = Selects internal factory set register. 1 = Selects manual trim register TUN[2:0] (Not factory tested).
IFL[1:0]	3, 2	01	Set the bias current for the low-IF circuits to provide for fine linearity adjustments. Program to 01 upon power-up.
PDBW[1:0]	1, 0	11	Sets the IF power detector bandwidth. 00 = 43MHz bandwidth. 01 = 26MHz bandwidth. 10 = 17MHz bandwidth. 11 = 13MHz bandwidth.

Table 4. VAS Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7	1	Factory use only. Must be programmed to 1 upon power-up.
VASS	6	0	Controls the VCO autoselect (VAS) start conditions function. 0 = VAS starts from the current VCO/VCOSB loaded in the VCO[1:0] and VSB[3:0] registers. 1 = VAS starts from the currently used VCO and VCOSB.
VAS	5	1	Controls the VCO autoselect (VAS) function. 0 = Disables the VCO autoselect function and allows manual VCO selection through the VCO[1:0] and VSB[3:0] bits. 1 = Enables the on-chip VCO autoselect state machine.
CPS	4	1	Sets the charge-pump current selection mode between automatic and manual. 0 = Charge-pump current is set manually through the CP[1:0] bits. 1 = Charge-pump current is automatically selected. Also requires ADE, ADL, and VAS bits to be programmed to 1.
ADL	3	0	Enables or disables the VCO tuning voltage ADC latch. 0 = Disables the ADC latch. 1 = Latches the ADC value.
ADE	2	0	Enables or disables VCO tuning voltage ADC. 0 = Disables ADC read. 1 = Enables ADC read.
LTC[1:0]	1, 0	11	Sets the VCO autoselect wait time. 00 = 14336/f_{XTAL}. 01 = 24576/f_{XTAL}. 10 = 34816/f_{XTAL}. 11 = 45056/f_{XTAL}.

Table 5. VCO Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7	0	Factory use only. Must be programmed to 0 upon power-up.
VCO[1:0]	6, 5	01	Controls which VCO band is activated when using manual VCO programming mode. This also serves as the starting point for VCO autoselect mode when VASS = 0. 00 = Select VCO-0. 01 = Select VCO-1. 10 = Select VCO-2. 11 = Not used.

Table 5. VCO Register (continued)

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
VSB[3:0]	4, 3, 2, 1	0100	Select a particular sub-band for each of the on-chip VCOs. Together with the VCO[1:0] bits a manual selection of a VCO band and a sub-band can be made. This also serves as the starting point for the VCO autoselect mode when VASS = 0. 0000 = Select sub-band 0. 0001 = Select sub-band 1. … 1111 = Select sub-band 15.
VCOB	0	1	Sets the VCO bias mode. 0 = Normal mode. 1 = Low-power mode.

Table 6. PDET/RF-FILT Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
PDBM[1:0]	7, 6	00	Power detector and buffer mode. 00 = Power detector is enabled, PWRDET buffer is off. On-chip closed-loop RFAGC. 01 = Power detector is enabled, PWRDET buffer is on with detector RMS voltage output at PWRDET pin (RFAGC is open loop with RF gain controlled by voltage applied to GC1). 10 = Unused. 11 = Power detector is enabled; PWRDET buffer is on with the GC1 voltage output at PWRDET pin (on-chip closed loop RFAGC).
PDET[2:0]	5, 4, 3	100	Sets the AGC attack point. 000 = -66dBm. 001 = -64dBm. 010 = -62dBm. 011 = -60dBm. 100 = -58dBm. 101 = -56dBm. 110 = -54dBm. 111 = -52dBm.
RFLT[2:0]	2, 1, 0	011	Sets the center frequency of the UHF tracking filter when used. 000 = Minimum frequency (see Table 17). ---------- 111 = Maximum frequency (see Table 17).

Table 7. MODE Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
RFVB	7	0	Bypass 3rd-stage RFVGA. 0 = Enables 3rd-stage RFVGA. 1 = Disables the 3rd-stage RFVGA.
RFFB	6	0	Bypass integrated RF filter. 0 = Enables optional RF filter. 1 = Disables optional RF filter.
HSLS	5	0	Selects between high-side and low-side LO injection. 1 = Low-side injection. 0 = High-side injection.
X	4, 3, 2, 1, 0	0	Factory use only. Must be programmed to 0 upon power-up.

Table 8. R-Divider MSB Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
R[8:1]	7, 6, 5, 4, 3, 2, 1, 0	00111111	Sets the PLL reference divider (R) number. Default R divide value is 126 decimal. R can range from 16 to 511 decimal.

Note: *When changing R-divider value, both registers R-Divider MSB and R-Divider LSB must be loaded as they are double buffered.*

Table 9. R-Divider LSB/CP Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
CP[1:0]	7, 6	00	Sets the charge-pump current. 00 = 1.5mA. 01 = 2mA. 10 = 2.5mA. 11 = 3mA.
X	5	0	Factory use only. Must be programmed to 0 upon power-up.
DRFD	4	1	Disable RF Detector 0 = Enables the wideband RF overload detector. 1 = Disables the wideband RF overload detector.
RFDA[1:0]	3, 2	11	Sets the RF overload detector attack point (subtract 6dB to each if PDIQ = 0). 00 = +37dB relative to IF attack point setting. 01 = +34dB relative to IF attack point setting. 10 = +31dB relative to IF attack point setting. 11* = +28dB relative to IF attack point setting. **Only 11 is factory tested.*
X	1	1	Factory use only. Must be programmed to 1 upon power-up.
R0	0	0	LSB of reference divider number

Note: *When changing R-divider value, both registers R-Divider MSB and R-Divider LSB must be loaded as they are double buffered.*

Table 10. N-Divider MSB Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
N[11:4]	7, 6, 5, 4, 3, 2, 1, 0	01111010	Sets the most significant bits of the PLL integer divide number (N). Default integer divider value is N = 1952 decimal. N can range from 1314 to 2687.

Note: *When changing N-divider value, both registers N-Divider MSB and N-Divider LSB must be loaded as they are double buffered.*

Table 11. N-Divider LSB/LIN Register

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
N[3:0]	7, 6, 5, 4	0000	Sets the least significant bits of the PLL integer divide number (N). Default integer divider value is N = 1952 decimal. N can range from 1314 to 2687.
X	3	0	Factory use only. Must be programmed to 0 upon power-up.
MIX	2	0	Sets linearity mode of mixers. 0 = Selects normal mode for mixer. 1 = Selects high linearity mode for mixer.
RFVGA	1	0	Sets linearity mode of 3rd-stage RFVGA. 0 = Selects normal mode for 3rd-stage RFVGA. 1 = Selects high linearity mode for 3rd-stage RFVGA.
STBY	0	0	Selects standby mode when STBY pin is logic-low. 0 = Normal operation. 1 = Disables the signal path and frequency synthesizer leaving only the serial bus, crystal oscillator, and XTALOUT buffer active.

Note: *When changing N-divider value, both registers N-Divider MSB and N-Divider LSB must be loaded as they are double buffered.*

Table 12. STATUS Register (Read Only)

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7, 6	1,1	Unused
ADC[2:0]	5, 4, 3	—	Indicates the 3-bit ADC conversion of the VCO tuning voltage (VTUNE).
VCP[1:0]	2, 1	—	Reflects the charge-pump current setting, when CPS = 1.
PWR	0	1	Logic-high indicates power has been cycled. STATUS register read operation resets PWR to 0.

Table 13. VAS STATUS Register (Read Only)

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
VVCO[1:0]	7, 6	—	Indicates which VCO has been selected by the VCO autoselect state machine. See Table 5 for VCO[1:0] definition.
VVSB[3:0]	5, 4, 3, 2	—	Indicates which sub-band of a particular VCO has been selected by either the VCO autoselect state machine. See Table 5 for VSB[2:0] definition.
VASA	1	—	Indicates whether VCO autoselection was successful. 0 = Indicates the autoselect function is disabled or unsuccessful VCO selection. 1 = Indicates successful VCO autoselection.
VASE	0	—	Status indicator for the VCO autoselect function. 0 = Indicates the VCO autoselect function is active. 1 = Indicates the VCO autoselect function is inactive.

Table 14. Factory Use Only Registers (0B, 0C, 0D, 0E, 0F, 10 and 11)

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7, 6, 5, 4, 3, 2, 1, 0	00000000	Factory use only. Must be programmed to 0 upon power-up.

Pin and Bit Truth Tables

The MAX2163 STBY can be controlled by either a hardware pin or a register bit. The truth table for each is described in Table 15.

For software control of the STBY mode, connect the STBY pin to ground.

Normal and High-Linearity Mode Definitions

Table 16 defines the register setup for normal and high-linearity modes.

2-Wire Serial Interface

The MAX2163 features a 2-wire I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX2163 and the master at clock frequencies up to 400kHz. The master device initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX2163 functions as an I²C slave device that transfers and receives data to and from the master. Pull SDA and SCL high with external pullup resistors of 1kΩ or greater referenced to MAX2163 V_{CCDIG} for proper I²C operation.

One bit transfers during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte into or out of the MAX2163 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Table 15. Standby Bit Truth Table

STBY PIN	STBY BIT	DEVICE STATE
VCC	0	Device in standby mode
VCC	1	Device in standby mode
GND	0	Device in normal mode
GND	1	Device in standby mode

Table 16. Register Setup for Normal and High-Linearity Modes

BIT	NORMAL MODE	HIGH LINEARITY MODE
RFVGA	0	1
MIX	0	1

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX2163 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX2163 has a 7-bit I²C slave address that must be sent to the device following a START condition to initiate communication. The slave address is internally programmed to C0 or C2 for WRITE and C1 or C3 for READ. See Table 2.

The MAX2163 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 1).

Write Cycle

When addressed with a write command, the MAX2163 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the 7 slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX2163 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to write to (see Table 1 for register addresses). The slave acknowledges the address, and the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit (MSB). The MAX2163 again issues an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the MAX2163 acknowledging each successful transfer, or the master can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Figure 2 illustrates an example in which registers 0 through 2 are written with 0x0E, 0x08, and 0xE1, respectively.

Read Cycle

When addressed with a read command, the MAX2163 allows the master to read back a single register or multiple successive registers.

A read cycle begins with the bus master issuing a START condition followed by the 7 slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX2163 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read (see Table 1 for register addresses). The slave acknowledges the address. Then a START condition is issued by the master, followed by the 7 slave address bits and a read bit (R/$\overline{W}$ = 1). The MAX2163 issues an ACK if the slave address byte is successfully received. The MAX2163 starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK and continue to read successive registers, or the master can terminate the transmission by issuing a NACK. The read cycle does not terminate until the master issues a STOP condition.

Figure 3 illustrates an example in which registers 0 through 2 are read back.

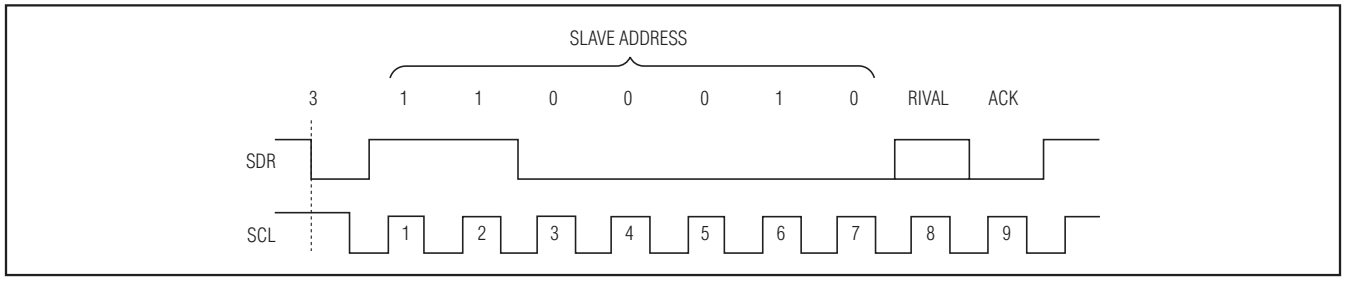


Figure 1. MAX2163 Slave Address Byte

START	WRITE 0B/CE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	1100000	0	—	0x00	—	0x0E	—	0x0E	—	0xE1	—	

Figure 2. Write Register 0 through 2 with 0x0E, 0x08, and 0xE1, respectively.

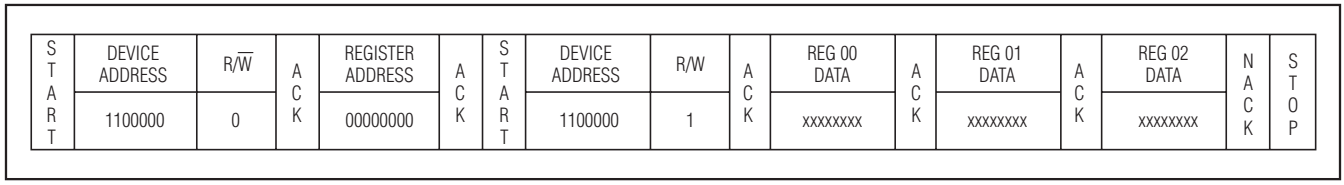


Figure 3. Receive Data from Read Registers

Applications Information

RF Input (UHFIN)

The MAX2163 UHFIN input is internally matched to 50Ω.

RF Gain Control (GC1)

The MAX2163 features multistage RF variable gain amplifiers controlled by pin GC1 that provide in excess of 54dB typical of RF gain control range. The voltage control range is 0.3V at maximum gain to 2.1V at minimum gain. The RF gain control can be configured for open-loop control or for closed-loop RF automatic gain control (AGC) when combined with the on-chip IF power detector. To set the response time of the AGC, connect a capacitor from GC1 to ground. See the *Closed-Loop RF Gain Control* section for more information.

Optional RF Tracking Filter

The MAX2163 features an optional RF tracking filter at the output of the 3rd-stage RFVGA. This filter is controlled by the RFLT bits as shown in the MODE register. See Table 7. To enable the filter, set RFFB bit to 0; to disable filter, set RFFB bit to 1. See Table 17 for proper center frequency settings. In the event that the RF tracking filter is not used, do not install the 18nH inductor.

Table 17. RFLT[2:0] Center Frequency Settings

RFLT	UHF (MHz)
000	470–488
001	488–512
010	512–542
011	542–572
100	572–608
101	608–656
110	656–710
111	710–806

RF Overload Detector

The MAX2163 includes an RF overload detector. The RF overload detector circuit is enabled or disabled with the DRFD bit as shown in Table 10 (R-Divider LSB/CP register).

IF Gain Control (GC2)

The MAX2163 features an IF variable gain amplifier that provides in excess of 65dB of IF gain control range. The voltage control VGC2 range is 0.3V at maximum gain to 2.1V at minimum gain. The IF VGA is controlled by the channel decoder.

IF Power Detector

The MAX2163 features a true RMS IF power detector at the mixer output with adjustable bandwidth. The power detector circuit is enabled or disabled with the PDBM[1:0] bits in the PDET/RF-FILT register (Table 6). The attack point can be set through the PDET[2:0] bits in the PDET/RF-FILT register (see Table 6 for a summary of attack-point settings).

The PWRDET pin can be configured to provide a low-impedance buffered and scaled version of either the GC1 voltage when using the on-chip closed loop AGC, or the IF power detectors RMS voltage for use in off-chip closed loop AGC schemes. The output voltage at this pin ranges from 0.3V to 2.1V, with 2.1V indicating the maximum RF input power. This output allows the baseband processor to monitor the received RF power level.

When using the on-chip closed-loop AGC function (PDBM = 11), the PWRDET buffer provides a low-impedance buffered version of the GC1 voltage. This output can be monitored by the demodulator LSI to determine the state of the RF front-end and subsequently used to control other circuits (external LNA) or various demodulator functions. The PWRDET output can also be disabled for reduced overall power consumption (PDBM = 00).

For use in off-chip closed-loop AGC schemes, the PWRDET buffer output can be configured to provide a low-impedance scaled version of the IF power detectors RMS voltage (PDBM = 10). In this mode, an external voltage is applied to the GC1 pin to close the loop.

Closed-Loop RF Gain Control

The MAX2163 can provide either open-loop RF gain control by the GC1 pin or closed-loop RF automatic gain control (AGC) by the on-chip power detector. Automatic RF gain control is enabled by setting the PDBM[1:0] bits to 00 as shown in the PDET/RF-FILT register (Table 6). Setting the PDBM[1:0] bits to 10 allows open-loop RF gain control by the GC1 pin.

When the RF AGC loop is disabled, RF gain is controlled by an external voltage that is applied to the GC1 pin. The GC1 pin's input voltage range is 0.3V to 2.1V with 0.3V providing the maximum RF gain.

When the RF AGC loop is enabled, the IF power detector output is internally connected to the GC1 input and the RF gain is controlled by the power detector's output voltage. An external capacitor connected from the GC1 pin to ground sets the AGC loop response time. The loop response time is calculated as follows:

$$t_{SETTLING} = 41.7 \times R \times C_{EXT}$$

where:

R = 1kΩ

C_{EXT} = External capacitor from GC1 to ground in farads.

The attack point (referred to as the RF input) of the AGC loop can be programmed from -66dBm to -52dBm and is controlled by the PDET[2:0] bits in the PDET/RF-FILT register (Table 6).

High-Side and Low-Side LO Injection

The MAX2163 allows selection between high-side and low-side LO injection through the HSLS bit in the MODE register (Table 7). To select low-side injection, set HSLS to 1; to select high-side injection, set HSLS to 0.

IF Filter

The nominal IF filter center frequency and bandwidth are 571kHz and 860kHz, respectively.

The center frequency of the IF bandpass filter is tuned at the factory; however, the factory-set trim can be bypassed and the center frequency can be adjusted through the FLTS and TUN[2:0] bits in the IF Filter register (Table 3). Set the FLTS bit to 0 to select the filter's center frequency to the factory-set tuning. Set the FLTS bit to 1 to allow the filter's center frequency to be adjusted with the TUN[2:0] bits (Table 3).

VCO Autoselect (VAS)

The MAX2163 includes three VCOs with each VCO having 16 sub-bands. The appropriate VCO and VCO sub-band for the desired local oscillator frequency can be manually selected by programming the VCO[1:0] and VSB[3:0] bits in the VCO register. The selected VCO and sub-band is reported in the VAS STATUS register (read only) (Table 13).

Alternatively, the MAX2163 can be set to autonomously choose a VCO and VCO sub-band. Automatic VCO selection is enabled by setting the VAS bit in the VAS register (Table 4) and is initiated once the N-divider LSB register word is loaded. **In the event that the R-divider is changed, both the R-Divider MSB and R-Divider LSB registers must be reprogrammed. Also, if the R-Divider or the N-Divider MSB is changed, the N-Divider LSB register must also be reprogrammed to initiate the VCO autoselect function.** The VCO and VCO sub-band that are programmed in the VCO[1:0] and VSB[3:0] bits serve as the starting point for the automatic VCO selection process when VASS = 0. When VASS = 1, the current VCO and VCO sub-bands serve as the starting point for the automatic VCO selection process.

During the selection process, the VASE bit in the VAS STATUS register is cleared to indicate the autoselection function is active. Upon successful completion, bits VASE and VASA are set and the VCO and sub-band selected are reported in the VAS STATUS register (Table 13). If the search is unsuccessful, VASA is cleared and VASE is set. This indicates that searching has ended, but no VCO has been found, and occurs when trying to tune to a frequency outside the VCO's specified frequency range.

Charge-Pump Select (CPS)

The MAX2163 allows for manual selection of the charge-pump current (CPS = 0) or automatic selection (CPS = 1). When in manual mode, the charge-pump current is programmed by bits CP[1:0] in the R-Divider LSB register (Table 9). In automatic selection mode, the charge-pump current is automatically set based on VTUNE voltage and current VCO sub-band. ADE, ADL, and VAS bits must be programmed to 1. The selected charge-pump current is reported in Table 18 .

Table 18. Charge-Pump Current Setting When CPS = 1

VSB[3]	ADC[2]	CP (mA)
0	0	2
0	1	3
1	0	1.5
1	1	2.5

3-Bit Analog-to-Digital Converter

The MAX2163 includes a 3-bit ADC. Its input is connected to the VCO tune pin (VTUNE). This ADC can be used for checking the lock status of the VCOs.

Table 19 summarizes the phase-locked loop (PLL) lock status based on ADC[2:0] values. The VCO autoselect routine only selects a VCO in the VAS locked range. This allows room for a VCO to drift over temperature and remain in a valid locked range.

When VCO autoselect is disabled, the ADC must first be enabled by setting the ADE bit in the VAS register. The ADC reading is latched by a subsequent programming of the ADC latch bit (ADL = 1). The ADC value is reported in the STATUS register (Table 12).

Loop-Time Constant Selection

The loop-time constant (LTC) function sets the wait time for an ADC read when in VCO autoselect mode. This wait time determines how long the VCO autoselect circuit waits for the PLL to settle before determining if VCO selection was successful. The loop time constant is selectable by the LTC[1:0] bits in the VAS register (Table 4).

XTALOUT Buffer

The reference buffer/divider is provided for driving external devices. The internal frequency divider is fixed at 2, and the buffer can provide a minimum $500mV_{P-P}$ signal swing into a load of 4kΩ||10pF with a guaranteed duty cycle of 45% to 55%. Upon power-up or coming out of shutdown, the XTALOUT buffer is held in shutdown for an additional 3ms (typ) by an internal timer circuit. This allows the crystal oscillator sufficient time to start up properly, without unwanted parasitic feedback from the output buffer.

Table 19. PLL and Lock Status

ADC[2:0]	PLL LOCK STATUS
000	Out of lock
001	Locked
010	Locked
011	Not used
100	Not used
101	Locked
110	Locked
111	Unlocked

Layout Considerations

The MAX2163 Evaluation Kit serves as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each $V_{CC_}$ pin to ground with a 0.1µF capacitor placed as close as possible to the pin.

When using the optional UHF tracking filter, keep the external inductor as close to the IC as possible and allow it to connect back to the top side ground as close as possible to the IC.

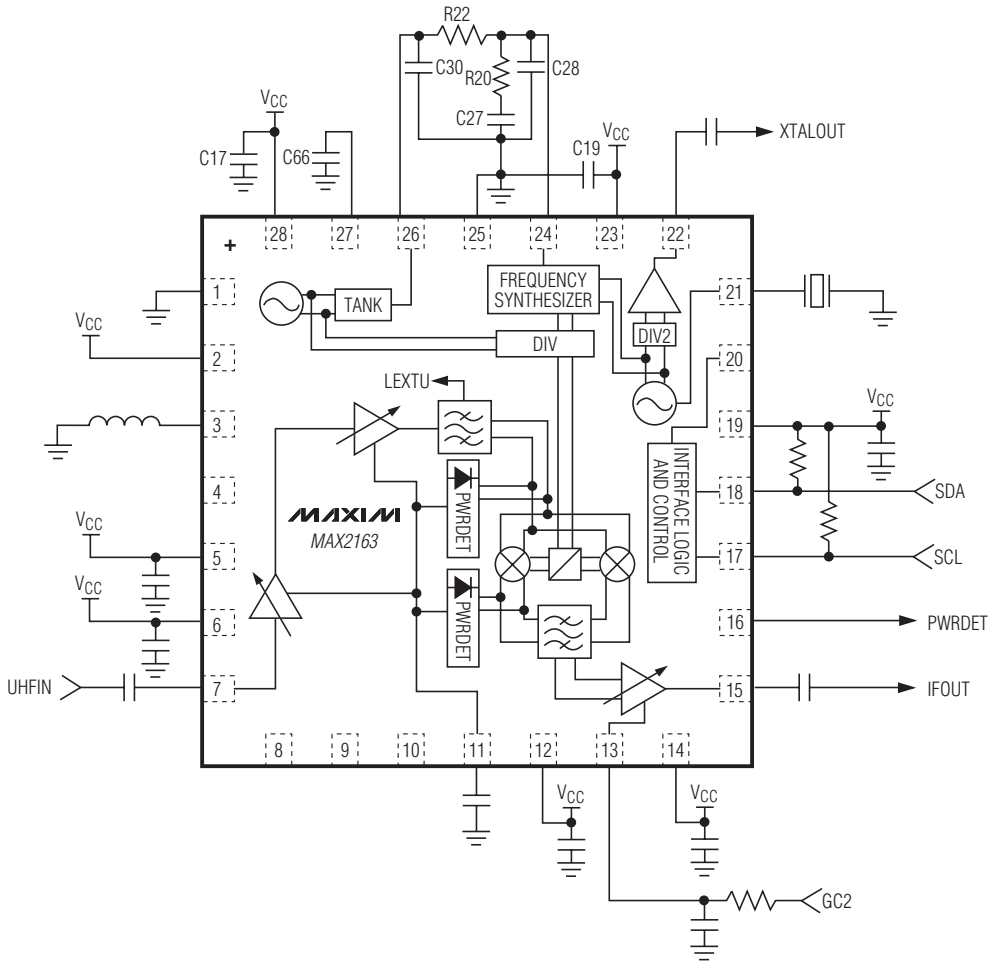
To ensure proper crystal oscillator startup, place the crystal near the MAX2163 XTAL pin (pin 21). The crystal ground should have a clear, short return back to the MAX2163 ground paddle near XTAL. Minimize the parasitic capacitance between the board traces of XTAL (pin 21) and XTALOUT (pin 22). Refer to the MAX2163 Evaluation Kit data sheet for a recommended board layout.

In addition, the ground returns for the VCO, VTUNE, and charge pump require special layout consideration (see the *Typical Application Circuit*). The LDO capacitor (C66) and VCCVCO bypass capacitor (C17) grounds should be routed back to the MAX2163 ground paddle near pin 28. The loop filter ground connections of C27, C28, and C30 should be connected together before tapping down to the overall ground plane with a clear path back to pin 25 (GNDSYN).

When using the TQFN packaged device, the exposed paddle must be soldered evenly to the board's ground plane for proper operation. Use abundant vias beneath the exposed paddle for maximum heat dissipation.

ISDB-T 1-Segment Tuner

Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855-8	**21-0140**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	4/09	Updated to add 28-pin MAX2163ETI to data sheet	All
2	10/09	Added note instructing to program all registers; corrected register tables and listed all factory use only registers	10, 12, 14, 15, 16

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2009 Maxim Integrated Products Maxim is a registered trademark of Maxim Integrated Products, Inc.