maxim integrated™

MAX270/MAX271

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

General Description

The MAX270/MAX271 are digitally-programmed, dual second-order continuous-time lowpass filters. Their typical dynamic range of 96dB surpasses most switched capacitor filters which require additional filtering to remove clock noise. The MAX270/MAX271 are ideal for anti-aliasing and DAC smoothing applications and can be cascaded for higher-order responses.

The two filter sections are independently programmable by either microprocessor (µP) control or pin strapping. Cutoff frequencies in the 1kHz to 25kHz range can be selected.

The MAX270 has an on-board, uncommitted op amp, while the MAX271 has an internal track-and-hold (T/H).

Applications

Lowpass Filtering

Anti-Aliasing Filter

Output Smoothing

Low-Noise Applications

Anti-Aliasing and Track-and-Hold (MAX271)

Features

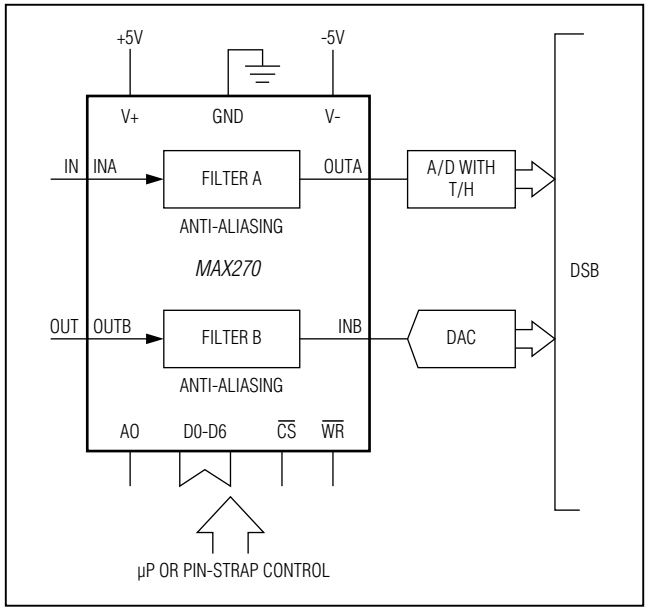
- **Continuous-Time Filtering - No Clock Required**
- **Dual 2nd-Order Lowpass Filters**
- **Sections Independently Programmable: 1kHz to 25kHz**
- **96dB Dynamic Range**
- **No External Components**
- **Cascadable for Higher Order**
- **Low-Power Shutdown Mode**
- **Track-and-Hold (MAX271)**

Ordering Information

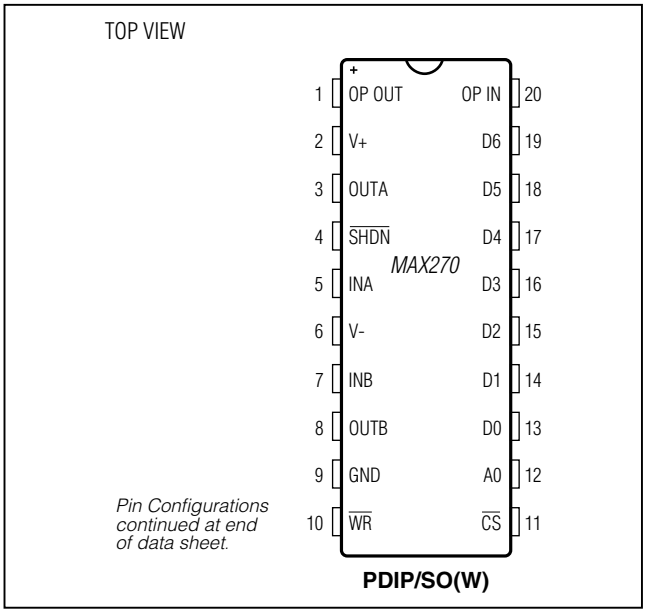
PART	TEMP RANGE	PIN-PACKAGE
MAX270CPP	0°C to +70°C	20 PDIP
MAX270CWP	0°C to +70°C	20 Wide SO
MAX270EPP	-40°C to +85°C	20 PDIP
MAX270EWP	-40°C to +85°C	20 Wide SO
MAX271CNG	0°C to +70°C	20 PDIP
MAX271CWG	0°C to +70°C	20 Wide SO
MAX271ENG	-40°C to +85°C	20 PDIP
MAX271EWG	-40°C to +85°C	20 Wide SO

Devices are available in a lead(Pb)-free/RoHS-compliant package. Specify lead-free by adding a plus (+) to the part number when ordering.

Typical Operating Circuit



Pin Configurations



Pin Configurations continued at end of data sheet.

PDIP/SO(W)

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-3701; Rev 2; 1/12

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

ABSOLUTE MAXIMUM RATINGS

V+ to V- .....-0.3V to +17V
V+ to GND.....-0.3V to +8.5V
V- to GND.....-0.3V to -8.5V
Input Voltage to GND, Any Input Pin ....(V- - 0.3V) to (V+ + 0.3V)
Duration of Output Short Circuit to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
MAX270
PDIP (derate 11.1mW/°C above +70°C) 889mW
SO (W) (derate 10mW/°C above +70°C.....800mW
MAX271
PDIP (derate 13.3mW/°C above +70°C) 1067mW
SO (W) (derate 11.7mW/°C above +70°C)..... 941mw
Operating Temperature Ranges:
MAX27_C_ _..... 0°C to +70°C
MAX27_E_ _.....-40°C to +85°C
Storage Temperature Range.....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing lead(Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Operating Frequency Range		(Note 1)			2		MHz
Programmed Cutoff Frequency (f_C) Range					1 to 25		kHz
Programmed Cutoff Frequency Error		f_C code = 53 (2.536kHz typ)			±2.9		%
		f_C code = 127 (25kHz typ)			±9.5		
Filter Gain		f_C code = 0 (1kHz typ), T_A = T_{MIN} to T_{MAX}	f_{IN} = 1kHz	-3.6		-2.4	dB
			f_{IN} = 8kHz			-33	
		f_C code = 127 (25kHz typ), T_A = T_{MIN} to T_{MAX}	f_{IN} = 25kHz	-6		-0.5	
			f_{IN} = 200kHz		-34		
Maximum Gain (Peaking)		f_C code = 0 (1kHz typ)				0.15	dB
		f_C code = 127 (25kHz typ)			0.15		
Wideband Noise		50Hz to 50kHz bandwidth	f_C code = 0 (1kHz typ)		12		μV_{RMS}
			f_C code = 127 (25kHz typ)		38		
DC CHARACTERISTICS							
DC Output Signal Swing OUTA, OUTB, OP OUT (MAX270) OUTA, OUTB, T/H OUT (MAX271)		R_{LOAD} = 5kΩ, T_A = T_{MIN} to T_{MAX}		-3		+3	V
Offset Voltage at Outputs OUTA, OUTB, OP OUT (MAX270) OUTA, OUTB, T/H OUT (MAX271)				-2		+2	mV
DC Input Leakage Current INA, INB (MAX270) INA, INB (MAX271)		T_A = T_{MIN} to T_{MAX}		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC FILTER CHARACTERISTICS (MAX270)						
Total Harmonic Distortion	THD	f_C code = 44 (2.01kHz typ), V_{IN} = 3.5V_{P-P} at 390.625Hz (Notes 2 and 3)			-70	dB
Signal Noise Plus Distortion	SINAD			73		
Spurious-Free Dynamic Range	SFDR		70			
UNCOMMITTED AMPLIFIER (MAX270)						
Slew Rate				1.2		V/µs
Bandwidth				2		MHz
TRACK AND HOLD (MAX271)						
Hold Settling Time		To 0.1% (Note 4)		500		ns
Acquisition Time		To 0.1% (Note 5)		1.8		µs
Hold Step				1		mV
Droop Rate		T_A = T_{MIN} to T_{MAX}		30		µV/µs
Offset Voltage at T/H OUT		Includes filter offset	-6		+6	mV
T/H OUT Disabled Output Leakage Current		T_A = T_{MIN} to T_{MAX}, $V_{T/H}$ = 0V (Track Mode)	-10		+10	µA
Total Harmonic Distortion	THD	f_C code = 44 (2.01kHz typ), V_{IN} = 3.5V_{P-P} at 390.625Hz, sampling rate = 50kHz (Notes 2, 6, 7)			-70	dB
Spurious-Free Dynamic Range	SFDR		70			
DIGITAL INPUTS						
Digital Input High Voltage		T_A = T_{MIN} to T_{MAX} (Note 8)	2.4			V
Digital Input Low Voltage					0.8	
Digital Input Current		T_A = T_{MIN} to T_{MAX}, digital input held at ±5V, includes MODE (MAX271)(Note 8)	-1		+1	µA
POWER REQUIREMENTS						
Supply Voltage Range				±2.375 to ±8		V
Supply Current		T_A = T_{MIN} to T_{MAX} (Note 9)			6.5	mA
Shutdown Supply Current		T_A = T_{MIN} to T_{MAX} (Note 10)			15	µA
Power-Supply Rejection Ratio at 1kHz	PSRR	f_C code = 0 (1kHz typ), V+ = 5V_{DC} + 10mV_{P-P} at 1kHz		30		dB

Note 1: All internal amplifiers limited to 2MHz bandwidth.
Note 2: Only filter A tested for these parameters.
Note 3: Spurious-Free Dynamic Range is the ratio of the fundamental to the largest of any harmonic or noise spur in dB.
Note 4: Includes T/H propagation delays. With 5kΩ, parallel 100pF load.
Note 5: ±2V input step settling 0.1% with 5kΩ parallel 100pF load.
Note 6: $\overline{T}$/H pin toggled at sampling rate, 50% duty cycle.
Note 7: THD and SFDR specifications for T/H include contributions from filter.
Note 8: Digital pins include $\overline{SHDN}$, $\overline{WR}$, $\overline{CS}$, A0, D0–D6 (MAX270) and $\overline{SHDN}$, T/H, A/$\overline{B}$, $\overline{WR}$, T/H EN, $\overline{CS}$, A0, A1, D0–D6, $\overline{T}$/H (MAX271).
Note 9: Input of uncommitted op amp disconnected with a 5kΩ feedback resistor from input to output.
Note 10: $\overline{WR}$, $\overline{CS}$, A0, D0–D6 held at +5V; $V_{\overline{SHDN}}$ = 0V (MAX270). $\overline{WR}$, $\overline{CS}$, A0, A1, D0–D6, $\overline{T}$/H, T/H, A/B, T/H, MODE held at +5V; $V_{\overline{SHDN}}$ = 0V (MAX271).

TIMING CHARACTERISTICS (Figure 2)

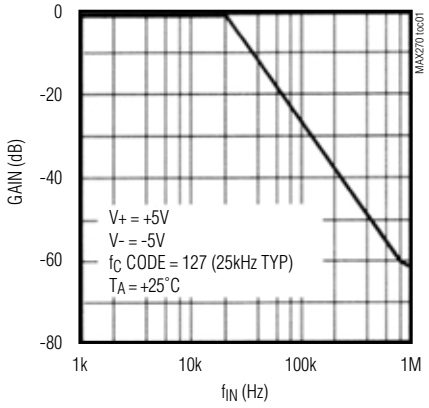
(V+ = +5V, V- = -5V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup	t_{WS}				0	ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{WH}				0	ns
$\overline{WR}$ Pulse Width	t_{SV}		100			ns
Address-Setup Time	t_{AS}		30			ns
Address-Hold Time	t_{AH}		10			ns
Data-Setup Time	t_{DS}		30			ns
Data-Hold time	t_{DH}		10			ns

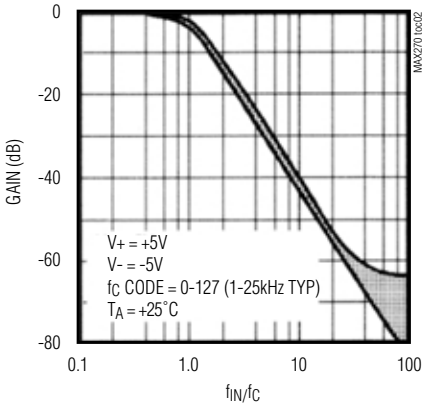
Note 11: All input control signals specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a +1.6V voltage level.

Typical Operating Characteristics

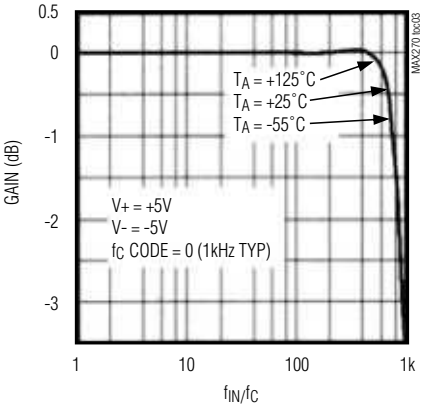
FILTER GAIN vs. FREQUENCY



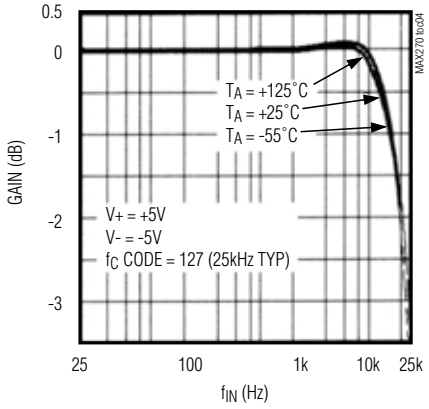
FILTER GAIN vs. FREQUENCY (NORMALIZED TO CUTOFF FREQUENCY)



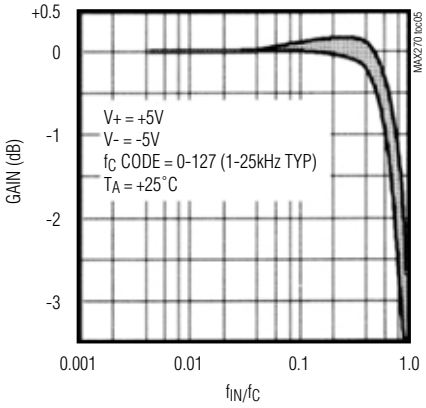
PASSBAND FILTER GAIN vs. FREQUENCY



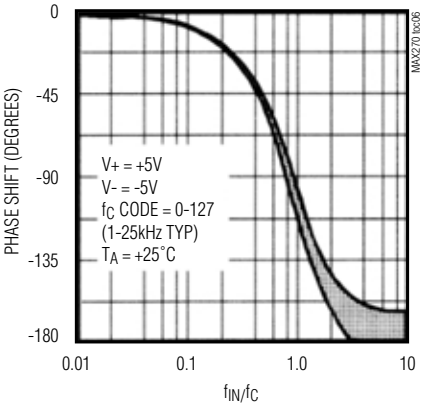
PASSBAND FILTER GAIN vs. FREQUENCY



PASSBAND FILTER GAIN vs. FREQUENCY (NORMALIZED TO CUTOFF FREQUENCY)



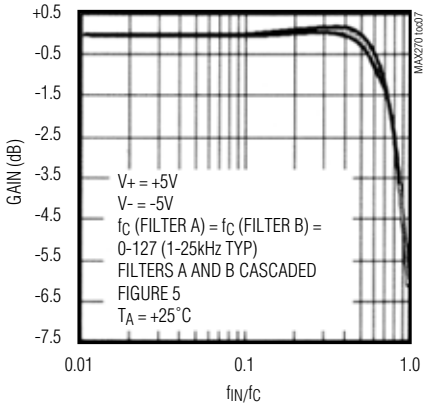
FILTER PHASE SHIFT vs. FREQUENCY (NORMALIZED TO CUTOFF FREQUENCY)



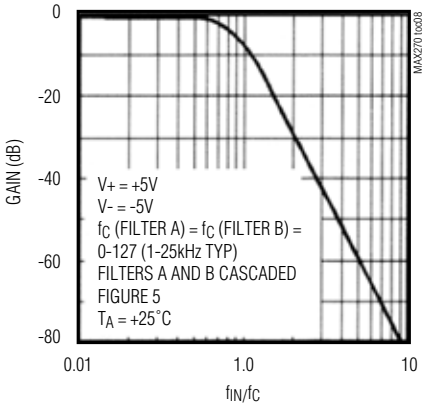
Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

Typical Operating Characteristics (continued)

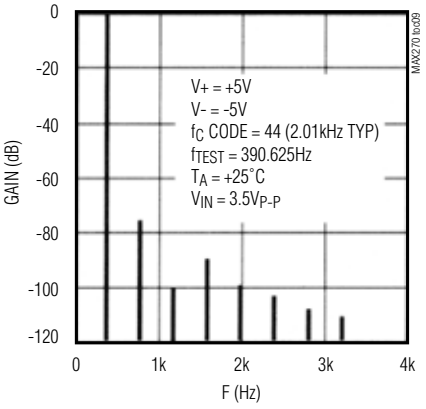
CASCADED FILTER GAIN vs. FREQUENCY (NORMALIZED TO CUTOFF FREQUENCY)



CASCADED FILTER GAIN vs. FREQUENCY (NORMALIZED TO CUTOFF FREQUENCY)



FILTER HARMONIC DISTORTION



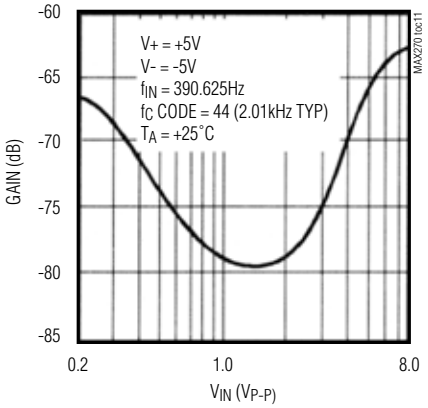
FILTER TOTAL HARMONIC DISTORTION PLUS NOISE vs.INPUT FREQUENCY

f_{IN} (Hz)	f_C CODE	f_C (Hz) (TYP)	THD PLUS NOISE (TYP)
190	0	1k	-78
390	44	2.01k	-73
1367	100	7.01k	-67
4875	127	25k	-66

MAX270 toc10

V+ = 5V, V- = -5V; V_{IN} = 3.5V_{P-P}; T_A = +25°C

FILTER TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT AMPLITUDE



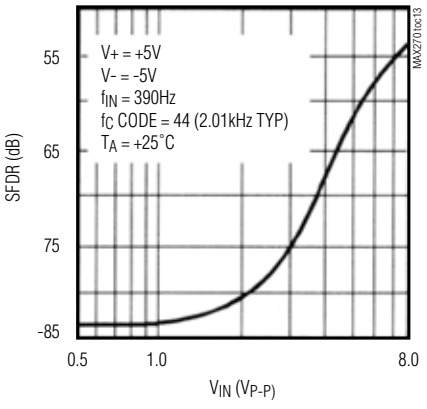
MAX271 FILTER PLUS TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. INPUT FREQUENCY

f_{IN} (Hz)	f_C CODE	f_C (Hz) (TYP)	SFDR (dB)
195	0	1k	73.5
781	72	4.01k	69.5
1562.5	105	8.08k	66
3906	124	19.4k	61.5

MAX270 toc12

V+ = 5V, V- = -5V; V_{IN} = 3.5V_{P-P};
T/H SWITCHED AT 50kHz, 50% DUTY CYCLE; T_A = +25°C

MAX271 FILTER PLUS TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. INPUT AMPLITUDE



MAX271 FILTER PLUS TRACK-AND-HOLD SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY

f_{SAMPLE} (Hz)	f_{IN} (Hz)	f_C CODE	f_C (Hz)	SFDR (dB)
100k	781	72	4.01k	72
200k	1562	105	8.08k	72
500k	3906	124	19.4k	64

MAX270 toc14

V+ = 5V, V- = -5V; V_{IN} = 3.5V_{P-P};
T/H SWITCHED AT 50kHz, 50% DUTY CYCLE; T_A = +25°C

Detailed Description

Figures 1a, 1b, and 1c show the MAX270/MAX271 functional diagrams. Both the MAX270 and MAX271 contain two independent, second-order, Sallen-Key, lowpass filter sections, A and B to provide a frequency vs. gain rolloff of approximately 40dB/decade. These are not switched-capacitor filters, but have a continuous-time design similar to discrete active filters built around op amps. The MAX270/MAX271 eliminate clock noise and aliasing problems which limit low-noise performance of switched-capacitor filters; resulting dynamic range is over 96dB.

Each filter section contains two banks of programmable capacitors, controlled by an internal 7-bit memory, which set filter cutoff frequencies (f_C) from 1kHz to 25kHz. The filters provide two program modes. In µP mode, cutoff frequencies are programmed by writing 7-bit data to one of two memory addresses (one for each filter section). Alternately, a pin-strap programming mode programs both filter sections simultaneously. In this mode, both memory latches are transparent (not addressable), and data pins D0–D6 may be pin-strapped (hard-wired) to set a common f_C for both filter sections.

The filters are trimmed at the wafer level, setting 0 for a maximum of 0.15dB passband peaking for f_C programmed to 1kHz. Maximum passband peaking at other codes is typically less than 0.15dB. Filter Q is not user-programmable.

The MAX270 includes an uncommitted op amp (noninverting input grounded); the MAX271 has an on-chip T/H that tracks and holds the output of either filter section (selectable). The held output is provided at T/H OUT. T/H functions are controlled by writing control bits to internal registers (in µP mode) or by control pins directly (in pin-strap mode).

The MAX270 and MAX271 provide a low quiescent current shutdown mode controlled by the $\overline{SHDN}$ pin, which turns off internal amplifiers and disconnects all outputs, reducing quiescent operating current to less than 15µA. When the MAX271 is in µP mode, shutdown mode is selected by writing control bits to memory (the $\overline{SHDN}$ pin is disabled).

Pin Description

MAX270

PIN	NAME	FUNCTION
1	OP OUT	Uncommitted Op Amp Output
2	V+	Positive Supply Voltage
3	OUTA	Filter A Output
4	$\overline{SHDN}$	Shutdown Control. Low level disconnects OUTA, OUTB, and OP OUT and places device into shutdown mode.
5	INA	Filter A Input
6	V-	Negative Supply Voltage
7	INB	Filter B Input
8	OUTB	Filter B Output
9	GND	Ground
10	$\overline{WR}$	Write Control Input. A low level writes data D0–D6 to program memory addressed by A0. High level latches data.
11	CS	Chip-Select Input. Must be low for $\overline{WR}$ input to be recognized.
12	A0	Three-Level Address Input Logic High: Addresses filter A Logic Low: Addresses filter B Connect to V-: Pin-strap mode
13-19	D0–D6	7-Bit Data Inputs. Allows programming of 128 cutoff frequencies in a 1kHz to 25kHz range.
20	OP IN	Uncommitted Op Amp Input

Note: *All digital input levels are TTL and CMOS compatible, unless otherwise noted.*

Pin Description (continued)

MAX271

PIN	NAME	FUNCTION, FP MODE (MODE = GND OR V-)	FUNCTION, FP MODE (MODE = GND OR V+)
1	T/H OUT	Track-and-Hold Output	
2	V+	Positive Supply Voltage	
3	OUTA	Filler A Signal Output	
4	$\overline{SHDN}$	—	$\overline{SHUTDOWN}$ Control. A low level disconnects outputs and places device into shutdown mode
5	INA	Filter A Signal Input	
6	V-	Negative Supply Voltage	
7	INB	Filter B Signal Input	
8	MODE	Selects µP mode when connected to GND or V- and pin-strap mode when connected to V+.	
9	OUTB	Filter B Signal Output	
10	GND	Ground	
11	T/H A/$\overline{B}$	—	Track-and-Hold Input Control. A high/low level internally connects OUTNOUTB to input of Track-and-Hold
12	$\overline{WR}$	$\overline{WRITE}$ Control Input. A low level writes data D0-D6 program memory addressed by A1, A0 (or performs function as described for address inputs). High level latches data.	—
13	T/H EN	X	Track-and-Hold Output Control. Low level disconnects T/H OUT. Connect pin high for normal operation
14	$\overline{CS}$	$\overline{Chip\ Select}$ Input. Must be low for $\overline{WR}$ input to be recognized.	—
15, 16	A1, A0	Address and µP Control Inputs. 0, 0 Programs f_C, filter A 0, 1 Programs f_C, filter B 1,0 Controls T/H functions: D0 performs T/H En pin function D1 performs T/H A/$\overline{B}$ pin function. 1,1 Controls device shutdown: D0 performs $\overline{SHDN}$ pin function Note: The $\overline{WR}$ pin must be strobed low to initiate a program/function (Figure 2).	—
17-23	D0–D6	7-bit Data Inputs. Allows programming of 128 cutoff frequencies (also performs control functions as described above).	7-bit Data Inputs. Program memory latches are transparent in this mode. Connect pins high or low to program filters A and B simultaneously to the same f_C.
24	$\overline{T}$/H	Track-and-Hold Control. Low level causes T/H OUT to track selected filter output. Filter output level held at T/H OUT synchronous with $\overline{T}$/H rising transition.	

X = Pin has no function in this mode.

Note: *All digital input levels are TTL and CMOS compatible, unless otherwise noted.*

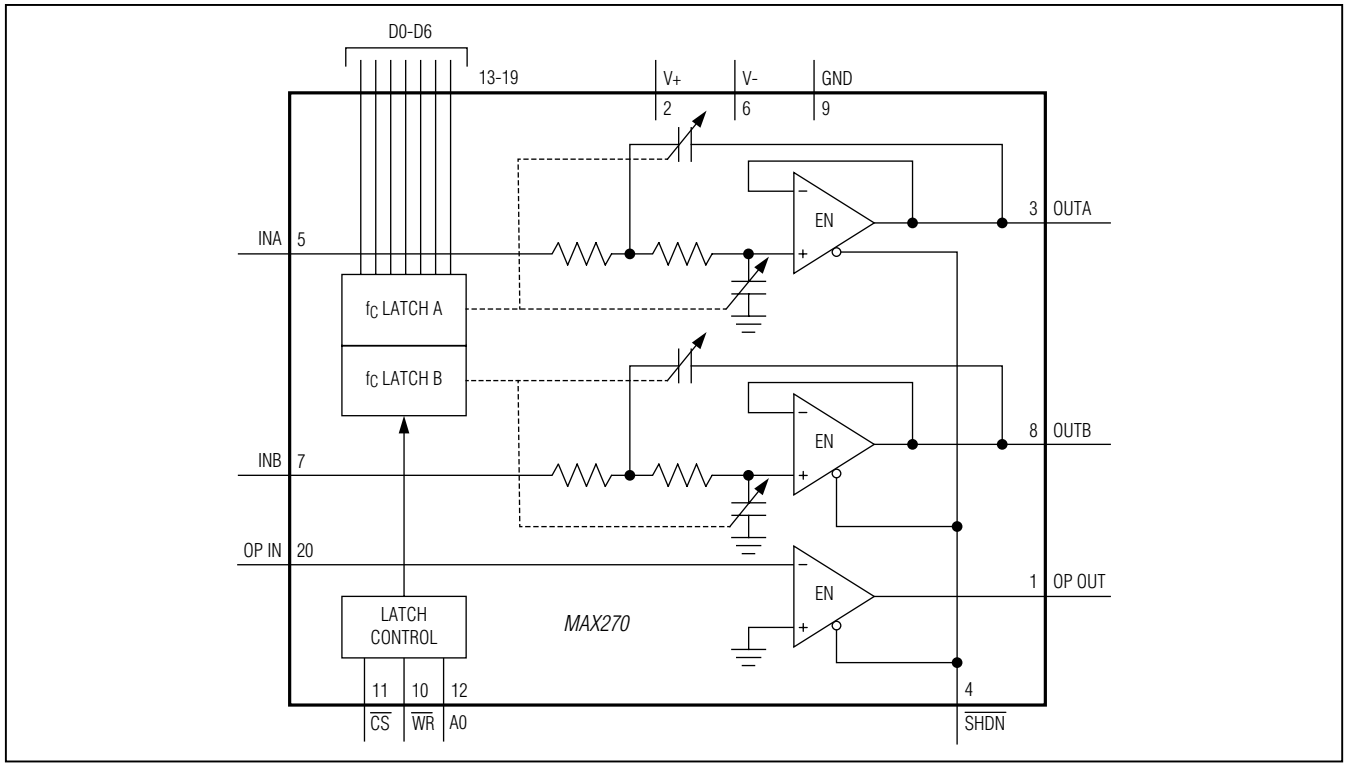


Figure 1a. MAX270 Block Diagram

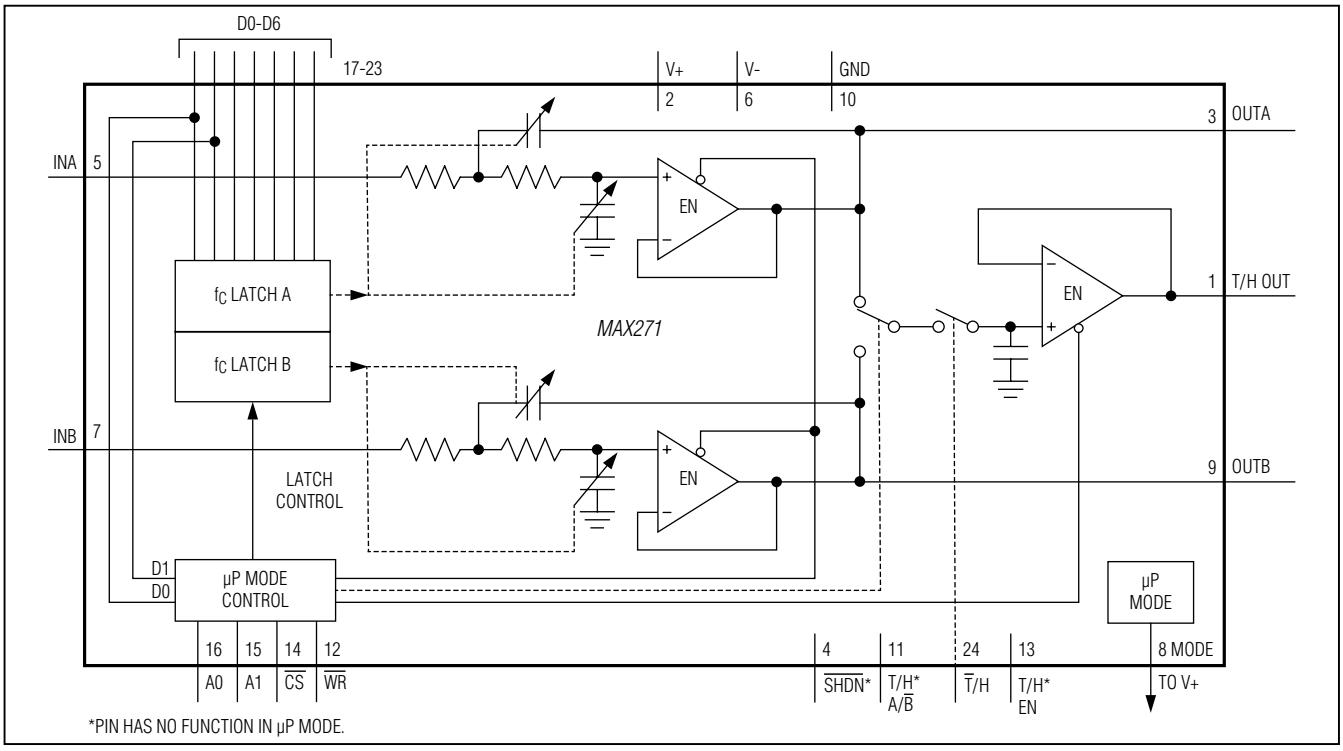


Figure 1b. MAX271 Block Diagram—µP Mode

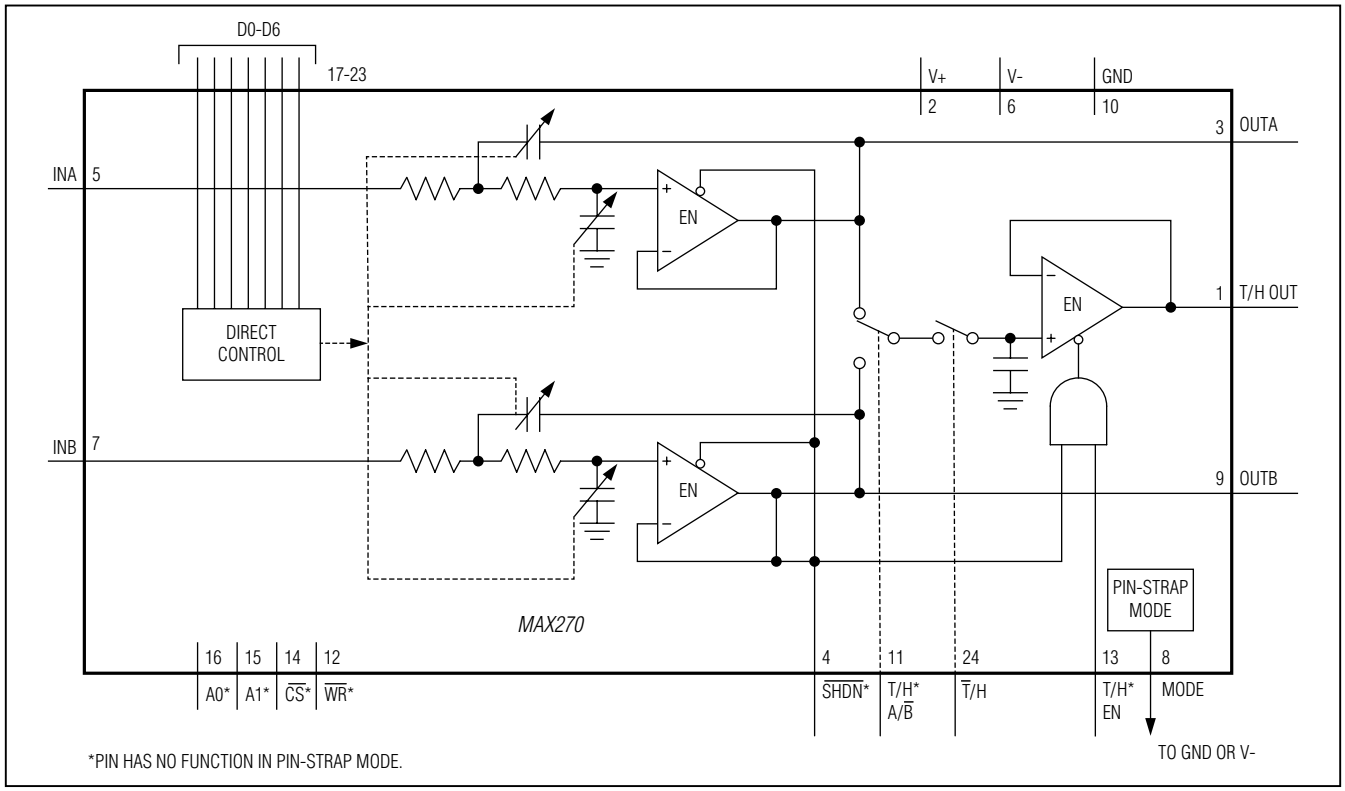


Figure 1c. MAX271 Block Diagram—Pin-Strap Mode

Filter Programming

Cutoff Frequency

f_C is the frequency of 3dB attenuation in the filter response.

Table 1 shows how data pins D0–D6 allow programming of 128 cutoff frequencies from 1kHz to 25kHz.

The equations for calculating f_C from the programmed code are as follows:

$$f_C = \frac{87.5}{87.5 - CODE} \times 1kHz \quad \text{for codes } 0-63 \ (f_C = 1kHz \text{ to } 3.57kHz)$$

$$f_C = \frac{262.5}{137.5 - CODE} \times 1kHz \quad \text{for codes } 64-127 \ (f_C = 3.57kHz \text{ to } 25kHz)$$

where CODE is the data on pins D0–D6 (0–127). D6 is the most significant bit (MSB).

Actual cutoff frequencies are subject to some error for each programmed code. Highest accuracy occurs at CODE = 0 where filters are trimmed for a 1kHz cutoff frequency. At higher codes, CODE vs. f_C errors increase; the frequency error at CODE = 127 {highest code) remains typically within ±9.5%. This means that the actual filter cutoff frequency, when programmed to CODE = 127, falls between 22.63kHz and 27.38kHz.

Table 1. Programmed Cutoff Frequency Codes (typ)

PROGRAMMED CODE	f_C (kHz)	PROGRAMMED CODE	f_C (kHz)	PROGRAMMED CODE	f_C (kHz)	PROGRAMMED CODE	f_C (kHz)
0	1.000	32	1.576	64	3.571	96	6.325
1	1.011	33	1.605	65	3.620	97	6.481
2	1.023	34	1.635	66	3.671	98	6.645
3	1.035	35	1.666	67	3.723	99	6.818
4	1.047	36	1.699	68	3.777	100	7.008
5	1.060	37	1.732	69	3.832	101	7.191
6	1.073	38	1.767	70	3.888	102	7.394
7	1.087	39	1.804	71	3.947	103	7.608
8	1.100	40	1.842	72	4.007	104	7.835
9	1.114	41	1.881	73	4.069	105	8.076
10	1.129	42	1.923	74	4.133	106	8.333
11	1.143	43	1.966	75	4.200	107	8.606
12	1.158	44	2.011	76	4.268	108	8.898
13	1.174	45	2.058	77	4.338	109	9.210
14	1.190	46	2.108	78	4.411	110	9.545
15	1.206	47	2.160	79	4.487	111	9.905
16	1.223	48	2.215	80	4.565	112	10.294
17	1.241	49	2.272	81	4.646	113	10.714
18	11.259	50	2.333	82	4.729	114	11.170
19	1.277	51	2.397	83	4.816	115	11.666
20	1.296	52	2.464	84	4.906	116	12.209
21	1.315	53	2.536	85	5.000	117	12.804
22	1.335	54	2.611	86	5.097	118	13.461
23	1.356	55	2.692	87	5.198	119	14.189
24	1.378	56	2.777	88	5.303	120	15.000
25	1.400	57	2.868	89	5.412	121	15.909
26	1.422	58	2.966	90	5.526	122	16.935
27	1.446	59	3.070	91	5.645	123	18.103
28	1.470	60	3.181	92	5.769	124	19.444
29	1.495	61	3.301	93	5.898	125	21.000
30	1.521	62	3.431	94	6.034	126	22.826
31	1.548	63	3.571	95	6.176	127	25.000

Programmed code is the data on pins D0–D6 (0–127). D6 is the MSB.

MAX270 Control Interlace

The A0 pin is a three-level input that selects the memory addresses for updating cutoff frequency data in µP mode:

A0	SELECTS
Logic Low	Filter B
Logic High	Filter A

Figure 2 shows µP-mode interface timing.

Connecting A0 to the negative supply selects pin-strap mode. Pin-strap mode allows filter programming with no timing requirements. Internal memory latches are disabled, permitting filters A and B to be programmed directly to f_C data strapped on D0–D6. This mode disables $\overline{CS}$ and $\overline{WR}$ controls, and filters A and B are programmed to the same f_C.

A low level on the $\overline{SHDN}$ pin shuts down all amplifiers and disconnects OUTA, OUTB, and OP OUT. Current consumption drops to less than 15µA in this mode.

MAX271 Control Interlace

Connecting the MODE pin to GND or V- selects the µP mode. In this mode, addressable program memory controls filter cutoff frequency programming and all T/H functions, except T/H. See the Figure 2 for timing characteristics. Table 2 describes available functions:

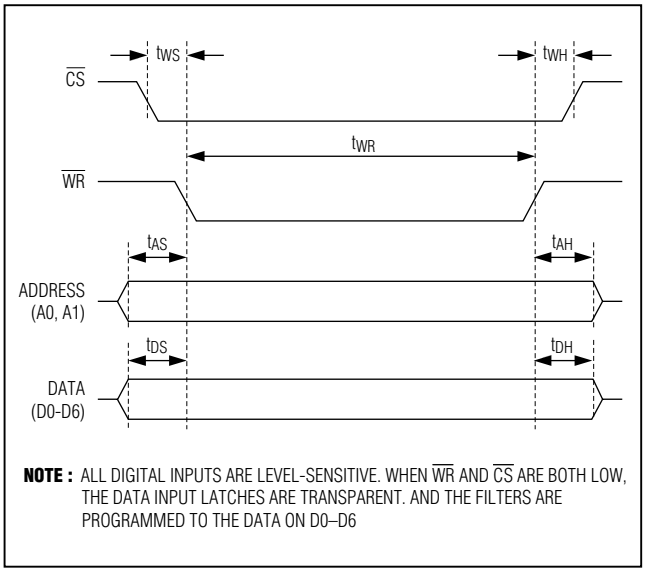


Figure 2. MAX270/MAX271 Digital Timing Diagram

In µP mode, $\overline{SHDN}$, T/H A/$\overline{B}$, and T/H EN pins are disabled. T/H remains enabled and performs the T/H tracking/holding function.

Tying MODE to V+ selects pin-strap mode. In this mode, both memory latches are transparent, and data on D0–D6 controls the f_C of filters A and 8 directly (filters A and 8 are programmed to the same f_C). Pin strap D0–D6 for operation without µP. A0, A1, $\overline{CS}$, and $\overline{WR}$ are disabled.

Table 2. MAX271 µP-Mode Interface

A1	A0	06	05	04	03	02	01	D0	FUNCTION
0	0	7-bit f_C data							Selects filter A
0	1	7-bit f_C data							Selects filter B
1	0	X	X	X	X	X	X	0	T/H OUT disabled
1	0	X	X	X	X	X	X	1	T/H OUT enabled
1	0	X	X	X	X	X	0	X	Selects OUTB as input to T/H
1	0	X	X	X	X	X	1	X	Selects OUTA as input to T/H
1	1	X	X	X	X	X	X	0	Filter shutdown mode. All outputs floated, 15µA max supply current
1	1	X	X	X	X	X	X	1	Removes filter from shutdown mode

X = Don't care

Digital Threshold Levels

All digital inputs are TTL and CMOS compatible, unless otherwise stated. Inputs are CMOS gates with less than 1µA leakage current and 8pF capacitance loading. Typical logic voltage thresholds are a function of the V+ supply voltage as shown below (voltages are referenced to GND).

V+ (V)	LOGIC THRESHOLD VOLTAGE (V)
8	+2.4
7	+2.3
6	+2.0
5	+1.75
4	+1.5
2.5	+1.0

Note: *For +5V single-supply operation, where incoming logic signals are referenced to V-, typical logic thresholds are +3.5V. Therefore, a CMOS (rail-to-rail) logic interface is recommended.*

Filter Performance

All MAX270/MAX271 internal amplifier and output stages for filter sections. uncommitted op amp, and T/H are identical. The outputs are designed to drive 5kΩ in parallel with a maximum capacitance of 100pF. At higher load levels, the output swing becomes asymmetric. All outputs can be short circuited to GND for an indefinite duration.

The MAX270/MAX271 operating frequency range is limited to approximately 2MHz by the bandwidth of the internal amplifiers.

Filter Noise

Wideband filter noise over a 50kHz bandwidth is $12\mu V_{RMS}$ and $38\mu V_{RMS}$ per section for f_C programmed to 1kHz and 25kHz, respectively. A dynamic range of over 96dB results.

Filter Input Impedance

At DC, the input impedance at INA and INB is equal to the DC input impedance of the amplifier, which is about 5MΩ. At higher frequencies, internal capacitors contribute to an effective input impedance that may fall as low as 100kΩ at 25kHz.

MAX271 Track-and-Hold

The MAX271 T/H is functionally equivalent to a switched 200pF capacitor buffered by a unity-gain amplifier (Figures 1b and 1c). When the $\overline{T}$/H pin is driven low, the output of filter A or filter B (whichever is selected via control interface) internally connects to the amplifier, and T/H OUT follows the filter output. The offset at T/H OUT (±6mV max) is the combined offset of the filter amplifier and the T/H buffer. When $\overline{T}$/H is pulled high, the switch disconnects the filter signal from the T/H. The T/H capacitor holds the stored charge, and that voltage is buffered at T/H OUT.

A low level at T/H EN disconnects T/H OUT, enabling multiplexed operation (Figure 3). T/H A/B selects between OUTA and OUTB as the T/H input. In FP mode, the T/H EN and T/H OUT functions are controlled by writing control bits to program memory, with T/H EN and T/H OUT pins disabled.

See the *Typical Operating Characteristics* graphs for T/H dynamic accuracy.

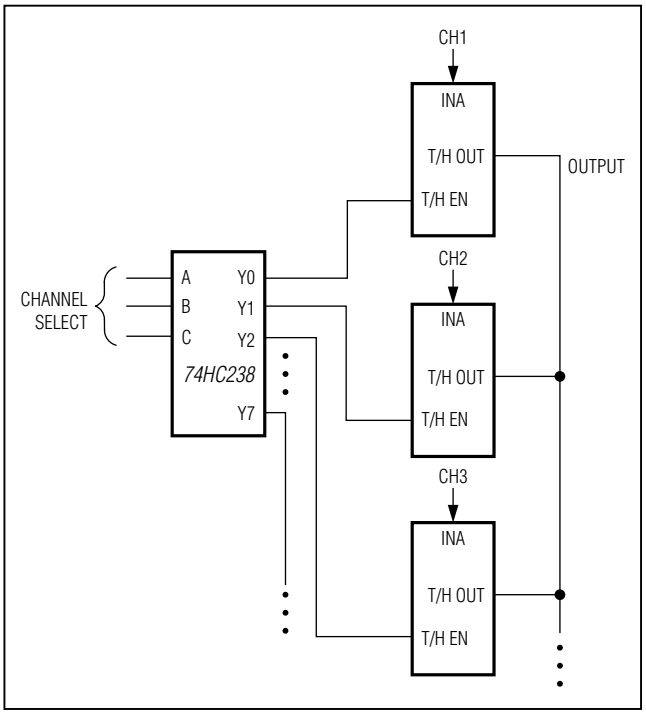


Figure 3. MAX271 Multiplexed Operation

Applications Information

Power-Supply Configurations

The MAX270/MAX271 power supplies must be properly bypassed. Best performance is achieved if V+ and V- are bypassed to GND with 4.7µF electrolytic (tantalum is preferred) and 0.1µF ceramic capacitors in parallel. These should be as close as possible to the chip supply pins.

Single supplies in the range of 4.75V to 16V may be used to power the MAX270/MAX271 as shown in Figure 4. Digital logic may be referenced to V- (system ground), but will not maintain TTL compatibility. CMOS (rail-to-rail) logic recommended. For µP-mode operation with a single supply, the MAX270 A0 pin must be configure with a voltage divider (Figure 4).

Lowest quiescent current in shutdown mode is achieved when A0 is either at V+ or V-.

Independent f_C Programming Without a µP

Figure 6 shows how filter sections A and B may be programmed to different cutoff frequencies without the use of a µP. The MAX690 µP supervisory circuit provides the proper programming sequence when the circuit is powered up by controlling the 74HC373 data buffer and the MAX270 addressing pin to load independent f_C data for filters A and B.

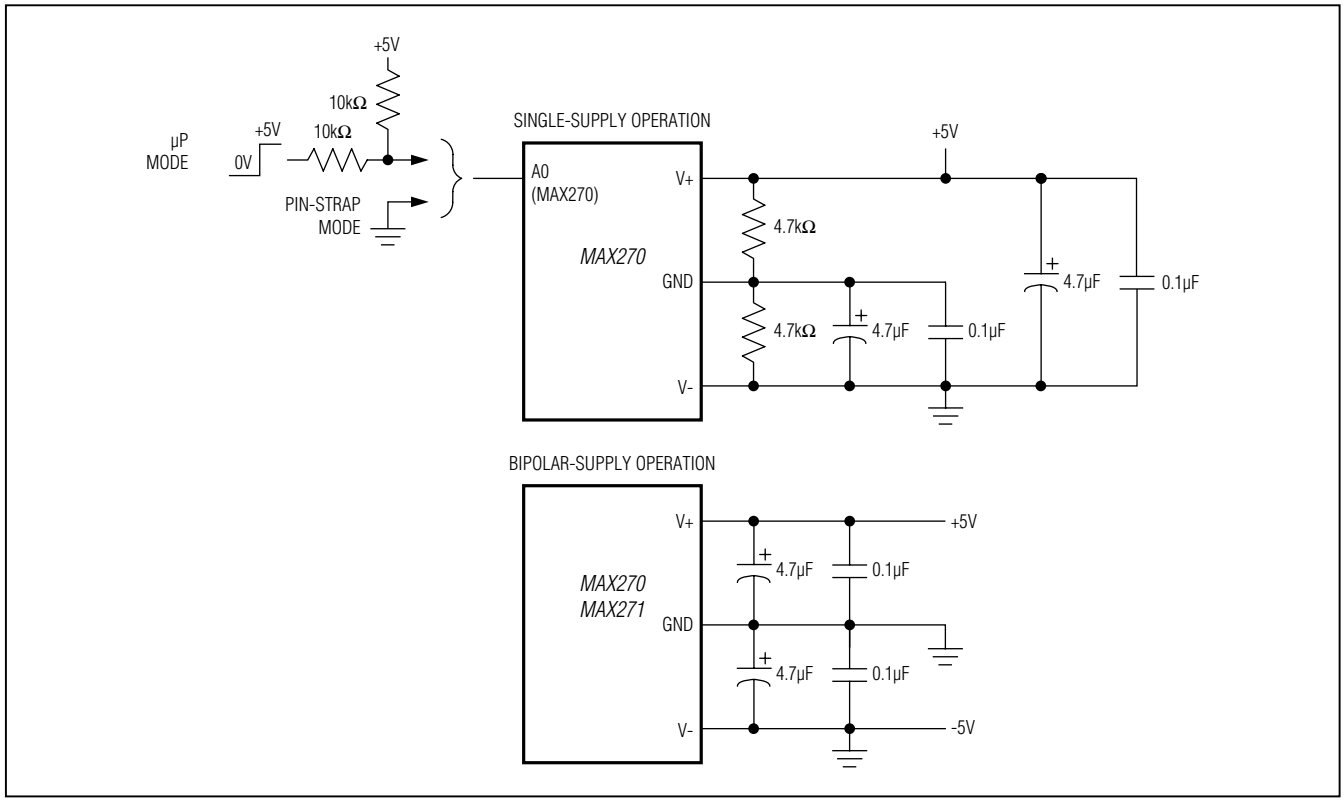


Figure 4. Power-Supply Configurations

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

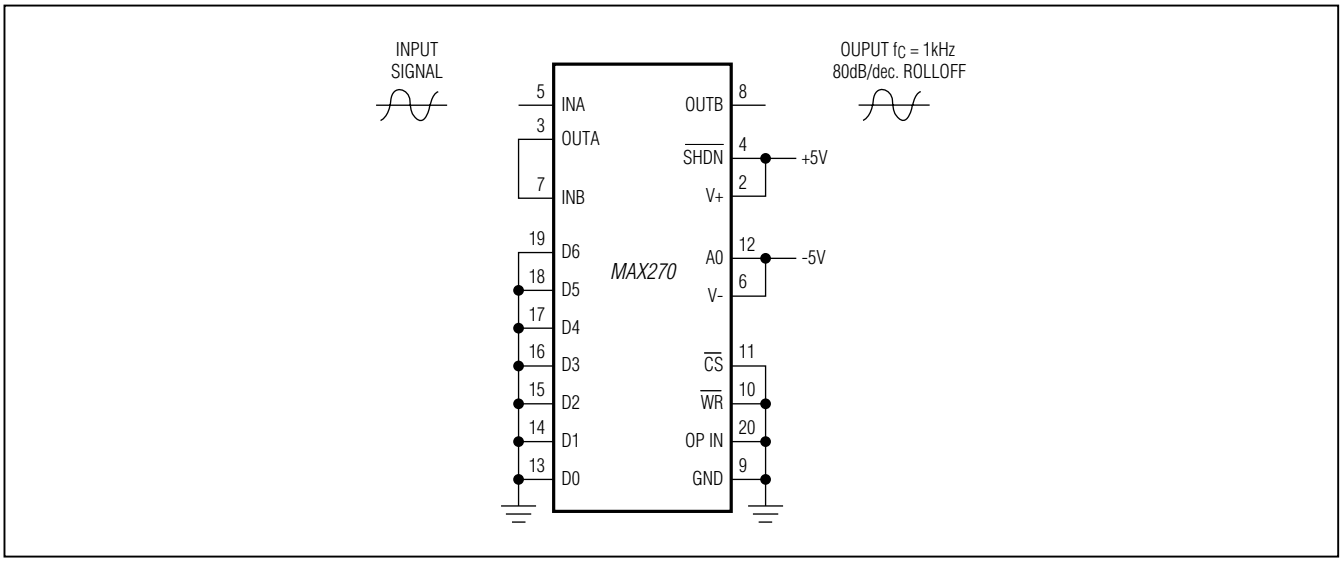


Figure 5. Cascading Filter Sections

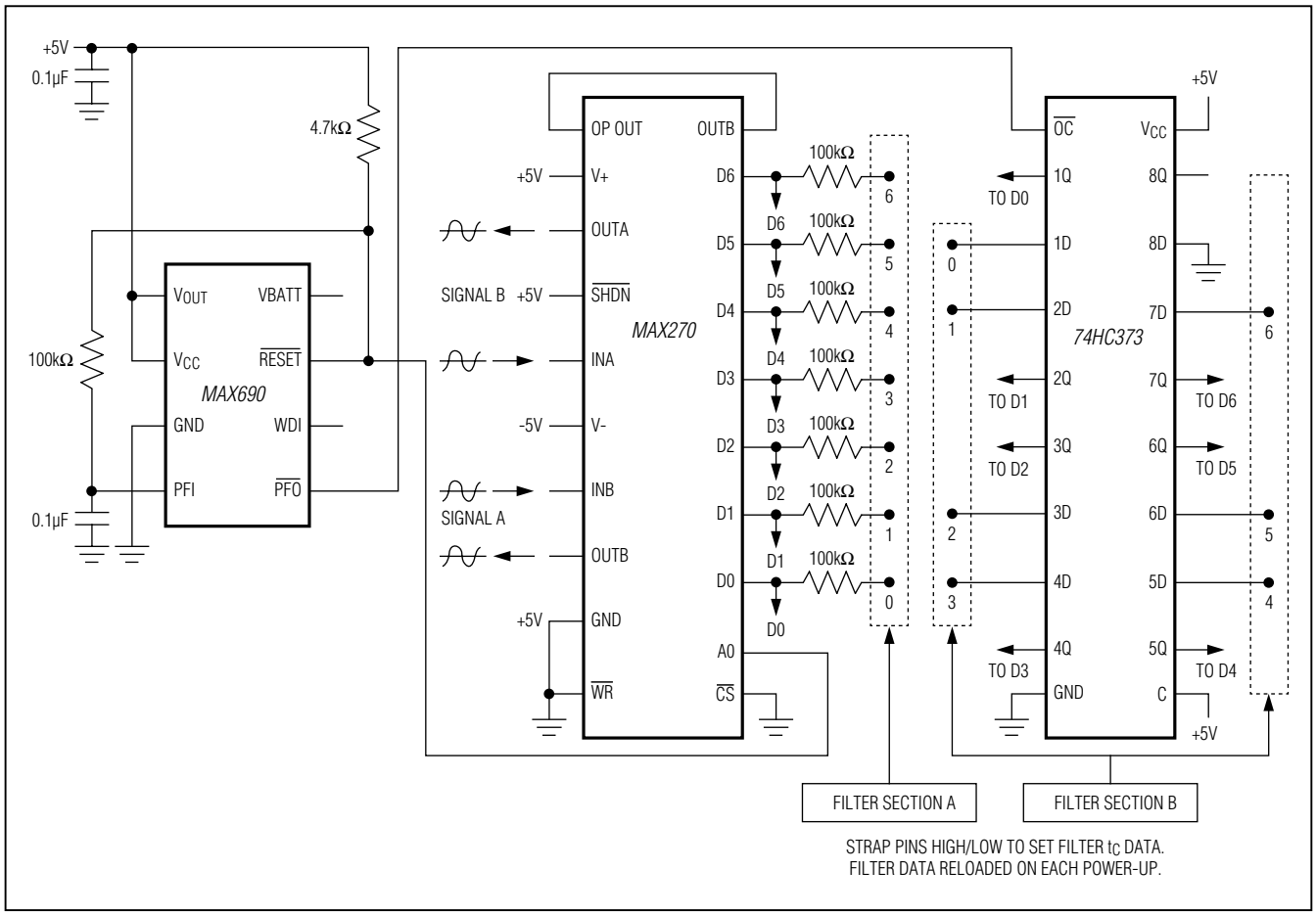
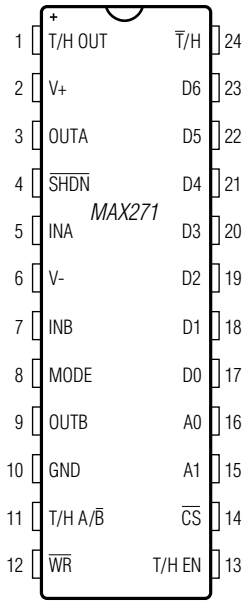


Figure 6. Independent f_C Programming without a µP

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

Pin Configurations (continued)

TOP VIEW



PDIP/SO(W)

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 PDIP	P20-2	21-0043	—
20 SO (W)	W20-3	21-0042	90-0108
24 PDIP	N24-3	21-0043	—
24 SO (W)	W24-2	21-0042	90-0182

Digitally-Programmed, Dual 2nd-Order Continuous Lowpass Filter

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/91	Initial release	—
1	8/91	Revised *Electrical Characteristics*	2
2	1/12	Revised *Ordering Information* and *Absolute Maximum Ratings*.	1, 2

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