MAX3420E USB Peripheral Controller with SPI Interface

General Description

The MAX3420E contains the digital logic and analog circuitry necessary to implement a full-speed USB peripheral compliant to USB specification rev 2.0. A built-in full-speed transceiver features ±15kV ESD protection and programmable USB connect and disconnect. An internal serial-interface engine (SIE) handles low-level USB protocol details such as error checking and bus retries. The MAX3420E operates using a register set accessed by an SPI interface that operates up to 26MHz. Any SPI master (microprocessor, ASIC, DSP, etc.) can add USB functionality using the simple 3- or 4-wire SPI interface.

Internal level translators allow the SPI interface to run at a system voltage between 1.71V and 3.6V. USB timed operations are done inside the MAX3420E with interrupts provided at completion so an SPI master does not need timers to meet USB timing requirements. The MAX3420E includes four general-purpose inputs and outputs so any microprocessor that uses I/O pins to implement the SPI interface can reclaim the I/O pins and gain additional ones.

The MAX3420E operates over the extended -40°C to +85°C temperature range and is available in a 32-pin LQFP package (7mm x 7mm) and a space-saving 24-pin TQFN package (4mm x 4mm).

Applications

- Cell Phones
- PC Peripherals
- Microprocessors and DSPs
- Custom USB Devices
- Cameras
- Desktop Routers
- PLCs
- Set-Top Boxes
- PDAs
- MP3 Players
- Instrumentation

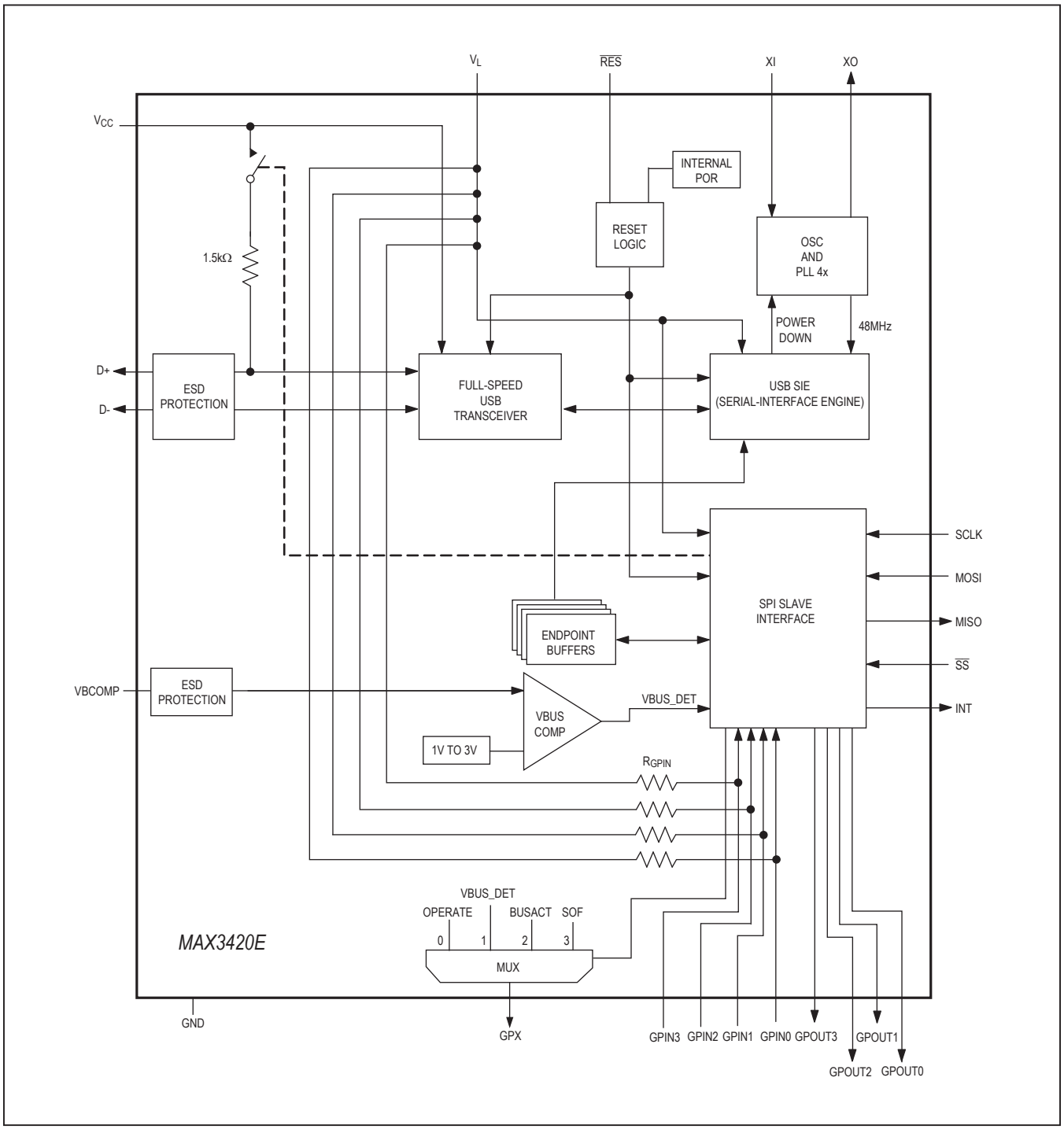
Benefits and Features

- Simplifies Adding USB to Any System
  - Microprocessor-Independent USB Solution
  - Complies with USB Specification Revision 2.0 (Full-Speed Operation)
  - Integrated Full-Speed USB Transceiver
  - Firmware/Hardware Control of an Internal D+ Pullup Resistor
  - Programmable 3 or 4-Wire 26MHz SPI Interface
  - Intelligent USB Serial-Interface Engine (SIE)
  - Automatically Handles USB Flow Control and Double Buffering
  - Handles Low-Level USB Signaling Details
  - Includes Timers for USB Time-Sensitive Operations, So SPI Master Does Not Need to Time Events
  - Four General-Purpose Inputs and Four General-Purpose Outputs
- Internal Comparator Detects V_{BUS} for Self-Powered Applications
- Interrupt Output Pin (Level or Programmable Edge) Allows Polled or Interrupt-Driven SPI Interface
- Double-Buffered Data Endpoints Increase Throughput by Allowing the SPI Master to Transfer Data Concurrently with USB Transfers Over the Same Endpoint
  - Built-In Endpoint FIFOs
  - EP0: CONTROL (64 Bytes)
  - EP1: OUT, Bulk or Interrupt, 2 x 64 Bytes (Double-Buffered)
  - EP2: IN, Bulk or Interrupt, 2 x 64 Bytes (Double-Buffered)
  - EP3: IN, Bulk or Interrupt (64 Bytes)
- SETUP Data Has Its Own 8-Byte FIFO, Simplifying Firmware
- ESD Protection on D+, D-, and VBCOMP Improves System Reliability

19-3781; Rev 6; 3/16

maxim integrated™

Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)

V_{CC} ..... -0.3V to +4V
V_L ..... -0.3V to +4V
VBCOMP ..... -0.3V to +6V
D+, D-, XI, XO ..... -0.3V to (V_{CC} + 0.3V)
SCLK, MOSI, MISO, $\overline{SS}$, $\overline{RES}$, GPOUT3–GPOUT0, GPIN3–GPIN0, GPX, INT..... -0.3V to (V_L + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
32-Pin LQFP (derate 20.7mW/°C above +70°C) 1653mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +3V to +3.6V, V_L = +1.71V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage V_{CC}	V_{CC}		3.0	3.3	3.6	V
Logic-Core Supply and Logic-Interface Voltage V_L	VL		1.71		3.60	V
V_{CC} Supply Current	I_{CC}	Continuously transmitting on D+ and D- at 12Mbps, C_L = 50pF on D+ and D- to GND, CONNECT = 0		15	30	mA
VL Supply Current	I_L	SCLK toggling at 20MHz, $\overline{SS}$ = low, GPIN3–GPIN0 = 0		6	20	mA
V_{CC} Supply Current During Idle	I_{CCID}	D+ = high, D- = low		1.5	5	mA
V_{CC} Suspend Supply Current	I_{CCSUS}	CONNECT = 0, PWRDOWN = 1		33	100	µA
V_L Suspend Supply Current	I_{LSUS}	CONNECT = 0, PWRDOWN = 1		15	50	µA
LOGIC-SIDE I/O						
MISO, GPOUT3–GPOUT0, GPX, INT Output High Voltage	V_{OH}	I_{LOAD} = +5mA, V_L < 2.5V	V_L - 0.45			V
		I_{LOAD} = +10mA, V_L ≥ 2.5V	V_L - 0.4			
MISO, GPOUT3–GPOUT0, GPX, INT Output Low Voltage	VOL	I_{LOAD} = -20mA, V_L < 2.5V			0.6	V
		I_{LOAD} = -20mA, V_L ≥ 2.5V			0.4	
SCLK, MOSI, GPIN3–GPIN0, $\overline{SS}$, $\overline{RES}$ Input High Voltage	V_{IH}		2/3 x V_L			V
SCLK, MOSI, GPIN3–GPIN0, $\overline{SS}$, $\overline{RES}$ Input Low Voltage	V_{IL}				0.4	V
SCLK, MOSI, $\overline{SS}$, $\overline{RES}$ Input Leakage Current	I_{IL}				1	µA
GPIN3–GPIN0 Pullup Resistor to VL	R_{GPIN}		10	20	30	kΩ
TRANSCEIVER SPECIFICATIONS						
Differential-Receiver Input Sensitivity		$\lvert V_{D+} - V_{D-} \rvert$	0.2			V
Differential-Receiver Common-Mode Voltage			0.8		2.5	V

Electrical Characteristics (continued)

(V_{CC} = +3V to +3.6V, V_L = +1.71V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Input Low Voltage	V_{IL}				0.8	V
Single-Ended Receiver Input High Voltage	V_{IH}		2.0			V
Single-Ended Receiver Hysteresis Voltage				0.2		V
D+, D- Input Impedance			300			kΩ
D+, D- Output Low Voltage	V_{OL}	R_L = 1.5kΩ from D+ to 3.6V			0.3	V
D+, D- Output High Voltage	V_{OH}	R_L = 15kΩ from D+ and D- to GND	2.8		3.6	V
Driver Output Impedance Excluding External Resistor		(Note 2)	2	7	11	Ω
D+ Pullup Resistor		REXT = 33Ω	1.425	1.5	1.575	kΩ
ESD PROTECTION (D+, D-, VBCOMP)						
Human Body Model		1µF ceramic capacitors from VBCOMP and V_{CC} to GND		±15		kV
IEC61000-4-2 Air-Gap Discharge		1µF ceramic capacitors from VBCOMP and V_{CC} to GND		±12		kV
IEC61000-4-2 Contact Discharge		1µF ceramic capacitors from VBCOMP and V_{CC} to GND		±8		kV
THERMAL SHUTDOWN						
Thermal-Shutdown Low-to-High				+160		°C
Thermal-Shutdown High-to-Low				+140		°C
CRYSTAL OSCILLATOR SPECIFICATIONS (XI, XO)						
XI Input High Voltage			2/3 x V_{CC}		V_{CC}	V
XI Input Low Voltage					0.4	V
XI Input Current					10	µA
XI, XO Input Capacitance				3		pF
VBCOMP COMPARATOR SPECIFICATIONS						
VBCOMP Comparator Threshold	V_{TH}		1.0	2.0	3.0	V
VBCOMP Comparator Hysteresis	V_{HYS}			375		mV
VBCOMP Comparator Input Impedance	R_{IN}		100			kΩ

Timing Characteristics

(V_{CC} = +3V to +3.6V, V_L = +1.71V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB TRANSMITTER TIMING CHARACTERISTICS						
D+, D- Rise Time	t_{RISE}	C_L = 50pF, Figures 6 and 7	4		20	ns
D+, D- Fall Time	t_{FALL}	C_L = 50pF, Figures 6 and 7	4		20	ns
Rise/Fall-Time Matching		C_L = 50pF, Figures 6 and 7 (Note 2)	90		110	%
Output-Signal Crossover Voltage		C_L = 50pF, Figures 6 and 7 (Note 2)	1.3		2.0	V
SPI BUS TIMING CHARACTERISTICS (V_L = 2.5V) (Figures 8 and 9) (Note 3)						
Serial Clock (SCLK) Period (Note 4)	t_{CP}	V_L = 1.71V	77.0			ns
		V_L = 2.5V	38.4			
SCLK Pulse-Width High	t_{CH}		17			ns
SCLK Pulse-Width Low	t_{CL}		17			ns
$\overline{SS}$ Fall to MISO Valid	t_{CSS}		20			ns
$\overline{SS}$ Leading Time Before the First SCLK Edge	t_L		30			ns
$\overline{SS}$ Trailing Time After the Last SCLK Edge	t_T		30			ns
Data-In Setup Time	t_{DS}		5			ns
Data-In Hold Time	t_{DH}		10			ns
$\overline{SS}$ Pulse High	t_{CSW}		200			ns
SCLK Fall to MISO Propagation Delay	t_{DO}				14.2	ns
SCLK Fall to MOSI Propagation Delay	t_{DI}				14.2	ns
SCLK Fall to MOSI Drive	t_{ON}		3.5			ns
$\overline{SS}$ High to MOSI High Impedance	t_{OFF}				20	ns
SUSPEND TIMING CHARACTERISTICS						
Time-to-Enter Suspend		PWRDOWN = 1 to oscillator stop			5	µs
Time-to-Exit Suspend		PWRDOWN = 1 to 0 to OSCOKIRQ (Note 5)		3		ms

Note 1: Parameters are 100% production tested at T_A = +25°C, and guaranteed by correlation over temperature.
Note 2: Design guaranteed by bench testing. Limits are not production tested.
Note 3: At V_L = 1.71V to 2.5V, derate all of the SPI timing characteristics by 50%. Not production tested.
Note 4: The minimum period is derived from SPI timing parameters.
Note 5: Time-to-exit suspend is dependent on the crystal used.

The MAX3420E connects to any microprocessor using 3 or 4 interface pins (Figure 1). On a simple microprocessor without SPI hardware, these can be bit-banged general-purpose I/O pins. Four GPIN and four GPOUT pins on the MAX3420E more than replace the µP pins necessary to implement the interface. Although the MAX3420E SPI hardware includes separate data-in (MOSI, (master-out, slave-in)) and data-out (MISO, (master-in, slave-out)) pins, the SPI interface can also be configured for the MOSI pin to carry bidirectional data, saving an interface pin. This is referred to as half-duplex mode.

Two MAX3420E features make it easy to connect to large, fast chips such as ASICs and DSPs (see Figure 2). First, the SPI interface can be clocked up to 26MHz. Second, a V_L pin and internal level translators allow running the system interface at a lower voltage than the 3.3V required for V_{CC}.

The MAX3420E provides an ideal method for electrically isolating a USB interface (Figure 3). USB employs flow control in which the device automatically answers host requests with a NAK handshake, until the microprocessor completes its data-transfer operations over the SPI port. This means that the SPI interface can run at any frequency up to 26MHz. Therefore, the designer is free to choose the interface operating frequency and to make opto-isolator choices optimized for cost or performance.

Typical Application Circuits

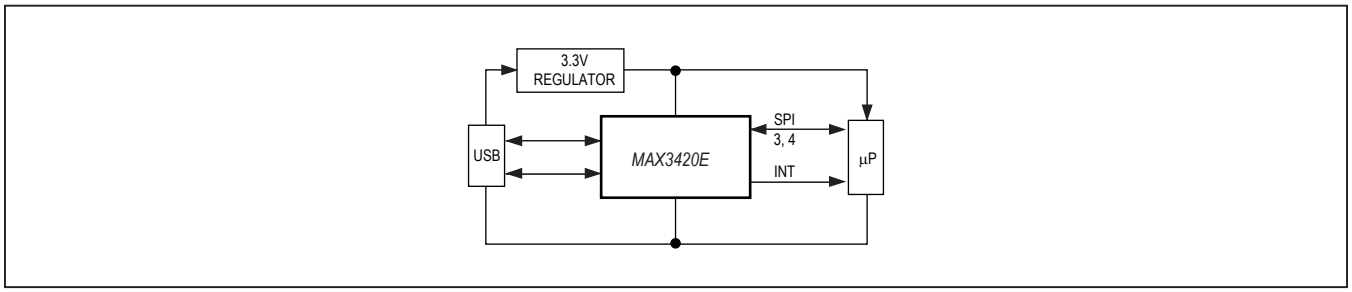


Figure 1. The MAX3420E Connects to Any Microprocessor Using 3 or 4 Interface Pins

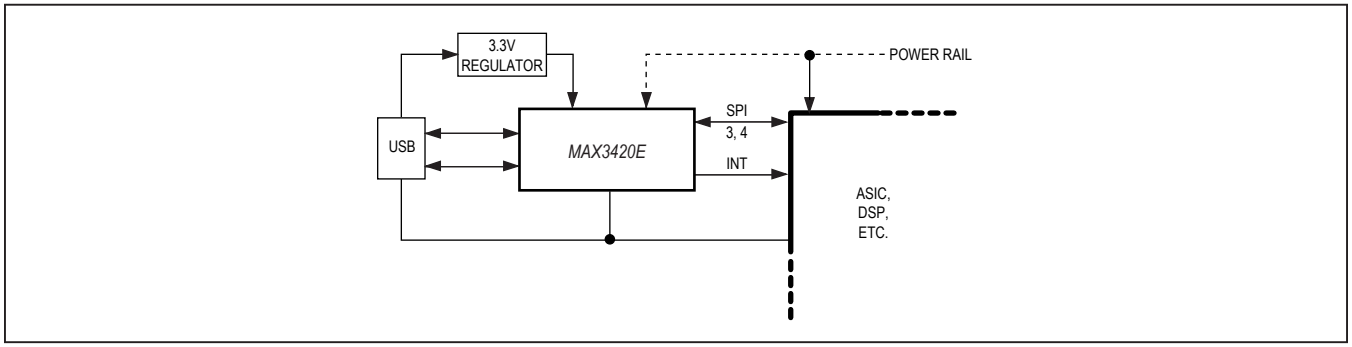


Figure 2. The MAX3420E Connected to a Large Chip

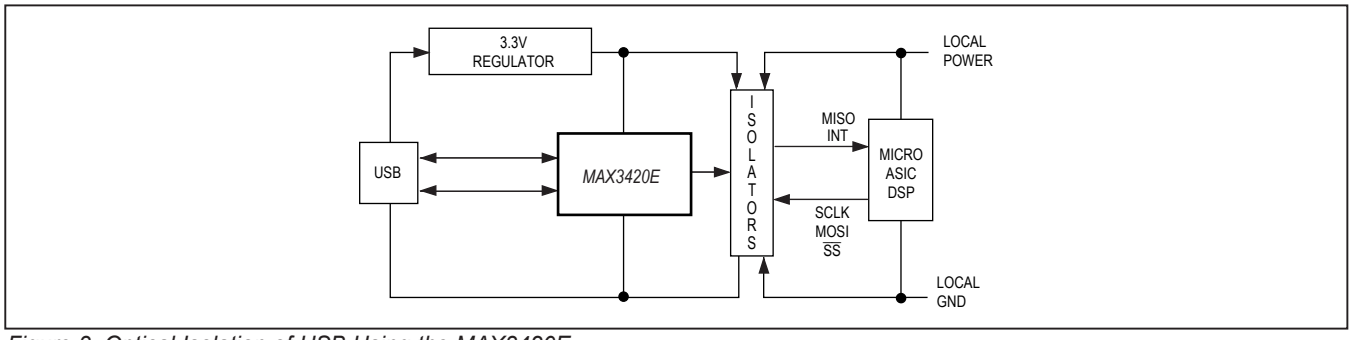
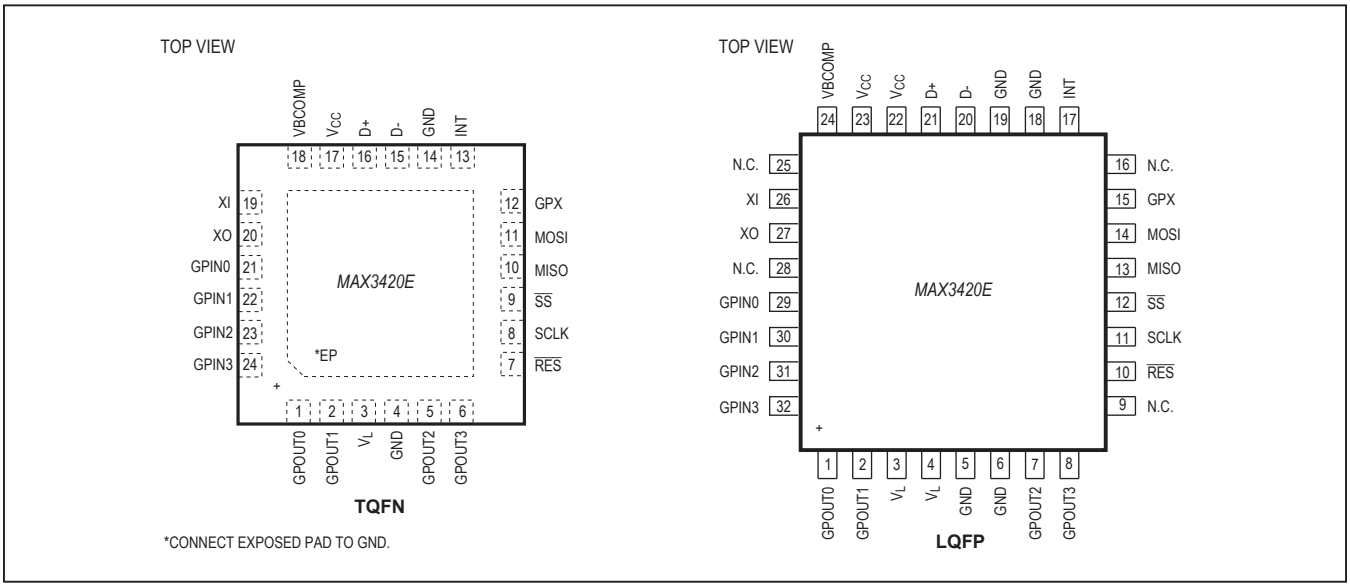


Figure 3. Optical Isolation of USB Using the MAX3420E

Pin Configurations



Pin Description

PIN		NAME	INPUT/ OUTPUT	FUNCTION
TQFN-EP	LQFP			
1	1	GPOUT0	Output	General-Purpose Push-Pull Outputs. GPOUT3–GPOUT0 logic levels are referenced to the voltage on V_L. The SPI master controls the GPOUT3–GPOUT0 states by writing to bit 3 through bit 0 of the IOPINS (R20) register.
2	2	GPOUT1		
3	3, 4	V_L	Input	Level-Translator Reference Voltage. Connect V_L to the system's 1.71V to 3.6V logic-level power supply. Bypass V_L to ground with a 0.1µF capacitor as close to the V_L pin as possible.
4, 14	5, 6, 18, 19	GND	Input	Ground
5	7	GPOUT2	Output	General-Purpose Push-Pull Outputs. GPOUT3–GPOUT0 logic levels are referenced to the voltage on V_L. The SPI master controls the GPOUT3–GPOUT0 states by writing to bit 3 through bit 0 of the IOPINS (R20) register.
6	8	GPOUT3		
7	10	$\overline{RES}$	Input	Device Reset. Drive $\overline{RES}$ low to clear all of the internal registers except for PINCTL (R17), USBCTL (R15), and SPI logic. See the *Device Reset* section for a description of resets available on the MAX3420E. **Note:** The MAX3420E is internally reset if either V_{CC} of V_L is not present. The register file is not accessible under these conditions.
8	11	SCLK	Input	SPI Serial-Clock Input. An external SPI master supplies this clock with frequencies up to 26MHz. The logic level is referenced to the voltage on V_L. Data is clocked into the SPI slave interface on the positive edge of SCLK. Data Is clocked out of the SPI slave interface on the falling edge of SCLK.
9	12	$\overline{SS}$	Input	SPI Slave-Select Input. The $\overline{SS}$ logic level is referenced to the voltage on V_L. When $\overline{SS}$ is driven high, the SPI slave interface is not selected and SCLK transitions are ignored. An SPI transfer begins with a high-to-low $\overline{SS}$ transition and ends with a low-to-high $\overline{SS}$ transition.

Pin Description (continued)

PIN		NAME	INPUT/ OUTPUT	FUNCTION
TQFN-EP	TQFN-EP			
10	13	MISO	Output	SPI Serial-Data Output (Master-In, Slave-Out). MISO is a push-pull output. MISO is three-stated in half-duplex mode or when $\overline{SS}$ = 1. The MISO logic level is referenced to the voltage on V_L.
11	14	MOSI	Input or Input/ Output	SPI Serial-Data Input (Master-Out, Slave-In). The logic level on MOSI is referenced to the voltage on V_L. MOSI can also be configured as a bidirectional MOSI/MISO input and output.
12	15	GPX	Output	General-Purpose Multiplexed Output. The internal MAX3420E signal that Appears on GPX is programmable by writing to the GPXB and GPXA bits of the PINCTL (R17) register. GPX indicates one of four signals: OPERATE (00, default), VBUS_DET (01), BUSACT (10), and SOF (11).
13	17	INT	Output	Interrupt Output. In edge mode, the logic level on INT is referenced to the voltage on V_L. In edge mode, INT is a push-pull output with programmable polarity. In level mode, INT is open-drain and active low. Set the IE bit in the CPUCTL (R16) register to enable INT.
15	20	D-	Input/ Output	USB D- Signal. Connect D- to a USB “B” connector through a 33Ω ±1% series resistor.
16	21	D+	Input/ Output	USB D+ Signal. Connect D+ to a USB “B” connector through a 33Ω ±1% series resistor. The 1.5kΩ D+ pullup resistor is internal to the device.
17	22, 23	V_{CC}	Input	USB Transceiver Power-Supply Input. Connect V_{CC} to a positive 3.3V power supply. Bypass V_{CC} to ground with a 1.0µF ceramic capacitor as close to the V_{CC} pin as possible.
18	24	VBCOMP	Input	V_{BUS} Comparator Input. VBCOMP is internally connected to a voltage comparator to allow the SPI master to detect (through an interrupt or checking a register bit) the presence or loss of power on V_{BUS}. Bypass VBCOMP to ground with a 1.0µF ceramic capacitor.
19	26	XI	Input	Crystal Oscillator Input. Connect XI to one side of a parallel resonant 12MHz ±0.25% crystal and a capacitor to GND. XI can also be driven by an external Clock referenced to V_{CC}.
20	27	XO	Output	Crystal Oscillator Output. Connect XO to the other side of a parallel resonant 12MHz ±0.25% crystal and a capacitor to GND. Leave XO unconnected if XI is driven with an external source.
21	29	GPIN0	Input	General-Purpose Inputs. GPIN3–GPIN0 are connected to V_L with internal pullup resistors. GPIN3–GPIN0 logic levels are referenced to the voltage on V_L. The SPI master samples GPIN3–GPIN0 states by reading bit 7 through bit 4 of the IOPINS (R20) register. Writing to these bits has no effect.
22	30	GPIN1		
23	31	GPIN2		
24	32	GPIN3		
—	9, 16, 25, 28	N.C.	—	No Internal Connection
—	—	EP	Input	Exposed Paddle (TQFN only). Connect EP to GND.

Register Description

The SPI master controls the MAX3420E by reading and writing 21 registers (Table 1). For a complete description of register contents, please refer to the "MAX3420E Programming Guide." A register access consists of the SPI master first writing an SPI command byte, followed by reading or writing the contents of the addressed register. All SPI transfers are MSB first. The command byte contains the register address, a direction bit (read = 0, write = 1), and the ACKSTAT bit (Figure 4). The SPI master addresses the MAX3420E registers by writing the binary value of the register number in the Reg4 through Reg0 bits of the command byte. For example, to access the IOPINS (R20) register, the Reg4 through Reg0 bits would be as follows: Reg4 = 1, Reg3 = 0, Reg2 = 1, Reg1 = 0, Reg0 = 0. The DIR (direction) bit determines the direction for the data transfer. DIR = 1 means the data byte(s) will be written to the register, and DIR = 0 means the data byte(s) will be read from the register. The ACKSTAT bit sets the ACKSTAT bit in the EPSTALLS (R9) register. The SPI master sets this bit to indicate that it has finished servicing a CONTROL transfer. Since the bit is frequently used, having it in the SPI command byte improves firmware efficiency. In SPI full-duplex mode, the MAX3420E clocks out eight USB status bits as the command byte is clocked in (Figure 5). In half-duplex mode, these status bits are accessed in the normal way, as register bits.

b7	b6	b5	b4	b3	b2	b1	b0
Reg4	Reg3	Reg2	Reg1	Reg0	0	DIR	ACKSTAT

Figure 4. SPI Command Byte

b7	b6	b5	b4	b3	b2	b1	b0
SUSPIRQ	URESIRQ	SUDAVIRQ	IN3BAVIRQ	IN2BAVIRQ	OUT1DAVIRQ	OUT0DAVIRQ	IN0BAVIRQ

Figure 5. USB Status Bits Clocked Out as First Byte of Every Transfer (Full-Duplex Mode Only)

The first five registers (R0–R4) access endpoint FIFOs. To access a FIFO, an initial command byte sets the register address and then consecutive reads or writes keep the same register address to access subsequent FIFO bytes.

The remaining registers (R5–R20) control the operation of the MAX3420E. Once a register address above R4 is set in the command byte, successive byte reads or writes in the same SPI access cycle ($\overline{SS}$ low) increment the register address after every byte read or written. This incrementing operation continues until R20 is accessed. Subsequent byte reads or writes continue to access R20. Note that this autoincrementing action stops with the next SPI cycle, which establishes a new register address. Addressing beyond R20 is ignored.

The MAX3420E register map is depicted in Table 1. For a complete description of all register contents, please refer to the *MAX3420E Programming Guide*.

Table 1. MAX3420E Register Map

REG	NAME	b7	b6	b5	b4	b3	b2	b1	b0	acc
R0	**EP0FIFO**	b7	b6	b5	b4	b3	b2	b1	b0	RSC
R1	**EP1OUTFIFO**	b7	b6	b5	b4	b3	b2	b1	b0	RSC
R2	**EP2INFIFO**	b7	b6	b5	b4	b3	b2	b1	b0	RSC
R3	**EP3INFIFO**	b7	b6	b5	b4	b3	b2	b1	b0	RSC
R4	**SUDFIFO**	b7	b6	b5	b4	b3	b2	b1	b0	RSC
R5	**EP0BC**	0	b6	b5	b4	b3	b2	b1	b0	RSC
R6	**EP1OUTBC**	0	b6	b5	b4	b3	b2	b1	b0	RSC
R7	**EP2INBC**	0	b6	b5	b4	b3	b2	b1	b0	RSC
R8	**EP3INBC**	0	b6	b5	b4	b3	b2	b1	b0	RSC
R9	**EPSTALLS**	0	ACKSTAT	STLSTAT	STLEP3IN	STLEP2IN	STLEP1OUT	STLEP0OUT	STLEP0IN	RSC
R10	**CLRTOGS**	EP3DISAB	EP2DISAB	EP1DISAB	CTGEP3IN	CTGEP2IN	CTGEP1OUT	0	0	RSC
R11	**EPIRQ**	0	0	SUDAVIRQ	IN3BAVIRQ	IN2BAVIRQ	OUT1DAVIRQ	OUT0DAVIRQ	IN0BAVIRQ	RC
R12	**EPIEN**	0	0	SUDAVIE	IN3BAVIE	IN2BAVIE	OUT1DAVIE	OUT0DAVIE	IN0BAVIE	RSC
R13	**USBIRQ**	URESDNIRQ	VBUSIRQ	NOVBUSIRQ	SUSPIRQ	URESIRQ	BUSACTIRQ	RWUDNIRQ	OSCOKIRQ	RC
R14	**USBIEN**	URESDNIE	VBUSIE	NOVBUSIE	SUSPIE	URESIE	BUSACTIE	RWUDNIE	OSCOKIE	RSC
R15	**USBCTL**	HOSCSTEN	VBGATE	CHIPRES	PWRDOWN	CONNECT	SIGRWU	0	0	RSC
R16	**CPUCTL**	0	0	0	0	0	0	0	IE	RSC
R17	**PINCTL**	EP3INAK	EP2INAK	EP0INAK	FDUPSPI	INTLEVEL	POSINT	GPXB	GPXA	RSC
R18	**REVISION**	0	0	0	0	0	1	0	0	R
R19	**FNADDR**	0	b6	b5	b4	b3	b2	b1	b0	R
R20	**IOPINS**	GPIN3	GPIN2	GPIN1	GPIN0	GPOUT3	GPOUT2	GPOUT1	GPOUT0	RSC

Note: The acc (access) column indicates how the SPI master can access the register.
R = read, RC = read or clear, RSC = read, set, or clear.
Writing to an R register (read only) has no effect.
Writing a 1 to an RC bit (read or clear) clears the bit.
Writing a zero to an RC bit has no effect.

Test Circuits and Timing Diagrams

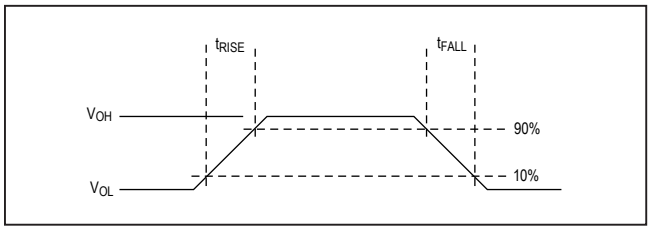


Figure 6. Rise and Fall Times

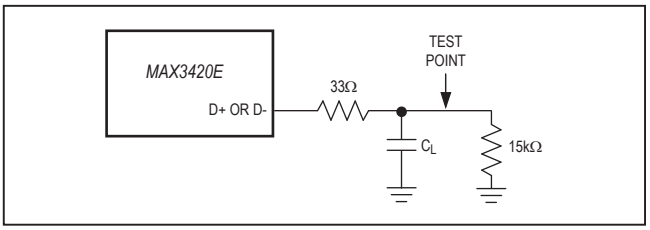


Figure 7. Load for D+/D- AC Measurements

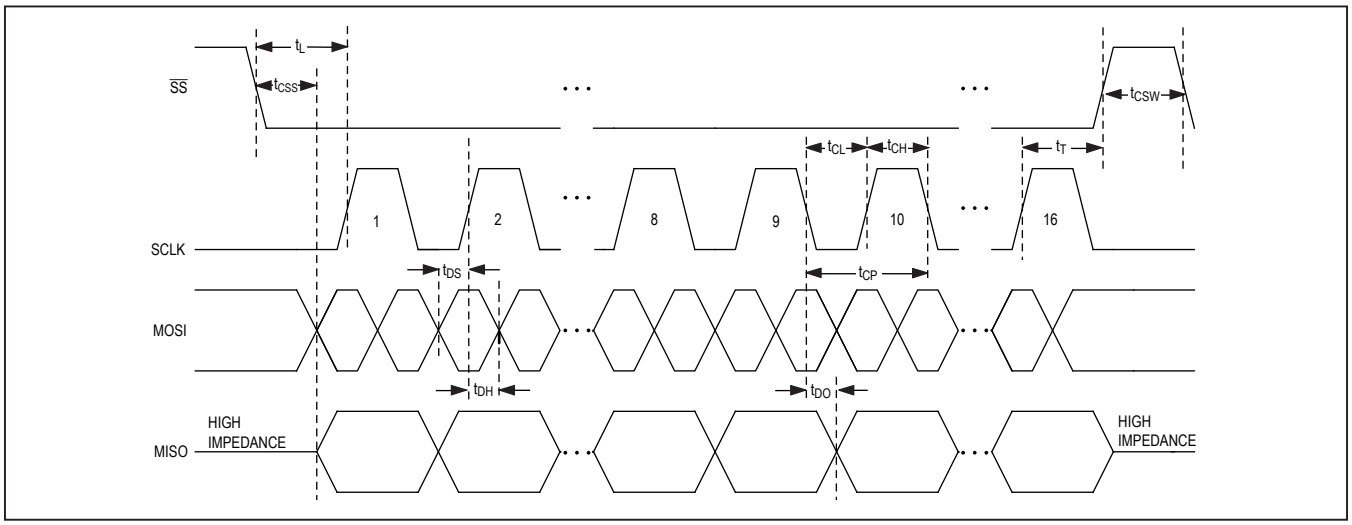
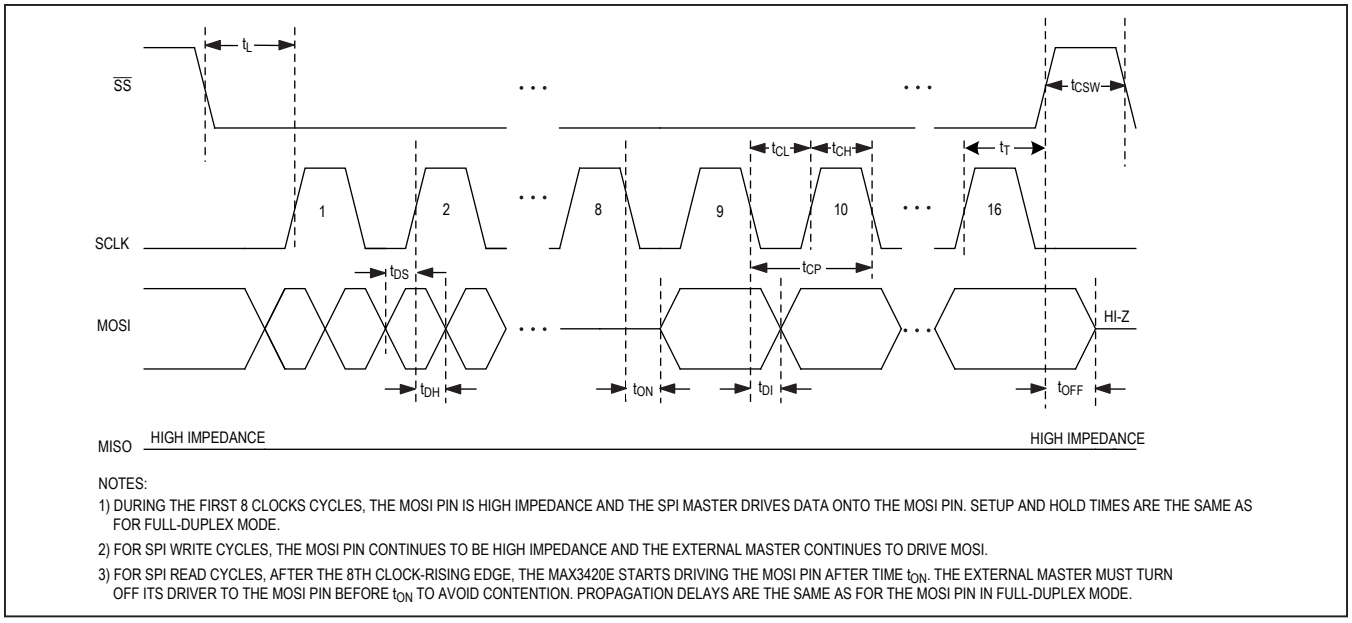


Figure 8. SPI Bus Timing Diagram (Full-Duplex Mode, SPI Mode (0,0))



NOTES:

1) DURING THE FIRST 8 CLOCKS CYCLES, THE MOSI PIN IS HIGH IMPEDANCE AND THE SPI MASTER DRIVES DATA ONTO THE MOSI PIN. SETUP AND HOLD TIMES ARE THE SAME AS FOR FULL-DUPLEX MODE.

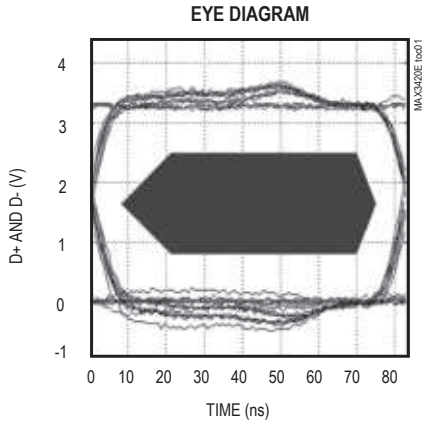
2) FOR SPI WRITE CYCLES, THE MOSI PIN CONTINUES TO BE HIGH IMPEDANCE AND THE EXTERNAL MASTER CONTINUES TO DRIVE MOSI.

3) FOR SPI READ CYCLES, AFTER THE 8TH CLOCK-RISING EDGE, THE MAX3420E STARTS DRIVING THE MOSI PIN AFTER TIME t_{ON}. THE EXTERNAL MASTER MUST TURN OFF ITS DRIVER TO THE MOSI PIN BEFORE t_{ON} TO AVOID CONTENTION. PROPAGATION DELAYS ARE THE SAME AS FOR THE MOSI PIN IN FULL-DUPLEX MODE.

Figure 9. SPI Bus Timing Diagram (Half-Duplex Mode, SPI Mode (0,0))

Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +3.3V, T_A = +25°C.)



Detailed Description

This device contains the digital logic and analog circuitry necessary to implement a full-speed USB peripheral that complies with the USB specification rev 2.0. ESD protection of ±15kV is provided on D+, D-, and VBCOMP. The MAX3420E features an internal USB transceiver and an internal 1.5kΩ resistor that connects between D+ and V_{CC} under the control of a register bit (CONNECT). This allows a USB peripheral to control the logical connection to the USB host. Any SPI master can communicate with the device through the SPI slave interface that operates in SPI mode (0,0) or (1,1). An SPI master accesses the MAX3420E by reading and writing to internal registers. A typical data transfer consists of writing a first byte that sets a register address and direction with additional bytes reading or writing data to the register or internal FIFO.

The MAX3420E contains 384 bytes of endpoint buffer memory, implementing the following endpoints:

- EP0: 64-byte bidirectional CONTROL endpoint
- EP1: 2 x 64-byte double-buffered BULK/INT OUT endpoint
- EP2: 2 x 64-byte double-buffered BULK/INT IN endpoint
- EP3: 64-byte BULK/INT IN endpoint

The choice to use EP1, EP2, EP3 as BULK or INTERRUPT endpoints is strictly a function of the endpoint descriptors that the SPI master returns to the USB host during enumeration.

The MAX3420E register set and SPI interface is optimized to reduce SPI traffic. An interrupt output pin, INT, notifies the SPI master when USB service is required: when a packet arrives, a packet is sent, or the host suspends or resumes bus activity. Double-buffered endpoints help sustain bandwidth by allowing data to move concurrently over USB and the SPI interface.

V_{CC}

Power the USB transceiver by applying a positive 3.3V supply to V_{CC}. Bypass V_{CC} to GND with a 1.0µF ceramic capacitor as close to the V_{CC} pin as possible.

V_L

The MAX3420E digital core is powered though the V_L pin. V_L also acts as a reference level for the SPI interface and all other inputs and outputs. Connect V_L to the system's logic-level power supply. Internal level translators and V_L allow the SPI interface and all general-purpose inputs and outputs to operate at a system voltage between 1.71V and 3.6V.

VBCOMP

The MAX3420E features a USB V_{BUS} detector input, VBCOMP. The VBCOMP pin can withstand input voltages up to 6V. Bypass VBCOMP to GND with a 1.0µF ceramic capacitor. According to USB specification rev 2.0, a self-powered USB device must not power the 1.5kΩ pullup resistor on D+ if the USB host turns off V_{BUS}. VBCOMP is internally connected to a voltage comparator so that the SPI master can detect the loss of V_{BUS} (through an interrupt (INT) or checking a bit

Table 2. Internal Pullup Resistor Control

CONNECT	VBGATE	VBUS_DET	PULLUP
0	X	X	Not Connected
1	0	X	Connected
1	1	0	Not Connected
1	1	1	Connected

(NOVBUSIRQ)) and disconnect the internal 1.5kΩ pullup resistor. If the device using the MAX3420E is bus powered (through a +3.3V regulator connected to V_{CC}), the MAX3420E VBCOMP input can be used as a general-purpose input. Using VBCOMP as a general-purpose input requires a 10kΩ pullup resistor from VBCOMP to V_L. See the *Applications Information* section for more details about this connection.

D+ and D-

The internal USB full-speed transceiver is brought out to the bidirectional data pins D+ and D-. These pins are ±15kV ESD protected. Connect D+ and D- to a USB "B"connector through 33Ω ±1% series resistors. A switchable 1.5kΩ pullup resistor is internally connected to D+. According to the USB rev 2.0 specification, a self-powered peripheral must disconnect its 1.5kΩ pullup resistor to D+ in the event that the host turns off bus power. The VBGATE bit in the USBCTL (R15) register provides the option for the MAX3420E internal logic to automatically disconnect the 1.5kΩ resistor on D+. The VBGATE and CONNECT bits of USBCTL (R15), along with the VBCOMP comparator output (VBUS_DET), control the pullup resistor between V_{CC} and D+, as shown in Table 2. Note that if VBGATE = 1 and VBUS_DET = 0, the pullup resistor is disconnected regardless of the CONNECT bit setting.

XI and XO

XI and XO connect an external 12MHz crystal to the internal oscillator circuit. XI is the crystal oscillator input, and XO is the crystal oscillator output. Connect one side of an external 12MHz ±0.25% parallel resonant crystal to XI, and connect XO to the other side. Connect load capacitors (20pF max) to ground on both XI and XO. XI can also be driven with an external 12MHz ±0.25% clock. If driving XI with an external clock, leave XO unconnected. The external clock must meet the voltage characteristics depicted in the *Electrical Characteristics* table. Internal logic is single-edge triggered. The external clock should have a nominal 50% duty cycle.

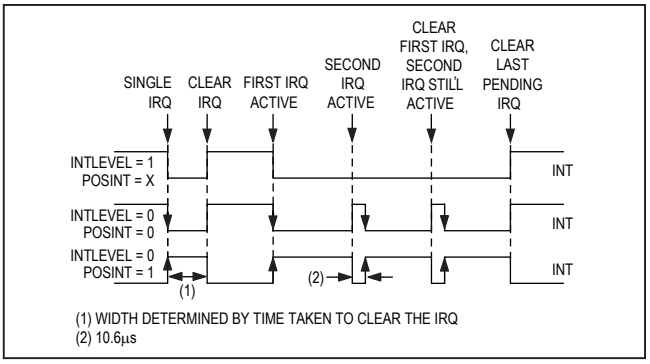


Figure 10. Behavior of the INT Pin for Different INTLEVEL and POSINT Bit Settings

$\overline{RES}$

Drive $\overline{RES}$ low to put the MAX3420E into a chip reset. A chip reset sets all registers to their default states, except for PINCTL (R17), USBCTL (R15), and SPI logic. All FIFO contents are unknown during chip reset. Bring the MAX3420E out of chip reset by driving $\overline{RES}$ high. The $\overline{RES}$ pulse width can be as short as 200ns. See the *Device Reset* section for a description of the resets available on the MAX3420E.

INT

The MAX3420E INT output pin signals when a USB event occurs that requires the attention of the SPI master. The SPI master must set the IE bit in the CPUCTL (R16) register to activate INT. When the IE bit is cleared, INT is inactive (open for level mode, high for negative edge, low for positive edge). INT is inactive upon power-up or after a chip reset.

The INT pin can be a push-pull or open-drain output. Set the INTLEVEL bit of the PINCTL (R17) register high to program the INT output pin to be an active-low level (open-drain output). An external pullup resistor to V_L is required for this setting. In level mode, the MAX3420E drives INT low when any of the interrupt flags are set. If multiple interrupts are pending, INT goes inactive only when the SPI master clears the last active interrupt request bit (Figure 10). The POSINT bit of the PINCTL (R17) register has no effect on INT in level mode.

Clear the INTLEVEL bit to program INT to be an edge (push-pull output). The active edge is programmable using the POSINT bit of the PINCTL (R17) register. In edge mode, the device produces an edge referenced to V_L any time an interrupt request is activated, or when an interrupt request is cleared and others are pending (Figure 10). Set the POSINT bit in the PINCTL (R17) register to make INT active high, and clear the POSINT bit to make INT active low.

GPIN3–GPIN0, GPOUT3–GPOUT0 and GPX

The MAX3420E has four general-purpose inputs (GPIN3–GPIN0), four general-purpose outputs (GPOUT3–POUT0), and a multiplexed output pin (GPX). GPIN3 through GPIN0 all have weak internal pullup resistors to V_L. These inputs can be read by sampling bits 7 through 4 of the IOPINS (R20) register. Writing to GPIN3 through GPIN0 has no effect. GPOUT3 through GPOUT0 are the general-purpose outputs. Update these outputs by writing to bits 3 through 0 of the IOPINS (R20) register. GPOUT3–GPOUT0 logic levels are referenced to the voltage on V_L. As shown in Figure 11, reading the state of a GPOUT3–GPOUT0 bit returns the state of the internal register bit, not the actual pin state. This is useful for doing read-modify-write operations to an output pin (such as blinking an LED), since the load on the output pin does not affect the register logic state.

GPX is a push-pull output with a 4-way multiplexer that selects its output signal. The logic level on GPX is referenced to V_L. The SPI master writes to the GPXB and GPXA bits of PINCTL (R17) register to select one of four internal signals as depicted in Table 3.

- **OPERATE:** This signal goes high when the MAX3420E is able to operate after a power-up or $\overline{RES}$ reset. OPERATE is the default GPX output.
- **VBUS_DET:** VBUS_DET is the VBCOMP comparator output. This allows the user to directly monitor the V_{BUS} status.
- **BUSACT:** USB BUS activity signal (active-high). This signal is active whenever there is traffic on the USB bus. The BUSACT signal is set whenever a SYNC field is detected. BUSACT goes low during bus reset or after 32-bit times of J-state.
- **SOF:** A square wave with a positive edge that indicates the USB start-of-frame (Figure 12).

Table 3. GPX Output State

GPXB	GPXA	GPX PIN OUTPUT
0	0	OPERATE (Default State)
0	1	VBUS_DET
1	0	BUSACT
1	1	SOF

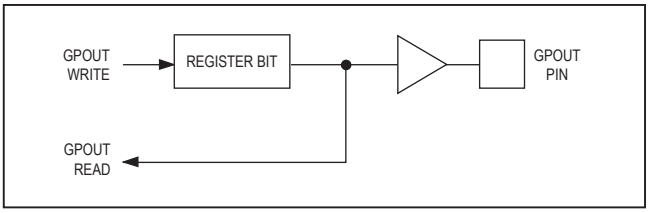


Figure 11. Behavior of Read and Write Operations on GPOUT3–GPOUT0

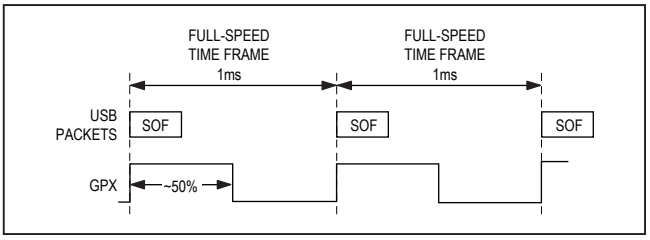


Figure 12. GPX Output in SOF Mode

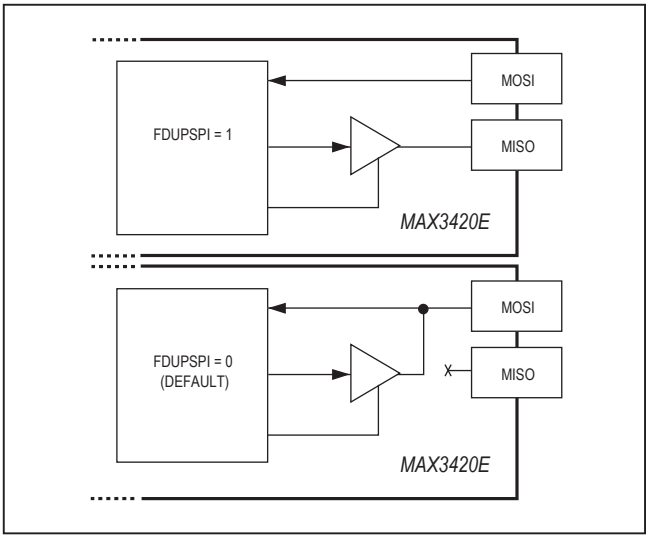


Figure 13. MAX3420E SPI Data Pins for Full-Duplex (Top) and Half-Duplex (Bottom) Operation

MOSI (Master-Out, Slave-In) and MISO (Master-In, Slave-Out)

The SPI data pins MOSI and MISO operate differently depending on the setting of a register bit called FDUPSPI (full-duplex SPI). Figure 13 shows the two configurations according to the FDUPSPI bit setting.

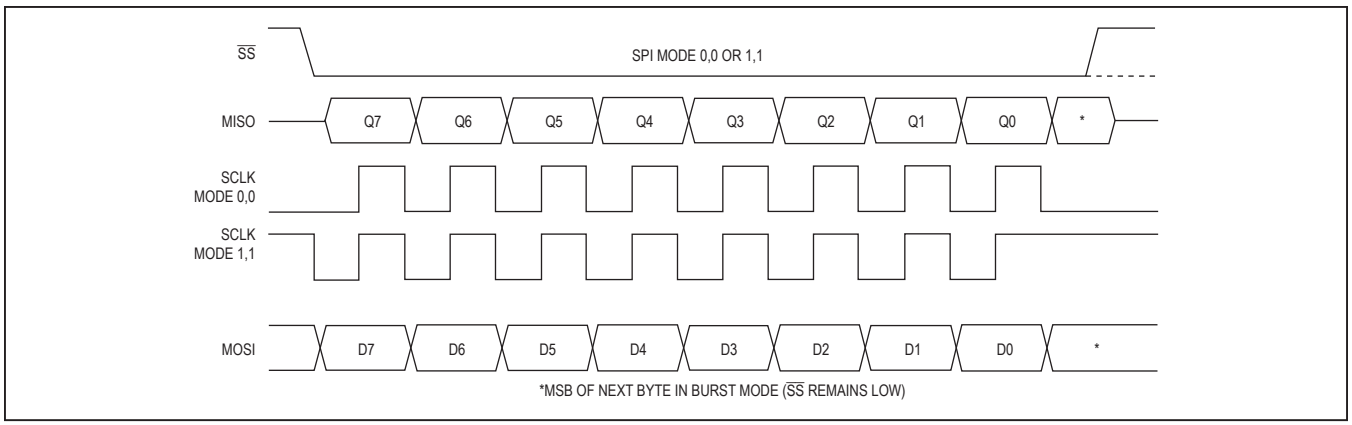


Figure 14. SPI Clocking Modes

In full-duplex mode (FDUPSPI = 1), the MOSI and MISO pins are separate, and the MISO pin drives only when $\overline{SS}$ is low. In this mode, the first eight SCLK edges (after $\overline{SS}$ = 0) clock the command byte into the MAX3420E on MOSI, and eight USB status bits are clocked out of the MAX3420E on MISO. For an SPI write cycle, any bytes following the command byte are clocked into the MAX3420E on MOSI, and zeros are clocked out on MISO. For an SPI read cycle, any bytes following the command byte are clocked out of the MAX3420E on MISO and the data on MOSI is ignored. At the conclusion of the SPI cycle ($\overline{SS}$ = 1), the MISO output three-states.

In half-duplex mode, the MOSI pin is a bidirectional pin and the MISO pin is three-stated. This saves a pin in the SPI interface. Because of the shared data pin, this mode does not offer the eight USB status bits (Figure 5) as the command byte is clocked into the MAX3420E. The MISO pin can be left unconnected in half-duplex mode.

SCLK (Serial Clock)

The SPI master provides the MAX3420E SCLK signal to clock the SPI interface. SCLK has no low-frequency limit, and can be as high as 26MHz. The MAX3420E changes its output data (MISO) on the falling edge of SCLK and samples input data (MOSI) on the rising edge of SCLK. The MAX3420E ignores SCLK transitions when $\overline{SS}$ is high. The inactive level of SCLK may be low or high, depending on the SPI operating mode (Figure 14).

$\overline{SS}$ (Slave Select)

The MAX3420E SPI interface is active only when $\overline{SS}$ is low. When $\overline{SS}$ is high, the MAX3420E three-states the SPI output pin and resets the internal MAX3420E SPI logic.

If $\overline{SS}$ goes high before a complete byte is clocked in, the byte-in-progress is discarded. The SPI master can terminate an SPI cycle after clocking in the first 8 bits (the command byte). This feature can be used in a full-duplex system to retrieve the USB status bits (Figure 5) without sending or receiving SPI data.

Applications Information

SPI Interface

The MAX3420E operates as an SPI slave device. A register access consists of the SPI master first writing an SPI command byte, followed by reading or writing the contents of the addressed register (see the *Register Description* section for more details). All SPI transfers are MSB first. The external SPI master provides a clock signal to the MAX3420E SCLK input. This clock frequency can be between DC and 26MHz. Bit transfers occur on the positive edge of SCLK. The MAX3420E counts bits and divides them into bytes. If fewer than 8 bits are clocked into the MAX3420E when $\overline{SS}$ goes high, the MAX3420E discards the partial byte.

The MAX3420E SPI interface operates without adjustment in either SPI mode (CPOL = 0, CPHA = 0) or (CPOL = 1, CPHA = 1). No mode bit is required to select between the two modes since the interface uses the rising edge of the clock in both modes. The two clocking modes are illustrated in Figure 14. Note that the inactive SCLK value is different for the two modes. Figure 14 illustrates the full-duplex mode, where data is simultaneously clocked into and out of the MAX3420E.

SPI Half- and Full-Duplex Operation

The MAX3420E can be programmed to operate in half-duplex (a bidirectional data pin) or full-duplex (one data-in and one data-out pin) mode. The SPI master sets a register bit called FDUPSPI (full-duplex SPI) to 1 for full-duplex, and 0 for half-duplex operation. Half-duplex is the power-on default.

Full-Duplex Operation

When the SPI master sets FDUPSPI = 1, the SPI interface uses separate data pins, MOSI and MISO to transfer data. Because of the separate data pins, bits can be simultaneously clocked into and out of the MAX3420E. The MAX3420E makes use of this feature by clocking out 8 USB status bits as the command byte is clocked in, as illustrated in Figure 15.

Reading from the SPI Slave Interface (MISO) in Full-Duplex Mode

In full-duplex mode the SPI master reads data from the MAX3420E slave interface using the following steps:

(1) When $\overline{SS}$ is high, the MAX3420E is unselected and three-states the MISO output.

(2) After driving SCLK to its inactive state, the SPI master selects the MAX3420E by driving $\overline{SS}$ low. The MAX3420E turns on its MISO output buffer and places the first data bit (Q7) on the MISO output (Figure 14).

(3) The SPI master simultaneously clocks the command byte into the MAX3420E MOSI pin, and USB status bits out of the MAX3420E MISO pin on the rising edges of the SCLK it supplies. The MAX3420E changes its MISO output data on the falling-edges of SCLK.

(4) After eight clock cycles, the master can drive $\overline{SS}$ high to deselect the MAX3420E, causing it to three-state its MISO output. The falling edge of the clock puts the MSB of the next data byte in the sequence on the MISO output (Figure 14).

(5) By keeping $\overline{SS}$ low, the master clocks register data bytes out of the MAX3420E by continuing to supply SCLK pulses (burst mode). The master terminates the transfer by driving $\overline{SS}$ high. The master must ensure that SCLK is in its inactive state at the beginning of the next access (when it drives $\overline{SS}$ low). In full-duplex mode, the MAX3420E ignores data on MOSI while clocking data out on MISO.

Writing to the SPI Slave Interface (MOSI) in Full-Duplex Mode

In full-duplex mode, the SPI master writes data to the MAX3420E slave interface through the following steps:

(1) The SPI master sets the clock to its inactive state. While $\overline{SS}$ is high, the master can drive the MOSI pin.

(2) The SPI master selects the MAX3420E by driving $\overline{SS}$ low and placing the first data bit to write on the MOSI input.

(3) The SPI master simultaneously clocks the command byte into the MAX3420E and USB status bits out of the MAX3420E MISO pin on the rising edges of the SCLK it supplies. The SPI master changes its MOSI input data on the falling edges of SCLK.

(4) After eight clock cycles, the master can drive $\overline{SS}$ high to deselect the MAX3420E.

(5) By keeping $\overline{SS}$ low, the master clocks data bytes into the MAX3420E by continuing to supply SCLK pulses (burst mode). The master terminates the transfer by driving $\overline{SS}$ high. The master must ensure that SCLK is inactive at the beginning of the next access (when it drives $\overline{SS}$ low). In full-duplex mode, the MAX3420E outputs USB status bits on MISO during the first 8 bits (the command byte), and subsequently outputs zeroes on MISO as the SPI master clocks bytes into MOSI.

Half-Duplex Operation

The MAX3420E is put into half-duplex mode at power-on, or when the SPI master clears the FDUPSPI bit. In half-duplex mode, the MAX3420E three-states its MISO pin and makes the MOSI pin bidirectional, saving a pin in the SPI interface. The MISO pin can be left unconnected in half-duplex operation.

Because of the single data pin, the USB status bits available in full-duplex mode are not available as the SPI master clocks in the command byte. In half-duplex mode these status bits are accessed in the normal way, as register bits.

The SPI master must operate the MOSI pin as bidirectional. It accesses a MAX3420E register as follows:

(1) The SPI master sets the clock to its inactive state. While $\overline{SS}$ is high, the master can drive the MOSI pin to any value.

(2) The SPI master selects the MAX3420E by driving $\overline{SS}$ low and placing the first data bit (MSB) to write on the MOSI input.

(3) The SPI master turns on its output driver and clocks the command byte into the MAX3420E on the rising edges of the SCLK it supplies. The SPI master changes its MOSI data on the falling edges of SCLK.

(4) After eight clock cycles, the master can drive $\overline{SS}$ high to deselect the MAX3420E.

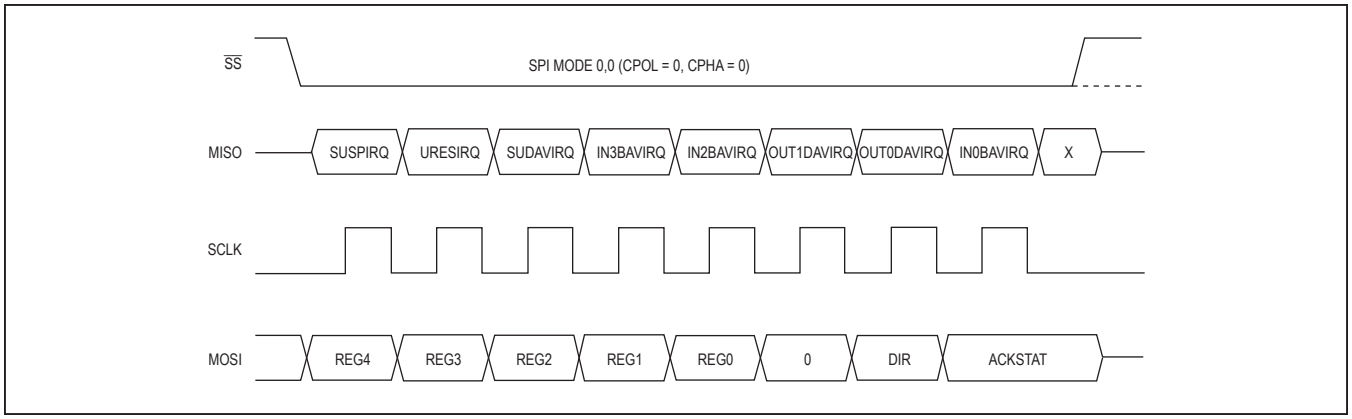


Figure 15. SPI Port in Full-Duplex Mode

(5) To write SPI data, the SPI master keeps its output driver on and clocks subsequent bytes into the MOSI pin. To read SPI data, after the eighth clock cycle the SPI master three-states its output driver and begins clocking in data bytes from the MOSI pin.

(6) The SPI master terminates the SPI cycle by returning $\overline{SS}$ high.

Figure 8 and Figure 9 show timing diagrams for full and half-duplex operation.

USB Serial-Interface Engine

The serial-interface engine (SIE) does most of the detailed work required by USB protocol:

- USB packet PID detection and checking
- CRC check and generation
- Automatic retries in case of errors
- USB packet generation
- NRZI data encoding and decoding
- Bit stuffing and unstuffing
- Various USB error condition detection
- USB bus reset, suspend, and wake-up detection
- USB resume signaling
- Automatic flow control (NAK)

PLL

An internal PLL multiplies the 12MHz oscillator signal by four to produce an internal 48MHz clock. When the chip is powered down, the oscillator is turned off to conserve power. When repowered, the oscillator and PLL require time to stabilize and lock. The OSCOKIRQ interrupt bit is used to indicate to the SPI master that the clocking system is stable and ready for operation.

Power Management

According to USB rev. 2.0 specification, when a USB host stops sending traffic for at least 3 milliseconds to a peripheral, the peripheral must enter a power-down state called SUSPEND. Once suspended, the peripheral must have enough of its internal logic active to recognize when the host resumes signaling, or if enabled for remote wakeup, that the SPI master wishes to signal a resume event. The following sections titled *Suspend* and *Wakeup and USB Resume* describe how the SPI master coordinates with the MAX3420E to accomplish this power management.

Suspend

After three milliseconds of USB bus inactivity, a USB peripheral is required to enter the USB suspend state and draw no more than 500µA of supply current. To accomplish this, after three milliseconds of USB bus inactivity, the MAX3420E sets the SUSPIRQ bit in the USBIRQ (R13) register and asserts the INT output, if SUSPIE = 1 and IE = 1. The SPI master must do any necessary power-saving housekeeping and then set the PWRDOWN bit in the USBCTL (R15) register. This instructs the MAX3420E to enter a power-down state, in which it does the following:

- Stops the 12MHz oscillator
- Keeps the INT output active (according to the mode set in the PINCTL (R17) register)
- Monitors the USB D+ line for bus activity
- Monitors the SPI port for any traffic

Note that the MAX3420E does not automatically enter a power-down state after three milliseconds of bus inactivity. This allows the SPI master to perform any preshutdown tasks before it requests the MAX3420E to enter the power-down state by setting PWRDOWN = 1.

Wakeup and USB Resume

The MAX3420E may wake up in three ways while it is in the power-down state:

(1) The SPI master clears the PWRDOWN bit in the USBCTL (R15) register (this is also achieved by a chip reset).

(2) The SPI master signals a USB remote wakeup by setting the SIGRWU bit in the USBCTL (R15) register. When SIGRWU = 1, the MAX3420E restarts the oscillator and waits for it to stabilize. After the oscillator stabilizes, the MAX3420E drives RESUME signaling (a 10ms K-state) on the bus. The MAX3420E times this interval to relieve the SPI master of having to keep accurate time. The MAX3420E also ensures that the RESUME signal begins only after at least 5ms of the bus idle state. When the MAX3420E finishes its RESUME signaling, it sets the RWUDNIRQ (remote-wakeup-done interrupt request) interrupt flag in the USBIRQ (R13) register. At this time the SPI master should clear the SIGRWU bit.

(3) The host resumes bus activity. To enable the MAX3420E to wake up from host signaling, the SPI master sets the HOSCSTEN (host oscillator start enable) bit of the USBCTL (R15) register. While in this mode, if the MAX3420E detects a 1 to 0 transition on D+, the MAX3420E restarts the oscillator and waits for it to stabilize.

Device Reset

The MAX3420E has three reset mechanisms:

- Power-On Reset. This is the most inclusive reset sets all internal register bits to a known state).
- Chip Reset. The SPI master can assert a chip reset by setting the bit CHIPRES = 1, which has the same effect as pulling the $\overline{RES}$ pin low. This reset clears only some register bits and leaves others alone.
- USB Bus Reset. A USB bus reset is the least inclusive (clears the smallest number of bits).

Power-On Reset

At power-on, all register bits except three are cleared. The following three bits are set to 1 to indicate that the IN FIFOs are available for loading by the SPI master (BAV = buffer available):

- IN3BAVIRQ
- IN2BAVIRQ
- IN0BAVIRQ

Chip Reset

Pulling the $\overline{RES}$ pin low or setting CHIPRES = 1 clears most of the bits that control USB operation, but keeps the SPI and pin-control bits unchanged so the interface between the SPI master and the MAX3420E is not disturbed. Specifically:

- CHIPRES is unchanged. If the SPI master asserted this reset by setting CHIPRES = 1, it removes the reset by writing CHIPRES = 0.
- CONNECT is unchanged, keeping the device connected if CONNECT = 1.
- The general-purpose outputs GPOUT3–GPOUT0 are unchanged, preventing output glitches.
- The GPX output selector (GPXB, GPXA) is unchanged.
- The bits that control the SPI interface are unchanged: FDUPSPI, INTLEVEL, and POSINT.
- The bits that control power-down and wakeup behavior are unchanged: HOSCSTEN, PWRDOWN, and SIGRWU.

All other bits except the three noted in the *Power-On Reset* section are cleared.

Note: The IRQ and IE bits are cleared using this reset. This means that firmware routines that enable interrupts should be called after a reset of this type.

USB Bus Reset

When the MAX3420E detects 21.33µs of SE0, it asserts the URESIRQ bit and clears certain bits. This reset is the least inclusive of the three resets. It maintains the bit states listed in the *Power-On Reset* and *Chip Reset* sections, plus it leaves the following bits in their previous states:

- Registers R0–R4 are unchanged. The actual data in the FIFOs is never cleared.
- The IE bit is unchanged.
- URESIE, URESIRQ, URESDNIE, and URESDNIRQ are unchanged, allowing the SPI master to check the state of USB bus resets.

As with the chip reset, most of the interrupt request and interrupt enable bits are cleared, meaning that the device firmware must reenable individual interrupts after a bus reset. The exceptions are the interrupts associated with the actual bus reset, allowing the SPI master to detect the beginning and end of the host signaling USB bus reset.

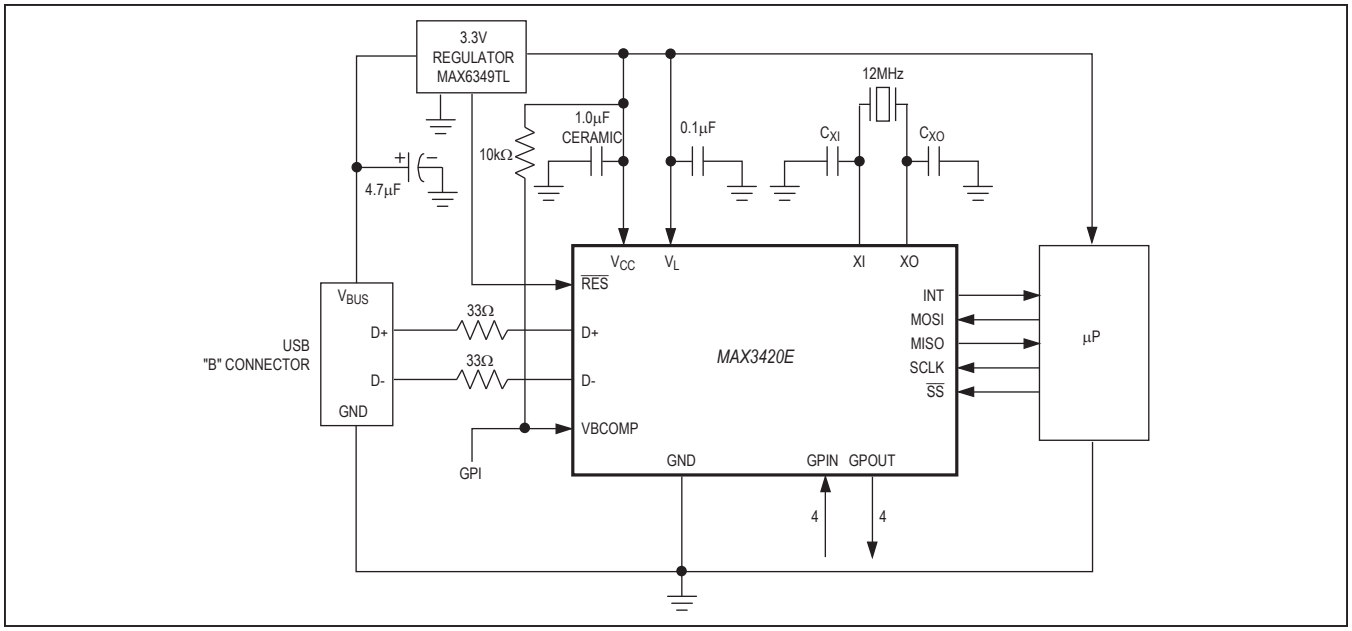


Figure 16. MAX3420E in a Bus-Powered Application

MAX3420E in a Bus-Powered Application

Figure 16 depicts the MAX3420E in a peripheral device that is powered by V_{BUS}. This configuration is advantageous because it requires no external power supply. V_{BUS} is specified from 4.75V to 5.25V, so a 3.3V regulator is required to power the MAX3420E. This diagram assumes that the microprocessor is powered by 3.3V as well, so the V_L pin (logic-level reference voltage) is connected to V_{CC}. Therefore, the GPIO (general-purpose inputs/outputs) are referenced to 3.3V.

USB is a hot-plug system (V_{BUS} is hot when the device is plugged in), so it is good design practice to use a power-on reset circuit to provide a clean reset to the system when the device is plugged in. The MAX6349TL serves as an excellent USB regulator, since it has very low quiescent current and a POR circuit built in.

Because this design is bus powered, it is not necessary to test for the presence of V_{BUS}. In this case, the bus voltage-detection input (VBCOMP) makes an excellent general-purpose input when pulled up to V_L. The VBCOMP input has two interrupts associated with it, VBUSIRQ and NOVBUSIRQ. These interrupts can detect both edges of any transitions on the VBCOMP input.

The configuration in Figure 16 shows the SPI interface using the maximum number of SPI interface pins. The data pins, MOSI and MISO, are separate, and the MAX3420E supplies an interrupt signal through the INT output pin to the µP to notify the µP when its attention is required.

MAX3420E in a Self-Powered Application

Figure 17 shows a self-powered design in which the µP has its own power source. This is a common configuration in battery-powered handheld devices. Figure 17 also illustrates the SPI interfacing with the minimum number of pins. This is achieved by using a single bidirectional data line and no interrupt pin connection. The MAX3420E register bit, FDUPSPI, configures the SPI interface for bidirectional operation.

Although Figure 17 shows $V_L = V_{CC}$, if the microcontroller uses a different interface voltage (1.71V to 3.6V) this reference voltage can be connected to V_L. Figure 17 shows a connection from the MAX3420E GPX output to the microcontroller. GPX can be programmed (see Table 3) to connect the output of the internal V_{BUS} comparator to the GPX output. This enables the microprocessor to detect a USB plug-in event even if the MAX3420E is put into its power-down state.

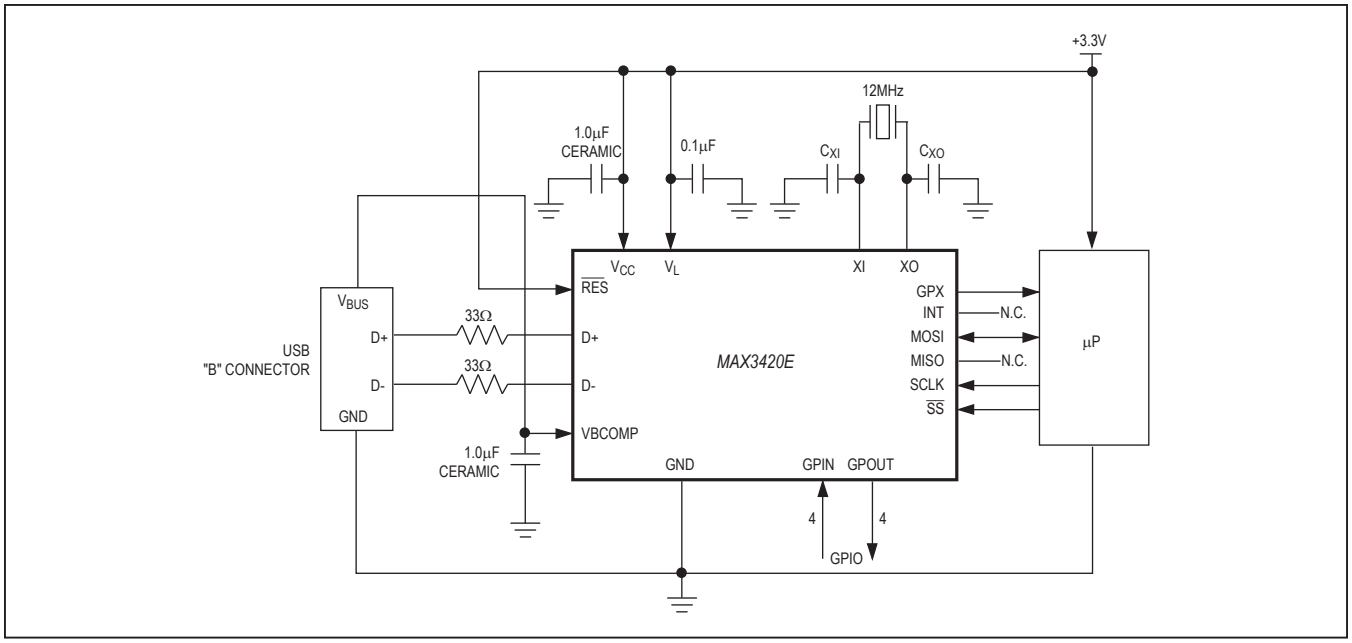


Figure 17. MAX3420E in a Self-Powered Application

The V_{BUS} detect input, VBCOMP, is an important MAX3420E feature. Because the µP is powered whether the USB device is plugged in or not, it needs some way to detect a plug-in event. A comparator inside the MAX3420E checks for a valid V_{BUS} connection on VBCOMP and provides a connect status bit to the µP. Once connected, the µP can delay the logical connection to the USB bus to perform any required initialization, and then connect by setting the CONNECT bit to 1 in the MAX3420E register USBCTL (R15). This connects the internal 1.5kΩ resistor from D+ to V_{CC}, to signal the host that a device has been plugged in.

If a host turns off V_{BUS} while the device is connected, the USB rev. 2.0 specification requires that the device must not power its 1.5kΩ pullup resistor connected to D+. The MAX3420E has two features to help service this event. First, the NOVBUSIRQ bit indicates the loss of VBUS. Second, the µP can set a bit called VBGATE (V_{BUS} gate) to instruct the MAX3420E to disconnect the pullup resistor anytime V_{BUS} goes away, regardless of the CONNECT bit setting.

Crystal Selection

The MAX3420E requires a crystal with the following specifications:

Frequency: 12MHz ±0.25%

C_{LOAD}: 18pF

C_O: 7pF max

Drive level: 200µW

Series resonance resistance: 60Ω max

Note: Series resonance resistance is the resistance observed when the resonator is in the series resonant condition. This is a parameter often stated by quartz crystal vendors and is called R1. When a resonator is used in the parallel resonant mode with an external load capacitance, as is the case with the MAX3420E oscillator circuit, the effective resistance is sometimes stated. This effective resistance at the loaded frequency of oscillation is:

$$R1 \times (1 + (C_O / C_{LOAD}))^2$$

For typical C_O and C_{LOAD} values, the effective resistance can be greater than R1 by a factor of 2.

ESD Protection

D+, D-, and VBCOMP possess extra protection against static electricity to protect the devices up to ±15kV. The ESD structures withstand high ESD in all operating modes: normal operation, suspend mode, and powered down. VBCOMP and V_{CC} require 1µF ceramic capacitors connected to ground as close to the pins as possible. D+, D-, and VBCOMP provide protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2
- ±12kV using the IEC 61000-4-2 Air Gap Method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 18 shows the Human Body Model, and Figure 19 shows the current waveform generated when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which then discharges into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 20 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. The Air-Gap Discharge test involves approaching the device with a charged probe.

Short-Circuit Protection

The MAX3420E withstands V_{BUS} shorts to D+ and D- on the USB connector side of the 33Ω series resistors.

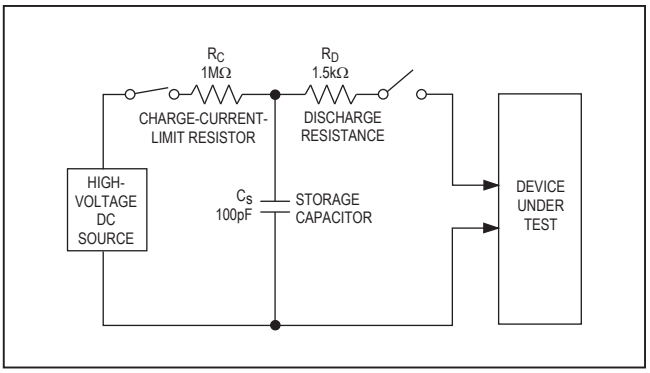


Figure 18. Human Body ESD Test Models

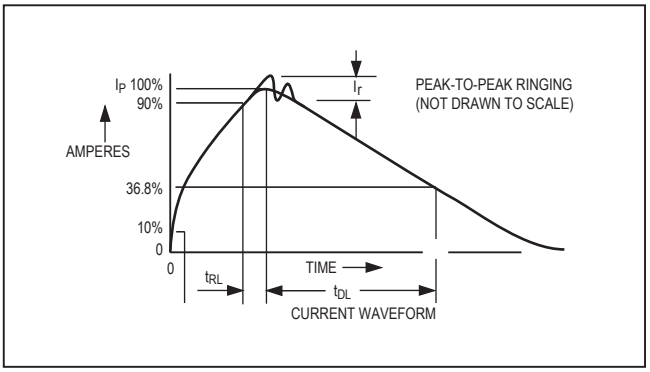


Figure 19. Human Body Model Current Waveform

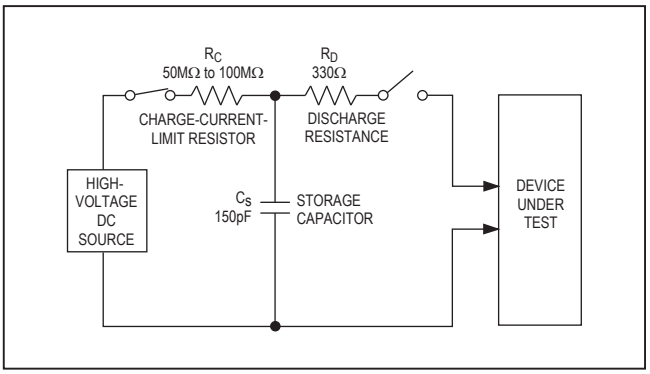


Figure 20. IEC 61000-4-2 ESD Test Model

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3420EETG+	-40°C to +85°C	24 TQFN-EP*
MAX3420EECJ+	-40°C to +85°C	32 LQFP
MAX3420EECJ/V+	-40°C to +85°C	32 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP*	T2444+4	**21-0139**	**90-0022**
32 LQFP	C32+1	**21-0054**	**90-0111**

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	6/07	Various changes	4, 5, 19, 20, 22, 23, 24, 25
3	12/10	Added the MAX3420EECJ/V+ part number to the Ordering Information	1
4	2/15	Added the *Benefits and Features* section	1
5	11/15	SCLK Fall to MISO Propagation Delay and SCLK Fall to MOSI Propagation Delay specifications updated in *Electrical Characteristics* table	10
6	3/16	Updated package types and package codes in *Ordering Information* table	21

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