19-5930; Rev 1; 1/12

EVALUATION KIT AVAILABLE

MAX34406

Quad Current-Sense Amplifier with Overcurrent Threshold Comparators

General Description

The MAX34406 is a quad, high-side, unidirectional, current-sense amplifier that offers precision accuracy. It provides analog outputs for each of the four amplifiers that can be routed to an external ADC, and contains four overcurrent comparators with a fixed 1.0V threshold. All four comparators are logically ORed, and the result can be delayed/filtered with an external capacitor before it is fed to a latched common shutdown open-drain output pin.

Applications

Network Switches/Routers

Base Stations

Servers

Smart Grid Network Systems

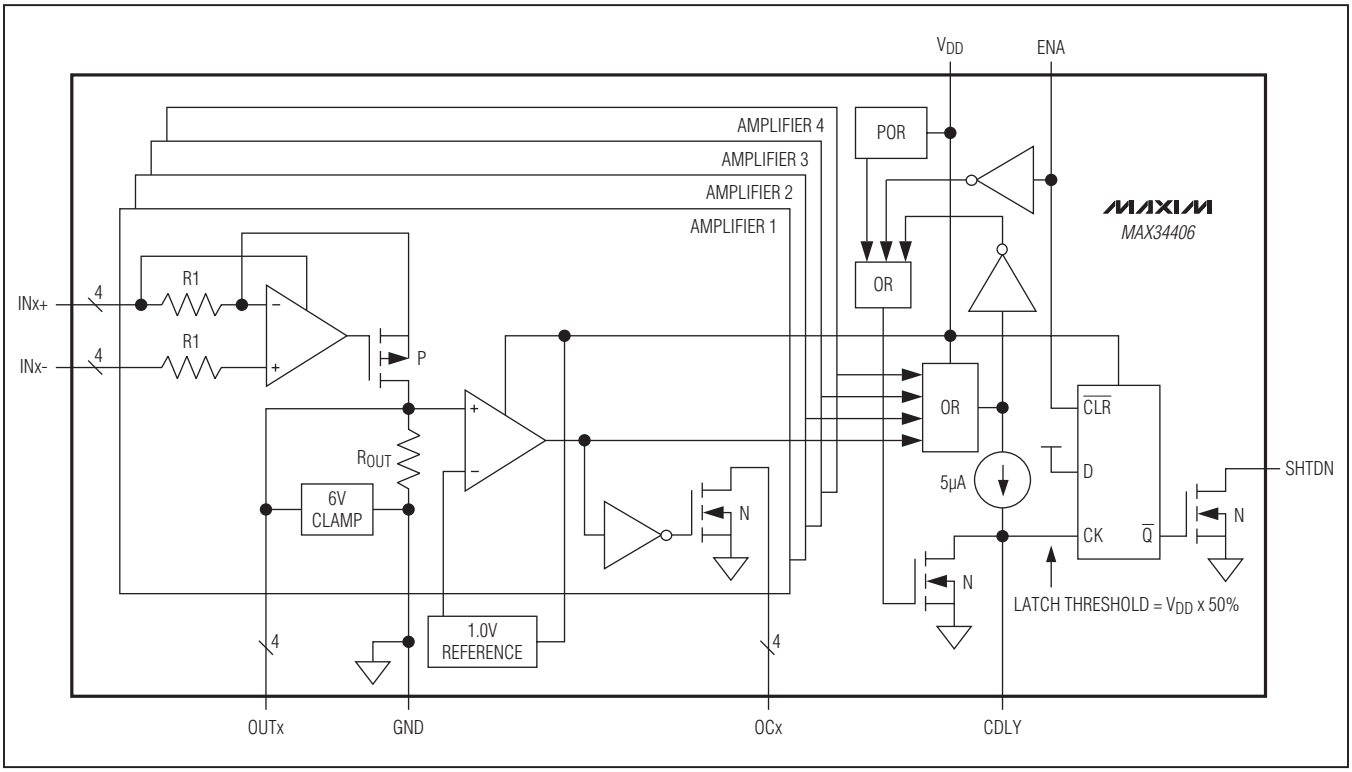
Industrial Controls

Features

- **Four Precision Current-Sense Amplifiers**
- **Fixed Gains of 25V/V, 50V/V, 100V/V, and 200V/V**
- **Less Than ±600µV of Input Offset**
- **Less Than ±0.6% of Gain Error (T/F/H) or ±0.8% of Gain Error (W)**
- **Wide 2.0V to 28V Common Mode Range**
- **Analog Voltage Outputs for Each Amplifier**
- **Independent Overcurrent Comparators with Fixed 1.0V Threshold**
- **Low Power Consumption**
- **-40°C to +85°C Temperature Range**
- **Small 24-Pin TQFN (4mm x 4mm) Package**

***Ordering Information** appears at end of data sheet.*

Block Diagram



*For related parts and recommended products to use with this part, refer to: **www.maxim-ic.com/MAX34406.related***

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on INx+ and INx- Relative to GND ..... -0.3V to +30V
Voltage Range on V_{DD} Relative to GND ..... -0.3V to +6V
Voltage Range on Remaining Pins Relative to GND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C) 2222.2mW

OUT1, OUT2, OUT3, OUT4 Short Circuit to GND .... Continuous
Operating Junction Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{INx+} = V_{INx-} = 12V, V_{SENSE} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Operating Range	V_{DD}			2.7		5.5	V
V_{DD} Supply Current	I_{DD}	(Note 2)				200	µA
Common-Mode Input Range	V_{CM}	Guaranteed by CMRR		2.0		28	V
Common-Mode Rejection Ratio	CMRR	V_{INx+} > 2.0V at T_A = +25°C		86	120		dB
Input Offset Voltage	V_{OS}	(Note 3)			±100	±600	µV
Gain (0.5V < V_{OUTx} < 1.5V)	G	MAX34406T			25		V/V
		MAX34406F			50		
		MAX34406H			100		
		MAX34406W			200		
Gain Error	GE	MAX34406T/F/H	(Note 4)			±0.6	%
		MAX34406W				±0.8	
OUTx Output Resistance	R_{OUTx}	MAX34406T/F/H	(Note 5)		10		kΩ
		MAX34406W			20		
OUTx Low Voltage	V_{OL}	MAX34406T				15	mV
		MAX34406F				30	
		MAX34406H				60	
		MAX34406W				120	
Bandwidth	BW	MAX34406T	V_{OUTx} = 2.0V (Note 5)		125		kHz
		MAX34406F			60		
		MAX34406H			30		
		MAX34406W			15		
ENA Input Logic-High	V_{IH}			V_{DD} x 0.7		V_{DD} + 0.3	V
ENA Input Logic-Low	V_{IL}			V_{GND} - 0.3		V_{DD} x 0.3	V
ENA Input Leakage						±1	µA
Output Logic-Low (SHTDN, OCx)	V_{OL}	I_{OL} = 2mA				0.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{INx+} = V_{INx-} = 12V, V_{SENSE} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C) (Note 1)x

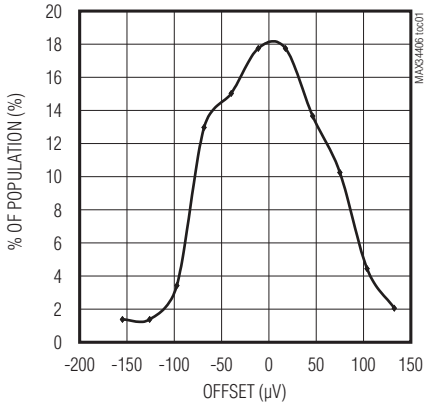
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage (SHTDN, OCx)	I_O				±1	µA
Comparator Threshold	V_{TH}		0.98	1.00	1.02	V
Comparator Offset	V_{COS}				±5	mV
Comparator Hysteresis	V_{HYS}			20		mV
Comparator Propagation Delay	t_D	Overdrive = ±50mV, output load = 2mA		3		µs
SHTDN Delay	t_{DLY}	V_{DD} = 3.3V, C_{CDLY} = 10nF		3.3		ms
		V_{DD} = 3.3V, C_{CDLY} = 22nF		7.3		
		V_{DD} = 3.3V, C_{CDLY} = 33nF		11		
		V_{DD} = 5.0V, C_{CDLY} = 10nF		5		
		V_{DD} = 5.0V, C_{CDLY} = 22nF		11		
		V_{DD} = 5.0V, C_{CDLY} = 33nF		16		

Note 1: All devices are 100% production tested at T_A= +25°C. All temperature limits are guaranteed by design.
Note 2: V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4} = 0V. All open-drain outputs left disconnected.
Note 3: V_{OS} is extrapolated from measurements for the gain-error test.
Note 4: Gain error is calculated by applying two values of V_{SENSE} and calculating the error of the slope vs. the ideal: Gain = 100, V_{SENSE} is 5mV and 15mV.
Note 5: The device is stable for any external capacitance value.

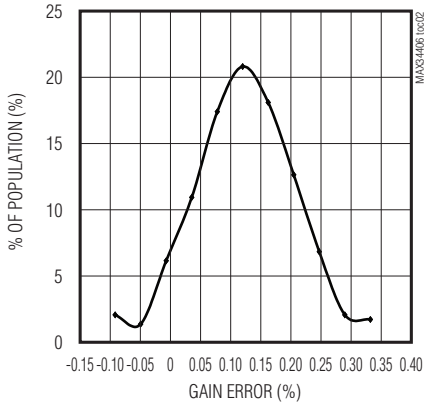
Typical Operating Characteristics

(V_{INx+} = V_{INx-} = 12V, T_A = +25°C, unless otherwise noted.)

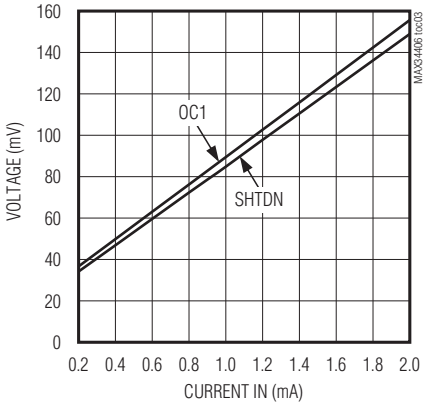
+25°C INPUT OFFSET



+25°C GAIN ERROR



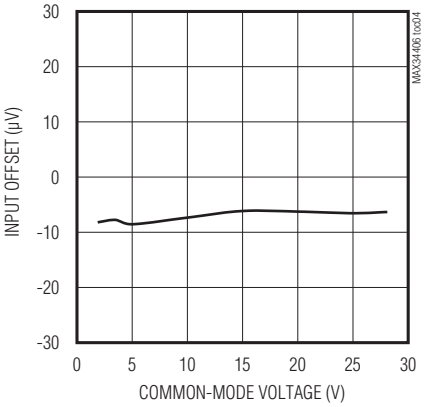
V_{OL} vs. I_{OL}



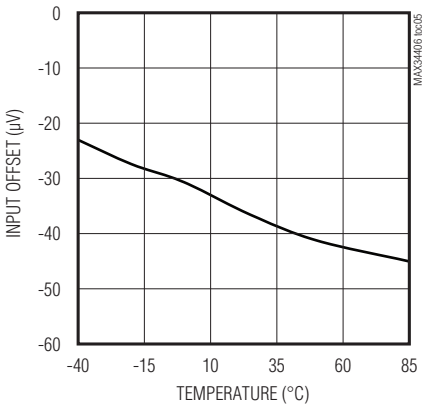
Typical Operating Characteristics (continued)

($(V_{INx+} = V_{INx-} = 12V, T_A = +25°C$, unless otherwise noted.)

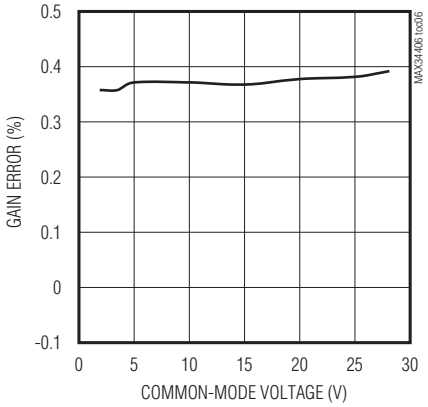
INPUT OFFSET vs. COMMON-MODE VOLTAGE



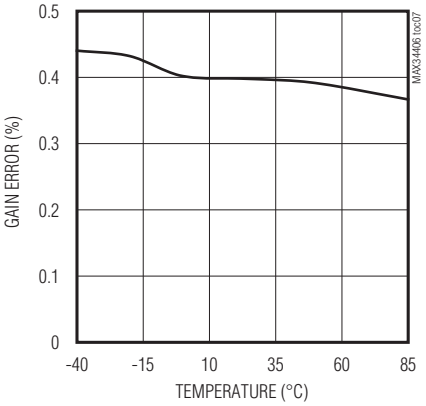
INPUT OFFSET vs. TEMPERATURE



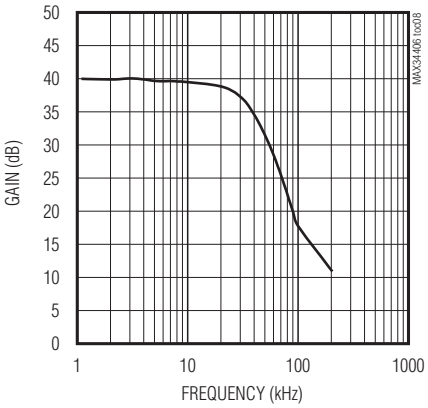
GAIN ERROR vs. COMMON-MODE VOLTAGE



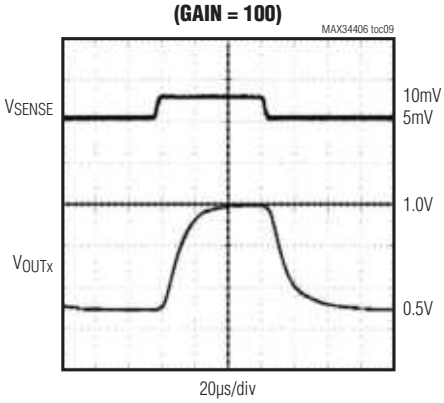
GAIN ERROR vs. TEMPERATURE



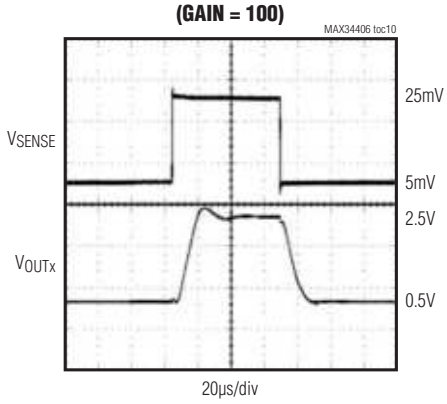
SMALL-SIGNAL GAIN vs. FREQUENCY (GAIN = 100)



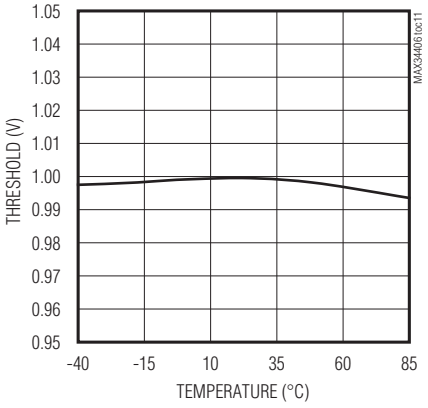
SMALL-SIGNAL PULSE RESPONSE (GAIN = 100)



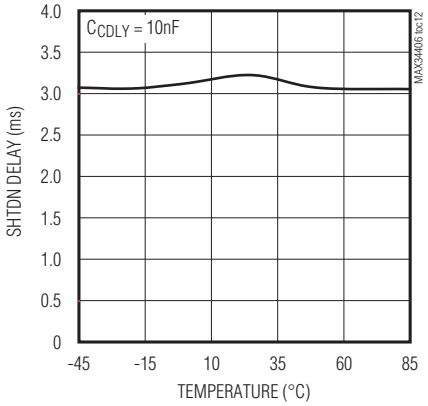
LARGE-SIGNAL PULSE RESPONSE (GAIN = 100)



COMPARATOR THRESHOLD vs. TEMPERATURE

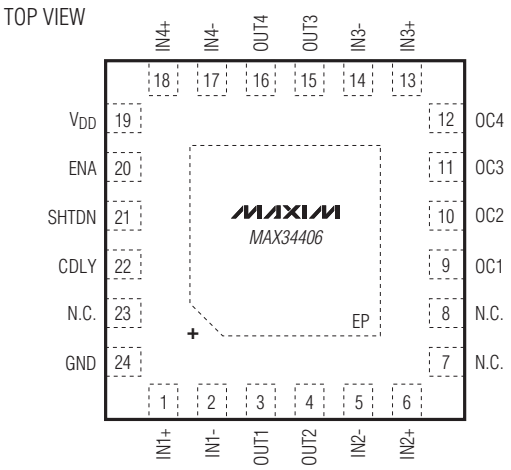


SHTDN DELAY vs. TEMPERATURE



Quad Current-Sense Amplifier with Overcurrent Threshold Comparators

Pin Configuration



TQFN
(4mm x 4mm)

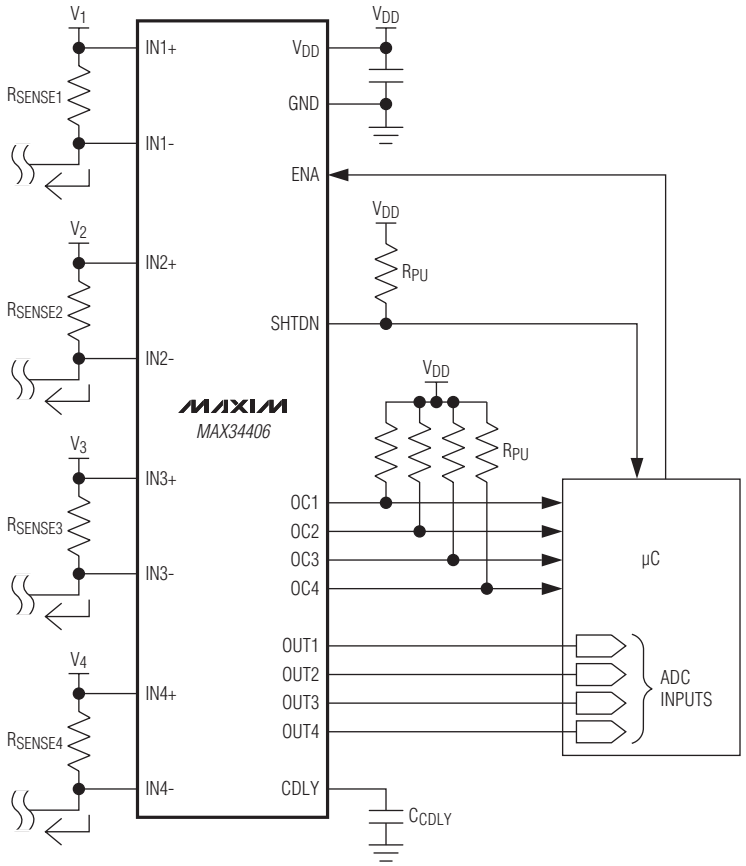
Pin Description

PIN	NAME	FUNCTION
1	IN1+	External Sense Resistor Power-Side Connection for Amplifier 1. Bias at this pin also provides the supply voltage for amplifier 1. This pin can be left open circuit if not needed.
2	IN1-	External Sense Resistor Load-Side Connection for Amplifier 1
3	OUT1	Output Voltage from Amplifier 1 Proportional to V_{SENSE}. This output is clamped at 6V.
4	OUT2	Output Voltage from Amplifier 2 Proportional to V_{SENSE}. This output is clamped at 6V.
5	IN2-	External Sense Resistor Load-Side Connection for Amplifier 2
6	IN2+	External Sense Resistor Power-Side Connection for Amplifier 2. Bias at this pin also provides the supply voltage for amplifier 2. This pin can be left open circuit if not needed.
7, 8, 23	N.C.	No Connection. Not internally connected.
9	OC1	Overcurrent Threshold Comparator Associated with Amplifier 1. Open-drain output. This output transitions to high impedance during an overcurrent event.
10	OC2	Overcurrent Threshold Comparator Associated with Amplifier 2. Open-drain output. This output transitions to high impedance during an overcurrent event.
11	OC3	Overcurrent Threshold Comparator Associated with Amplifier 3. Open-drain output. This output transitions to high impedance during an overcurrent event.
12	OC4	Overcurrent Threshold Comparator Associated with Amplifier 4. Open-drain output. This output transitions to high impedance during an overcurrent event.
13	IN3+	External Sense Resistor Power-Side Connection for Amplifier 3. Bias at this pin also provides the supply voltage for amplifier 3. This pin can be left open circuit if not needed.

Pin Description (continued)

PIN	NAME	FUNCTION
14	IN3-	External Sense Resistor Load-Side Connection for Amplifier 3
15	OUT3	Output Voltage from Amplifier 3 Proportional to V_{SENSE}. This output is clamped at 6V.
16	OUT4	Output Voltage from Amplifier 4 Proportional to V_{SENSE}. This output is clamped at 6V.
17	IN4-	External Sense Resistor Load-Side Connection for Amplifier 4
18	IN4+	External Sense Resistor Power-Side Connection for Amplifier 4. Bias at this pin also provides the supply voltage for amplifier 4. This pin can be left open circuit if not needed.
19	V_{DD}	Supply Voltage for Reference, Comparators, and Logic. A +2.7V to +5.5V supply. This pin should be decoupled to GND with a 100nF ceramic capacitor.
20	ENA	SHTDN Enable Input. CMOS digital input. Connect to GND to clear the latch and unconditionally deassert (force low) the SHTDN output. Connect to V_{DD} to enable normal latch operation of the SHTDN output. ENA should be toggled low once V_{DD} reaches nominal operating voltage.
21	SHTDN	Shutdown Output. Open-drain output. This output transitions to high impedance when any of the four overcurrent comparator outputs (OC1 to OC4) are asserted (high impedance) as long as the ENA pin is high. Toggling the ENA pin allows SHTDN to reset to logic-low.
22	CDLY	Shutdown Delay Capacitor. A capacitor (C_{CDLY}) from this pin to GND delays the transition of the SHTDN pin. The delay time can be calculated by the following formula: $t_{DLY} = C_{CDLY} \times (V_{DD}/10\mu A)$. The capacitor connected to CDLY is discharged when ENA is low and upon V_{DD} being applied (i.e., at power-on reset), and also any time all OCx outputs are low (i.e., inactive). If the shutdown delay is not required, this pin can be left unconnected.
24	GND	Ground Reference
—	EP	Exposed Pad. Connect to ground or leave unconnected.

Typical Application Circuit



Detailed Description

The MAX34406 quad-channel, unidirectional, high-side, current-sense amplifier features a 2.0V to 28V input common-mode range. This feature allows the monitoring of current out of a voltage supply as low as 2.0V. The device monitors current through a current-sense resistor and amplifies the voltage across that resistor.

Current-sense amplifier output voltages (OUT1 to OUT4) are compared to a fixed 1.0V reference; if V_{OUTx} exceeds 1.0V, the corresponding overcurrent warning output (OC1 to OC4) is asserted. If the enable input (ENA) is logic-high, SHTDN asserts when any of the four overcurrent outputs go logic-high. Assertion of SHTDN on overcurrent can be delayed and/or filtered by attaching an external capacitor to CDLY. Once SHTDN is latched high impedance, it remains so until ENA is toggled.

The unidirectional current-sense amplifiers used in each channel of the device have a well established history. For each channel, an op amp is used to force the current through an internal gain resistor at IN+, which has a value of R1, such that its voltage drop equals the voltage drop across an external sense resistor, R_{SENSE}. There is an internal resistor at IN- with the same value as R1 to minimize offset voltage. The current through R1 is sourced by a high-voltage p-channel FET. Its source current is the same as its drain current, which flows through a second gain resistor, R_{OUTx}. This produces an output voltage, V_{OUTx}, whose magnitude is $I_{LOAD} \times R_{SENSE} \times R_{OUTx}/R1$. The gain accuracy is based on the matching of the two gain resistors, R1 and R_{OUTx} (Table 1). Total gain = 25V/V for the MAX34406T, 50V/V for the MAX34406F, 100V/V for the MAX34406H, and 200V/V for the MAX34406W. The output is protected from input overdrive by use of a 6V clamp-protection circuit.

Table 1. Internal Gain Setting Resistors (Typical Values)

GAIN (V/V)	R1 (Ω)	R_{OUTx} (kΩ)
200	100	20
100	100	10
50	200	10
25	400	10

Applications Information

Choosing the Sense Resistor

Choose R_{SENSE} based on the criteria detailed in the following sections.

Voltage Loss

A high R_{SENSE} value causes the power-source voltage to drop due to IR loss. For minimal voltage loss, use the lowest R_{SENSE} value.

OUTx Swing vs. V_{INx+} and V_{SENSE}

The device is unique because the supply voltage for the current-sense amplifier in each channel is the input common-mode voltage for that channel (the average voltage at INx+ and INx-). There are no separate supply voltage pins for the current-sense amplifiers. Therefore, the OUTx voltage swing for a given channel is limited by the minimum voltage at IN+ for that channel.

$$V_{OUTx(MAX)} = V_{INx+(MIN)} - V_{SENSE(MAX)} - V_{OH}$$

and

$$R_{SENSE} = \frac{V_{OUTx}(MAX)}{G \times I_{LOAD}(MAX)}$$

V_{SENSE} full scale should be less than V_{OUTx}/gain at the minimum INx+ voltage. For best performance with a 3.6V supply voltage, select R_{SENSE} to provide approximately 120mV (gain of 25V/V), 60mV (gain of 50V/V), 30mV (gain of 100V/V), or 15mV (gain of 200V/V) of sense voltage for the full-scale current in each application. These can be increased by use of a higher minimum input voltage.

Accuracy

In the linear region ($V_{OUTx} < V_{OUTx(MAX)}$), there are two components to accuracy: input offset voltage (V_{OS}) and gain error (GE). For all variants of the device, $V_{OS} = \leq$ 600µV (max); gain error is 0.6% (max) for the MAX34406T/F/H or 0.8% (max) for the MAX34406W. Use the linear equation to calculate total error:

$$\text{Error (\%)} = GE \pm \left(\frac{V_{OS}}{V_{SENSE}} \right) \times 100$$

where GE is gain error, V_{SENSE} is the voltage across the sense resistor R_{SENSE}, and V_{OS} is offset voltage. A high R_{SENSE} value allows lower currents to be measured more accurately because offsets are less significant when the sense voltage is larger.

Efficiency and Power Dissipation

At high current levels, the I^2R losses in R_{SENSE} can be significant. Take this into consideration when choosing the resistor value and its power dissipation (wattage) rating. Also, the sense resistor's value might drift if it is allowed to heat up excessively. The precision V_{OS} of the device allows the use of small sense resistors to reduce power dissipation and reduce hot spots.

Kelvin Connections

Because of the high currents that flow through R_{SENSE}, take care to eliminate parasitic trace resistance from causing errors in the sense voltage. Either use a four-terminal current-sense resistor or use Kelvin (force and sense) PCB layout techniques.

Minimizing Trace Resistance

PCB trace resistance from R_{SENSE} to the INx+ inputs contributes to gain error in the current-sense amplifiers. Care should be taken to minimize this resistance (shown as R_{TRC} in Figure 1). Total gain including error caused by trace resistance can be calculated as follows:

$$G = \frac{R_{OUTx}}{R1 + R_{TRC}}$$

For example, assume a gain of 100V/V, as in the MAX34406H. From Table 1, R1 = 100Ω and R_{OUTx} = 10kΩ. Then every 10mΩ of PCB trace resistance adds -0.01% gain error.

Optional Output Filter Capacitor

When designing a system that uses a sample-and-hold stage in the ADC, the sampling capacitor momentarily loads OUTx and causes a drop in the output voltage. If sampling time is very short (less than a microsecond), consider using a ceramic capacitor across OUTx and GND to hold V_{OUTx} constant during sampling. This also decreases the small-signal bandwidth of the current-sense amplifier and reduces noise at OUTx.

Input Filters

Some applications of current-sense amplifiers need to measure currents accurately even in the presence of both differential and common-mode ripple, as well as a wide variety of input transient conditions. For example, high-frequency ripple at the output of a switching buck or boost regulator results in a common-mode voltage at the device's inputs. Alternatively, the fast load-current transients, when measuring at the input of a switching buck or boost regulator, can cause high-frequency differential sense voltages to occur at the device's inputs, although the signal of interest is the average DC value. Such high-frequency differential sense voltages can result in a voltage offset at the device output.

The device allows a method of filtering to help improve performance in the presence of input common-mode voltage and input differential voltage transients. Figure 2 shows a differential input filter.

The capacitor C_{IN} between INx+ and INx- along with the resistor R_{IN} between the sense resistor and INx- helps filter against input differential voltages and prevents them from reaching the device.

The corner frequency of this filter is determined by the choice of R_{IN}, C_{IN}, and the value of the input resistance at INx- (R1). See Table 1 for R1 values at the different gain options.

The value of R_{IN} should be chosen to minimize its effect on the input offset voltage due to the bias current at INx-.

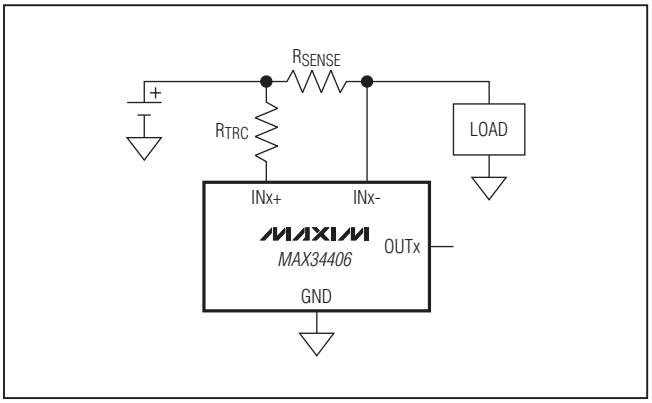


Figure 1. Input Trace Resistance

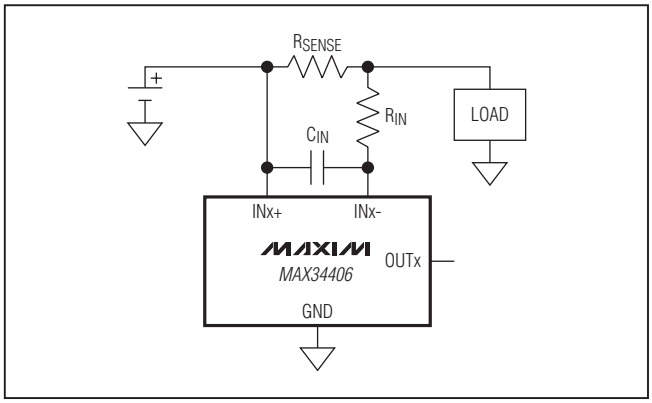


Figure 2. Differential Input Filter

R_{IN} x I_{BIAS} contributes to the input voltage offset. I_{BIAS} is typically 0.2µA.

Placing R_{IN} at the INx- input voltage does not affect the gain error of the device because the gain is given by the ratio between R_{OUTx} and R1 at INx+.

Bidirectional Application

Some systems can require a precise bidirectional current-sense amplifier to accurately monitor currents.

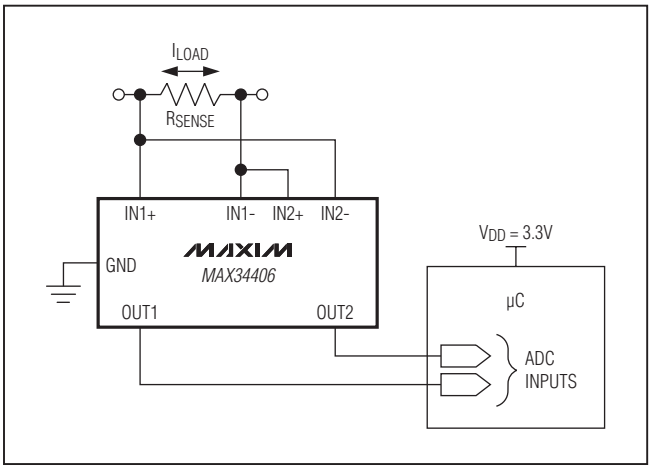


Figure 3. Bidirectional Application

Measurement of the two separate outputs with respect to GND yields an accurate measure of the bidirectional currents (Figure 3).

Choosing the Delay Capacitor

The SHTDN output asserts upon overcurrent detection on any of the 4 channels. OC1 to OC4 are logically ORed together; SHTDN latches the output after some delay. SHTDN latch delay is determined by the following equation:

$$t_{DLY} = C_{CDLY} \times (V_{DD} \div 10\mu A)$$

Example C_{CDLY} and t_{DLY} pairs are given in the *Electrical Characteristics* table.

Ordering Information

PART	GAIN (V/V)	TEMP RANGE	PIN-PACKAGE
MAX34406TETG+*	25	-40°C to +85°C	24 TQFN-EP**
MAX34406TETG+T*	25	-40°C to +85°C	24 TQFN-EP**
MAX34406FETG+*	50	-40°C to +85°C	24 TQFN-EP**
MAX34406FETG+T*	50	-40°C to +85°C	24 TQFN-EP**
MAX34406HETG+	100	-40°C to +85°C	24 TQFN-EP**
MAX34406HETG+T	100	-40°C to +85°C	24 TQFN-EP**
MAX34406WETG+*	200	-40°C to +85°C	24 TQFN-EP**
MAX34406WETG+T*	200	-40°C to +85°C	24 TQFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	1/12	Removed the requirement for the bleed resistor on CDLY; added the function to discharge the CDLY capacitor when all four OCx outputs are low (*Block Diagram*, *Electrical Characteristics* table t_{DLY} specification, *Pin Description*, *Typical Application Circuit*, and *Choosing the Delay Capacitor* section)	1, 3, 6, 7, 10

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