19-2166; Rev 2; 04/19

# Low-Jitter 155MHz/622MHz Clock Generator

MAX3670

## General Description

The MAX3670 is a low-jitter 155MHz/622MHz reference clock generator IC designed for system clock distribution and frequency synchronization in OC-48 and OC-192 SONET/SDH and WDM transmission systems. The MAX3670 integrates a phase/frequency detector, an operational amplifier (op amp), prescaler dividers and input/output buffers. Using an external VCO, the MAX3670 can be configured easily as a phase-lock loop with bandwidth programmable from 15Hz to 20kHz.

The MAX3670 operates from a single +3.3V or +5.0V supply, and dissipates 150mW (typ) at 3.3V. The operating temperature range is from -40°C to +85°C. The chip is available in a 5mm × 5mm, 32-pin QFN package.

## Applications

OC-12 to OC-192 SONET/WDM Transport Systems

Clock Jitter Clean-Up and Frequency Synchronization

Frequency Conversion

System Clock Distribution

## Features

- **Single +3.3V or +5.0V Supply**
- **Power Dissipation: 150mW at +3.3V Supply**
- **External VCO Center Frequencies ($f_{VCO}$): 155MHz to 670MHz**
- **Reference Clock Frequencies: $f_{VCO}$, $f_{VCO}/2$, $f_{VCO}/8$**
- **Main Clock Output Frequency: $f_{VCO}$**
- **Optional Output Clock Frequencies: $f_{VCO}$, $f_{VCO}/2$, $f_{VCO}/4$, $f_{VCO}/8$**
- **Low Intrinsic Jitter: < 0.4ps$_{RMS}$**
- **Loss-of-Lock Indicator**
- **PECL Clock Output Interface**

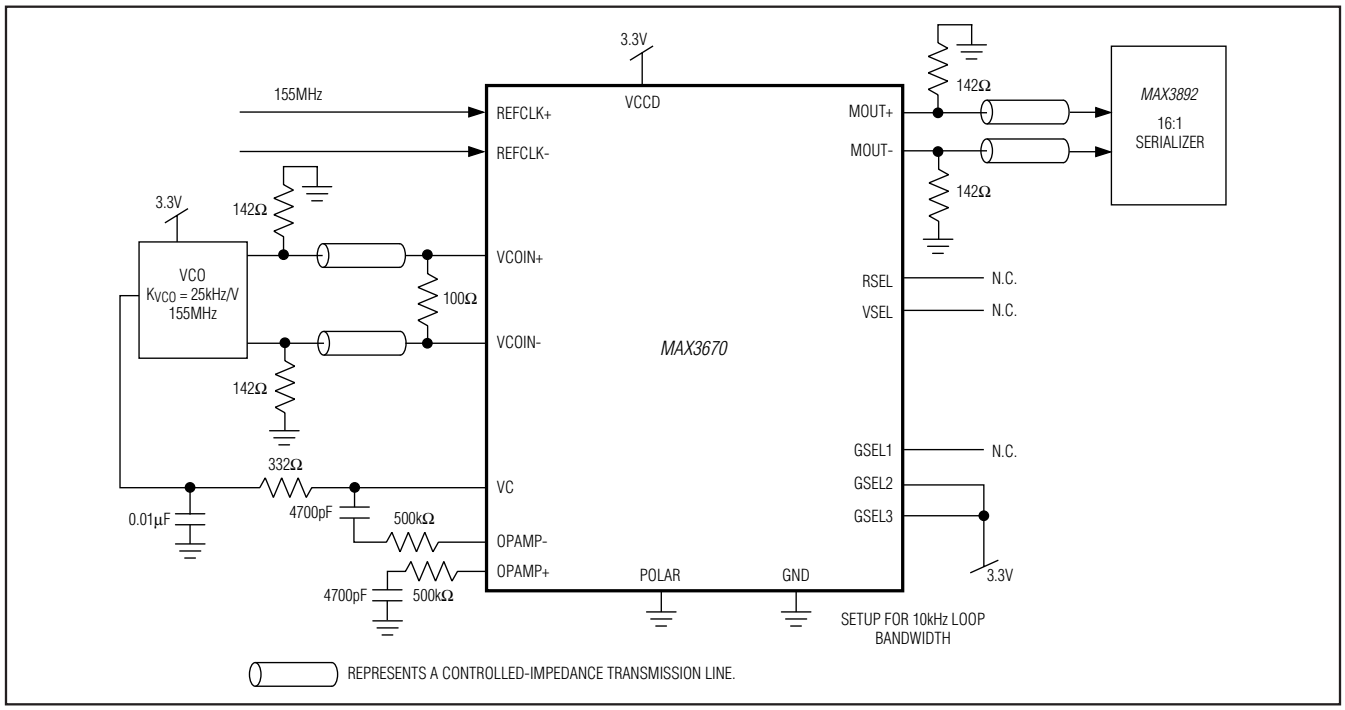
## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3670EGJ | -40°C to +85°C | 32 QFN-EP* |
| MAX3670ETJ2 | -40°C to +85°C | 32 Thin QFN-EP* |

*Suffix 2 denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*

***Pin Configuration appears at end of data sheet.***

## Typical Application Circuit



# Low-Jitter 155MHz/622MHz Clock Generator

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range.....-0.5V to +7V
Voltage Range at C2+, C2-, THADJ, CTH, GSEL1, GSEL2, GSEL3, LOL, RSEL, REFCLK-, REFCLK+, VSEL, VCOIN+, VCOIN-, VC, POLAR, PSEL1, PSEL2, COMP, OPAMP+, OPAMP- .....-0.5V to ($V_{CC}$ + 0.5V)
Continuous Power Dissipation ($T_A$ = +70°C)
32 QFN (derate 33.3mW/°C above +70°C) .....2.7W
32 Thin QFN (derate 34.5mW/°C above +70°C).....2.8W
PECL Output Current (MOUT+, MOUT-, POUT+, POUT-).....56mA
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range. .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.3V ±10% or $V_{CC}$ = +5.0V ±10%, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | (Note 2) | | 48 | 72 | mA |
| **INPUT SPECIFICATIONS** (REFCLK±, VCOIN±) | | | | | | |
| Input High Voltage | $V_{IH}$ | | $V_{CC}$ - 1.16 | | $V_{CC}$ - 0.88 | V |
| Input Low Voltage | $V_{IL}$ | | $V_{CC}$ - 1.81 | | $V_{CC}$ - 1.48 | V |
| Input Bias Voltage | | | | $V_{CC}$ - 1.3 | | V |
| Common-Mode Input Resistance | | | 7.5 | 11.5 | 17.5 | kΩ |
| Differential Input Resistance | | | 12.8 | 21.0 | 32.5 | kΩ |
| Differential Input Voltage Swing | | AC-coupled | 300 | | 1900 | mVp-p |
| **PECL OUTPUT SPECIFICATIONS** | | | | | | |
| Output High Voltage | $V_{OH}$ | 0°C to +85°C | $V_{CC}$ - 1.025 | | $V_{CC}$ - 0.88 | V |
| | | -40°C to 0°C | $V_{CC}$ - 1.085 | | $V_{CC}$ - 0.88 | |
| Output Low Voltage | $V_{OL}$ | 0°C to +85°C | $V_{CC}$ - 1.81 | | $V_{CC}$ - 1.62 | V |
| | | -40°C to 0°C | $V_{CC}$ - 1.83 | | $V_{CC}$ - 1.556 | |
| **TTL SPECIFICATIONS** | | | | | | |
| Output High Voltage | $V_{OH}$ | Sourcing 20µA | 2.4 | | $V_{CC}$ | V |
| Output Low Voltage | $V_{OL}$ | Sinking 2mA | | | 0.4 | V |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.3V ±10% or $V_{CC}$ = +5.0V ±10%, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OPERATIONAL AMPLIFIER SPECIFICATIONS** (Note 3) | | | | | | |
| Op Amp Output Voltage Range | $V_O$ | $V_{CC}$ = +3.3V ±10% | 0.3 | | $V_{CC}$ - 0.3 | V |
| | | $V_{CC}$ = +5.0V ±10% | 0.5 | | $V_{CC}$ - 0.5 | |
| Op Amp Input Offset Voltage | $\lvert V_{OS} \rvert$ | | | | 3 | mV |
| Op Amp Open-Loop Gain | $A_{OL}$ | | | 90 | | dB |
| **PHASE FREQUENCY DETECTOR (PFD)/CHARGE-PUMP (CP) SPECIFICATIONS** (Note 4) | | | | | | |
| Full-Scale PFD/CP Output Current | $\lvert I_{PD} \rvert$ | High gain | 16 | 20 | 24.4 | µA |
| | | Low gain | 4 | 5 | 6.2 | |
| PFD/CP Offset Current | | High gain | | | 0.80 | % $\lvert I_{PD} \rvert$ |
| | | Low gain | | | 1.08 | |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.3V ±10% or $V_{CC}$ = +5.0V ±10%, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CLOCK OUTPUT SPECIFICATIONS** | | | | | | |
| Clock Output Frequency | | | | | 670 | MHz |
| Optional Clock Output Frequency | | $f_{VCO}$ = 622MHz | | 622/311/ 155/78 | | MHz |
| | | $f_{VCO}$ = 155MHz | | 155/78/ 38/19 | | |
| Clock Output Rise/Fall Time | | Measured from 20% to 80% | | | 280 | ps |
| Clock Output Duty Cycle | | (Note 6) | 45 | | 55 | % |
| **NOISE SPECIFICATIONS** | | | | | | |
| Random Noise Voltage at Loop-Filter Output | $V_{NOISE}$ | Freq > 1kHz (Note 7) | | | 1.14 | $\mu V_{RMS}/\sqrt{Hz}$ |
| Spurious Noise Voltage at Loop-Filter Output | | (Note 8) | | 50 | | $\mu V_{RMS}$ |
| Power-Supply Rejection at Loop-Filter Output | PSR | (Note 9) | 30 | | | dB |
| **REFERENCE CLOCK INPUT SPECIFICATIONS** | | | | | | |
| Reference Clock Frequency | | | | 622/ 155/78 | 670 | MHz |
| Reference Clock Duty Cycle | | | 30 | | 70 | % |

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## AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.3V ±10% or $V_{CC}$ = +5.0V ±10%, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted.) (Note 5)

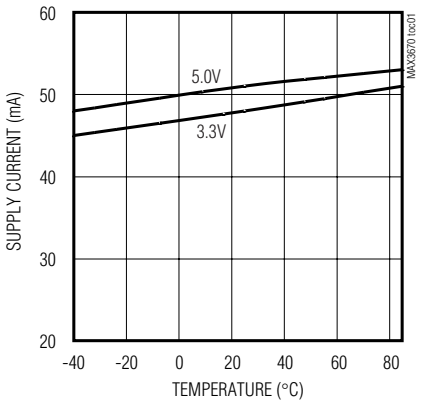
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PLL SPECIFICATIONS** | | | | | | |
| PLL Jitter Transfer Bandwidth | BW | (Note 10) | 15 | | 20,000 | Hz |
| Jitter Transfer Function | | $F_{JITTER} \le BW$ (Note 11) | | | 0.1 | dB |
| **OP AMP SPECIFICATION** | | | | | | |
| Unity-Gain Bandwidth | | | | 7 | | MHz |
| **VCO INPUT SPECIFICATION** | | | | | | |
| VCO Input Frequency | $f_{VCO}$ | | | 622/155 | 670 | MHz |
| VCO Input Slew Rate | | | 0.5 | | | V/ns |

**Note 1:** Specifications at -40°C are guaranteed by design and characterization.
**Note 2:** Measured with PECL outputs unterminated.
**Note 3:** OPAMP specifications met with 10kΩ load to ground or 5kΩ load to $V_{CC}$ (POLAR = 0 and POLAR = $V_{CC}$).
**Note 4:** PFD/CP currents are measured from pins OPAMP+ to OPAMP-. See Table 3 for gain settings.
**Note 5:** AC characteristics are guaranteed by design and characterization.
**Note 6:** Measured with 50% VCO input duty cycle.
**Note 7:** Random noise voltage at op amp output with 800kΩ resistor connected between VC and OPAMP-, PFD/CP gain ($K_{PD}$) = 5µA/UI, and POLAR = 0. Measured with the PLL open loop and no REFCLK or VCO input.
**Note 8:** Spurious noise voltage due to PFD/CP output pulses measured at op amp output with $R_1$ = 800kΩ, $K_{PD}$ = 5µA/UI, and compare frequency 400 times greater than the higher-order pole frequency (see *Design Procedure*).
**Note 9:** PSR measured with a 100mVp-p sine wave on $V_{CC}$ in a frequency range from 100Hz to 2MHz. External resistors $R_1$ matched to within 1%, external capacitors $C_1$ matched to within 10%. Measured closed loop with PLL bandwidth set to 200Hz.
**Note 10:** The PLL 3dB bandwidth is adjusted from 15Hz to 20kHz by changing external components $R_1$ and $C_1$, by selecting the internal programmable divider ratio and phase-detector gain. Measured with VCO gain of 220ppm/V and $C_1$ limited to 2.2µF.
**Note 11:** Measured at BW = 20kHz. When input jitter frequency is above PLL transfer bandwidth (BW), the jitter transfer function rolls off at -20dB/decade.

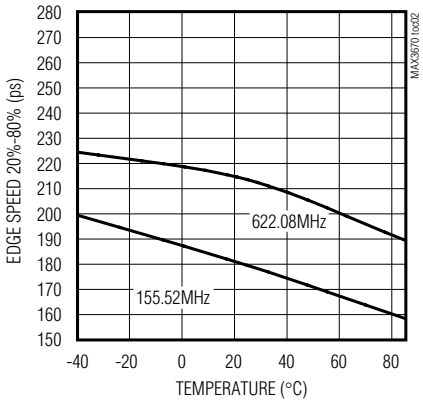
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

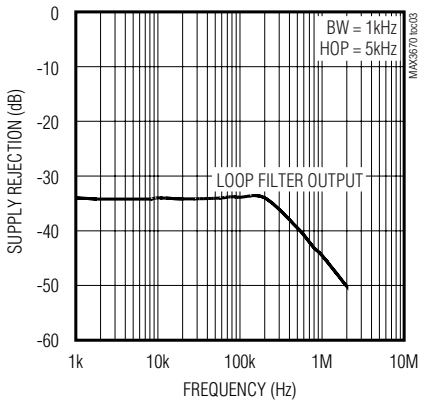
**SUPPLY CURRENT vs. TEMPERATURE**



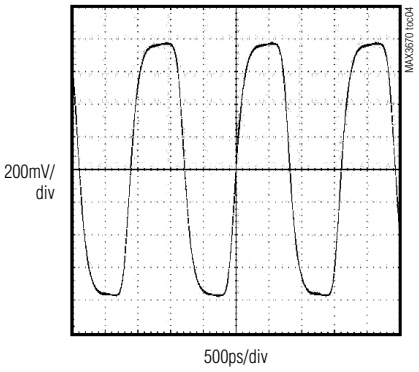

**EDGE SPEED vs. TEMPERATURE**



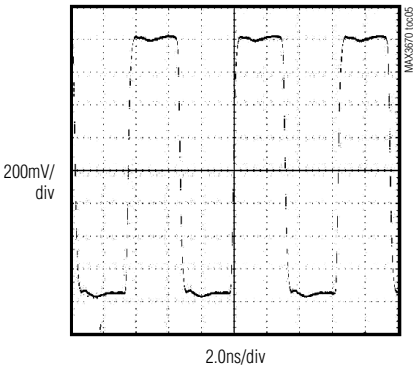

**POWER-SUPPLY REJECTION vs. FREQUENCY**




**622MHz CLOCK OUTPUT (DIFFERENTIAL OUTPUT)**




**155MHz CLOCK OUTPUT (DIFFERENTIAL OUTPUT)**

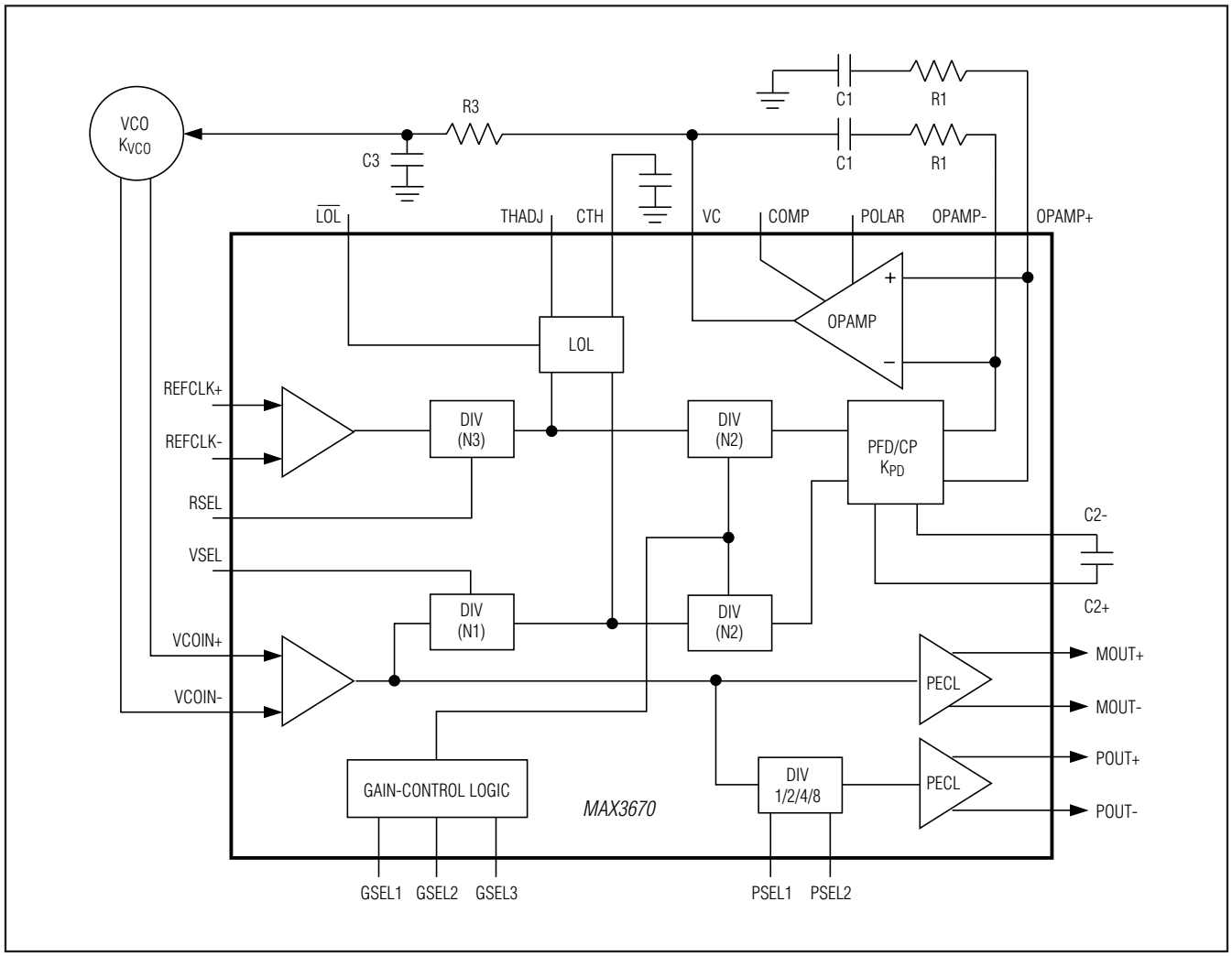


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## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | C2+ | Positive Filter Input. External capacitor connected between C2+ and C2- used for setting the higher-order pole frequency (see *Setting the Higher-Order Poles*). |
| 2 | C2- | Negative Filter Input. External capacitor connected between C2+ and C2- used for setting the higher-order pole frequency (see *Setting the Higher-Order Poles*). |
| 3, 9, 15 | VCCD | Positive Digital Supply Voltage |
| 4 | THADJ | Threshold Adjust Input. Used to adjust the Loss-of-Lock threshold (see *LOL Setup*). |
| 5 | CTH | Threshold Capacitor Input. A capacitor connected between CTH and ground used to control the Loss-of-Lock conditions (see *LOL Setup*). |
| 6 | GSEL1 | Gain Select 1 Input. Three-level pin used to set the phase-detector gain ($K_{PD}$) and the frequency-divider ratio ($N_2$) (see Table 3). |
| 7 | GSEL2 | Gain Select 2 Input. Three-level pin used to set the phase-detector gain ($K_{PD}$) and the frequency-divider ratio ($N_2$) (see Table 3). |
| 8 | GSEL3 | Gain Select 3 Input. Three-level pin used to set the phase-detector gain ($K_{PD}$) and the frequency-divider ratio ($N_2$) (see Table 3). |
| 10 | $\overline{LOL}$ | Loss-of-Lock. $\overline{LOL}$ signals a TTL low when the reference frequency differs from the VCO frequency. $\overline{LOL}$ signals a TTL high when the reference frequency equals the VCO frequency. |
| 11 | GND | Supply Ground |
| 12 | RSEL | Reference Clock Select Input. Three-level pin used to set the predivider ratio ($N_3$) for the input reference clock (see Table 1). |
| 13 | REFCLK | Positive Reference Clock Input |
| 14 | REFCLK- | Negative Reference Clock Input |
| 16 | VSEL | VCO Clock Select Input. Three-level pin used to set the predivider ratio ($N_1$) for the input VCO clock (see Table 2). |
| 17 | POUT- | Negative Optional Clock Output, PECL |
| 18 | POUT+ | Positive Optional Clock Output, PECL |
| 19, 22 | VCCO | Positive Supply Voltage for PECL Outputs |
| 20 | MOUT- | Negative Main Clock Output, PECL |
| 21 | MOUT+ | Positive Main Clock Output, PECL |
| 23 | VCOIN- | Negative VCO Clock Input |
| 24 | VCOIN+ | Positive VCO Clock Input |
| 25 | VC | Control Voltage Output. The voltage output from the op amp that controls the VCO. |
| 26 | POLAR | Polarity Control Input. Polarity control of op amp input. POLAR = GND for VCOs with positive gain transfer. POLAR = $V_{CC}$ for VCOs with negative gain transfer. |
| 27 | PSEL1 | Optional Clock Select 1 Input. Used to set the divider ratio for the optional clock output (see Table 4). |
| 28 | PSEL2 | Optional Clock Select 2 Input. Used to set the divider ratio for the optional clock output (see Table 4). |
| 29 | VCCA | Positive Analog Supply Voltage for the Charge Pump and Op Amp |
| 30 | COMP | Compensation Control Input. Op amp compensation reference control input. COMP = GND for VCOs whose control pin is $V_{CC}$ referenced. COMP = $V_{CC}$ for VCOs whose control pin is GND referenced. |
| 31 | OPAMP- | Negative Op Amp Input (POLAR = 0), Positive Op Amp Input (POLAR = 1) |
| 32 | OPAMP+ | Positive Op Amp Input (POLAR = 0), Negative Op Amp Input (POLAR = 1) |
| — | EP | Exposed Pad. The exposed pad must be soldered to the circuit board ground plane for proper thermal and electrical performance. |

## Functional Diagram




## Detailed Description

The MAX3670 contains all the blocks needed to form a PLL except for the VCO, which must be supplied separately. The MAX3670 consists of input buffers for the reference clock and VCO, input and output clock-divider circuitry, LOL detection circuitry, gain-control logic, a phase-frequency detector and charge pump, an op amp, and PECL output buffers.

This device is designed to clean up the noise on the reference clock input and provide a low-jitter system clock output.

### Input Buffer for Reference Clock and VCO

The MAX3670 contains differential inputs for the reference clock and the VCO. These inputs can be DC-coupled and are internally biased with high impedance so that they can be AC-coupled (Figure 1 in the *Interface Schematic* section). A single-ended VCO or reference clock can also be applied.

### Input and Output Clock-Divider Circuitry

The reference clock and VCO input buffers are followed by a pair of clock dividers that prescale the input frequency of the reference clock and VCO to 77.76MHz.

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Depending on the input clock frequency of 77.76MHz, 155.52MHz, or 622.08MHz, the clock divider ratio must be set to 1, 2, or 8, respectively. The POUT output buffer is preceded by a clock divider that scales the main clock output by 1, 2, 4, or 8 to provide an optional clock.

### LOL Detection Circuitry

The MAX3670 incorporates a loss-of-lock ($\overline{LOL}$) monitor that consists of an XOR gate, filter, and comparator with adjustable threshold (see "LOL Setup" in the *Applications* section). A loss-of-lock condition is signaled with a TTL low when the reference clock frequency differs from the VCO frequency.

### Gain-Control Logic

The gain-control circuitry facilitates the tuning of the loop bandwidth by setting phase-detector gain and frequency-divider ratio. The gain-control logic can be programmed to divide from 1 to 1024, in binary multiples, and to adjust the phase detector gain to 5µA/UI or 20µA/UI (see Table 3 in *Setting the Loop Bandwidth* section).

### Phase-Frequency Detector and Charge Pump

The phase-frequency detector incorporated into the MAX3670 produces pulses proportional to the phase difference between the reference clock and the VCO input. The charge pump converts this pulse train to a current signal that is fed to the op amp.

### Op Amp

The op amp is used to form an active PLL loop filter capable of driving the VCO control voltage input. Using the POLAR input, the op amp input polarity can be selected to work with VCOs having positive or negative gain-transfer functions. The COMP pin selects the op amp internal compensation. Connect COMP to ground if the VCO control voltage is $V_{CC}$ referenced. Connect COMP to $V_{CC}$ if the VCO control voltage is ground referenced.

## Design Procedure

### Setting Up the VCO and Reference Clock

The MAX3670 accepts 77.76MHz, 155.52MHz, or 622.08MHz (including FEC rates) reference clock frequencies. The RSEL input must be set so that the reference clock is prescaled to 77.76MHz (or FEC rate), to provide the proper range for the PFD and LOL detection circuitry. Table 1 shows the divider ratio for the different reference frequencies.

**Table 1. Reference Clock Divider**

| INPUT PIN RSEL | REFERENCE CLOCK INPUT FREQ. (MHz) | DIVIDER RATIO $N_3$ | PREDIVIDER OUTPUT FREQ. (MHz) |
|---|---|---|---|
| $V_{CC}$ | 77.76 | 1 | 77.76 |
| OPEN | 155.52 | 2 | 77.76 |
| GND | 622.08 | 8 | 77.76 |

The MAX3670 is designed to accept 77.76MHz, 155.52MHz, or 622.08MHz (including FEC rates) voltage-controlled oscillator (VCO) frequencies. The VSEL input must be set so that the VCO input is prescaled to 77.76MHz (or FEC rate), to provide the proper range for the PFD and LOL detection circuitry. Table 2 shows the divider ratio for the different VCO frequencies.

**Table 2. VCO Clock Divider**

| INPUT PIN VSEL | VCO CLOCK INPUT FREQ. (MHz) | DIVIDER RATIO $N_1$ | PREDIVIDER OUTPUT FREQ. (MHz) |
|---|---|---|---|
| $V_{CC}$ | 77.76 | 1 | 77.76 |
| OPEN | 155.52 | 2 | 77.76 |
| GND | 622.08 | 8 | 77.76 |

### Setting the Loop Bandwidth

To eliminate jitter present on the reference clock, the proper selection of loop bandwidth is critical. If the total output jitter is dominated by the noise at the reference clock input, then lowering the loop bandwidth will reduce system jitter. The loop bandwidth (K) is a function of the VCO gain ($K_{VCO}$), the gain of the phase detector ($K_{PD}$), the loop filter resistor ($R_1$), and the total feedback-divider ratio (N = N1 × N2). The loop bandwidth of the MAX3670 can be approximated by

$$K = \frac{K_{PD} R_1 K_{VCO}}{2\pi N}$$

For stability, a zero must be added to the loop in the form of resistor $R_1$ in series with capacitor $C_1$ (see *Functional Diagram*). The location of the zero can be approximated as

$$f_Z = \frac{1}{2\pi R_1 C_1}$$

Due to the second-order nature of the PLL jitter transfer, peaking will occur and is proportional to $f_Z/K$. For certain applications, it may be desirable to limit jitter

## Table 3. Gain Logic Pin Setup

| INPUT PIN GSEL1 | INPUT PIN GSEL2 | INPUT PIN GSEL3 | KPD (µA/UI) | DIVIDER RATIO $N_2$ |
|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | 20 | 1 |
| OPEN | $V_{CC}$ | $V_{CC}$ | 20 | 2 |
| GND | $V_{CC}$ | $V_{CC}$ | 20 | 4 |
| $V_{CC}$ | OPEN | $V_{CC}$ | 20 | 8 |
| OPEN | OPEN | $V_{CC}$ | 20 | 16 |
| GND | OPEN | $V_{CC}$ | 20 | 32 |
| $V_{CC}$ | GND | $V_{CC}$ | 20 | 64 |
| OPEN | GND | $V_{CC}$ | 20 | 128 |
| GND | GND | $V_{CC}$ | 20 | 256 |
| $V_{CC}$ | $V_{CC}$ | GND | 20 | 512 |
| OPEN | $V_{CC}$ | GND | 20 | 1024 |
| $V_{CC}$ | $V_{CC}$ | OPEN | 5 | 1 |
| OPEN | $V_{CC}$ | OPEN | 5 | 2 |
| GND | $V_{CC}$ | OPEN | 5 | 4 |
| $V_{CC}$ | OPEN | OPEN | 5 | 8 |
| OPEN | OPEN | OPEN | 5 | 16 |
| GND | OPEN | OPEN | 5 | 32 |
| $V_{CC}$ | GND | OPEN | 5 | 64 |
| OPEN | GND | OPEN | 5 | 128 |
| GND | GND | OPEN | 5 | 256 |
| $V_{CC}$ | OPEN | GND | 5 | 512 |
| OPEN | OPEN | GND | 5 | 1024 |

peaking in the PLL passband region to less than 0.1dB. This can be achieved by setting $f_Z \le K/100$.

The three-level GSEL pins (see *Functional Diagram*) select the phase-detector gain ($K_{PD}$) and the frequency-divider ratio ($N_2$). Table 3 summarizes the settings for the GSEL pins. A more detailed analysis of the loop filter is located in application note HFDN-13.0.

### Setting the Higher-Order Poles

Spurious noise is generated by the phase detector switching at the compare frequency, where $f_{COMPARE} = f_{VCO}/(N_1 \times N_2)$. Reduce the spurious noise from the digital phase detector by placing a higher-order pole (HOP) at a frequency much less than the compare frequency. The HOP should, however, be placed high enough in frequency that it does not decrease the overall loop-phase margin and impact jitter peaking. These two conditions can be met by selecting the HOP frequency to be $(K \times 4) < f_{HOP} \le f_{COMPARE}$, where K is the loop bandwidth.

The HOP can be implemented either by providing a compensation capacitor $C_2$, which produces a pole at

$$f_{HOP} = \frac{1}{2\pi(20k\Omega)(C_2)}$$

or by adding a lowpass filter, consisting of $R_3$ and $C_3$, directly on the VCO tuning port, which produces a pole at

$$f_{HOP} = \frac{1}{2\pi R_3 C_3}$$

Using $R_3$ and $C_3$ may be preferable for filtering more noise in the PLL, but it may still be necessary to provide filtering via $C_2$ when using large values of $R_1$ and $N_1 \times N_2$ to prevent clipping in the op amp.

### Setting the Optional Output

The MAX3670 optional clock output can be set to binary subdivisions of the main clock frequency. The PSEL1 and PSEL2 pins control the binary divisions. Table 4 shows the pin configuration along with the possible divider ratios.

## Table 4. Setting the Optional Clock Output Driver

| INPUT PIN PSEL1 | INPUT PIN PSEL2 | VCO TO POUT DIVIDER RATIO |
|---|---|---|
| $V_{CC}$ | $V_{CC}$ | 1 |
| GND | $V_{CC}$ | 2 |
| $V_{CC}$ | GND | 4 |
| GND | GND | 8 |

## Applications Information

### PECL Interfacing

The MAX3670 outputs (MOUT+, MOUT-, POUT+, POUT-) are designed to interface with PECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thévenin equivalent of 50Ω to $V_{CC}$ - 2V can be used with fixed-impedance transmission lines with proper termination. To ensure best performance, the differential outputs must have balanced loads. It is important to note that if optional clock output is not used, it should be left unconnected to save power (see Figure 2).

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### Layout

The MAX3670 performance can be significantly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the reference and VCO clock signals. Power-supply decoupling should be placed as close to $V_{CC}$ pins as possible. Take care to isolate the input from the output signals to reduce feedthrough.

### VCO Selection

The MAX3670 is designed to accommodate a wide range of VCO gains, positive or negative transfer slopes, and $V_{CC}$-referenced or ground-referenced control voltages. These features allow the user a wide range of options in VCO selection; however, the proper VCO must be selected to allow the clock generator circuitry to operate at the optimum levels. When selecting a VCO, the user needs to take into account the phase noise and modulation bandwidth. Phase noise is important because the phase noise above the PLL bandwidth will be dominated by the VCO noise performance. The modulation bandwidth of the VCO contributes an additional higher-order pole (HOP) to the system and should be greater than the HOP set with the external filter components.

### Noise Performance Optimization

Depending on the application, there are many different ways to optimize the PLL performance. The following are general guidelines to improve the noise on the system output clock.

1) If the reference clock noise dominates the total system-clock output jitter, then decreasing the loop bandwidth (K) reduces the output jitter.
2) If the VCO noise dominates the total system clock output jitter, then increasing the loop bandwidth (K) reduces the output jitter.
3) Smaller total divider ratio (N1 × N2), lower HOP, and smaller $R_1$ reduce the spurious output jitter.
4) Smaller $R_1$ reduces the random noise due to the op amp.

### LOL Setup

The $\overline{LOL}$ output indicates if the PLL has locked onto the reference clock using an XOR gate and comparator. The comparator threshold can be adjusted with THADJ, and the XOR gate output can be filtered with a capacitor between CTH and ground (Figure 3 in the *Interface Schematic* section). When the voltage at pin CTH exceeds the voltage at pin THADJ, then the $\overline{LOL}$ output goes low and indicates that the PLL is not locked. Note that excessive jitter on the reference clock input at frequencies above the loop bandwidth may degrade LOL functionality.

The user can set the amount of frequency or phase difference between VCO and reference clock at which $\overline{LOL}$ indicates an out-of-lock condition. The frequency difference is called the beat frequency. The CTH pin can be connected to an external capacitor, which sets the lowpass filter frequency to approximately

$$f_L = \frac{1}{2\pi C_{TH} 60k\Omega}$$

This lowpass filter frequency should be set about 10 times lower than the beat frequency to make sure the filtered signal at CTH does not drop below the THADJ threshold voltage. The internal compare frequency of the part is 77.78MHz. For a 1ppm sensitivity (beat frequency of 77Hz), the filter needs to be at 7.7Hz, and CTH should be at 0.33µF.

The voltage at THADJ will determine the level at which the $\overline{LOL}$ output flags. THADJ is set to a default value of 0.6V which corresponds in a 45° phase difference. This value can be overridden by applying the desired threshold voltage to the pin. The range of THADJ is from 0V (0°) to 2.4V (180°).

## Interface Schematics

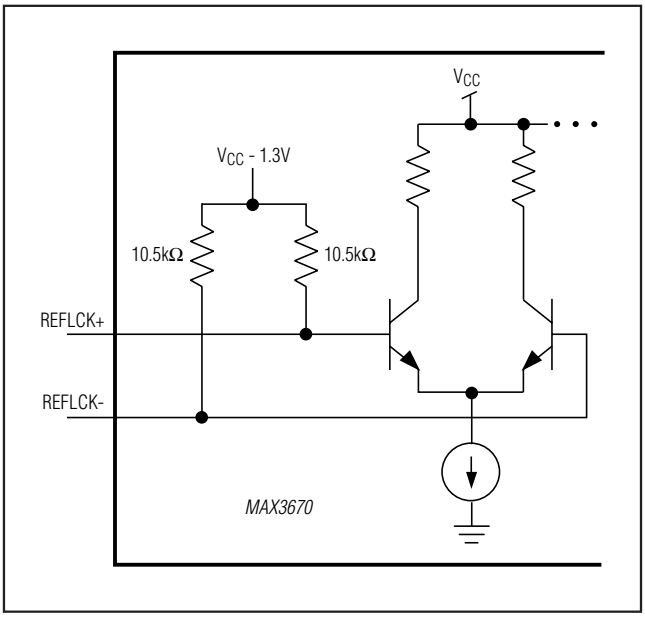



*Figure 1. Input Interface*

## Interface Schematics (continued)

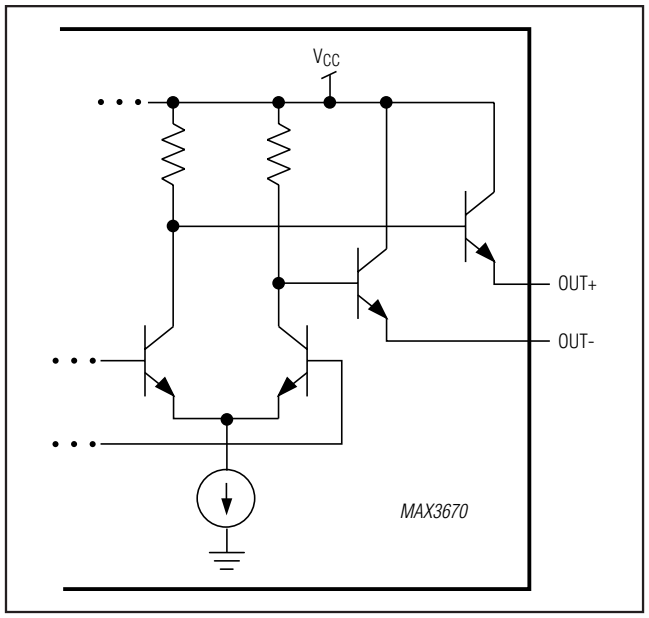



Figure 2. Output Interface

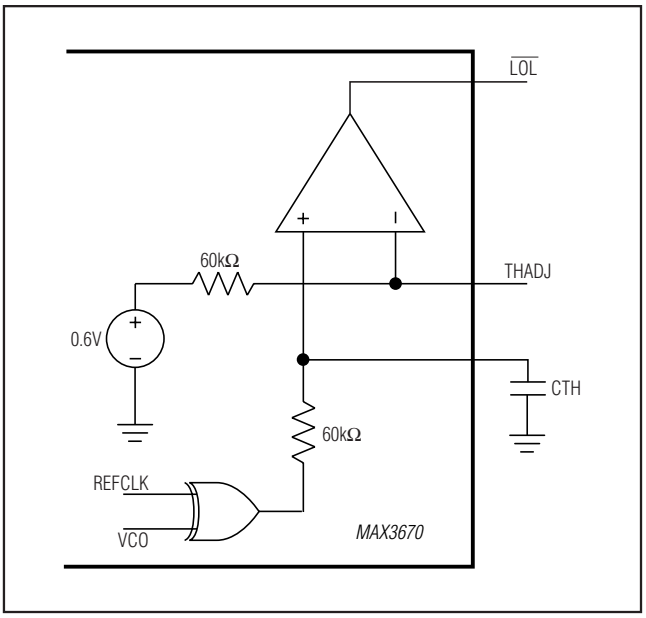
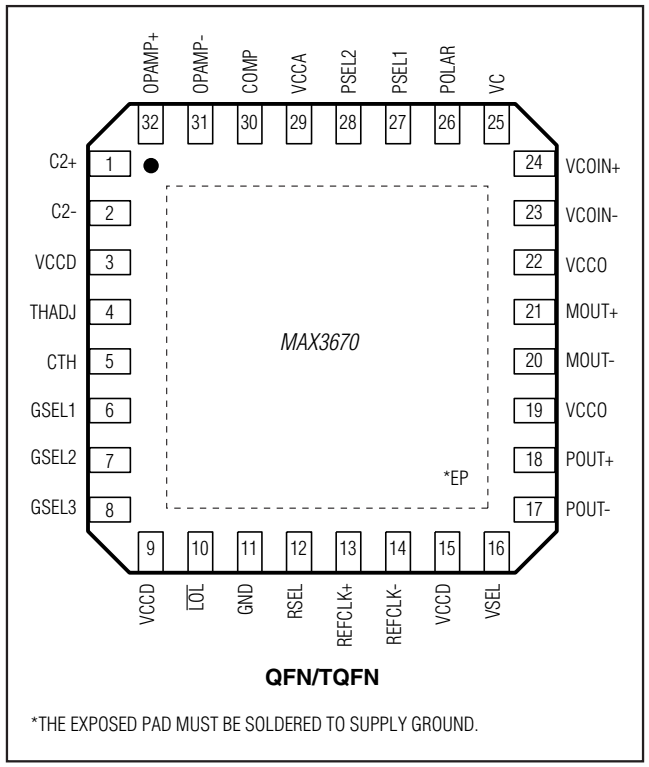



Figure 3. Loss-of-Lock Indicator

## Pin Configuration




**QFN/TQFN**

*THE EXPOSED PAD MUST BE SOLDERED TO SUPPLY GROUND.

## Chip Information

TRANSISTOR COUNT: 2478

## Package Information

For the latest package outline information and land patterns, go to www.microsemi.com. Note that a "+", "#", or"-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 32 QFN-EP | G3255-1 | 21-0091 |
| 32 TQFN-EP | T3255+3 | 21-0140 |

# Low-Jitter 155MHz/622MHz Clock Generator

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 9/01 | Initial release. | — |
| 1 | 5/03 | Added the PKG CODE column to the *Ordering Information* table; updated the package outline drawing in the *Package Information* section. | 1, 12 |
| 2 | 9/09 | Added the lead(Pb)-free TQFN package to the *Ordering Information* table; replaced the package outline drawing with a table in the *Package Information* section. | 1, 11 |



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