19-4115; Rev 1; 04/19

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

General Description

The MAX3678 is a low-jitter frequency synthesizer with intelligent dynamic clock switching optimized for systems where redundant clock failover switching is needed. It contains a monolithic phase-locked loop (PLL) that accepts two reference clock inputs and generates nine phase-aligned outputs. The device continuously monitors the signal status for both reference clock inputs. In the event that the primary clock fails, the PLL automatically switches to the secondary clock input without generating a phase bump at the clock outputs, using a glitchless switchover mechanism. A manual switch mode is also provided for user-controlled switching. The device features ultra-low jitter generation of $0.3ps_{RMS}$ (integrated 12kHz to 20MHz) and excellent power-supply noise rejection.

The MAX3678 operates from a single +3.3V supply and typically consumes 400mW. The operating temperature range is from 0°C to +85°C, and is available in a 8mm x 8mm, 56-pin TQFN package.

Applications

Redundant Clock Distribution in Servers

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Frequency Translation

Jitter Cleanup and Frequency Synchronization

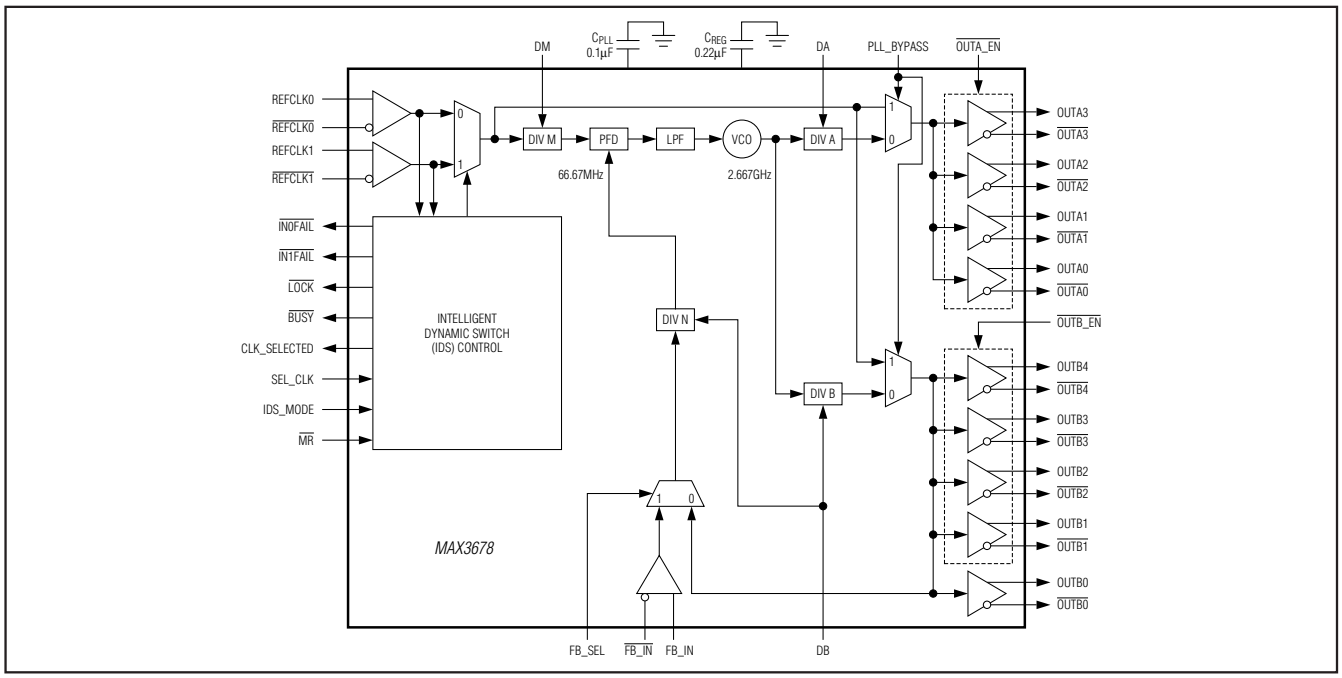
Features

- **Two Reference Clock Inputs: LVPECL**
- **Nine Phase-Aligned Clock Outputs: LVPECL**
- **Automatic or Manual Dynamic Switching Between Two Reference Clock Inputs**
- **Input Frequencies: 66.67MHz, 133.33MHz, 266.67MHz, 333.33MHz**
- **Output Frequencies: 66.67MHz, 133.33MHz, 266.67MHz, 333.33MHz**
- **Low-Jitter Generation: $0.3ps_{RMS}$ (12kHz to 20MHz)**
- **Clock Failure Indicator for Both Reference Clocks**
- **External Feedback Provides Zero-Delay Capability**
- **Low Output Skew: 20ps Typical**
- **Typical Power Dissipation: 400mW at +3.3V**
- **Operating Temperature: 0°C to +85°C**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3678UTN2	0°C to +85°C	56 TQFN-EP*

Functional Diagram



Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}, VCC_VCO).....-0.3V to +4.0V
LVPECL Output Current (OUTA[3:0], $\overline{OUTA[3:0]}$, OUTB[4:0], $\overline{OUTB[4:0]}$) .....-56mA
All Other Pins (REFCLK0, $\overline{REFCLK0}$, REFCLK1, $\overline{REFCLK1}$, $\overline{IN0FAIL}$, $\overline{IN1FAIL}$, $\overline{LOCK}$, $\overline{BUSY}$, CLK_SELECTED, SEL_CLK, IDS_MODE, $\overline{MR}$, RSVD, FB_SEL, FB_IN, $\overline{FB_IN}$, DM, DA, DB, CPLL, CREG, PLL_BYPASS, $\overline{OUTA_EN}$, $\overline{OUTB_EN}$).....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above 70°C).....3808mW
Operating Junction Temperature (T_J).....-55°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	LVPECL outputs unterminated		120	175	mA
POWER-ON RESET						
V_{CC} Rising		(Note 1)		2.55		V
V_{CC} Falling		(Note 1)		2.45		V
LVCMOS/LVTTL INPUTS ($\overline{MR}$, SEL_CLK, IDS_MODE, PLL_BYPASS, FB_SEL)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			75	µA
Input Low Current	I_{IL}	V_{IN} = GND	-75			µA
LVCMOS/LVTTL OUTPUTS (CLK_SELECTED, $\overline{IN0FAIL}$, $\overline{IN1FAIL}$, $\overline{BUSY}$, $\overline{LOCK}$)						
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +8mA			0.4	V
LVPECL INPUTS (REFCLK0, $\overline{REFCLK0}$, REFCLK1, $\overline{REFCLK1}$, FB_IN, $\overline{FB_IN}$) (Note 2)						
Input High Voltage	V_{IH}				V_{CC} - 0.7	V
Input Low Voltage	V_{IL}		V_{CC} - 2.0			V
Input Bias Voltage	V_{CMI}		V_{CC} - 1.8	V_{CC} - 1.34		V
Differential-Input Swing			0.15		1.9	V_{P-P}
Differential-Input Impedance				> 40		kΩ
Common-Mode Input Impedance				> 14		kΩ
Input Capacitance				1.5		pF
Input Current		V_{IH} = V_{CC} - 0.7V, V_{IL} = V_{CC} - 2.0V	-100		+100	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Inrush Current When Power is Off (Steady State)	I_{DC}	(Notes 3, 4)		8		mA
Input Inrush Current Overshoot When Power is Off	$I_{OVERSHOOT}$	(Notes 3, 4)		6		mA
REFERENCE CLOCK INPUTS (REFCLK0, $\overline{REFCLK0}$, REFCLK1, $\overline{REFCLK1}$)						
Reference Clock Frequency	f_{REF}			Table 1		MHz
Reference Clock Frequency Tolerance		(Note 5)	-25		+25	ppm
Reference Clock Duty Cycle			40		60	%
Reference Clock Amplitude Detection Assert Threshold	V_{DT}	Differential swing (Notes 5, 6, 7)	100	200	400	mV_{P-P}
LVPECL OUTPUTS (OUTA[3:0], $\overline{OUTA[3:0]}$, OUTB[4:0], $\overline{OUTB[4:0]}$) (Note 8)						
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.70	V_{CC} - 1.55	V
Differential-Output Swing			1.1	1.45	1.8	V_{P-P}
Output Current When Disabled		V_O = V_{CC} - 2.0V to V_{CC} - 0.7V			130	µA
Output Frequency	f_{OUT}			Tables 2, 3		MHz
Output Rise/Fall Time	t_R, t_F	20% to 80% (Note 5)	150		600	ps
Output Duty Cycle		PLL_BYPASS = 0	48		52	%
		PLL_BYPASS = 1 (Note 9)	45		55	%
Output-to-Output Skew	t_{SKEW}			20		ps
OTHER AC ELECTRICAL SPECIFICATIONS						
PLL Jitter Transfer Bandwidth				55		kHz
Jitter Peaking				0.1		dB
PFD Compare Frequency				66.67		MHz
VCO Center Frequency				2.667		GHz
Random Jitter Generation		Integrated 12kHz to 20MHz (Notes 5, 6)		0.3	1.0	ps_{RMS}
Deterministic Jitter Caused by Power-Supply Noise		(Note 10)		5		ps_{P-P}
Phase-Error Detection Window	ϕerr	(Notes 5, 11)	±0.5	±0.75	±1.0	ns
Rate of Output Period Change Per Cycle	Δt/cycle			100		ppm/ cycle
Output Frequency Transient Relative to the Initial Lock Frequency	$\lvert\Delta f/f_O\rvert$	During PLL switching (Notes 5, 12)		150	600	ppm

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Difference Between Reference Clock and VCO Within Which the PLL is Considered in Lock				500		ppm
Frequency Difference Between Reference Clock and VCO at Which the PLL is Considered Out-of-Lock				800		ppm
PLL Lock Time	t_{LOCK}	Figure 2		400		µs
Master Reset ($\overline{MR}$) Minimum Pulse Width				100		ns
Propagation Delay from Input to FB_IN		FB_SEL = 1 (Notes 5, 13)	-100		+100	ps
Propagation Delay from Input to Any Output		PLL_BYPASS = 1		1.0		ns

Note 1: See the *Power-On-Reset (POR)* section for more information.
Note 2: LVPECL inputs can be AC- or DC-coupled.
Note 3: For hot-pluggable purposes, the device can receive LVPECL inputs when no supply voltage is applied. Measured with V_{CC} pins connected to GND. See Figure 1.
Note 4: Measured with LVPECL input (V_{IH}, V_{IL}) as specified.
Note 5: Guaranteed by design and characterization.
Note 6: Measured using reference clock input with 550ps rise/fall time (20% to 80%).
Note 7: When input differential swing is below the specified threshold, a clock failure is declared. See Figure 8.
Note 8: LVPECL outputs terminated 50Ω to V_{TT} = V_{CC} - 2V.
Note 9: Measured with 50% duty cycle at reference clock input.
Note 10: Measured with 50mV_{P-P} sinusoidal noise on the power supply, f_{NOISE} = 100kHz.
Note 11: See the *Phase Qualification* section for more information.
Note 12: This specification is not met when the intelligent dynamic switch (IDS) operation follows that of Case 2b (Figure 4).
Note 13: Measured using 133.33MHz clock at reference input and feedback input with matched slew rates.

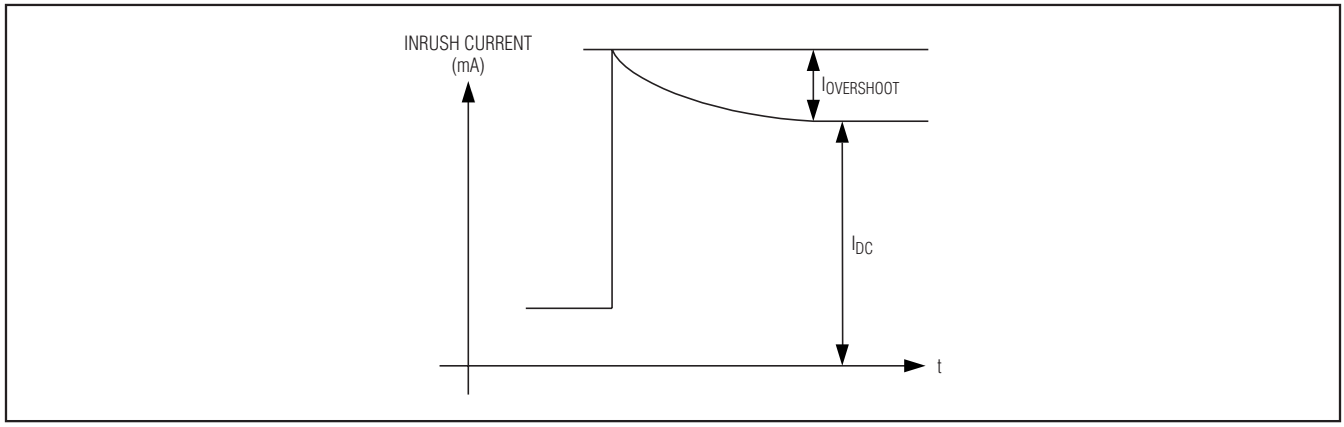
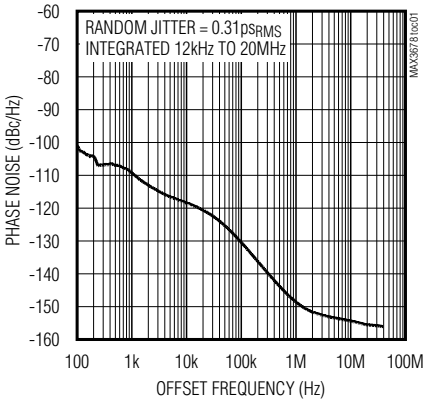


Figure 1. LVPECL Input Inrush Current

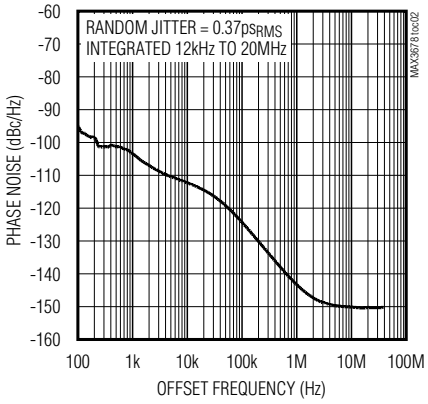
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

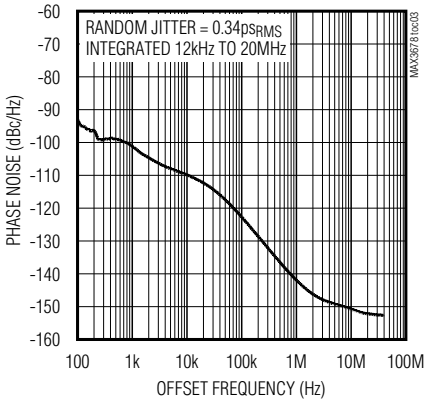
PHASE NOISE AT 133.33MHz



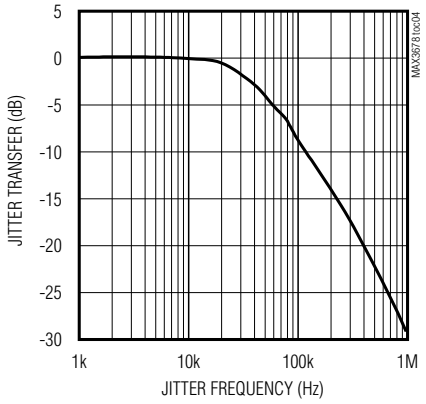
PHASE NOISE AT 266.67MHz



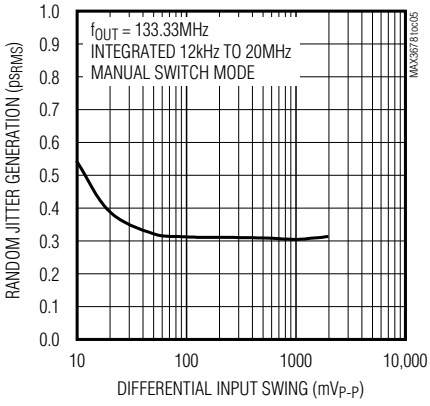
PHASE NOISE AT 333.33MHz



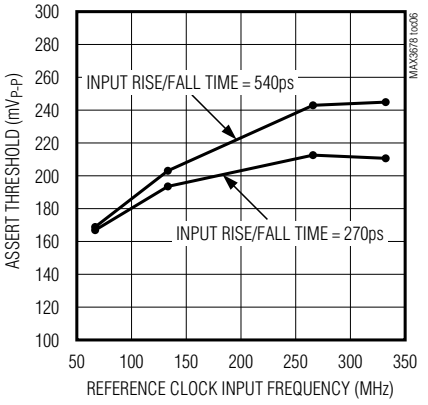
JITTER TRANSFER



RANDOM JITTER GENERATION vs. DIFFERENTIAL-INPUT SWING



REFERENCE CLOCK AMPLITUDE DETECTION ASSERT THRESHOLD vs. INPUT FREQUENCY

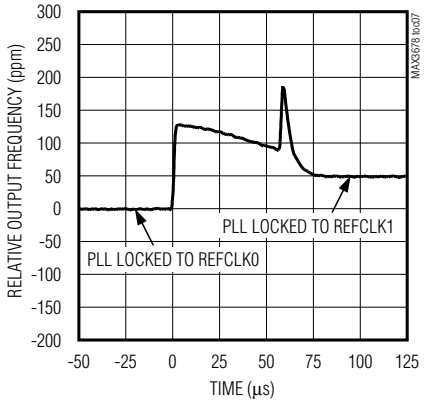


Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

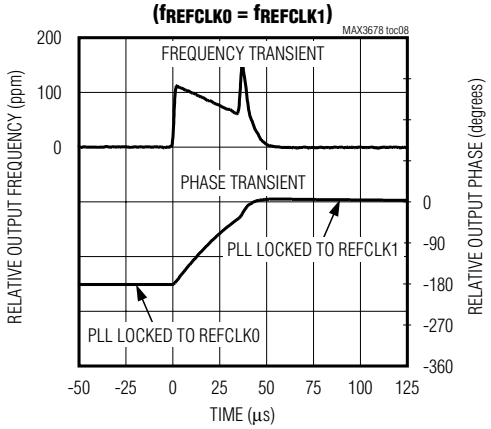
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

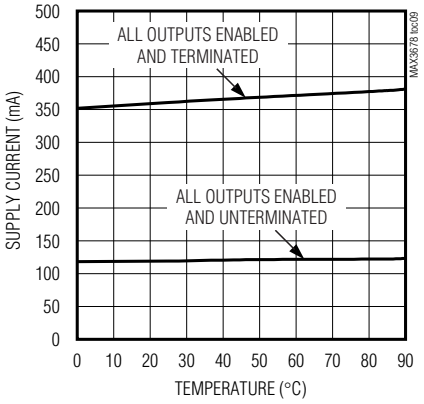
SWITCHING TRANSIENT (Δf = 50ppm)
$f_{REFCLK1}$ = ($f_{REFCLK0}$ + 50ppm)



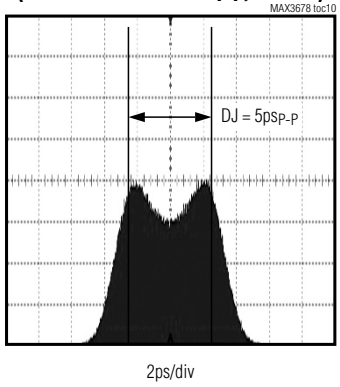
SWITCHING TRANSIENT (Δϕ = 180°)
($f_{REFCLK0}$ = $f_{REFCLK1}$)



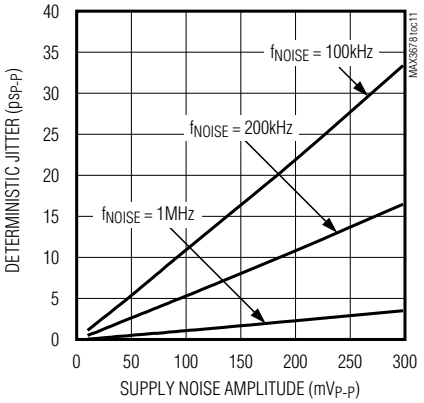
SUPPLY CURRENT vs. TEMPERATURE



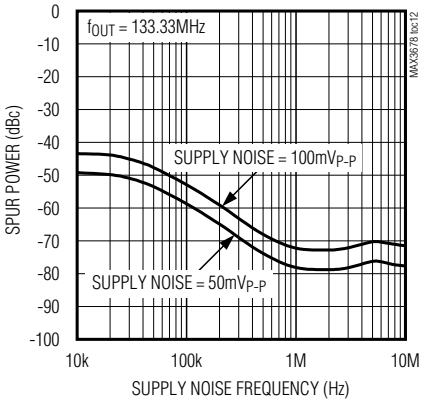
JITTER HISTOGRAM WITH SUPPLY NOISE
(SUPPLY NOISE = 50mV_{P-P}, 100kHz)



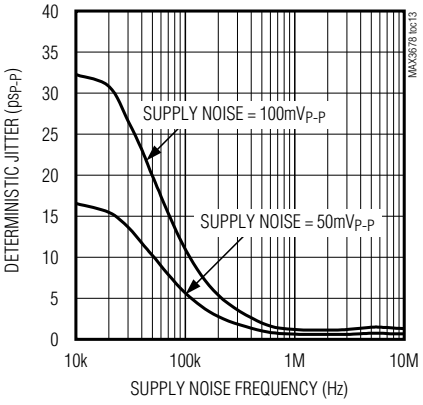
DETERMINISTIC JITTER
vs. POWER-SUPPLY NOISE AMPLITUDE



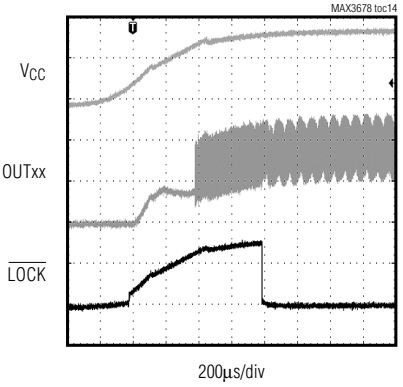
SPURS CAUSED BY POWER-SUPPLY NOISE
vs. SUPPLY NOISE FREQUENCY



DETERMINISTIC JITTER
vs. POWER-SUPPLY NOISE FREQUENCY



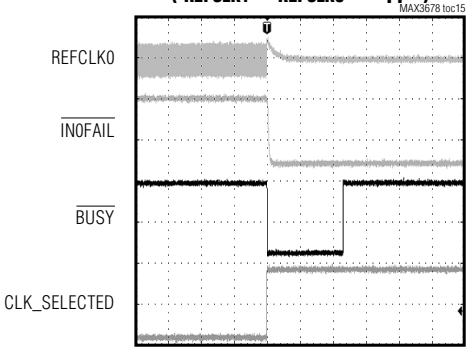
POWER-ON-RESET TIMING



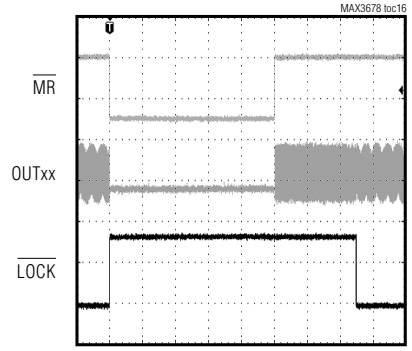
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

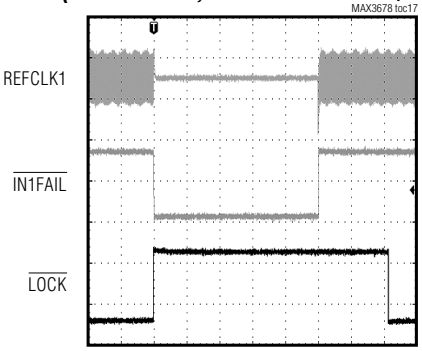
IDS-INITIATED SWITCH TIMING ($f_{REFCLK1} = f_{REFCLK0} + 50ppm$)



MASTER RESET TIMING



CLOCK HOLDOVER TIMING (REFCLK0 OPEN, REFCLK1 TOGGLED ON/OFF)



Pin Description

PIN	NAME	FUNCTION
1	$\overline{IN0FAIL}$	REFCLK0 Failure Indicator, LVCMOS/LVTTL Output. Low indicates REFCLK0 fails the clock qualification. Once a failed clock is detected, the indicator status is latched and updated every 128 PFD cycles (~ 2µs).
2	CLK_SELECTED	Selected Reference Clock Indicator, LVCMOS/LVTTL Output. High indicates PLL is locked to REFCLK1. Low indicates PLL is locked to REFCLK0.
3	RSVD	Reserved. Connect to GND.
4	REFCLK0	Reference Clock Input 0, Differential LVPECL
5	$\overline{REFCLK0}$	
6	DM	Four-Level Control Input for Reference Clock Input Divider. See Table 1.
7, 22, 30, 41, 49, 52	V_{CC}	Power Supply. Connect to +3.3V.
8, 14, 23, 29, 42, 48, 53	GND	Supply Ground
9	$\overline{MR}$	Master Reset, LVCMOS/LVTTL Input. Connect this pin high or leave open for normal operation. Has internal 90kΩ pullup to V_{CC}. Connect low to reset the device. A reset is not required at power-up. If the output divider settings are changed on the fly, a reset is required to phase align the outputs. This input has a 100ns minimum pulse width and is asynchronous to the reference clock. While in reset, all clock outputs are held to logic-low. See Table 6.
10	REFCLK1	Reference Clock Input 1, Differential LVPECL
11	$\overline{REFCLK1}$	
12	SEL_CLK	Reference Clock Select, LVCMOS/LVTTL Input. Connect low or leave open to select REFCLK0 as the reference clock. Has internal 90kΩ pulldown to GND. Connect high to select REFCLK1 as the reference clock. In manual switch mode (IDS_MODE = 1), the PLL locks to a reference clock selected by the SEL_CLK pin. In automatic switch mode (IDS_MODE = 0), the PLL initially locks to a reference clock selected by the SEL_CLK pin, but the internal circuit can override this control input for automatic switchover when a reference clock failure is detected. See the *Detailed Description* section for more information.

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Pin Description (continued)

PIN	NAME	FUNCTION
13	VCC_VCO	Power Supply for VCO. Connect to +3.3V.
15	CPLL	Connection for PLL Filter Capacitor. Connect a 0.1µF capacitor between this pin and GND.
16	CREG	Connection for VCO Regulator Capacitor. Connect a 0.22µF capacitor between this pin and GND.
17	FB_SEL	External Feedback Select, LVCMOS/LVTTL Input. Connect high to select external feedback for zero-delay buffer configuration. Connect low or leave open for internal feedback. Has internal 90kΩ pulldown to GND.
18	FB_IN	External Feedback Clock Input, Differential LVPECL. Used for zero-delay buffer configuration.
19	$\overline{FB_IN}$	
20	$\overline{OUTB0}$	Clock Output B0, Differential LVPECL
21	OUTB0	
24	$\overline{OUTB1}$	Clock Output B1, Differential LVPECL
25	OUTB1	
26	$\overline{OUTB2}$	Clock Output B2, Differential LVPECL
27	OUTB2	
28	DB	Four-Level Control Input for B-Group Output Divider. See Table 3.
31	$\overline{OUTB3}$	Clock Output B3, Differential LVPECL
32	OUTB3	
33	$\overline{OUTB4}$	Clock Output B4, Differential LVPECL
34	OUTB4	
35	$\overline{OUTB_EN}$	Three-Level Control Input for B-Group Output Enable. See Table 5.
36	$\overline{OUTA_EN}$	Three-Level Control Input for A-Group Output Enable. See Table 4.
37	$\overline{OUTA3}$	Clock Output A3, Differential LVPECL
38	OUTA3	
39	$\overline{OUTA2}$	Clock Output A2, Differential LVPECL
40	OUTA2	
43	DA	Four-Level Control Input for A-Group Output Divider. See Table 2.
44	$\overline{OUTA1}$	Clock Output A1, Differential LVPECL
45	OUTA1	
46	$\overline{OUTA0}$	Clock Output A0, Differential LVPECL
47	OUTA0	
50	PLL_BYPASS	PLL Bypass Control, LVCMOS/LVTTL Input. Connect low or open for normal operation. Has internal 90kΩ pulldown to GND. Connect high to bypass the PLL, connecting the selected reference clock directly to the clock outputs. In this mode, the clock qualification function is not valid, and the device operates in manual mode for reference clock selection.
51	IDS_MODE	Intelligent Dynamic Switch (IDS) Mode Control, LVCMOS/LVTTL Input. Connect high for manual switch mode. The internal automatic switch function is disabled, and the PLL locks to the reference clock selected by SEL_CLK. Connnect low or leave open for automatic switch mode. Has internal 90kΩ pulldown to GND. In automatic switch mode, the PLL initially locks to the reference clock selected by SEL_CLK, and automatically switches to the valid secondary clock input when the primary clock fails. See the *Detailed Description* section for more information.
54	$\overline{BUSY}$	Intelligent Dynamic Switch (IDS) Activity Indicator, LVCMOS/LVTTL Output. Low indicates the IDS is busy switching reference clocks.
55	$\overline{LOCK}$	PLL Lock Indicator, LVCMOS/LVTTL Output. Low indicates PLL is locked.

Pin Description (continued)

PIN	NAME	FUNCTION
56	$\overline{\text{IN1FAIL}}$	REFCLK1 Failure Indicator, LVCMOS/LVTTL Output. Low indicates REFCLK1 fails the clock qualification. Once a failed clock is detected, the indicator status is latched and updated every 128 PFD cycles (~ 2µs).
—	EP	Exposed Pad. Connect to supply ground for proper electrical and thermal performance.

Detailed Description

The MAX3678 is a frequency synthesizer with intelligent dynamic clock switching designed specifically for systems with redundant clock routing. The device integrates two differential LVPECL reference inputs, IDS control, a PLL with configurable dividers, nine differential LVPECL clock outputs, and a selectable external feedback input for zero-delay buffer applications (see the *Functional Diagram*).

The two reference clock inputs are continuously monitored for clock failure by the internal PLL and associated logic. If the primary clock fails, the PLL automatically switches to the secondary clock using a glitchless switchover mechanism. A manual switch mode is also provided for user-controlled switching.

The PLL accepts reference input frequencies of 66.67MHz, 133.33MHz, 266.67MHz, or 333.33MHz and generates output frequencies of 66.67MHz, 133.33MHz, 266.67MHz, or 333.33MHz. The nine clock outputs are organized into two groups (A and B). Each group has a configurable frequency divider and output-enable control.

Phase-Locked Loop (PLL)

The PLL contains a phase-frequency detector (PFD), lowpass filter (LPF), and voltage-controlled oscillator (VCO). The PFD compares the divided reference frequency to the divided VCO output at 66.67MHz, and generates a control signal to keep the VCO phase and frequency locked to the selected reference clock. Using a high-frequency VCO (2.667GHz) and low-loop bandwidth (55kHz), the MAX3678 attenuates reference clock jitter while maintaining lock and generates low-jitter clock outputs at multiple frequencies. Typical jitter generation is $0.3ps_{RMS}$ (integrated 12kHz to 20MHz).

To minimize supply noise-induced jitter, the VCO supply (VCC_VCO) is isolated from the core logic and output buffer supplies. Additionally, the MAX3678 uses an internal low-dropout (LDO) regulator to attenuate noise from the power supply. This allows the device to achieve excellent power-supply noise rejection, significantly reducing the impact on jitter generation.

Intelligent Dynamic Switch (IDS)

The MAX3678 continuously monitors both the primary reference input and secondary reference input and provides a clock failure indicator for each of them ($\overline{\text{IN0FAIL}}$, $\overline{\text{IN1FAIL}}$). It is assumed that both reference inputs, REFCLK0 and REFCLK1, are at the same frequency (within ±25ppm), but there is no phase relationship. See the following definitions for clarification.

- **Primary Reference Clock:** The input reference clock selected by SEL_CLK.
- **Secondary Reference Clock:** The input reference clock not selected by SEL_CLK.
- **PLL Reference Clock:** The reference clock that the PLL locks to, selected by either SEL_CLK or the IDS control block. IDS can override SEL_CLK.

The IDS control has two modes of operation—automatic switch mode and manual switch mode—controlled by the IDS_MODE input. Automatic switch mode requires that the PLL not be bypassed (PLL_BYPASS = 0).

Automatic Switch Mode (IDS_MODE = 0 and PLL_BYPASS = 0)

When the IDS_MODE pin is set low or left open, the automatic switch mode is enabled. The PLL initially locks to the primary reference clock selected by SEL_CLK. Upon the detection of the primary reference clock failure, the IDS control block overrides the SEL_CLK for switch control, and the PLL automatically switches over to the secondary qualified reference clock input and changes the CLK_SELECTED output. When an input clock switch occurs, the output clock phase alignment to the new reference clock occurs over an extended period of time. During this time period, the maximum rate of output period change per cycle is typically 100ppm/cycle.

The following are case examples that demonstrate the IDS operations with REFCLK0 selected as the primary reference clock (SEL_CLK = 0).

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Case 1. Power-Up, PLL Locks to REFCLK0

During power-up, the REFCLK0 input is selected as the PLL reference clock. The PLL locks to REFCLK0 if it is valid ($\overline{IN0FAIL}$ = 1) and makes CLK_SELECTED = 0 (Figure 2). The $\overline{LOCK}$ output goes from initially unlocked status ($\overline{LOCK}$ = 1) to locked status ($\overline{LOCK}$ = 0). The device continues to run in this loop and monitors the signal status for both REFCLK0 and REFCLK1.

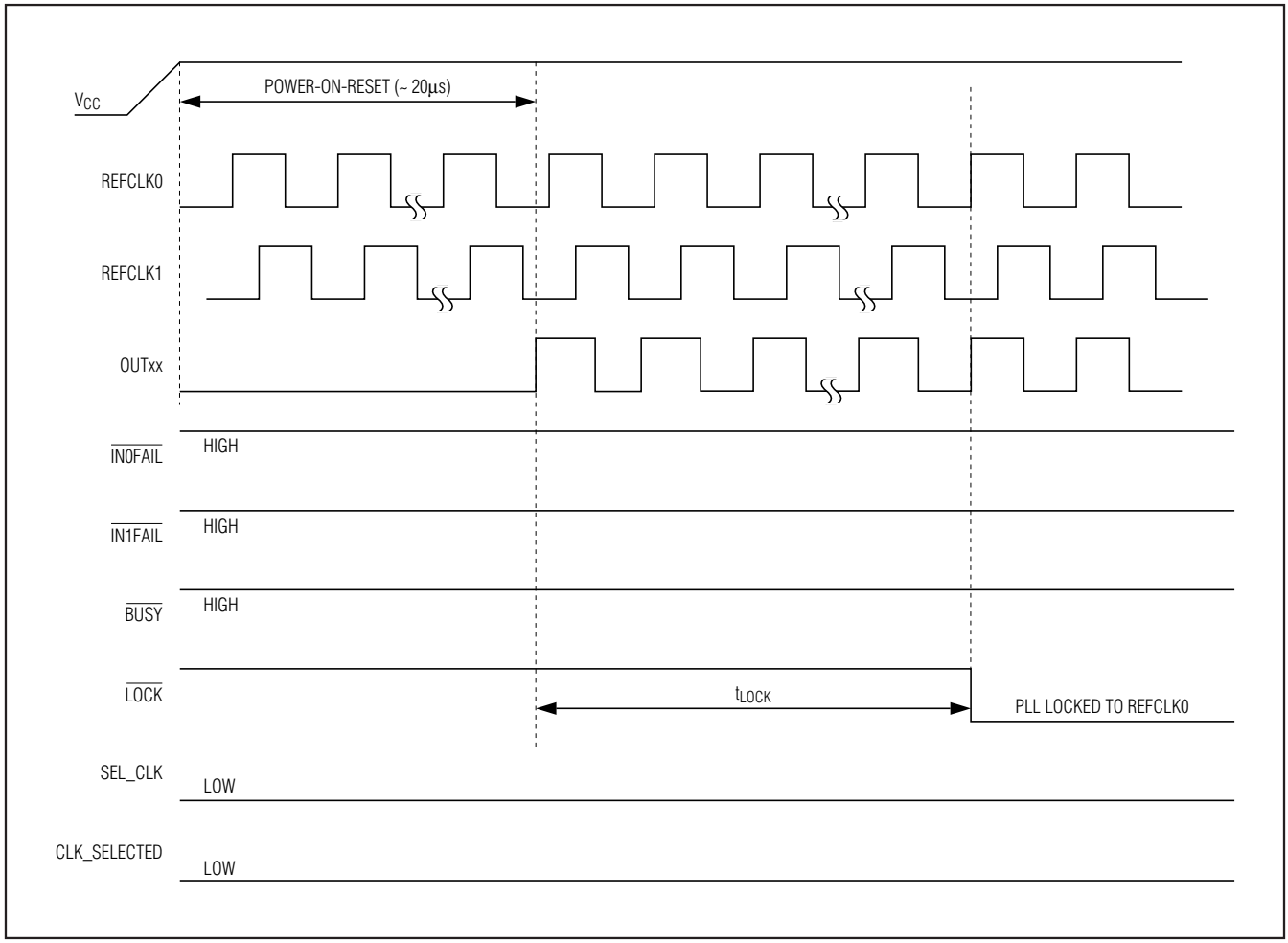


Figure 2. Power-Up, PLL Locks to REFCLK0

Case 2a. REFCLK0 Becomes Invalid, IDS Initiates a Switch

When $\overline{\text{IN0FAIL}}$ is asserted low ($\overline{\text{IN0FAIL}}$ = 0), the IDS initiates a switch, making CLK_SELECTED = 1, and REFCLK1 becomes the PLL reference clock if it is valid ($\overline{\text{IN1FAIL}}$ = 1) (Figure 3). Note that a switch happens only if the other reference clock input is valid. During the switching process, the $\overline{\text{BUSY}}$ signal is asserted as 0 and deasserted as 1 when the switch is completed, meaning that the output clock phase is realigned to the new reference clock. During this period of time, the PLL lock indicator ($\overline{\text{LOCK}}$) indicates that the PLL is in lock. The PLL remains locked to REFCLK1 as long as REFCLK1 is valid.

Once a clock failure is detected on the reference clock (REFCLK0 in this example), the failure indicator is latched for 128 PFD cycles (~ 2µs) and is updated every 128 PFD cycles. This latch function is released when a valid signal is detected.

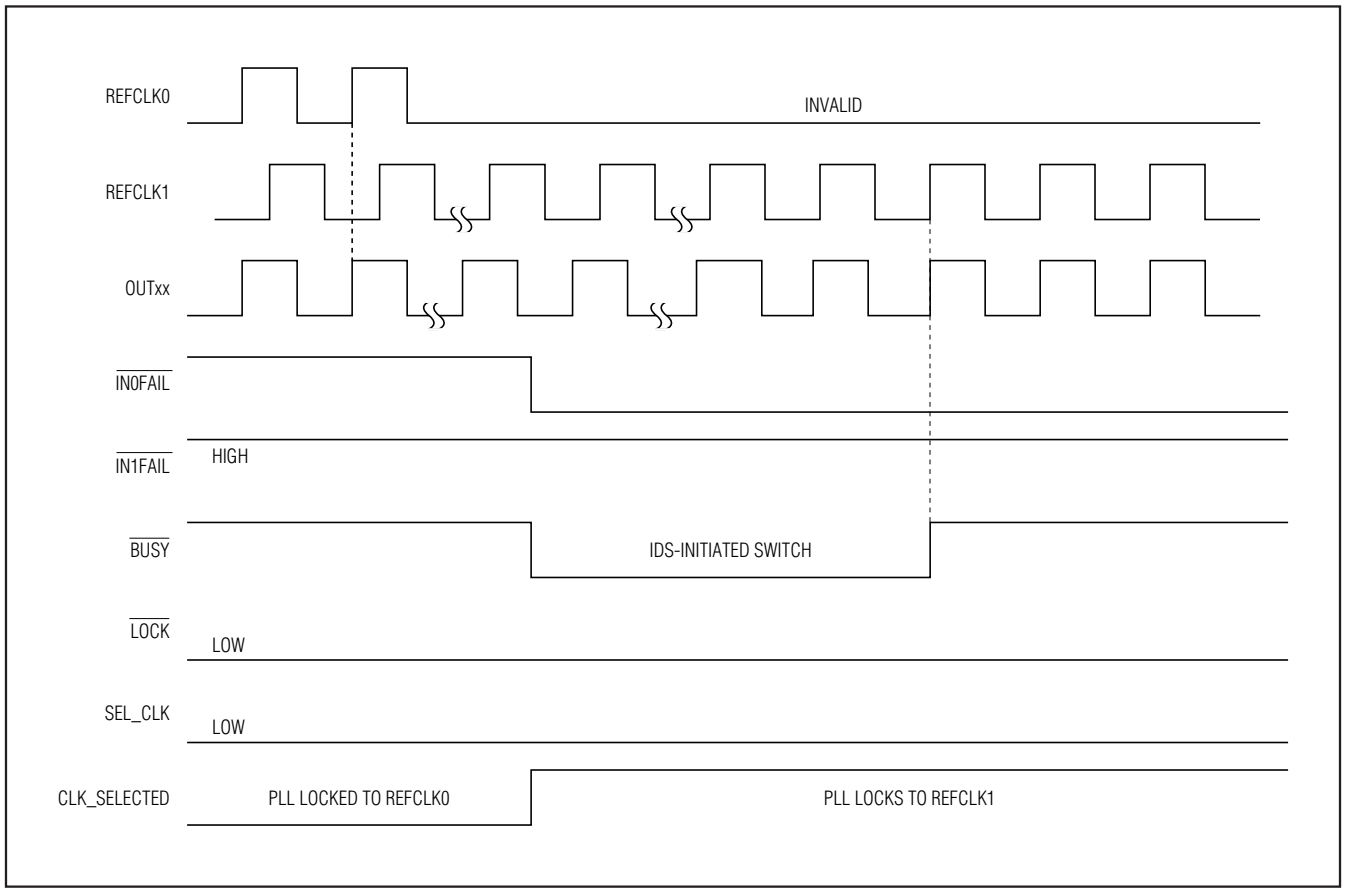


Figure 3. REFCLK0 Becomes Invalid, IDS Initiates a Switch

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Case 2b. REFCLK0 Becomes Invalid, IDS Initiates a Switch, IDS Sequence Includes Holdover Mode

When REFCLK0 fails, IDS initiates a switch to REFCLK1 if it is valid. While the PLL is in the process of switching, random clock-phase variation may cause internal qualification circuits to temporarily disqualify REFCLK1, resulting in the PLL being forced to enter holdover mode. While in holdover mode, IDS continues monitoring the signal status for both REFCLK0 and REFCLK1. When REFCLK1 is requalified, IDS selects REFCLK1, and the PLL locks to REFCLK1 to exit holdover mode (Figure 4).

Note that the specification for output frequency transient is not met when the IDS operation follows a sequence that includes holdover mode.

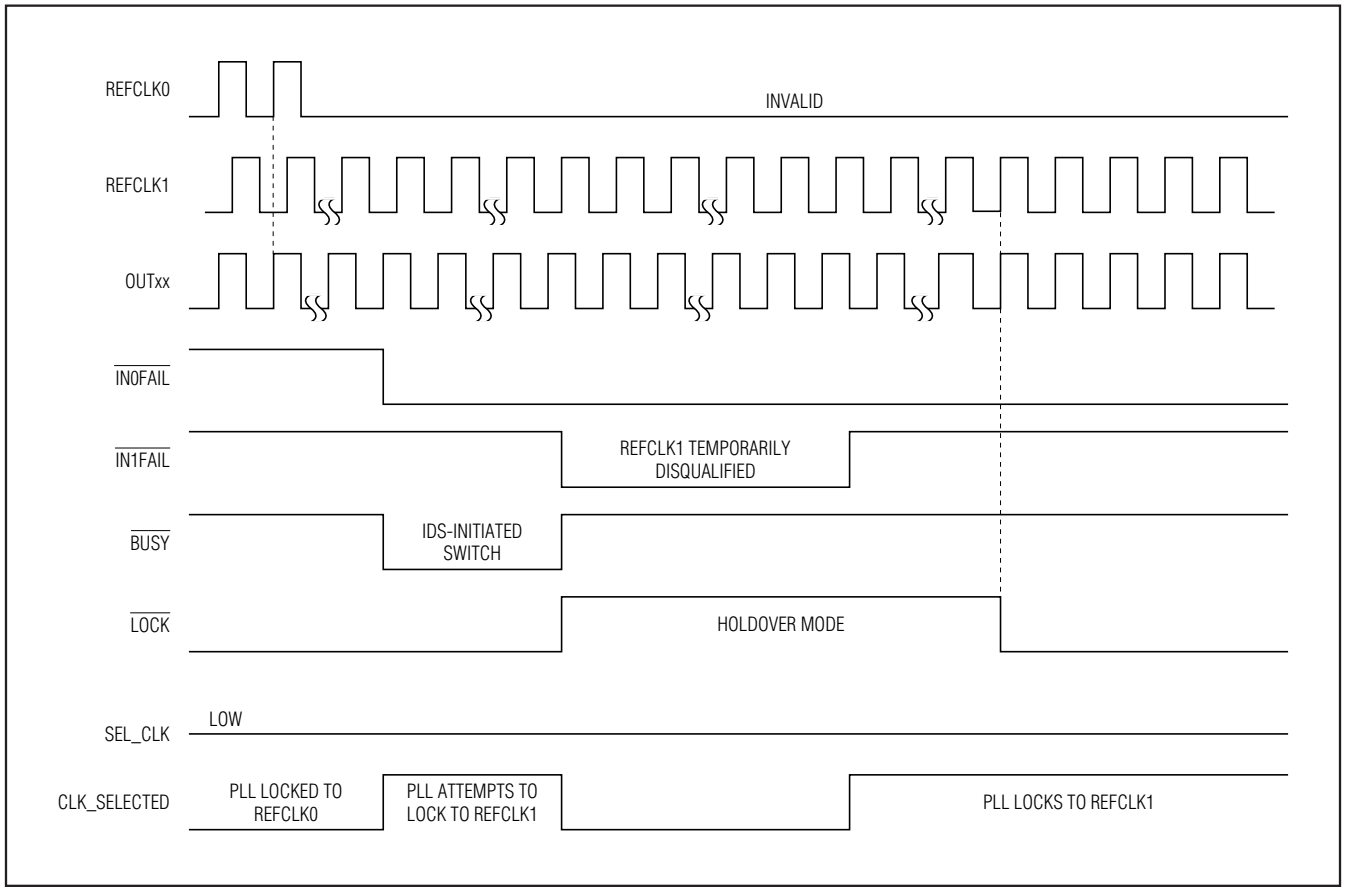


Figure 4. REFCLK0 Becomes Invalid, IDS Initiates a Switch, IDS Sequence Includes Holdover Mode

Case 3. PLL Switches to REFCLK1 and REFCLK0 Becomes Valid

After REFCLK0 fails, the PLL switches from REFCLK0 to REFCLK1, no longer making the primary reference clock selected by SEL_CLK the PLL reference clock. The PLL remains locked to REFCLK1 even if REFCLK0 becomes valid during or after switching to REFCLK1, given REFCLK1 remains valid (Figure 5).

Case 4. User-Requested PLL Switch in Automatic Switch Mode

In automatic switch mode, the MAX3678 allows the user to redefine the primary reference clock by toggling the SEL_CLK input. The PLL monitors the SEL_CLK transition and initiates a switch if the new reference clock selected by SEL_CLK is different from the current reference clock (CLK_SELECTED) and is valid.

For example, the user can request the PLL to switch back to REFCLK0 by toggling the SEL_CLK pin 0 to 1, then back to 0. The PLL monitors SEL_CLK and responds to the user-requested switch given that REFCLK0 is valid (Figure 5). The minimum SEL_CLK toggling pulse width is 2 PFD cycles (~ 30ns).

It is recommended to verify the CLK_SELECTED state to ensure that the requested switch did occur correctly. If the desired switch did not occur, the SEL_CLK pin should be toggled again.

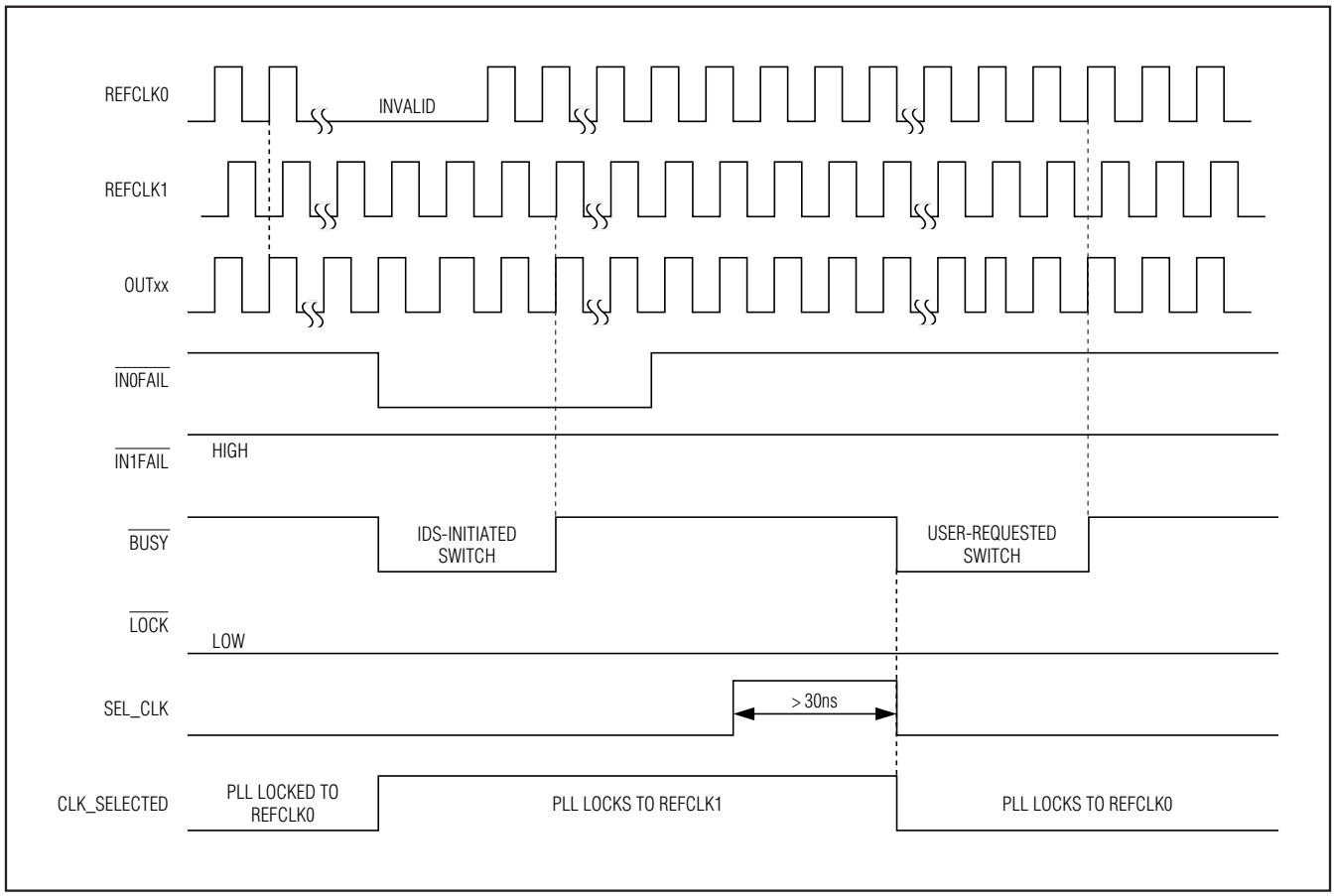


Figure 5. PLL Switches to REFCLK1 and REFCLK0 Becomes Valid, User Requests Switch

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Case 5: Both REFCLK0 and REFCLK1 Fail, PLL in Holdover Mode

If both REFCLK0 and REFCLK1 are not valid, the PLL goes into holdover mode, where the VCO frequency smoothly drifts from the previously locked frequency to the trimmed center frequency. When this happens, the clock output frequency accuracy is dominated by the on-chip VCO, which is approximately ±0.5% at room temperature and may change -100ppm/°C over temperature. The IDS continues monitoring the signal status for both REFCLK0 and REFCLK1.

If both REFCLK0 and REFCLK1 are detected valid at the same time, the PLL locks to the reference clock selected by SEL_CLK. If only one of them is valid, the PLL locks to the valid reference clock (Figure 6).

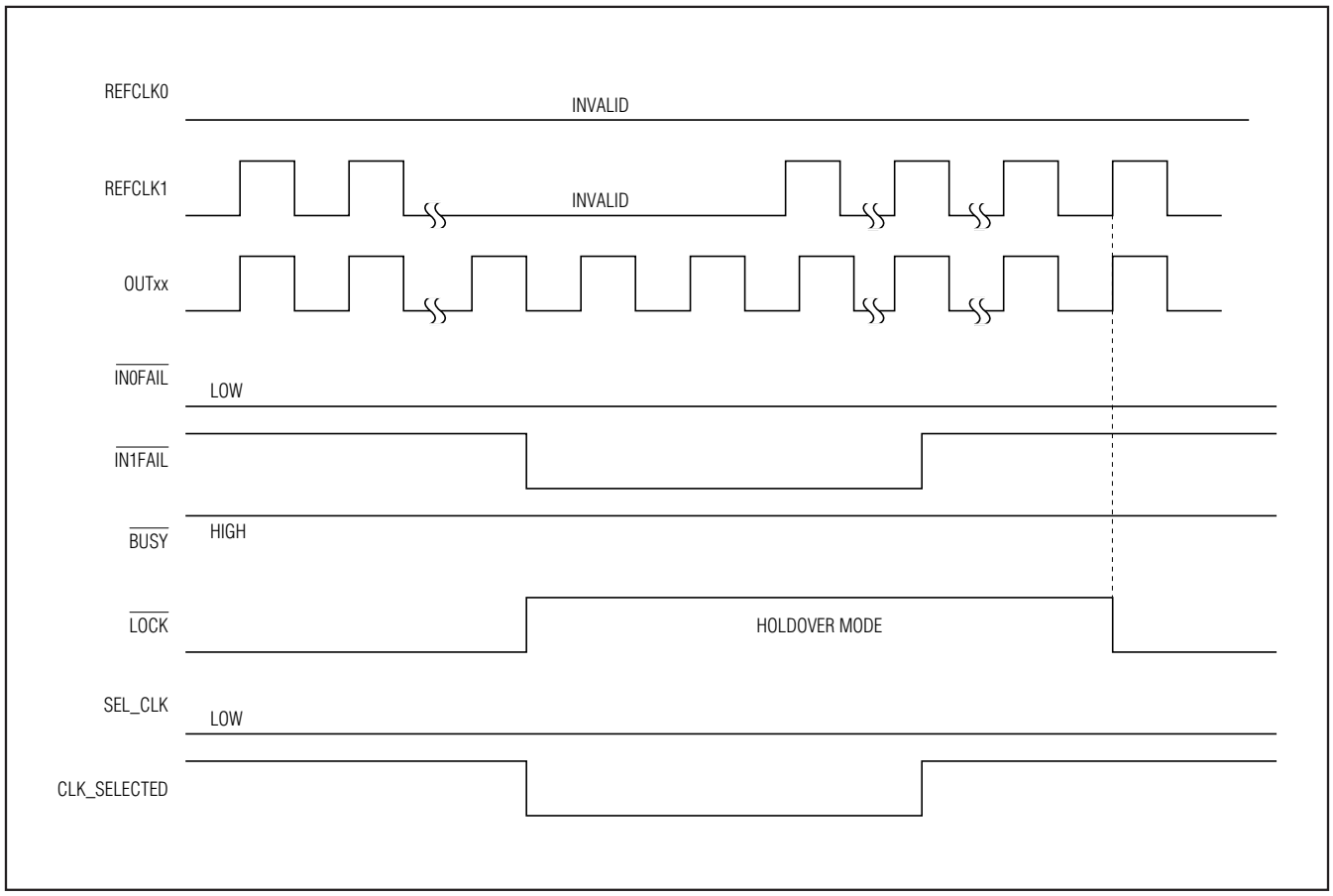


Figure 6. REFCLK0 and REFCLK1 Become Invalid, PLL in Holdover Mode

Manual Switch Mode (IDS_MODE = 1)

The manual switch mode is provided for user-controlled switching. In manual switch mode, the PLL locks to a reference clock selected by SEL_CLK. For example, if SEL_CLK = 0, the PLL locks to REFCLK0 and forces CLK_SELECTED = 0; if SEL_CLK is changed to SEL_CLK = 1, the PLL switches to REFCLK1 and makes CLK_SELECTED = 1.

In manual switch mode, the $\overline{\text{IN0FAIL}}$ and $\overline{\text{IN1FAIL}}$ status indicators are still valid, but the manual-requested switch happens whether or not the selected reference clock is valid.

Clock Failure Conditions

The MAX3678 clock failure detection is performed using the combination of amplitude qualification and PLL frequency and phase error qualification. The failure status is indicated for REFCLK0 and REFCLK1 at $\overline{\text{IN0FAIL}}$ and $\overline{\text{IN1FAIL}}$, respectively. Once an indicator is asserted low, it is latched and updated every 128 PFD cycles (~ 2µs).

It should be noted that when the PLL is locked to a reference clock, the clock failure indicator for the other reference clock is only valid for amplitude qualification and frequency qualification.

Amplitude Qualification

A reference clock input fails amplitude qualification if any of the following conditions occur:

A) Either one or both inputs (REFCLKx, $\overline{\text{REFCLKx}}$) are shorted to V_{CC} or GND.

B) Both inputs (REFCLKx, $\overline{\text{REFCLKx}}$) are disconnected from the source and have the following terminations connected: (a) 100Ω differential, (b) 130Ω to V_{CC} and 82Ω to GND at each input. See Figure 7 for positions of open circuits that can be detected.

C) Input reference clock differential swing is below the clock failure assert threshold as specified in the *Electrical Characteristics*. See Figure 8.

The response time for conditions A through C is typically between 50ns and 300ns.

Phase Qualification

A reference clock input fails phase qualification when the phase error at the PFD output exceeds the error window (ϕerr) for more than 5 of 8 PFD cycles, as specified in the *Electrical Characteristics*. A reference clock input is qualified when phase error at the PFD output is within the phase error window for 8 consecutive PFD cycles. Note that phase qualification only applies to the reference input currently being used by the PLL.

Frequency Qualification

A reference clock input becomes frequency qualified if the input frequency is within ±2.4% of the nominal frequency. The reference input becomes frequency disqualified if the input frequency moves away from the nominal frequency by more than ±8%.

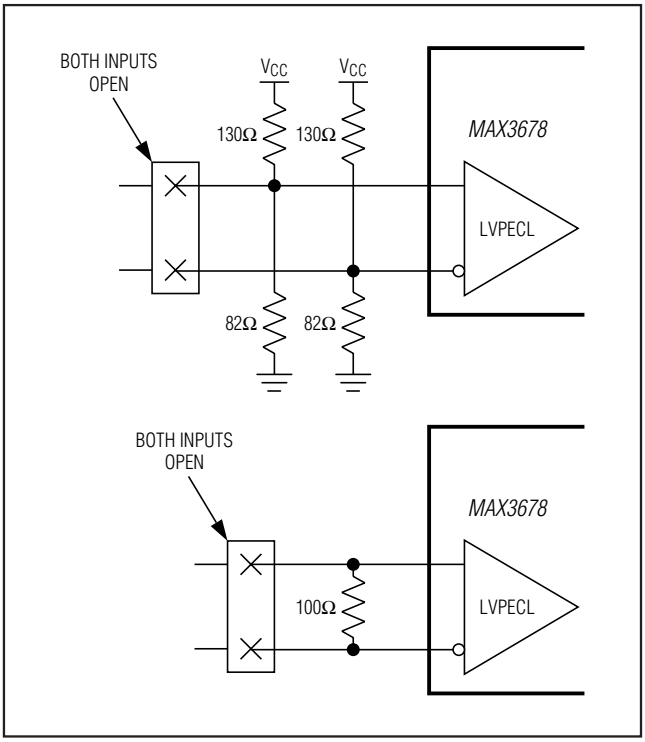


Figure 7. Positions for Open-Circuit Detection

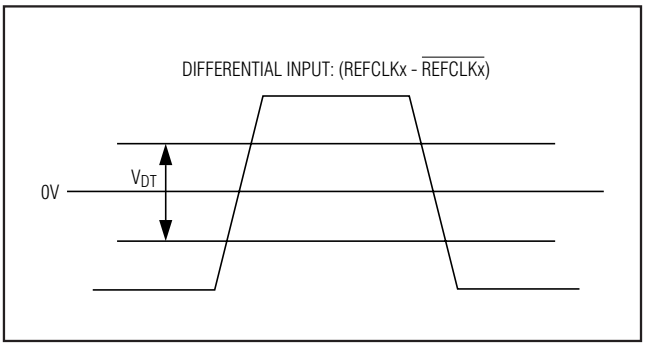


Figure 8. Input Amplitude Detection Threshold

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Table 1. Divider M Configuration for Input Frequencies

CONNECTION FROM DM PIN	INPUT FREQUENCY (MHz)
GND	66.67
V_{CC}	133.33
Open	266.67
10kΩ to GND	333.33

Table 2. Divider A Configuration for A-Group Output Frequencies

CONNECTION FROM DA PIN	OUTPUT FREQUENCY AT OUTA[3:0] (MHz)
GND	66.67
V_{CC}	133.33
Open	266.67
10kΩ to GND	333.33

Table 3. Divider B Configuration for B-Group Output Frequencies

CONNECTION FROM DB PIN	OUTPUT FREQUENCY AT OUTB[4:0] (MHz)
GND	66.67
V_{CC}	133.33
Open	266.67
10kΩ to GND	333.33

PLL Out-of-Lock Condition

If the frequency difference between the reference clock input and the VCO at the PFD input becomes within 500ppm, the PLL is considered to be in lock ($\overline{LOCK}$ = 0). When the frequency difference between the reference clock input and the VCO at the PFD input becomes greater than 800ppm, the PLL is considered out-of-lock. It should be noted that the LOCK indicator is not part of the frequency qualification used to initiate switching between reference clocks.

Input and Output Frequencies

The MAX3678 input and output dividers are configured using four-level control inputs DM, DA, and DB. Each divider is independent and can have a unique setting. The input connection and associated frequencies are listed in Tables 1, 2, and 3.

Output-Enable Controls

Each output group (A and B) has a three-level control input $\overline{OUTA_EN}$ and $\overline{OUTB_EN}$. See Tables 4 and 5 for configuration settings. When clock outputs are disabled, they are high impedance. Unused enabled outputs should be left open.

Clock Holdover

In automatic switch mode (IDS_MODE = 0), if both REFCLK0 and REFCLK1 are not valid, the lock indicator deasserts ($\overline{LOCK}$ = 1) and the PLL goes into holdover mode, where the VCO frequency smoothly drifts from the previously locked frequency to the trimmed center frequency. When this happens, the clock output frequency accuracy is dominated by the

Table 4. OUTA[3:0] Enable Control

CONNECTION FROM $\overline{OUTA_EN}$ PIN	A-GROUP OUTPUT ENABLED	A-GROUP OUTPUT DISABLED TO HIGH IMPEDANCE
GND	OUTA0, OUTA1, OUTA2, OUTA3	—
V_{CC}*	—	OUTA0, OUTA1, OUTA2, OUTA3
Open	OUTA0, OUTA1	OUTA2, OUTA3

**Connecting both $\overline{OUTA_EN}$ and $\overline{OUTB_EN}$ to V_{CC} enables a factory test mode and forces all indicators to GND. This is not a valid mode of operation.*

Table 5. OUTB[4:0] Enable Control

CONNECTION FROM $\overline{OUTB_EN}$ PIN	B-GROUP OUTPUT ENABLED	B-GROUP OUTPUT DISABLED TO HIGH IMPEDANCE
GND	OUTB0, OUTB1, OUTB2, OUTB3, OUTB4	—
V_{CC}*	OUTB0	OUTB1, OUTB2, OUTB3, OUTB4
Open	OUTB0, OUTB1, OUTB2	OUTB3, OUTB4

**Connecting both $\overline{OUTA_EN}$ and $\overline{OUTB_EN}$ to V_{CC} enables a factory test mode and forces all indicators to GND. This is not a valid mode of operation.*

on-chip VCO, which is approximately ±0.5% at room temperature and may change -100ppm/°C over temperature. While in holdover mode, IDS continues monitoring the signal status for both REFCLK0 and REFCLK1 using amplitude and frequency qualification (phase qualification is not valid). The CLK_SELECTED indicator is low and $\overline{BUSY}$ remains high. To exit holdover mode, at least one of the reference clocks must be valid and selected as the PLL reference clock.

In manual switch mode (IDS_MODE = 1), if the selected reference clock is not valid, the PLL does not go into holdover mode.

Power-On-Reset (POR)

At power-on, an internal signal is generated to hold the MAX3678 in a reset state. This internal reset time is about 20µs after V_{CC} reaches 3.0V (Figure 2). During the power-on-reset time, the outputs are held to logic-low (OUTxx = low and $\overline{OUTxx}$ = high). See Table 6 for output signal status during power-on-reset. After this internal reset time, the PLL starts to lock to the reference clock selected by SEL_CLK.

Master Reset

After power-up, an external master reset ($\overline{MR}$) can be provided to reset the internal dividers. This input requires a minimum reset pulse width of 100ns (active low) and is asynchronous to the reference clock. While $\overline{MR}$ is low, all clock outputs are held to logic-low (OUTxx = low, $\overline{OUTxx}$ = high). See Table 6 for the output signal status during master reset. When the master reset input is deasserted ($\overline{MR}$ = 1), the PLL starts to lock to the reference clock selected by SEL_CLK.

Master reset is only needed for applications where divider configurations are changed on the fly and the clock outputs need to maintain phase alignment. A master reset is not required at power-up.

External Feedback for Zero-Delay Buffer

The MAX3678 can be operated with either internal or external PLL feedback path, controlled by the FB_SEL input. Connecting FB_SEL to GND selects internal feedback. For applications where a known phase relationship between the reference clock input and the external feedback input (FB_IN, $\overline{FB_IN}$) are needed for phase synchronization, connect FB_SEL to V_{CC} for zero-delay buffer configuration and provide external feedback to the FB_IN input.

PLL Bypass Mode

PLL bypass mode is provided for test purposes. In this mode, the device receives two reference clocks to the 2:1 mux, controlled by the SEL_CLK input. The selected primary reference clock is connected to the LVPECL clock outputs directly.

In PLL bypass mode (PLL_BYPASS = 1), the output clock frequency is the same as the input clock frequency. In this case, the clock amplitude and frequency qualifications are still valid, but the phase qualification is not available and the device is running in manual switch mode.

BUSY Indicator

A $\overline{BUSY}$ signal is generated to indicate that the PLL is in the process of phase aligning to the new reference clock. When $\overline{BUSY}$ = 0, the PLL is in switch mode; when $\overline{BUSY}$ = 1, the PLL operates normally.

Table 6. Output Signal Status During Power-On-Reset or Master Reset

OUTPUT	DURING POWER-ON-RESET (FOR ~ 20µs AFTER V_{CC} > 3.0V)	DURING MASTER RESET ($\overline{MR}$ = 0)	NOTES
CLK_SELECTED	0		—
$\overline{IN0FAIL}$	1		Forced high regardless of reference input qualification.
$\overline{IN1FAIL}$	1		Forced high regardless of reference input qualification.
$\overline{LOCK}$	1		PLL out-of-lock.
$\overline{BUSY}$	1		No switch happens.
OUTA[3:0]	Logic-Low		—
OUTB[4:0]	Logic-Low		—

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Applications Information

Interfacing with LVPECL Inputs

Figure 9 shows the equivalent LVPECL input circuit for REFCLK0, REFCLK1, and FB_IN. These inputs are internally biased to allow AC- or DC-coupling and have > 40kΩ differential input impedance. When AC-coupled, these inputs can accept LVDS, CML, and LVPECL signals.

Interfacing with LVPECL Outputs

Figure 10 shows the equivalent LVPECL output circuit. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to $V_{TT} = V_{CC} - 2V$. If a separate termination voltage (V_{TT}) is not available, other termination methods can be used such as shown in Figures 11 and 12. Unused outputs, enabled or disabled, can be left open or properly terminated. For more information on LVPECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Layout Considerations

The clock inputs and outputs are critical paths for the MAX3678, and care should be taken to minimize discontinuities on the transmission lines. Maintain 100Ω differential (or 50Ω single-ended) impedance in and out of the MAX3678. Avoid using vias and sharp corners. Termination networks should be placed as close as possible to receiving clock inputs. Provide space between differential output pairs to reduce crosstalk, especially if the A and B group outputs are operating at different frequencies.

Power Supply and Ground Connections

The MAX3678 has seven supply connection pins; installation of a bypass capacitor at each supply pin is recommended. All seven supply connections should be driven from the same source to eliminate the possibility of independent power-supply sequencing. Excessive supply noise can result in increased jitter.

The 56-pin TQFN package features an exposed pad (EP), which provides a low-resistance thermal path for heat removal from the IC and must be connected to the circuit board ground plane for proper operation.

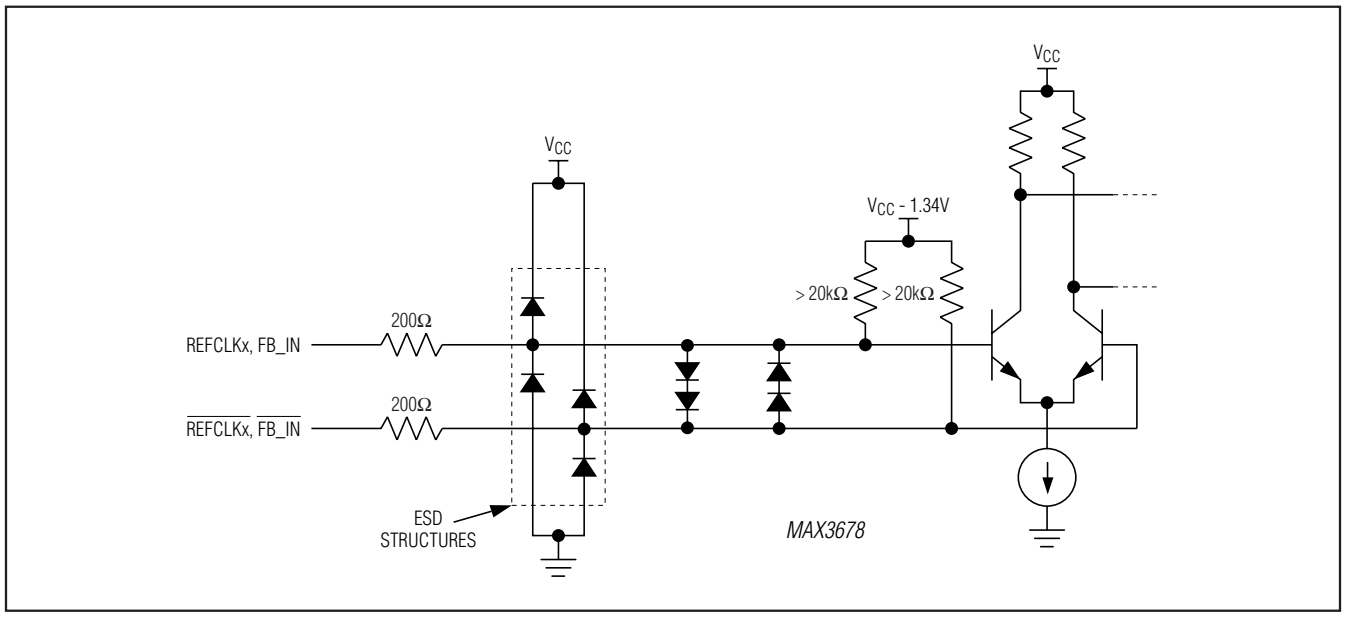


Figure 9. Equivalent LVPECL Input Circuit

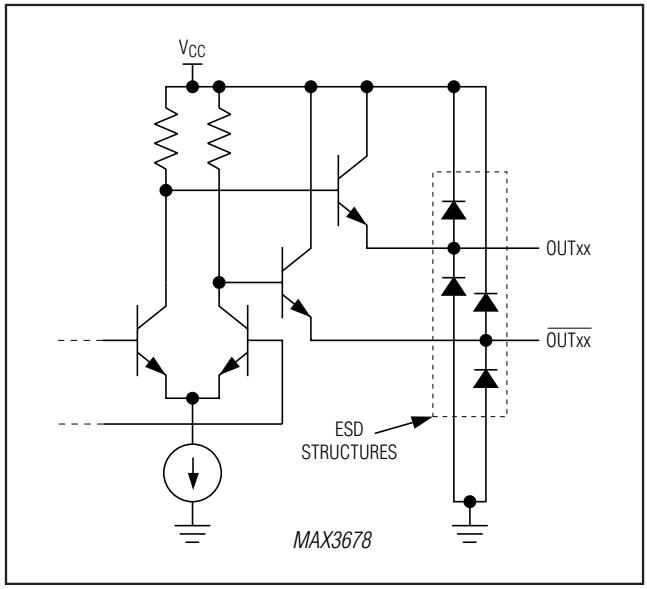


Figure 10. Equivalent LVPECL Output Circuit

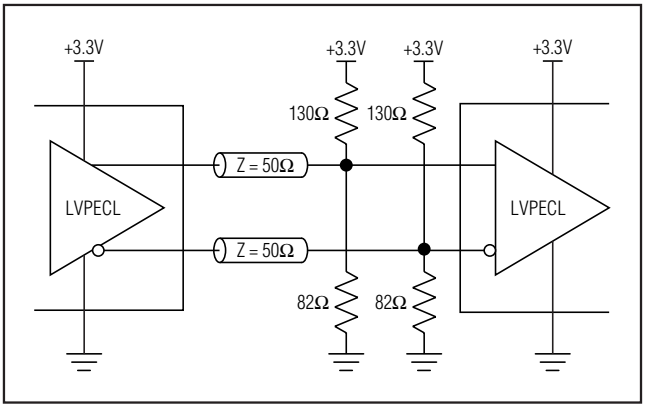


Figure 11. Thevenin Equivalent LVPECL Termination

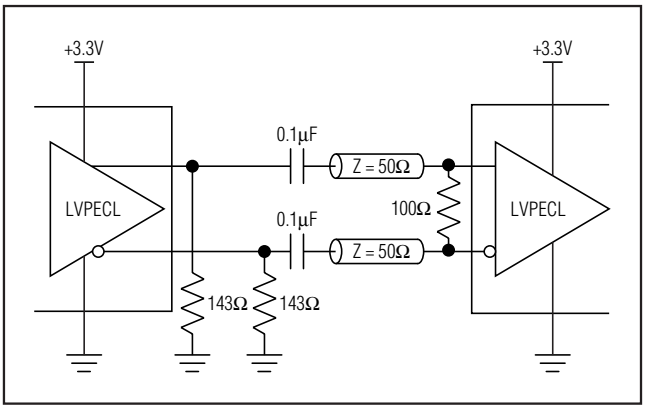
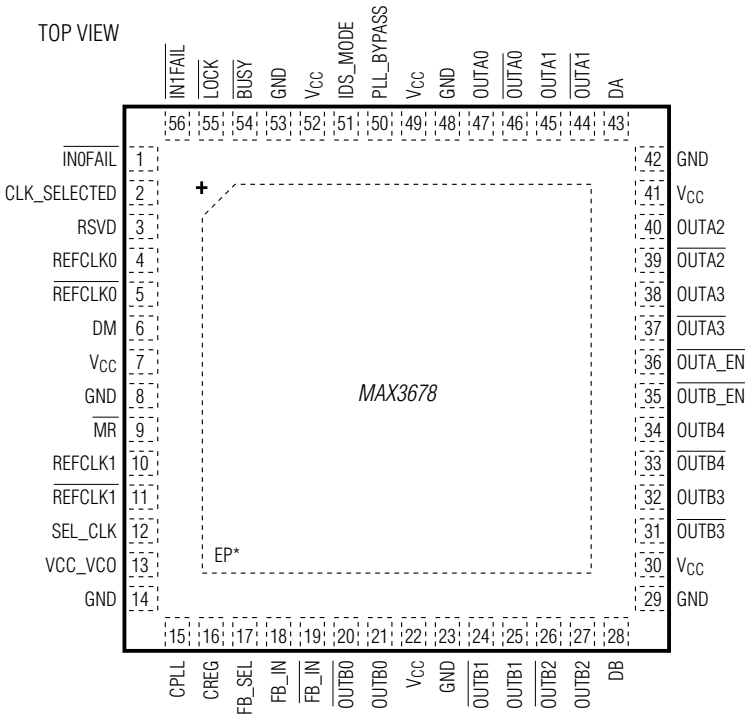


Figure 12. AC-Coupled LVPECL Termination

Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching

Pin Configuration



THIN QFN
(8mm × 8mm × 0.8mm)

*THE EXPOSED PAD OF THE TQFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

Chip Information

TRANSISTOR COUNT: 28,366

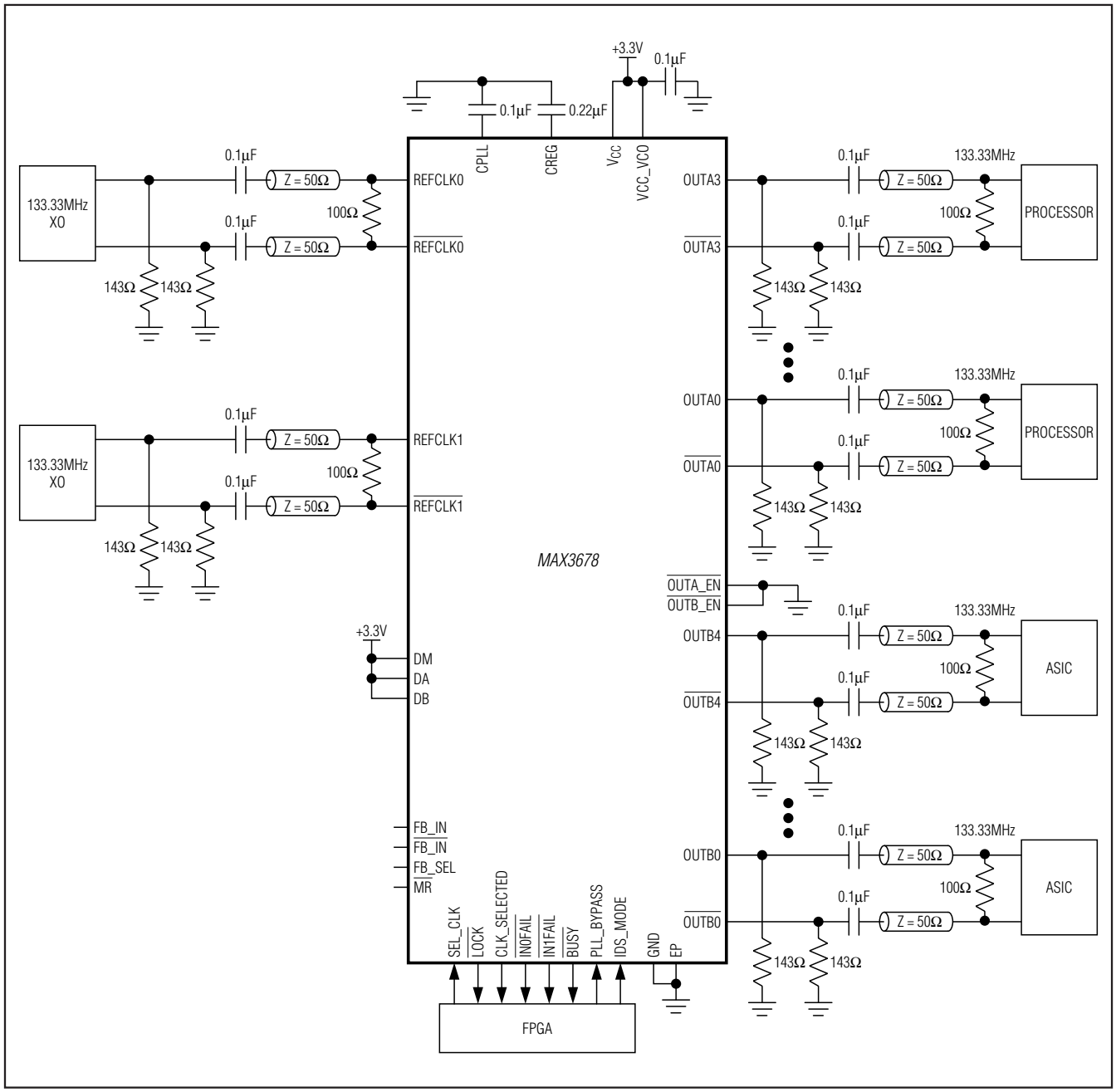
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **http://www.microsemi.com**

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5688+3	21-0135

Typical Application Circuit





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