19-5144; Rev 0; 2/10

EVALUATION KIT AVAILABLE

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

General Description

The MAX3945 is a +3.3V, multirate, low-power limiting amplifier optimized for Fibre Channel and Ethernet transmission systems at data rates up to 11.3Gbps. The high-sensitivity limiting amplifier limits the signal generated by a transimpedance amplifier into a CML-level differential output signal. All differential inputs and outputs (I/O) are optimally back terminated for 50Ω transmission line PCB design. The MAX3945's dual-path limiting amplifier has programmable filtering to optimize sensitivity for different data rates and to suppress relaxation oscillations that could occur in some optical systems. The MAX3945 incorporates two loss-of-signal (LOS) circuits and a programmable time mask for the LOS output.

A 3-wire digital interface reduces the pin count and enables control of LOS threshold, LOS polarity, LOS mode, CML output level, input offset correction, receive (Rx) polarity, Rx input filter, and Rx deemphasis without the need for external components.

The MAX3945 is packaged in a 3mm x 3mm, 16-pin TQFN package.

Applications

1x/2x/4x/8x SFF/SFP/SFP+ MSA Fibre-Channel Optical Transceiver

10GBASE-SR/LR SFP+ Optical Transceiver

10G PON ONU

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3945ETE+	-40°C to +85°C	16 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Application Circuit appears at end of data sheet.

Features

- **130mW Power Dissipation Enables < 1W SFP+ Modules**
- **Enables Single-Module Design Compliance with 1000BASE-SX/LX and 10GBASE-SR/LR Specifications**
- **-25.3dBm Optical Sensitivity at 1.25Gbps Using a 10.32Gbps ROSA**
- **Selectable 1GHz/2.1GHz/2.5GHz/3GHz Input Filters at RATE_SEL = 0 Setting**
- **Supports SFF-8431 SFP+ MSA and SFF-8472 Digital Diagnostic**
- **Total Power Dissipation of 130mW at 3.3V Power Supply with RSSI Monitor-Based LOS**
- **Total Power Dissipation of 154mW at 3.3V Power Supply with Rx Input-Based LOS**
- **4mV$_{P-P}$ Input Sensitivity at 11.3Gbps**
- **4ps$_{P-P}$ DJ at 11.3Gbps with RATE_SEL = 1**
- **4ps$_{P-P}$ DJ at 8.5Gbps with RATE_SEL = 1**
- **5ps$_{P-P}$ DJ at 4.25Gbps with RATE_SEL = 0, BW1 = 1, BW0 = 1**
- **9.0ps$_{P-P}$ DJ at 1.25Gbps with RATE_SEL = 0, BW1 = 0, BW0 = 0**
- **26ps Rise and Fall Time with RATE_SEL = 1**
- **52ps Rise and Fall Time with RATE_SEL = 0**
- **CML Output with Level Adjustment and Squelch Mode**
- **Programmable CML Output Deemphasis**
- **CML Output Polarity Select**
- **LOS Polarity Select**
- **Programmable Masking Time for the LOS Output**
- **LOS Assert/Deassert Level Adjustment**
- **Choice of Rx Input-Based LOS or RSSI Monitor-Based LOS**
- **3-Wire Digital Interface Compatible with Maxim's SFP+ Family of Products**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +4.0V
Voltage Range at SDA, SCL, CSEL, LOS, CAZ, RPMIN ..... -0.3V to (V_{CC} + 0.3V)
Voltage Range at ROUT+, ROUT- ..... (V_{CC} - 2V) to (V_{CC} + 0.3V)
Voltage Range at RIN+, RIN- ..... (V_{CC} - 1.7V) to (V_{CC} + 0.3V)
Current Range Into LOS ..... -1mA to +5mA
Current Range Into SDA ..... -1mA to +1mA
Current Out of ROUT+, ROUT- 40mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 14.7mW/°C above +70°C) 1.176W
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Includes the CML output current, V_{DIFF_ROUT} = 400mV_{P-P}, RXDE_EN = 0, LOS1_EN = 1, LOS2_EN = 0		46.6	62	mA
		Includes the CML output current, V_{DIFF_ROUT} = 400mV_{P-P}, RXDE_EN = 0, LOS1_EN = 0, LOS2_EN = 1		39.4	52.5	
Power-Supply Voltage	V_{CC}		2.85		3.63	V
Power-Supply Noise		f < 10MHz			100	mV_{P-P}
		10MHz < f < 20MHz			10	
GENERAL						
Input Data Rate			1.06	10.32	11.3	Gbps
Input/Output SNR			14.1			
BER					10E-12	
POWER-ON RESET (POR)						
POR Deassert Threshold				2.55	2.75	V
POR Assert Threshold			2.3	2.45		V
INPUT SPECIFICATIONS						
Differential Input Resistance RIN+/RIN-	R_{IN_DIFF}		75	100	125	Ω
Input Sensitivity (Note 1)	V_{INMIN}	RATE_SEL = 1, input transition time 25ps, 10.32Gbps, PRBS23-1 pattern		4	8	mV_{P-P}
		RATE_SEL = 0, input transition time 260ps, 1.25Gbps, K28.5 pattern		1	2	
Input Overload	V_{INMAX}		1.2			V_{P-P}
Input Return Loss	SDD11	DUT is powered on, f ≤ 5GHz		10		dB
		DUT is powered on, f ≤ 16GHz		7		
	SCC11	DUT is powered on, 1GHz < f ≤ 5GHz		13		dB
		DUT is powered on, 1GHz < f ≤ 16GHz		5		
RPMIN Input-Current High	I_{IH}	LOS1_EN = 0 and LOS2_EN = 1, V_{RPMIN} = 2V		50		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External RPMIN Filter Capacitor			100			pF
OUTPUT SPECIFICATIONS						
Differential Output Resistance ROUT+/ROUT-	$R_{OUTDIFF}$		75	100	125	Ω
Output Return Loss	SDD22	DUT is powered on, f ≤ 5GHz		13		dB
		DUT is powered on, f ≤ 16GHz		7		
	SCC22	DUT is powered on, 1GHz < f ≤ 5GHz		10		
		DUT is powered on, 1GHz < f ≤ 16GHz		6		
Differential Output-Voltage High		$5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 0, SET_CML[7:0] = 169d (decimal)	595	800	1005	mV_{P-P}
		$10mV_{P-P} \le V_{IN} \le 1200mV$, RATE_SEL = 1, SET_CML[7:0] = 181d	595	800	1005	
Differential Output-Voltage Medium		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 1, SET_CML[7:0] = 91d	300	400	515	mV_{P-P}
SET_CML DAC Range			60		255	Decimal
Differential Output Signal When Squelched (Note 1)		Outputs AC-coupled, SET_CML[7:0] = 181d, at 8.5Gbps, SQ_EN = 1		6	15	mV_{P-P}
Data Output Transition Time (20% to 80%) (Note 1)	t_R/t_F	$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, $V_{DIFF_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 25ps, pattern 11110000		26	35	ps
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, $V_{DIFF_ROUT} = 800mV_{P-P}$, input transition time 260ps, pattern 11110000		52	90	
TRANSFER CHARACTERISTICS						
Deterministic Jitter (Notes 1, 2)	DJ	$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 8.5Gbps, RATE_SEL = 1, $V_{DIFF_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	8	ps_{P-P}
		$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, $V_{DIFF_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	9	
		$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 11.3Gbps, RATE_SEL = 1, $V_{DIFF_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	9	
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, BW1 = 0, BW0 = 0, $V_{DIFF_ROUT} = 800mV_{P-P}$, input transition time 260ps		9	30	
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 4.25Gbps, RATE_SEL = 0, BW1 = 1, BW0 = 1, $V_{DIFF_ROUT} = 800mV_{P-P}$, input transition time 28ps		5	10	

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Random Jitter (Note 1)	RJ	Input = 60mV$_{P-P}$ at 10.32Gbps, RATE_SEL = 1, RXDE_EN = 0, input transition time 28ps, pattern 11110000, V_{DIFF_ROUT} = 800mV$_{P-P}$		0.28	0.51	ps$_{RMS}$
Low-Frequency Cutoff (Simulated Value)		RATE_SEL = 0, C_{CAZ} = 0.1µF		2		kHz
		RATE_SEL = 1, C_{CAZ} = 0.1µF		0.7		
Small-Signal Bandwidth (Simulated Value)	f_{3dB}	RATE_SEL = 0, BW1 = 0, BW0 = 0		1.0		GHz
		RATE_SEL = 0, BW1 = 0, BW0 = 1		2.1		
		RATE_SEL = 0, BW1 = 1, BW0 = 0		2.5		
		RATE_SEL = 0, BW1 = 1, BW0 = 0		3.0		
		RATE_SEL = 1		9		
Rx INPUT-BASED LOS SPECIFICATIONS (LOS1_EN = 1 and LOS2_EN = 0) (Note 1)						
LOS Assert Sensitivity Range		(Note 3)	14		77	mV$_{P-P}$
SET_LOS DAC Range			7		63	Decimal
LOS Hysteresis		10log($V_{DEASSERT}$/V_{ASSERT})	1.25	2.1		dB
LOS Assert/Deassert Time		(Note 4)	2.3	20	80	µs
Low Assert Level		SET_LOS[5:0] = 7d (Note 3)	8	11	14	mV$_{P-P}$
Low Deassert Level			14	18	22	
Medium Assert Level		SET_LOS[5:0] = 32d (Note 3)	39	49	58	mV$_{P-P}$
Medium Deassert Level			65	82	95	
High Assert Level		SET_LOS[5:0] = 63d (Note 3)	77	96	112	mV$_{P-P}$
High Deassert Level			127	158	182	
LOS Output Masking Time Range		SET_LOSTIMER[6:0] = 0d for minimum and SET_LOSTIMER[6:0] = 127d for maximum	0		2920	µs
LOS Output Masking DAC Resolution		SET_LOSTIMER[6:0] = 1d to 127d	23	35	50	µs
RSSI MONITOR-BASED LOS SPECIFICATIONS (LOS1_EN = 0 and LOS2_EN = 1) (Note 1)						
LOS Assert Sensitivity Range		(Note 5)	8.3		90	mV
SET_LOS DAC Range			4		63	Decimal
LOS Hysteresis		10log($V_{DEASSERT}$/V_{ASSERT})	1.25	2.1		dB
LOS Assert/Deassert Time		(Note 4)	2.3	20	80	µs
Low Assert Level		SET_LOS[5:0] = 4d (Note 5)	5.1	6.7	8.3	mV
Low Deassert Level			9.0	10.8	12.7	
Medium Assert Level		SET_LOS[5:0] = 32d (Note 5)	45	50	55	mV
Medium Deassert Level			77	85	92	
High Assert Level		SET_LOS[5:0] = 63d (Note 5)	90	98	106	mV
High Deassert Level			153	167	180	
LOS Output Masking Time Range		SET_LOSTIMER[6:0] = 0d for minimum and SET_LOSTIMER[6:0] = 127d for maximum	0		2920	µs
LOS Output Masking DAC Resolution		SET_LOSTIMER[6:0] = 1d to 127d	23	35	50	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT LEVEL VOLTAGE DAC (SET_CML)						
Full-Scale Voltage	V_{FS}	100Ω differential resistive load, RXDE_EN = 0		1192		mV_{P-P}
		100Ω differential resistive load, RATE_SEL = 1, RXDE_EN = 1, RXDE1 = 1, RXDE0 = 1 (maximum deemphasis)		828		
Resolution		100Ω differential resistive load, RXDE_EN = 0		4.5		mV_{P-P}
		100Ω differential resistive load, RATE_SEL = 1, RXDE_EN = 1, RXDE1 = 1, RXDE0 = 1 (maximum deemphasis)		3.3		
Integral Nonlinearity	INL	SET_CML[7:0] > 60d		±0.9		LSB
LOS THRESHOLD VOLTAGE DAC (SET_LOS)						
Full-Scale Voltage	V_{FS}	LOS1_EN = 1, LOS2_EN = 0		96		mV_{P-P}
		LOS1_EN = 0, LOS2_EN = 1		98		mV
Resolution		LOS1_EN = 1, LOS2_EN = 0		1.52		mV_{P-P}
		LOS1_EN = 0, LOS2_EN = 1		1.56		mV
Integral Nonlinearity	INL	SET_LOS[5:0] > 3d		±0.7		LSB
CONTROL I/O SPECIFICATIONS						
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC}	V_{CC} - 0.5		V_{CC}	V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC}	0		0.4	V
3-WIRE DIGITAL I/O SPECIFICATIONS (SDA, CSEL, SCL)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			0.082		V
Input Leakage Current	$I_{IL,IH}$	V_{IN} = 0V or V_{CC}, internal pullup or pulldown (75kΩ typ)			85	µA
Output High Voltage	V_{OH}	External pullup of 4.7kΩ to V_{CC}	V_{CC} - 0.5		V_{CC}	V
Output Low Voltage	V_{OL}	External pullup of 4.7kΩ to V_{CC}	0		0.4	V
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (see Figure 5)						
SCL Clock Frequency	f_{SCL}		0	400	1000	kHz
SCL Pulse-Width High	t_{CH}		500			ns
SCL Pulse-Width Low	t_{CL}		500			ns
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL External Load	C_B	Total bus capacitance on one line with 4.7kΩ to V_{CC}			20	pF

Note 1: Guaranteed by design and characterization, T_A = -40°C to +95°C.

Note 2: Deterministic jitter is measured with a repeating K28.5 pattern [00111110101100000101] for 1.25Gbps to 8.5Gbps data. At 10.32Gbps and 11.3Gbps, a repeating K28.5 plus 59 0s and K28.5 plus 59 1s pattern is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ).

Note 3: LOS1_EN = 1, data rates of 1.25Gbps to 8.5Gbps with K28.5 pattern, and 6.4GHz input filter. For data rates of 10.32Gbps to 11.3Gbps, the input filter is 12.5GHz and the pattern is PRBS23-1.

Note 4: Measurement includes an input AC-coupling capacitor of 100nF and C_{CAZ} of 100nF. The signal at the RIN or RPMIN input is switched between two amplitudes: Signal_ON and Signal_OFF.

1) Receiver operates at sensitivity level plus 1dB power penalty
   a) Signal_OFF = 0
      Signal_ON = (+8dB) + 10log(min_assert_level)
   b) Signal_ON = (+1dB) + 10log(max_deassert_level)
      Signal_OFF = 0
2) Receiver operates at overload
   Signal_OFF = 0
   Signal_ON = $1.2V_{P-P}$
   max_deassert_level and min_assert_level are measured for one SET_LOS setting

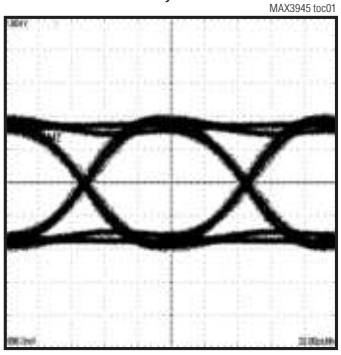
Note 5: LOS1_EN = 0, LOS2_EN = 1, DC voltage applied to the RPMIN input.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

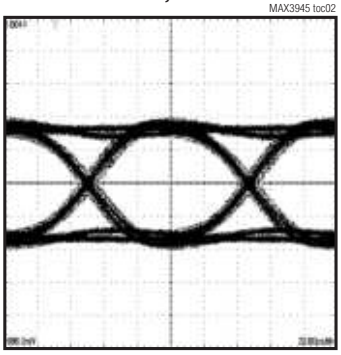
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

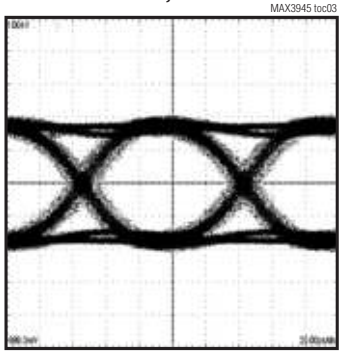
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -10dBm, RXDE1 = 1, RXDE0 = 0



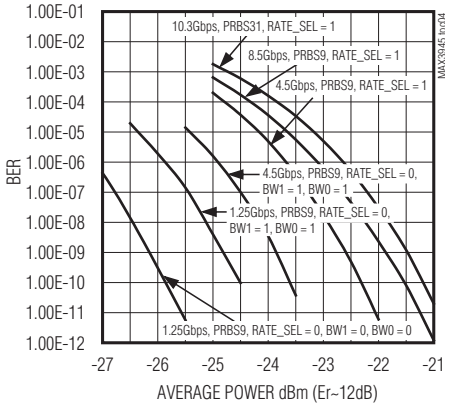
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -15dBm, RXDE1 = 1, RXDE0 = 0



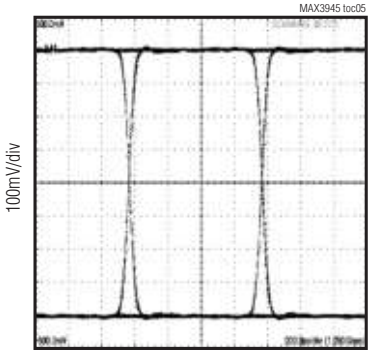
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -20dBm, RXDE1 = 1, RXDE0 = 0



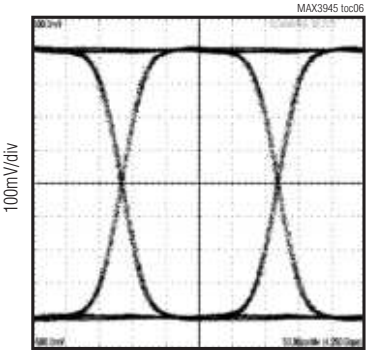
OPTICAL BER CURVES (NEC NR3312)



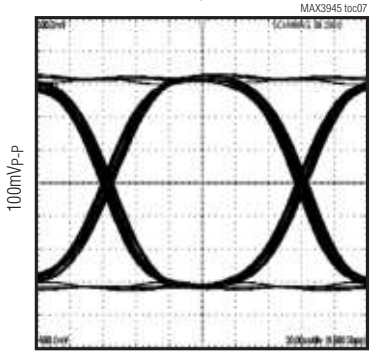
K28.5 PATTERN AT 1.25Gbps, SET_CML[7:0] = 169d, RATE_SEL = 0, BW0 = 0, BW1 = 0



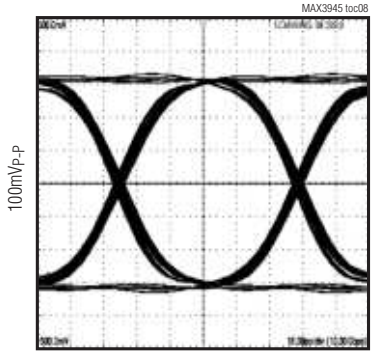
K28.5 PATTERN AT 4.25Gbps, SET_CML[7:0] = 169d, RATE_SEL = 0, BW0 = 1, BW1 = 1



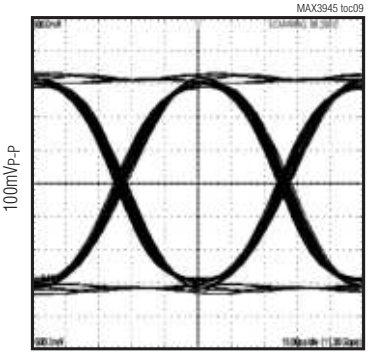
K28.5 PATTERN AT 8.5Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0



K28.5 PATTERN AT 10.3Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0



K28.5 PATTERN AT 11.3Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0

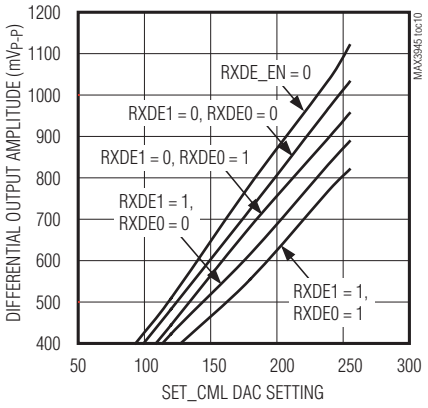


1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

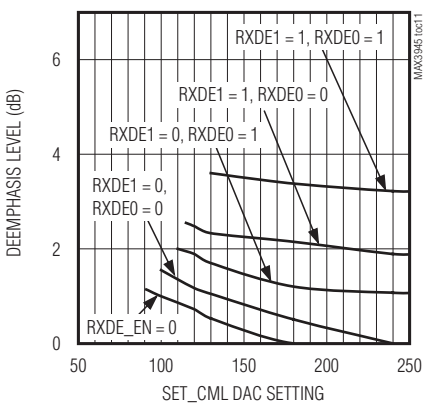
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

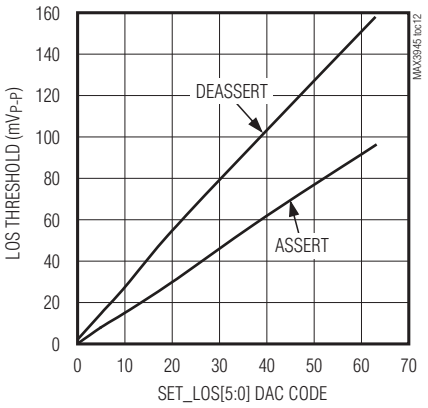
DIFFERENTIAL OUTPUT SIGNAL LEVEL vs. SET_CML DAC SETTING



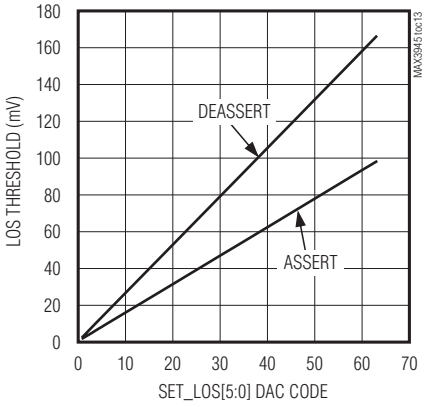
DEEMPHASIS VALUE vs. SET_CML DAC SETTING (RATE_SEL = 1)



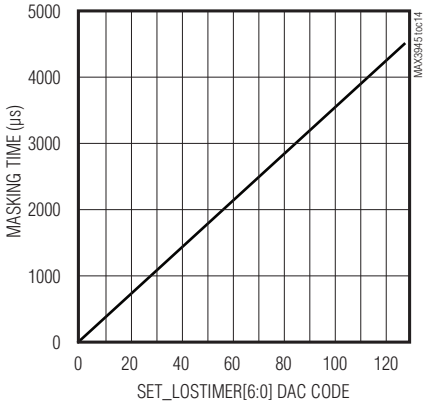
Rx INPUT-BASED LOS THRESHOLD vs. DAC CODE (LOS1_EN = 1 AND LOS2_EN = 0)



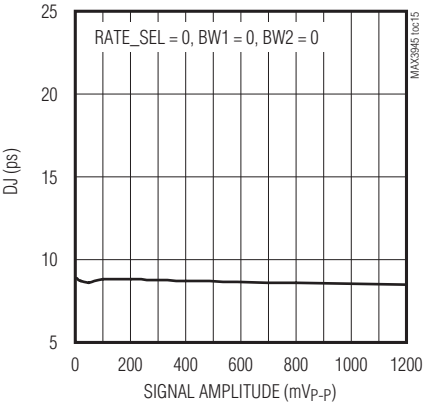
RSSI MONITOR-BASED LOS THRESHOLDS (LOS1_EN = 0 AND LOS2_EN = 1)



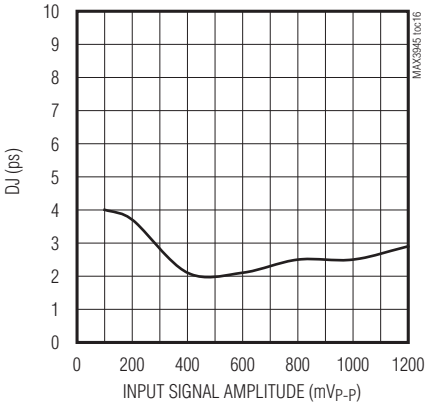
LOS MASKING TIME vs. DAC SETTING



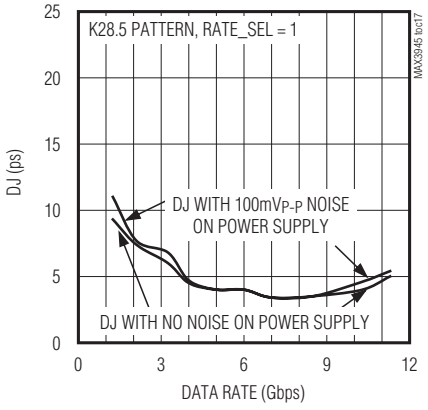
DETERMINISTIC JITTER vs. INPUT AMPLITUDE AT 1.25Gbps (K28.5 PATTERN, 933MHz INPUT FILTER)



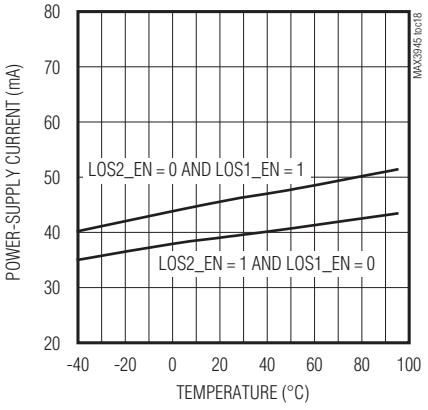
DETERMINISTIC JITTER AT 10.32Gbps (PRBS7 PATTERN WITH 100 CIDs, RATE_SEL = 1)



DETERMINISTIC JITTER vs. DATA RATE (INPUT = 100mVP-P)



POWER-SUPPLY CURRENT vs. TEMPERATURE (SET_CML[7:0] = 91d)

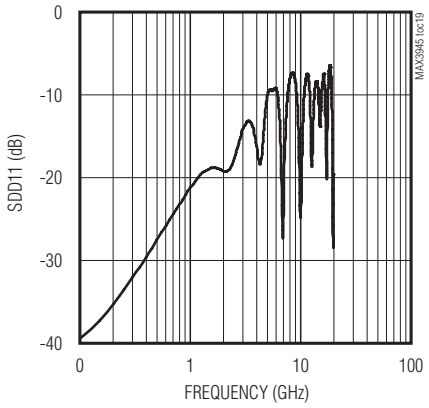


1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

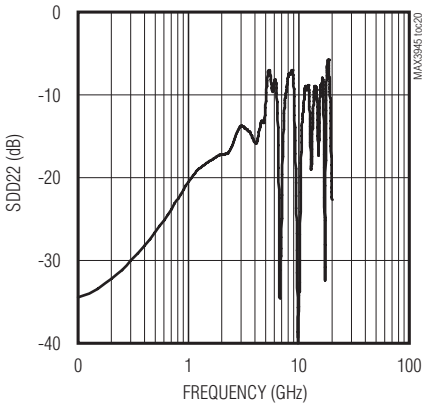
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

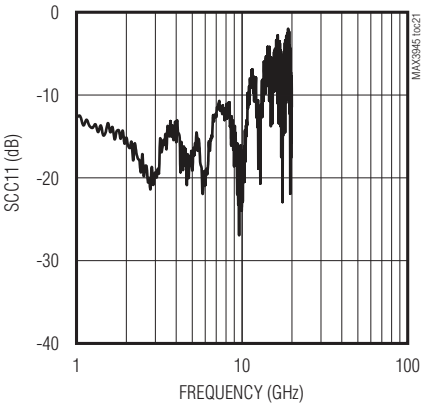
INPUT RETURN GAIN (SDD11) (INPUT POWER OF 0dBm, ENABLED)



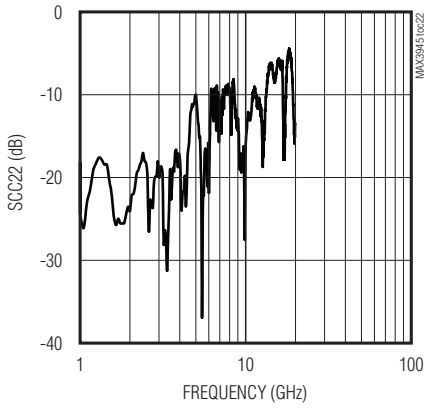
OUTPUT RETURN GAIN (SDD22) (INPUT POWER OF 0dBm, ENABLED)



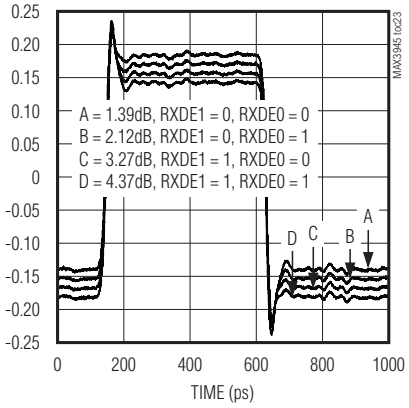
INPUT COMMON-MODE RETURN GAIN (SCC11) (INPUT POWER OF 0dBm, ENABLED)



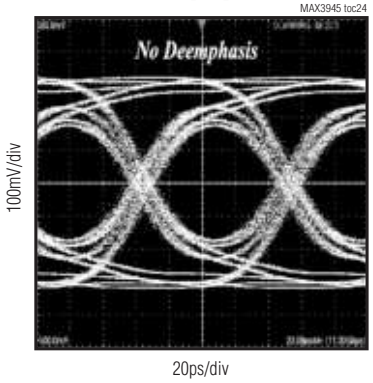
OUTPUT COMMON-MODE RETURN GAIN (SCC22) (INPUT POWER OF 0dBm, ENABLED)



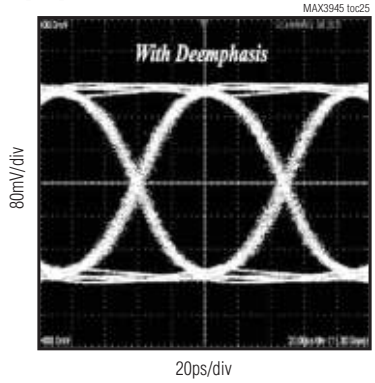
TRANSIENT RESPONSE (10.3Gbps, 10 ONES 10 ZEROS PATTERN, SET_CML[7:0] = 92d)



ELECTRICAL EYE DIAGRAM AFTER 6in OF FR4 AND 72in OF CABLE WITH NO DEEMPHASIS (11.3Gbps K28.5, RATE_SEL = 1, SET_CML[7:0] = 160d, RXDE_EN = 0)

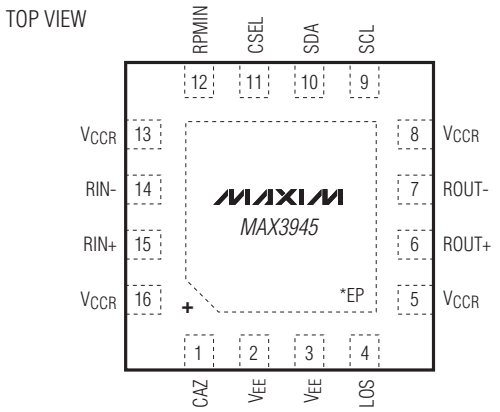


ELECTRICAL EYE DIAGRAM AFTER 6in OF FR4 AND 72in OF CABLE WITH DEEMPHASIS (11.3Gbps K28.5, RATE_SEL = 1, SET_CML[7:0] = 160d, RXDE_EN = 1, RXDE0 = 1, RXDE1 = 1)



1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

Pin Configuration



THIN QFN (3mm × 3mm)

*THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Pin Description

PIN	NAME	FUNCTION
1	CAZ	Offset-Correction Loop Capacitor. A capacitor connected between this pin and the adjacent V_{EE} pin sets the time constant of the offset-correction loop. The offset correction can be disabled through the digital interface by setting bit AZ_EN = 0 and by connecting this pin to ground.
2, 3	V_{EE}	Ground for Limiting Amplifier
4	LOS	Loss-of-Signal Output. This output is an open-drain output. LOS is asserted when the level of the input signal drops below the preset threshold set by SET_LOS[5:0]. LOS is deasserted when the signal level is above the threshold. The polarity of the LOS output can be inverted by setting LOS_POL = 0. The LOS circuitry can be disabled by setting LOS1_EN = 0 and LOS2_EN = 0. See Table 8.
5, 8, 13, 16	V_{CCR}	Power Supply. Provides supply voltage to the limiting amplifier. All pins must be connected to the supply voltage.
6	ROUT+	Noninverted Output, CML. Back terminated for 50Ω load.
7	ROUT-	Inverted Output, CML. Back terminated for 50Ω load.
9	SCL	Serial-Clock Input, TTL/CMOS. This pin has a 75kΩ internal pulldown.
10	SDA	Serial-Data Bidirectional I/O. TTL/CMOS input and open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ pullup resistor to meet the 3-wire digital timing specification. (Data line collision protection is implemented.)
11	CSEL	Chip-Select Input, TTL/CMOS. Internally pulled down by a 75kΩ resistor. CSEL = 1 starts an SPI cycle, while CSEL = 0 ends the SPI cycle and resets the control state machine.
12	RPMIN	High-Impedance Receive Power-Monitor Input. Connect to ground when not used.
14	RIN-	Inverted Data Input, CML, with 50Ω Termination
15	RIN+	Noninverted Data Input, CML, with 50Ω Termination
—	EP	Exposed Pad. Must be soldered to circuit ground.

Detailed Description

The MAX3945 is designed to operate from 1.0625Gbps to 11.3Gbps. It consists of a dual-path limiter, offset-correction circuitry, CML output stage, and LOS circuitry. The characteristics of the MAX3945 can be controlled through the on-chip 3-wire interface. The registers that control the part's functionality are RXCTRL1, RXCTRL2, RXSTAT, SET_CML, SET_LOS, MODECTRL, and SET_LOSTIMER. The MAX3945 provides integrated DACs to allow the use of low-cost controller ICs. Figure 1 shows simplified input and output structures.

Dual-Path Limiter

The limiting amplifier features a low data-rate path (1.0625Gbps to 4.25Gbps) and a high data-rate path (up to 11.3Gbps), allowing for overall system optimization. Figure 2 shows the functional diagram. Data path selection is controlled by the RATE_SEL bit. The low data-rate path further features a programmable filter that provides optimization for 1.0625Gbps, 1.25Gbps, 2.125Gbps, and 4.25Gbps operation. It is important to tailor the bandwidth of the first stages to get the best receive sensitivity and to reduce the maximum receive bandwidth for a given data rate. Table 1 summarizes the RATE_SEL, BW1, and BW0 control bit functions. The high data-rate mode (RATE_SEL = 1) is recommended for operation up to 11.3Gbps.

The polarity of ROUT+/ROUT- relative to RIN+/RIN- is programmed by the RX_POL bit, as shown in Table 2.

Offset-Correction Circuitry

The offset-correction circuitry is provided to remove PWD caused by intrinsic offset voltages within the differential amplifier stages. An external 0.1µF capacitor connected between the CAZ pin and ground sets the offset-correction loop cutoff frequency to approximately 2kHz when RATE_SEL = 0 and to approximately 0.7kHz when RATE_SEL = 1. The offset-correction loop can be disabled using the AZ_EN bit, as shown in Table 3.

CML Output Stage

CML Output Enable and Squelch

The CML output stage is optimized for differential 100Ω loads. The output stage is controlled by a combination of the RX_EN and SQ_EN bits and the internal LOS status. See Table 4.

Table 1. Rate Select and Bandwidth Control

RXCTRL1[3:1]			OPERATION MODE DESCRIPTION		
BW1	BW0	RATE_SEL	DATA RATE (Gbps)	FILTER BANDWIDTH (MHz)	RISE/FALL TIME (ps)
0	0	0	1.0625 to 1.25	1000	52
0	1	0	2.125	2100	52
1	0	0	2.125	2500	52
1	1	0	4.25	3000	52
X	X	1	11.3	9000	26

Table 2. Signal Polarity Control

RX_POL	OPERATION MODE DESCRIPTION
0	Inversed polarity of the differential signal path
1	Normal polarity of the differential signal path

Table 3. Offset-Correction Enable/Disable Control

AZ_EN	OPERATION MODE DESCRIPTION
0	Autozero loop is disabled
1	Autozero loop is enabled

Table 4. CML Output Stage Operation Modes

RX_EN	SQ_EN	LOS STATUS	OPERATION MODE DESCRIPTION
0	X	X	CML output disabled
1	0	X	CML output enabled
1	1	0	CML output enabled
1	1	1	CML output disabled

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

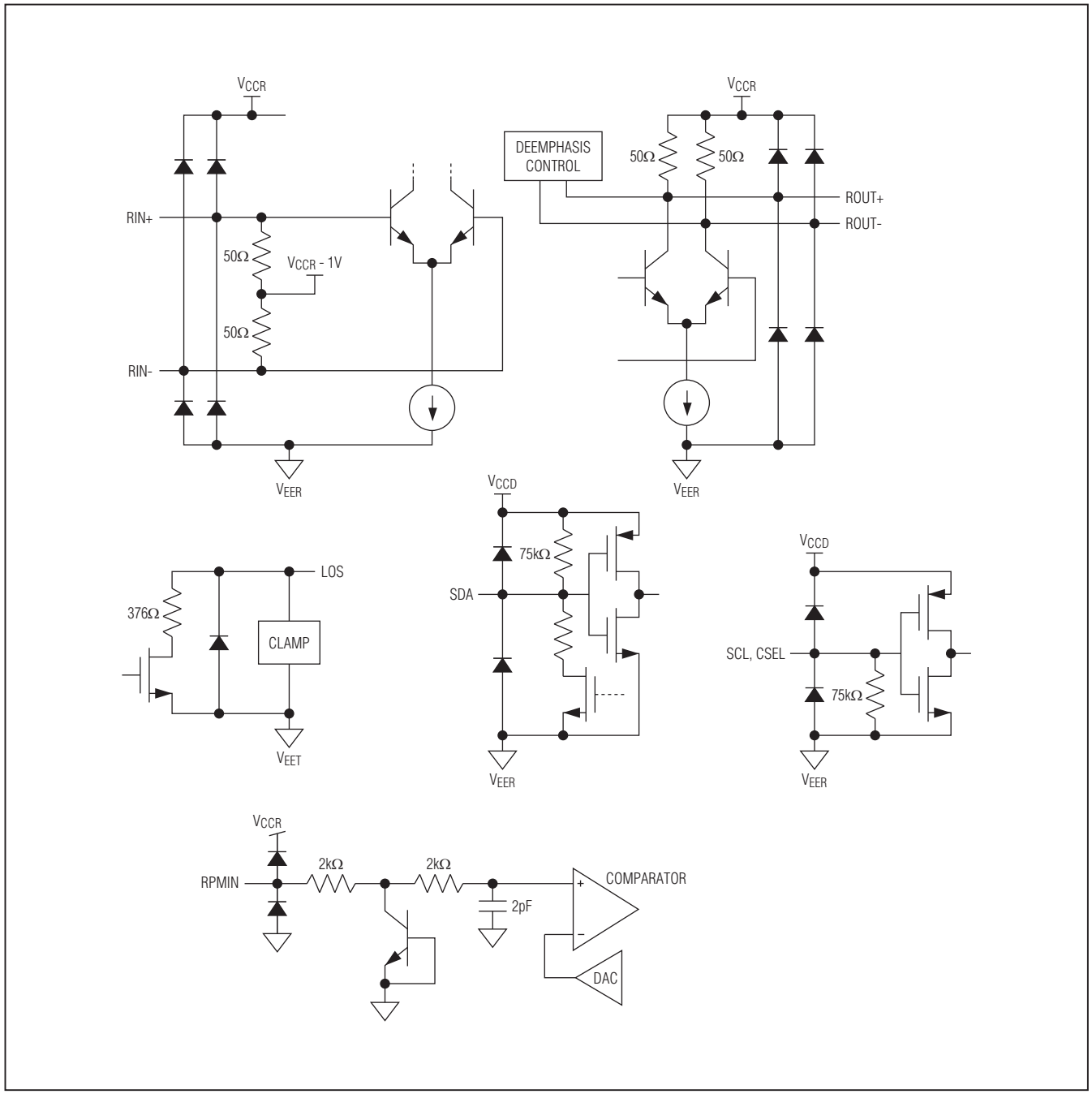


Figure 1. Simplified Input/Output Structures

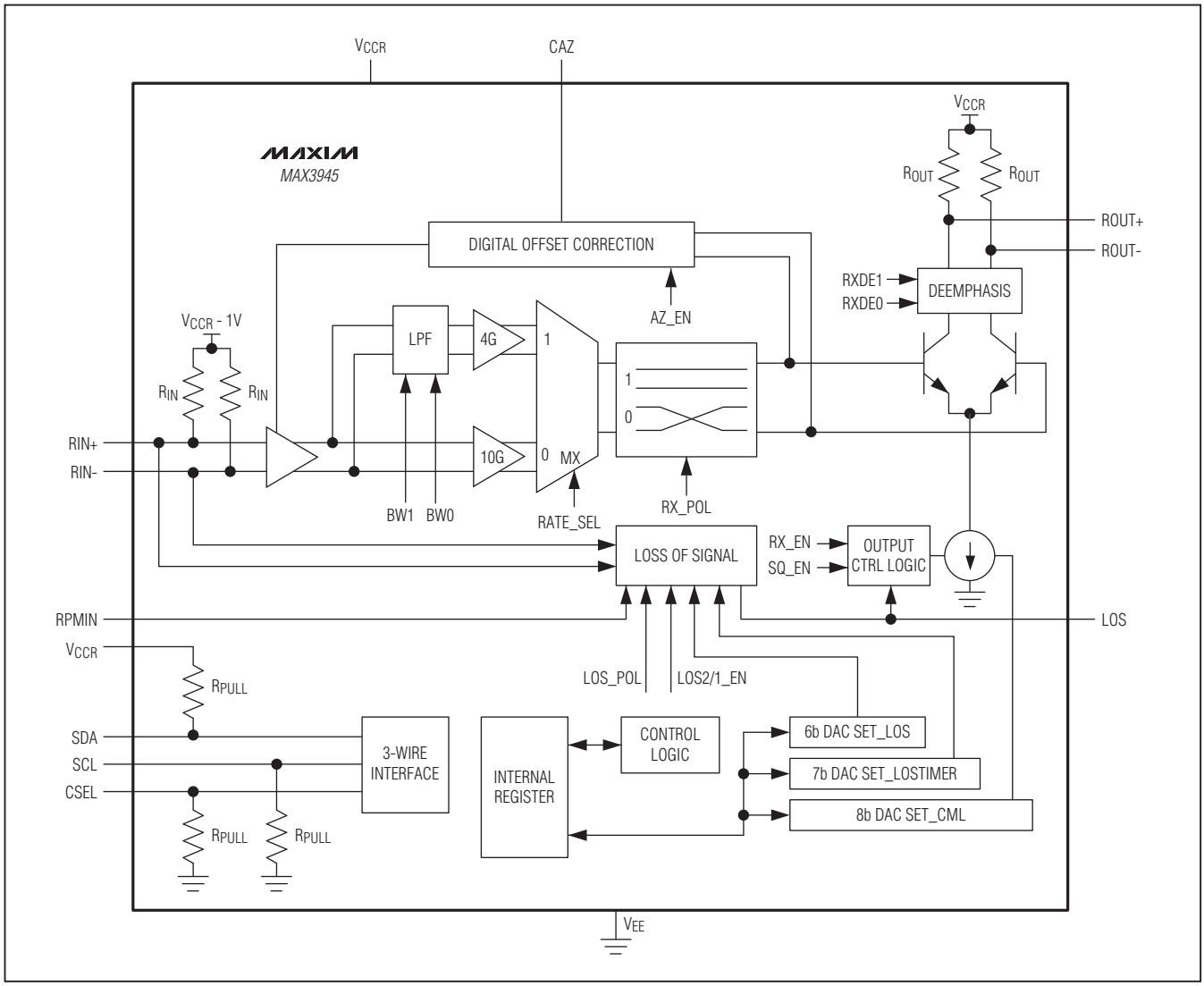


Figure 2. Functional Diagram

CML Output Deemphasis

The CML output stage is optimized for differential 100Ω transmission lines on a standard FR4 board. The RXDE1 and RXDE0 bits add programmable analog output deemphasis to compensate for FR4 board losses and SFP connector losses. Table 5 describes the deemphasis control settings.

Programmable CML Output Amplitude

The 8-bit SET_CML register controls the amplitude of the CML output stage. The maximum programmable output level depends on the operational mode of the MAX3945. These output levels (which assume an ideal 100Ω differential load) and their corresponding control bits are described in Table 6. Table 7 shows the output DAC resolution dependency.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

Table 5. Output Signal Deemphasis Control

RXCTRL2[1]	RXCTRL1[7:6]		OPERATION MODE DESCRIPTION	
RXDE_EN	RXDE1	RXDE0	MODE	DEEMPHASIS (dB)
0	X	X	Deemphasis block is disabled	0
1	0	0	Deemphasis block is enabled Level 1	0.3
1	0	1	Deemphasis block is enabled Level 2	1.1
1	1	0	Deemphasis block is enabled Level 3	2.1
1	1	1	Deemphasis block is enabled Level 4	4.3

Table 6. CML Output Amplitude Range (Typical)

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		MODE	OUTPUT AMPLITUDE (mV_{P-P})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	Low data-rate path	400 to 1192
1	0	X	X	High data-rate path	400 to 1147
1	1	0	0	High data-rate path with deemphasis	400 to 1041
1	1	0	1	High data-rate path with deemphasis	400 to 987
1	1	1	0	High data-rate path with deemphasis	400 to 908
1	1	1	1	High data-rate path with deemphasis	400 to 828

Table 7. CML Output DAC Resolution (Typical)

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		MODE	RESOLUTION (mV_{P-P})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	Low data-rate path	4.5
1	0	X	X	High data-rate path	4.5
1	1	0	0	High data-rate path with deemphasis	4.1
1	1	0	1	High data-rate path with deemphasis	3.9
1	1	1	0	High data-rate path with deemphasis	3.6
1	1	1	1	High data-rate path with deemphasis	3.3

Table 8. LOS Control

LOS2_EN	LOS1_EN	OPERATION MODE DESCRIPTION
0	0	LOS circuitry is disabled and powered down
X	1	LOS circuitry is enabled and Rx input amplitude is detected
1	0	LOS circuitry is enabled and RPMIN input amplitude is detected

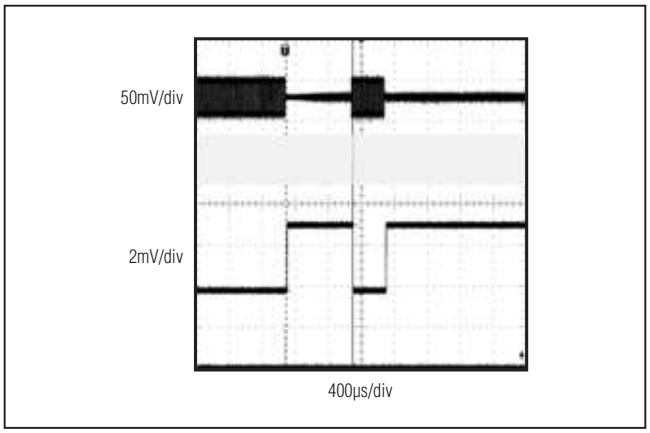


Figure 3. LOS Response to a Short Burst of Input Signal

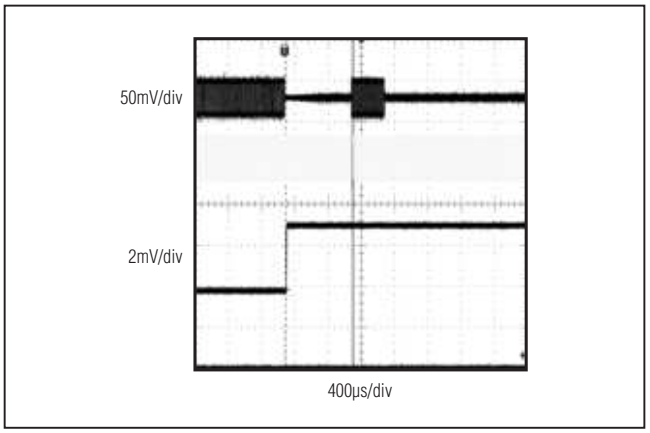


Figure 4. LOS Response to a Short Burst of Input Signal (Any changes in LOS are masked until the end of the LOS masking period.)

LOS Circuitry

The LOS circuitry has two operational modes controlled by the LOS1_EN and LOS2_EN bits (see Table 8). In the first mode, the LOS block detects the differential amplitude of the input signal and compares it against a preset threshold controlled by the 6-bit SET_LOS register. In the second mode, the LOS block compares the voltage at the RPMIN pin to a preset threshold also controlled by the 6-bit SET_LOS register. The second mode enables low-power LOS detection based on average photodiode current.

The LOS assert threshold is approximately 1.5mV$_{P-P}$ x SET_LOS[5:0]. The LOS deassert level is approximately 1.6 times the assert level to avoid LOS chatter. LOS polarity, squelch, and LOS masking time are unaffected by the selection of LOS1_EN or LOS2_EN.

Programmable LOS Output Masking Time

This feature masks false input signals that can occur after a loss-of-light event in a fiber optic link. These false input signals, caused by some transimpedance amplifier implementations, can corrupt the LOS output and cause system-level link diagnostic errors.

The LOS output masking time can be programmed from 0 to 4500µs in 35µs steps using the 7-bit SET_LOSTIMER[6:0] register. The output mask timer is initiated on the first transition of the LOS signal and prevents any further changes in the LOS output signal until the end of the programmed LOS timing period. The LOS output masking time should be carefully chosen to extend beyond any expected input glitch. Figure 3 shows the LOS signal changing after approximately 800µs to a change in the input signal where the LOS output masking time function is not used. Figure 4 shows masking of the LOS signal by the LOS output masking time function to a change in the input signal.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

Table 9. Digital Communication Word Structure

BIT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Address							RWN	Data that is written or read.							

Table 10. Register Descriptions and Addresses

ADDRESS	NAME	FUNCTION
H0x00	RXCTRL1	Receiver Control Register 1
H0x01	RXCTRL2	Receiver Control Register 2
H0x02	RXSTAT	Receiver Status Register
H0x03	SET_CML	CML Output Level Setting Register
H0x04	SET_LOS	LOS Threshold Assert Level Setting Register
H0x0E	MODECTRL	General Control Register
H0x12	SET_LOSTIMER	LOS Timer Setting Register

3-Wire Digital Communication

General

The MAX3945 implements a proprietary 3-wire digital interface. An external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. The master starts to generate a clock signal after the CSEL has been set to 1. All data transfers are most significant bit (MSB) first.

Protocol

Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3945. The RWN bit determines if the cycle is read or write. See Table 9.

Register Addresses

The MAX3945 contains seven registers available for programming. Table 10 shows the registers and addresses.

Write Mode (RWN = 0)

The master generates 16 total clock cycles at SCL. The master outputs a total of 16 bits (MSB first) to the SDA line at falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing, and Table 11 defines the various timing parameters.

Read Mode (RWN = 1)

The master generates 16 total clock cycles at SCL. The master outputs a total of 8 bits (MSB first) to the SDA line at falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing.

Mode Control

Normal mode allows read-only instruction for all registers except MODECTRL. Normal mode is the default mode.

Setup mode allows the master to write unrestricted data into any register except the RXSTAT register. To enter setup mode, the MODECTRL register (address = H0x0E) must be set to H0x12. After the MODECTRL register has been set to H0x12, the next operation is unrestricted. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

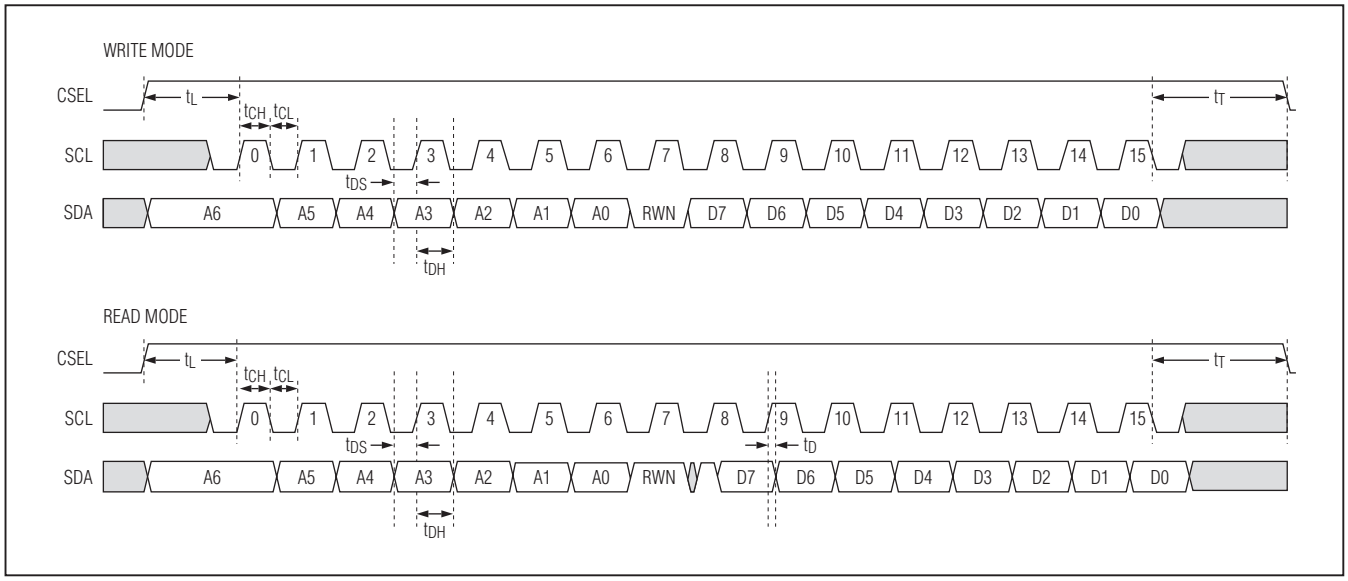


Figure 5. Timing for the 3-Wire Digital Interface

Table 11. Interface Timing Parameters

SYMBOL	DEFINITION
t_L	CSEL leading time before the first SCL edge
t_{CH}	SCL pulse-width high
t_{CL}	SCL pulse-width low
t_D	SCL rise to SDA propagation time
t_{DS}	SDA setup time
t_{DH}	SDA hold time
t_T	CSEL trailing time after last SCL edge

Register Descriptions

Receiver Control Register 1 (RXCTRL1)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	RXDE1	RXDE0	X*	SOFTRES	BW1	BW0	RATE_SEL	X*	H0x00
Default Value	0	0	1	0	1	1	1	1	

**Do not change default setting.*

Bits 7 and 6: RXDE[1:0]. These 2 bits are used to control deemphasis of the output waveform. See Table 5 for the bit settings and corresponding deemphasis levels.

Bit 4: SOFTRES. When this bit is set to 1 during a 3-wire interface write operation, all registers are set to the default state when CSEL goes low.

Bits 3 and 2: BW[1:0]. When RATE_SEL = 0, these 2 bits control the bandwidth of the limiting amplifier. See Table 1 for the settings and corresponding filter selection.

Bit 1: RATE_SEL. RATE_SEL selects between the low bandwidth data path (1.0625Gbps to 4.25Gbps) and the high bandwidth data path (4.25Gbps to 11.3Gbps). When RATE_SEL is set to 1, the high bandwidth path is chosen. When RATE_SEL is set to 0, the low bandwidth path is chosen.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

Receiver Control Register 2 (RXCTRL2)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	LOS2_EN	LOS1_EN	LOS_POL	RX_POL	SQ_EN	RX_EN	RXDE_EN	AZ_EN	H0x01
Default Value	0	1	1	1	0	1	0	1	

Bit 7: LOS2_EN. Enables or disables the RSSI monitor-based LOS circuitry, in combination with the LOS1_EN bit. The below table shows when the RSSI monitor-based LOS is disabled and enabled.

LOS2_EN	LOS1_EN	RX_EN	Rx INPUT-BASED LOS	RSSI MONITOR-BASED LOS
0	0	X	Disabled and powered down	Disabled and powered down
0	1	1	Enabled	Disabled and powered down
X	1	0	Disabled and powered down	Disabled and powered down
1	1	1	Enabled	Disabled and powered down
1	0	0	Disabled and powered down	Enabled
1	0	1	Disabled and powered down	Enabled

Bit 6: LOS1_EN. Controls the Rx input-based LOS circuitry. When RX_EN is set to 0, the LOS detector is also disabled.

0 = disabled

1 = enabled

Bit 5: LOS_POL. Controls the polarity of the LOS pin.

0 = inverse

1 = normal

Bit 4: RX_POL. Controls the polarity of the CML output.

0 = inverse

1 = normal

Bit 3: SQ_EN. When SQ_EN = 1, the CML output is squelched when LOS is asserted.

0 = disabled

1 = enabled

Bit 2: RX_EN. Enables or disables the receive circuitry.

0 = disabled

1 = enabled

Bit 1: RXDE_EN. Enables or disables the deemphasis on the CML output.

0 = disabled

1 = enabled

Bit 0: AZ_EN. Enables or disables the autozero circuitry.

0 = disabled

1 = enabled

Receiver Status Register (RXSTAT)

Bit #	7	6	5	4	3	2	1 (STICKY)	0 (STICKY)	ADDRESS
Name	X	X	X	X	X	X	POR_2d	LOS_2d	H0x02
Default Value	X	X	X	X	X	X	X	X	

Bit 1: POR_2d. When the V_{CC} supply voltage is below 2.3V, the POR circuitry sets POR_2d high. When the supply voltage is above 2.75V, the POR circuitry deasserts, but the POR_2d bit remains high until it is read.

Bit 0: LOS_2d. Copy of the LOS status. This is a sticky bit, which means that it is cleared on a read. The first 0-to-1 transition is latched until the bit is read by the master or POR occurs.

CML Output Level Setting Register (SET_CML)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_CML[7] (MSB)	SET_CML[6]	SET_CML[5]	SET_CML[4]	SET_CML[3]	SET_CML[2]	SET_CML[1]	SET_CML[0] (LSB)	H0x03
Default Value	0	1	0	1	1	1	0	0	

Bits 7 to 0: SET_CML[7:0]. The SET_CML register is an 8-bit register that can be set up to 255 for maximum CML output amplitude. See Table 13 for equations to determine CML output level vs. SET_CML.

LOS Threshold Assert Level Setting Register (SET_LOS)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	SET_LOS[5] (MSB)	SET_LOS[4]	SET_LOS[3]	SET_LOS[2]	SET_LOS[1]	SET_LOS[0] (LSB)	H0x04
Default Value	X	X	0	0	1	1	0	0	

Bits 5 to 0: SET_LOS[5:0]. The SET_LOS register is a 6-bit register used to program the LOS threshold. See the *Typical Operating Characteristics* section for a typical LOS threshold voltage vs. DAC code for both the Rx input-based LOS and the RSSI monitor-based LOS.

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

General Control Register (MODECTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	MODECTRL[7] (MSB)	MODECTRL[6]	MODECTRL[5]	MODECTRL[4]	MODECTRL[3]	MODECTRL[2]	MODECTRL[1]	MODECTRL[0] (LSB)	H0x0E
Default Value	0	0	0	0	0	0	0	0	

Bits 7 to 0: MODECTRL[7:0]. The MODECTRL register enables a switch between normal and setup modes. The setup mode is achieved by setting this register to H0x12. MODECTRL must be updated before each write operation.

LOS Timer Setting Register (SET_LOSTIMER)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	SET_ LOSTIMER[6] (MSB)	SET_ LOSTIMER[5]	SET_ LOSTIMER[4]	SET_ LOSTIMER[3]	SET_ LOSTIMER[2]	SET_ LOSTIMER[1]	SET_ LOSTIMER[0] (LSB)	H0x12
Default Value	X	0	0	0	0	0	0	0	

Bits 6 to 0: SET_LOSTIMER[6:0]. The SET_LOSTIMER register is a 7-bit register that can be set from 0 to 127. See the *Typical Operating Characteristics* section for a typical timer period vs. DAC code.

Table 12. Register Map

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Receiver Control Register 1 Address = H0x00	RXCTRL1	R	RW	7	RXDE1	0	Rx deemphasis MSB control with RXDE_EN = 1
		R	RW	6	RXDE0	0	Rx deemphasis LSB control with RXDE_EN = 1
		R	RW	5	X	1	Must be set to 1
		R	RW	4	SOFTRES	0	Soft reset control bit
		R	RW	3	BW1	1	Input bandwidth control with RATE_SEL = 0: 00: 1GHz 01: 2.1GHz 10: 2.5GHz 11: 3GHz
		R	RW	2	BW0	1	
		R	RW	1	RATE_SEL	1	Rate-select control 0: 1G/4G mode 1: fast mode
		R	RW	0	X	1	Must be set to 1

Table 12. Register Map (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Receiver Control Register 2 Address = H0x01	RXCTRL2	R	RW	7	LOS2_EN	0	RSSI monitor-based LOS 0: disabled 1: enabled when LOS1_EN = 0
		R	RW	6	LOS1_EN	1	Rx input-based LOS 0: disabled 1: enabled
		R	RW	5	LOS_POL	1	LOS polarity 0: inverse 1: normal
		R	RW	4	RX_POL	1	Rx polarity 0: inverse 1: normal
		R	RW	3	SQ_EN	0	Squelch 0: disabled 1: enabled
		R	RW	2	RX_EN	1	Rx control 0: disabled 1: enabled
		R	RW	1	RXDE_EN	0	Rx deemphasis 0: disabled 1: enabled
		R	RW	0	AZ_EN	1	Rx autozero control 0: disabled 1: enabled
Receiver Status Register Address = H0x02	RXSTAT	R	R	1 (sticky)	POR_2d	X	POR -> V_{CC} low limit violation
		R	R	0 (sticky)	LOS_2d	X	Copy of LOS status

Table 12. Register Map (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
CML Output Level Setting Register Address = H0x03	SET_CML	R	RW	7	SET_CML[7]	0	MSB output level DAC
		R	RW	6	SET_CML[6]	1	
		R	RW	5	SET_CML[5]	0	
		R	RW	4	SET_CML[4]	1	
		R	RW	3	SET_CML[3]	1	
		R	RW	2	SET_CML[2]	1	
		R	RW	1	SET_CML[1]	0	
		R	RW	0	SET_CML[0]	0	LSB output level DAC
LOS Threshold Assert Level Setting Register Address = H0x04	SET_LOS	R	RW	5	SET_LOS[5]	0	MSB LOS threshold DAC
		R	RW	4	SET_LOS[4]	0	
		R	RW	3	SET_LOS[3]	1	
		R	RW	2	SET_LOS[2]	1	
		R	RW	1	SET_LOS[1]	0	
		R	RW	0	SET_LOS[0]	0	LSB LOS threshold DAC
General Control Register Address = H0x0E	MODECTRL	RW	RW	7	MODECTRL[7]	0	MSB mode control
		RW	RW	6	MODECTRL[6]	0	
		RW	RW	5	MODECTRL[5]	0	
		RW	RW	4	MODECTRL[4]	0	
		RW	RW	3	MODECTRL[3]	0	
		RW	RW	2	MODECTRL[2]	0	
		RW	RW	1	MODECTRL[1]	0	
		RW	RW	0	MODECTRL[0]	0	LSB mode control
LOS Timer Setting Register Address = H0x12	SET_LOSTIMER	R	RW	6	SET_LOSTIMER[6]	0	MSB LOS timer
		R	RW	5	SET_LOSTIMER[5]	0	
		R	RW	4	SET_LOSTIMER[4]	0	
		R	RW	3	SET_LOSTIMER[3]	0	
		R	RW	2	SET_LOSTIMER[2]	0	
		R	RW	1	SET_LOSTIMER[1]	0	
		R	RW	0	SET_LOSTIMER[0]	0	LSB LOS timer

Design Procedure

Programming CML Output Levels

See Tables 13 and 14. For each value of the bits RXDE1 and RXDE0 in Table 13, the value of deemphasis does vary with the SET_CML[7:0] setting. In Table 13, the values of deemphasis are given for the setting SET_CML[7:0] = 120d. The variation of deemphasis for other values of SET_CML[7:0] is shown in the *Typical Operating Characteristics* (see the Deemphasis Value vs. SET_CML DAC Setting (RATE_SEL = 1) graph). Note that even though RXDE_EN = 0, there is still some deemphasis for RATE_SEL = 1 for values of amplitude control below SET_CML[7:0] = 170d.

Select the Coupling Capacitor

For AC-coupling, the coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low frequency cutoff (f_{IN}) is decreased: $f_{IN} = 1/[2\pi(50)(C_{IN})]$. The recommended value of C_{IN} and C_{OUT} is 0.1µF for the MAX3945.

Select the Offset-Correction Capacitor

The capacitor between CAZ and ground determines the time constant of the signal path DC-offset cancellation loop. A 0.1µF capacitor between CAZ and ground is recommended for the MAX3945.

Applications Information

Layout Considerations

Use good, high-frequency layout techniques and multiple-layer boards with uninterrupted ground planes to minimize EMI and crosstalk.

Exposed-Pad Package

The exposed pad on the 16-pin TQFN provides a very low-thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3945 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Table 13. CML Output Amplitude Equations (Typical)

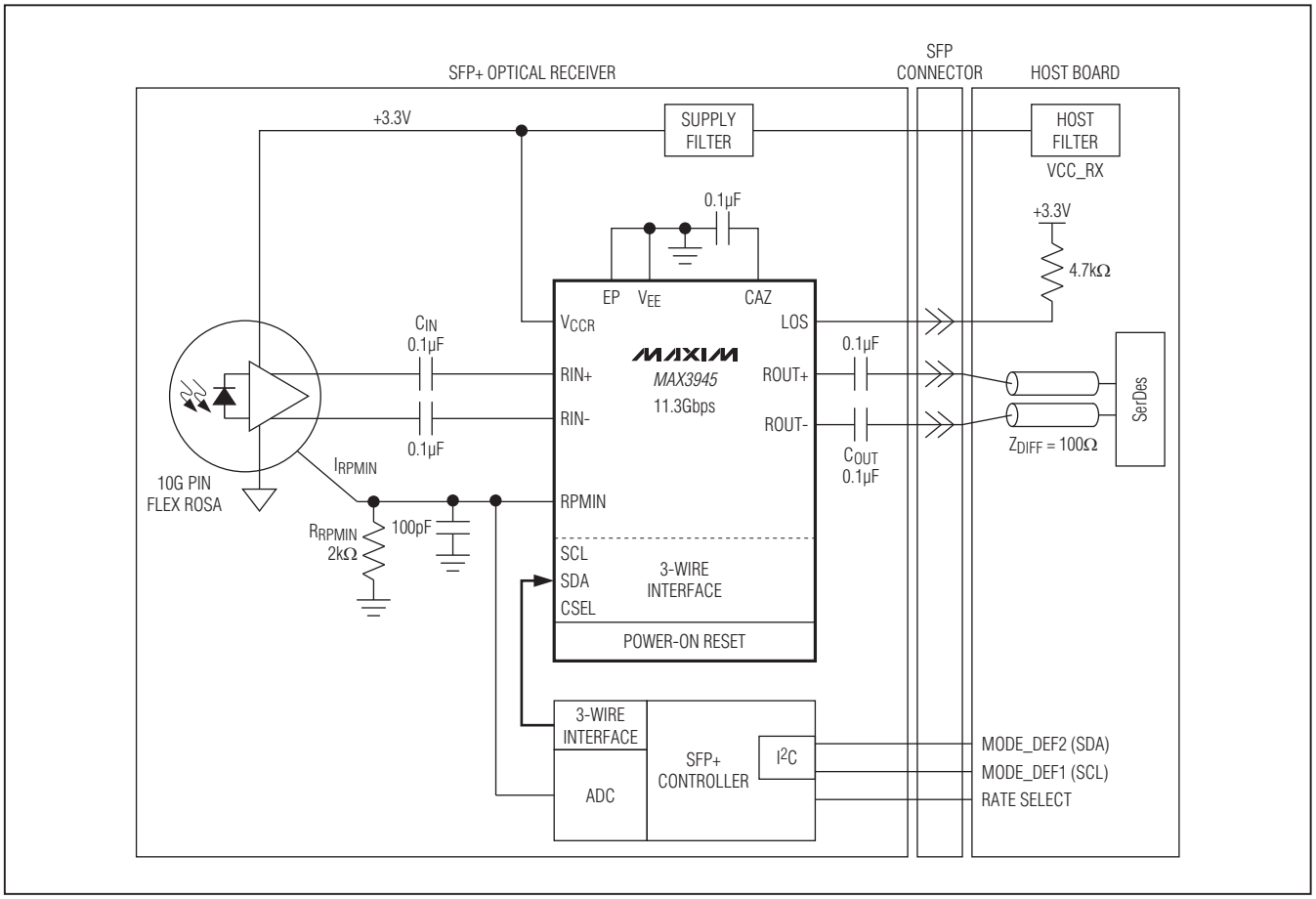
RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		DEEMPHASIS (dB) (SET_CML[7:0] = 120d)	EQUATION FOR (V_{ROUT+} - V_{ROUT-})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	0	45mV$_{P-P}$ + 4.5mV$_{P-P}$ x SET_CML
1	0	X	X	0.72	4.5mV$_{P-P}$ x SET_CML
1	1	0	0	1.17	-4mV$_{P-P}$ + 4.1mV$_{P-P}$ x SET_CML
1	1	0	1	1.89	-7mV$_{P-P}$ + 3.9mV$_{P-P}$ x SET_CML
1	1	1	0	2.48	-10mV$_{P-P}$ + 3.6mV$_{P-P}$ x SET_CML
1	1	1	1	3.86	-13mV$_{P-P}$ + 3.3mV$_{P-P}$ x SET_CML

Table 14. SET_CML DAC Codes for 400mV$_{P-P}$ and 800mV$_{P-P}$ Output Levels

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		SET_CML DAC CODE	
RATE_SEL	RXDE_EN	RXDE1	RXDE0	400mV$_{P-P}$	800mV$_{P-P}$
0	X	X	X	80	169
1	0	X	X	91	181
1	1	0	0	98	194
1	1	0	1	106	208
1	1	1	0	115	225
1	1	1	1	126	245

1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier

Typical Application Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 TQFN-EP	T1633+5	21-0136

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2010 Maxim Integrated Products Maxim is a registered trademark of Maxim Integrated Products, Inc.