19-3618; Rev 3; 5/07

EVALUATION KIT AVAILABLE

Audio/Video Switch for Dual SCART Connectors

General Description

The MAX4397 dual SCART switch matrix routes audio and video signals between an MPEG encoder and two external SCART connectors under I²C control, and meets the requirements of EN50049-1, IEC 933-1, Canal+, and BSkyB standards.

The video and audio channels feature input source selection multiplexers, input buffers, and output buffers for routing all inputs to selected outputs. The MAX4397D audio encoder input is differential DC-coupled, while the MAX4397S audio encoder input is single-ended AC-coupled. Except for the MAX4397D's audio encoder input, all other inputs and outputs are AC-coupled with internal DC-biasing set to predefined levels.

The MAX4397 provides programmable gain control from +5dB to +7dB in 1dB steps for Red, Green, and Blue component video signals. All other video outputs have a fixed +6dB gain. Additional features include an internal Luma and Chroma (Y/C) mixer that generates a Composite video signal (CVBS) to supply an RF modulator output, and internal video reconstruction low-pass filters with passband ripple between -1dB and +1dB from 100kHz to 5.5MHz. The MAX4397 TV audio channel features clickless switching and programmable volume control from -56dB to +6dB in 2dB steps. The VCR audio output also has programmable gain for -6dB, 0dB, or +6dB. The device also generates monaural audio from left and right stereo inputs. All audio drivers deliver a $3.0V_{RMS}$ minimum output.

The MAX4397 operates with standard 5V and 12V power supplies and supports slow-switching and fast-switching signals. The I²C interface programs the gain and volume control, and selects the input source for routing.

The MAX4397 is available in a compact 48-pin thin QFN package and is specified over the 0°C to +70°C commercial temperature range.

Applications

Satellite Set-Top Boxes

Cable Set-Top Boxes

TVs

VCRs

DVDs

Features

- **Video Outputs Drive $2V_{P-P}$ into 150Ω**
- **Audio Outputs Drive $3V_{RMS}$ into 10kΩ**
- **Clickless, Popless Audio Gain Control and Switching**
- **AC-Coupled Video Inputs with Internal Clamp and Bias**
- **DC-Coupled Video Outputs**
- **Composite Video Signal Created Internally from Y/C Inputs**
- **Internal Video Reconstruction Filters Provide -40dB at 27MHz**
- **Differential (MAX4397D) or Single-Ended (MAX4397S) Audio Encoder Input**
- **Red/Chroma Switch for Bidirectional I/O**
- **I²C-Programmable RGB Gain from +5dB to +7dB**
- **I²C-Programmable Audio Gain Control from +6dB to -56dB**
- **Meets EN50049-1, IEC 933-1, Canal+, and BSkyB Requirements**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4397DCTM	0°C to +70°C	48 Thin QFN-EP* (7mm x 7mm)	T4877-6
MAX4397SCTM	0°C to +70°C	48 Thin QFN-EP* (7mm x 7mm)	T4877-6

*EP = Exposed paddle.

Pin Configuration and Typical Application Circuits appear at end of data sheet.

System Block Diagram appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Audio/Video Switch for Dual SCART Connectors

ABSOLUTE MAXIMUM RATINGS

V_{VID} to GNDVID .....-0.3V to +6V
V_{12} to GNDAUD .....-0.3V to +14V
V_{AUD} to GNDAUD .....-0.3V to +6V
GNDAUD to GNDVID .....-0.1V to +0.1V
All Video Inputs, ENCIN_FS, VCRIN_FS, SET to GNDVID .....-0.3V to (V_{VID} + 0.3V)
All Audio Inputs, AUDBIAS to GNDAUD .....-0.3V to (V_{AUD} + 0.3V)
SDA, SCL, DEV_ADDR to GNDVID .....-0.3V to +6V
All Audio Outputs, TV_SS, VCR_SS to GNDAUD.....-0.3V to (V_{12} + 0.3V)
All Video Outputs, TVOUT_FS to V_{VID}, V_{AUD}, GNDAUD, GNDVID .....Continuous
All Audio Outputs to V_{VID}, V_{AUD}, V_{12}, GNDVID, GNDAUD .....Continuous
Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 27mW/°C above +70°C).....2105.3mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{12} = 12V, V_{VID} = V_{AUD} = 5V, 0.1µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_{AUD} to GNDAUD, V_{12} to GNDAUD, and V_{VID} to GNDVID, SET = 100kΩ nominal, R_{LOAD} = 150Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VID} Supply Voltage Range	V_{VID}	Inferred from video gain test at 4.75V and 5.2V	4.75	5.0	5.25	V
V_{AUD} Supply Voltage Range	V_{AUD}	Inferred from audio gain test at 4.75V and 5.2V	4.75	5.0	5.25	V
V_{12} Supply Voltage Range	V_{12}	Inferred from slow switching levels	11.4	12.0	12.6	V
V_{VID} Quiescent Supply Current	I_{VID_Q}	All video output amplifiers are enabled, no load		69	100	mA
V_{VID} Standby Supply Current	I_{VID_S}	All video output amplifiers are in shutdown, and TV_FS_OUT driver is in shutdown, no load		40	60	mA
V_{AUD} Quiescent Supply Current	I_{AUD_Q}	No load		2.4	6	mA
V_{12} Quiescent Supply Current	I_{12_Q}	No load		3.6	6	mA
VIDEO CHARACTERISTICS						
Voltage Gain	G_V	CVBS and Y/C, $1V_{P-P}$ input	+5.5	+6.0	+6.5	dB
		R,G,B, $1V_{P-P}$ input, (programmable gain control)	+4.5	+5.0	+5.5	
			+5.5	+6.0	+6.5	
			+6.5	+7.0	+7.5	
LP Filter Attenuation	ATTN	T_A = +25°C, f = 6MHz, V_{IN} = $1V_{P-P}$		1.2	3.3	dB
LP Filter Suppression	SPPR	T_A = +25°C, f = 27MHz, V_{IN} = $1V_{P-P}$	35	50		dB
Slew Rate	SR	V_{OUT} = $2V_{P-P}$		8		V/µs
Settling Time	t_S	V_{OUT} = $2V_{P-P}$, settle to 0.1% (Note 2)		380		ns
Gain Matching	AG	$1V_{P-P}$ input, between RGB or Y/C	-0.5		+0.5	dB
Differential Gain	DG	5-step modulated staircase		0.4		%
Differential Phase	DP	5-step modulated staircase		0.2		degrees
Signal-to-RMS Noise	SNR_V	V_{IN} = $1V_{P-P}$		65		dB

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Group Delay Variation	ΔGD	f = 0.1MHz to 4.43MHz		14		nS
Sync-Tip Clamp Level	V_CLMP	RGB, Composite, and Luma input, no signal, no load		1.21		V
Chroma Bias	V_BIAS	Chroma input only, no signal, no load		1.9		V
Droop	D	Set by input current	-2		+2	%
Power-Supply Rejection Ratio	PSRR_V	DC, $0.5V_{P-P}$		48		dB
Input Impedance	Z_{IN}	CVBS, Y, or RGB video inputs, $V_{IN} > V_{_CLMP}$		4		MΩ
		Chroma video input, $V_{IN} = V_{_BIAS}$		11		kΩ
Input Clamp Current	I_{CLMP}	V_{IN} = 1.75V	2.5	5	8.0	µA
Pulldown Resistance	RP	Enable VCR_R/C_OUT and TV_R/C_OUT pulldown through I^2C, (see registers 7 and 9 for loading register details)		10		Ω
Output Pin Bias Voltage	V_{OUT}	RGB, Composite, and Luma, no signal, no load		1.08		V
		Chroma, no signal, no load		2.27		
Crosstalk	XTLK	Between any two active inputs, f = 4.43MHz, $V_{IN} = 1V_{P-P}$		-50		dB
Mute Suppression	M_SPR_V	f = 4.43MHz, $V_{IN} = 1V_{P-P}$, on one input only		-50		dB
AUDIO CHARACTERISTICS (Note 3)						
Voltage Gain (From Application Input)	G_A	TV or VCR to stereo, gain = 0dB, $V_{IN} = 1V_{P-P}$	-0.5	0	+0.5	dB
		TV or VCR to mono, gain = 0dB, $V_{IN} = 1V_{P-P}$	2.5	3	3.5	
		ENC to stereo, gain = 0dB, $V_{IN} = 1V_{P-P}$	3.02	3.52	4.02	
		ENC to mono, gain = 0dB, $V_{IN} = 1V_{P-P}$	6.02	6.52	7.02	
Gain Matching Between Channels	ΔG_A	Gain = 0dB, $V_{IN} = 1V_{P-P}$	-0.5	0	+0.5	dB
Flatness	ΔA	f = 20Hz to 20kHz, $0.5V_{RMS}$ input, gain = 0dB		0.01		dB
Frequency Bandwidth	BW	$0.5V_{RMS}$ input, frequency where output is -3dB referenced to 1kHz		230		kHz
Input DC Level (Excluding Encoder Inputs that are High Impedance)	V_{IN}	Gain = 0dB		0.2308 x V_{12}		V
Encoder Input Common-Mode Voltage Range	V_{CM}	MAX4397D only, input differential signal = 0V	1.2		V_{AUD} - 0.7	V

Audio/Video Switch for Dual SCART Connectors

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 5V, 0.1µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_{AUD} to GNDAUD, V_{12} to GNDAUD, and V_{VID} to GNDVID, SET = 100kΩ nominal, R_{LOAD} = 150Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Encoder Common-Mode Rejection Ratio	CMRR	MAX4397D only, over V_{CM} range		40		dB
Input Signal Amplitude	V_{IN_AC}	Single-ended inputs, f = 1kHz, THD < 1%		3		V_{RMS}
		ENC inputs differential level, MAX4397D, f = 1kHz, THD < 1%		2.08		
		ENC inputs single-ended, MAX4397S, f = 1kHz, THD < 1%		1.31		
Input Resistance (Measured at Parts Input)	R_{IN}	Single ended: VCR_INR, VCR_INL, TV_INR, TV_INL		0.1		MΩ
		Encoder, MAX4397D: ENC_INL+, ENC_INL-, ENC_INR+, ENC_INR-		1		
		Encoder, MAX4397S: ENC_INL, ENC_INR		0.1		
Output DC Level	V_{OUT_DC}	V_{IN} = 0V		0.5 x V_{12}		V
Signal-to-Noise Ratio	SNR_A	f = 1.0kHz, 1V_{RMS} application input, gain = 0dB, 20Hz to 20kHz		95		dB
Total Harmonic Distortion Plus Noise	THD+N	R_{LOAD} = 10kΩ, f = 1.0kHz, 0.5V_{RMS} output		0.004		%
		R_{LOAD} = 10kΩ, f = 1.0kHz, 2V_{RMS} output		0.004		
Output Impedance	ZO	f = 1kHz		1		Ω
Volume Attenuation Step	ASTEP	1.414V_{P-P} input, programmable gain to TV SCART volume control range extends from -56dB to +6dB	1.5	2	2.5	dB
		1.414V_{P-P} input, programmable gain to VCR audio extends from -6dB to +6dB	5.5	6	6.5	
Power-Supply Rejection Ratio	PSRR_A	From V_{12}, f = 1kHz, 0.5V_{P-P}, (C_{AUD_BIAS} = 47µF), gain = 0dB		75		dB
		From V_{AUD}, f = 1kHz, 0.5V_{P-P}, V_{AUD} ≥ +4.75V, V_{AUD} ≤ +5.25V, gain = 0dB		75		
Mute Suppression	M_SPR_A	f = 1kHz, 0.5V_{RMS} input, set through I^2C, see register 1 for loading register details		90		dB
Audio Clipping Level	VCLIP	f = 1kHz, 2.5V_{RMS} input, gain = 6dB, THD < 1%		3.6		V_{RMS}
Left-to-Right Crosstalk	XTLK_LR	f = 1kHz, 0.5V_{RMS} input, gain = 0dB		80		dB
Crosstalk	XTLK_CC	TV SCART to VCR SCART or VCR SCART to TV SCART, f = 1kHz, 0.5V_{RMS} input, gain = 0dB		90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 5V, 0.1µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_{AUD} to GNDAUD, V_{12} to GNDAUD, and V_{VID} to GNDVID, SET = 100kΩ nominal, R_{LOAD} = 150Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INTERFACE: SDA AND SCL (Note 5)						
Low-Level Input Voltage	V_{IL}		0		0.8	V
High-Level Input Voltage	V_{IH}		2.6			V
Hysteresis of Schmitt Trigger Input				0.2		V
SDA Low-Level Output Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA			0.6	
Output Fall Time for SDA Line		400pF bus load			250	ns
Spike Suppression				50		ns
Input Current			-10		+10	µA
Input Capacitance				5		pF
SCL Clock Frequency			0		400	kHz
Hold Time	$t_{HD,STA}$		0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated Start Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for Stop Condition	$t_{SU,STO}$		0.6			µs
Bus Free Time Between a Stop and Start	t_{BUF}		1.3			µs
OTHER DIGITAL PINS (Note 5)						
DEV_ADDR Low Level					0.8	V
DEV_ADDR High Level			2.6			V
SLOW SWITCHING SECTION (Note 5)						
Input Low Level			0		2	V
Input Medium Level			4.5		7.0	V
Input High Level			9.5		V_{12}	V
Input Current				50	100	µA
Output Low Level		10kΩ to ground, internal TV, 11.4V < V_{12} < 12.6V	0		1.5	V
Output Medium Level		10kΩ to ground, external 16/9, 11.4V < V_{12} < 12.6V	5.0		6.5	V
Output High Level		10kΩ to ground, external 4/3, 11.4V < V_{12} < 12.6V	10		V_{12}	V

Audio/Video Switch for Dual SCART Connectors

ELECTRICAL CHARACTERISTICS (continued)

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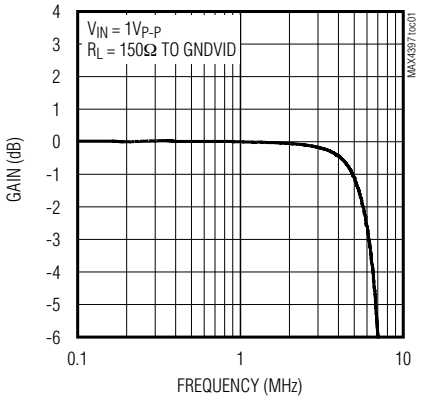
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
FAST SWITCHING SECTION (Note 5)						
Input Low Level			0		0.4	V
Input High Level			1		3	V
Input Current				1	10	µA
Output Low Level		I_{SINK} = 0.5mA	0	0.01	0.2	V
Output High Level		I_{SOURCE} = 20mA, V_{VID} - V_{OH}		0.75	2	V
Fast Switching Output to RGB Skew		(Note 4)		30		ns
Fast Switching Output Rise Time		150Ω to ground		30		ns
Fast Switching Output Fall Time		150Ω to ground		30		ns

Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: The settling time is measured from the 50% of the input swing to the 0.1% of the final value of the output.
Note 3: Maximum load capacitance is 200pF. All the listed parameters are measured at application's inputs, unless otherwise noted. See the *Typical Application Circuits*.
Note 4: Difference in propagation delays of fast-blanking signal and RGB signals. Measured from 50% input transition to 50% output transition. Signal levels to be determined.
Note 5: Guaranteed by design.

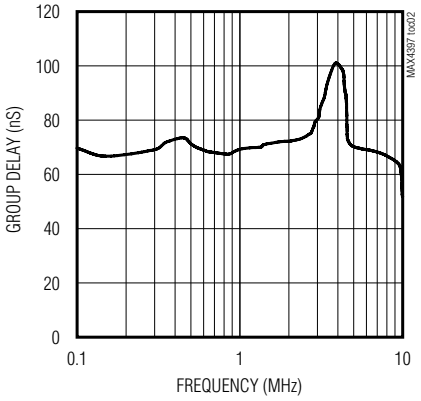
Typical Operating Characteristics

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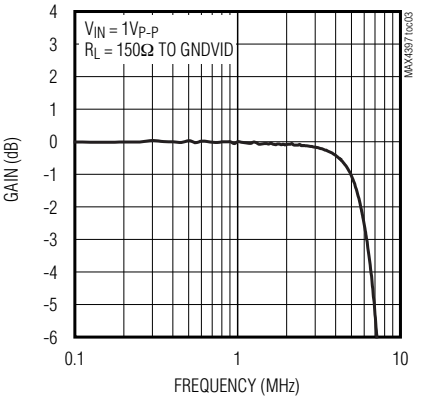
R/G/B VIDEO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



GROUP DELAY vs. FREQUENCY



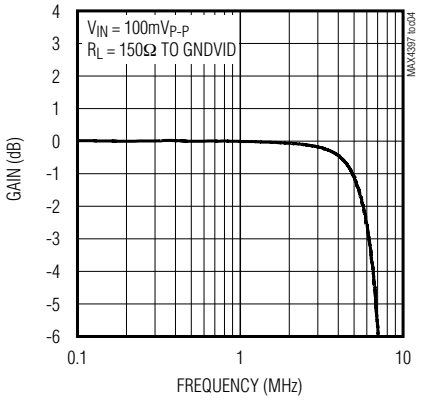
Y VIDEO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



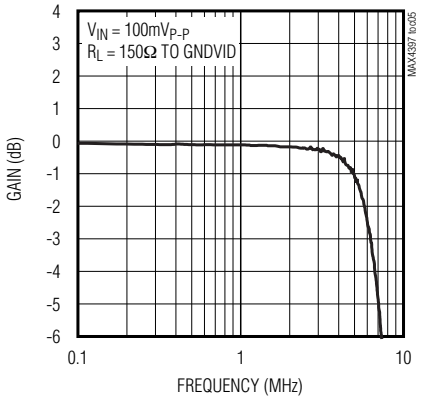
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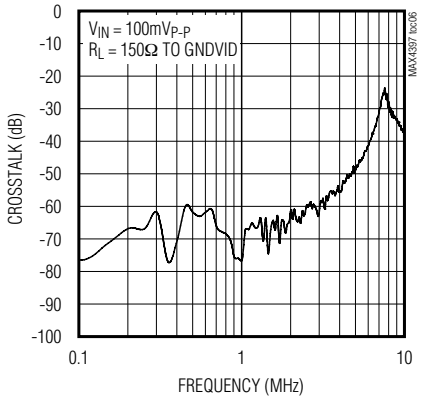
R/G/B VIDEO SMALL-SIGNAL BANDWIDTH vs. FREQUENCY



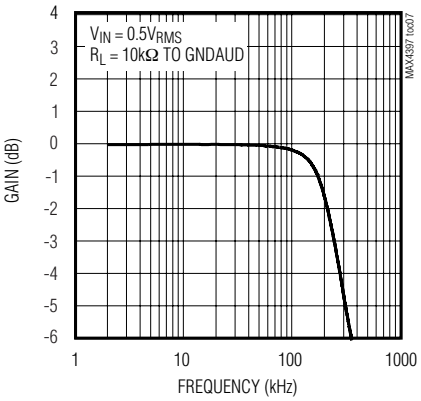
Y VIDEO SMALL-SIGNAL BANDWIDTH vs. FREQUENCY



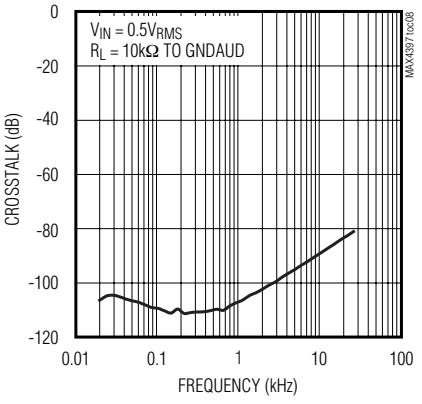
VIDEO CROSSTALK vs. FREQUENCY



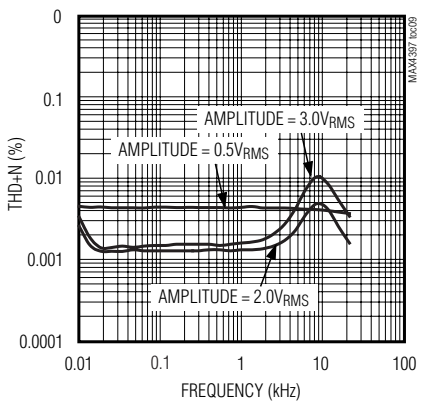
AUDIO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



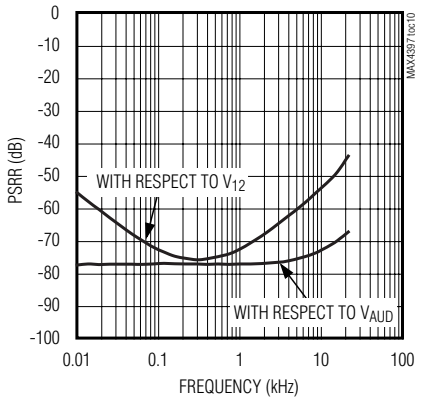
AUDIO CROSSTALK vs. FREQUENCY



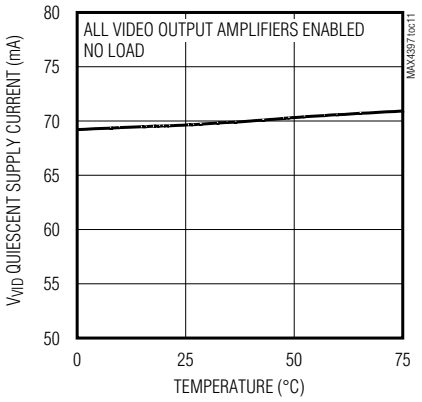
AUDIO TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



V_{VID} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

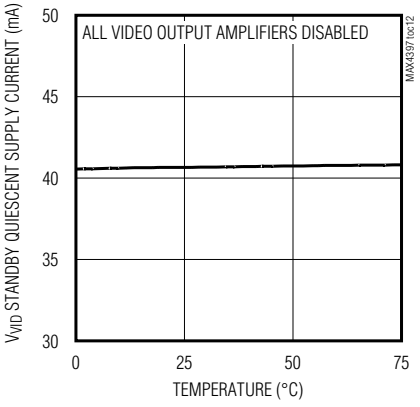


Audio/Video Switch for Dual SCART Connectors

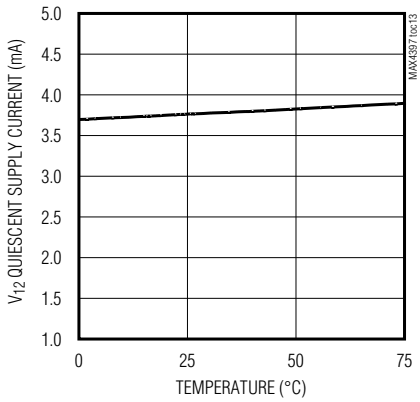
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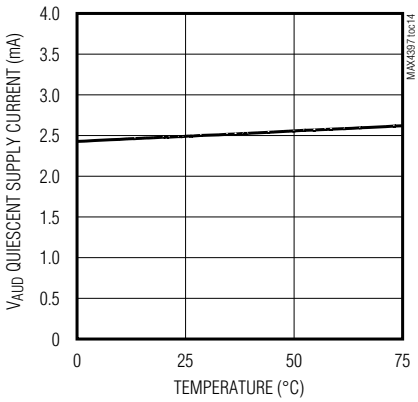
V_{VID} STANDBY QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



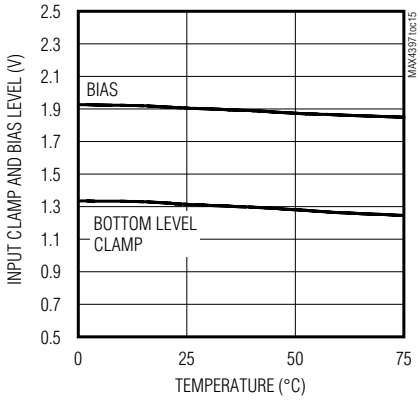
V_{12} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



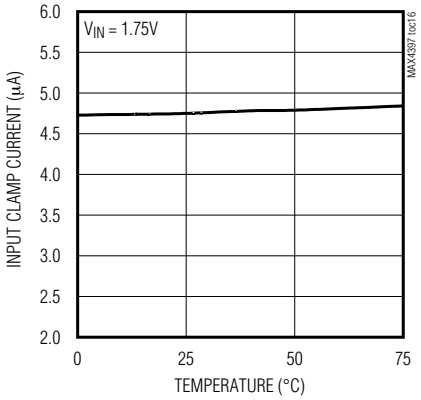
V_{AUD} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



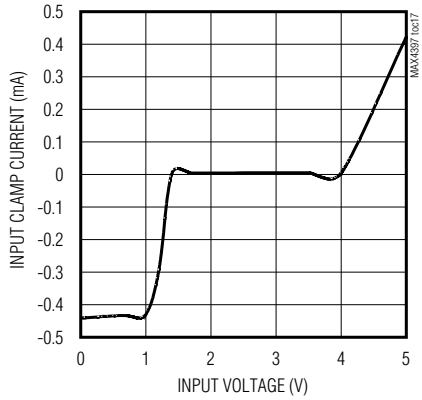
INPUT CLAMP AND BIAS LEVEL vs. TEMPERATURE



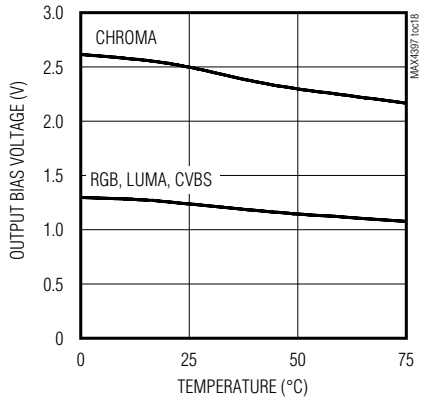
INPUT CLAMP CURRENT vs. TEMPERATURE



INPUT CLAMP CURRENT vs. INPUT VOLTAGE



OUTPUT BIAS VOLTAGE vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX4397D	MAX4397S		
1	1	SDA	Bidirectional Data I/O. I^2C-compatible, 2-wire interface data input/output. Output is open drain.
2	2	SCL	Serial Clock Input. I^2C-compatible, 2-wire clock interface.
3	3	DEV_ADDR	Device Address Set Input. Connect to GNDVID to set write and read addresses of 94h or 95h, respectively. Connect to V_{VID} to set write and read address of 96h or 97h, respectively.
4	—	ENC_INL+	Digital Encoder Left-Channel Audio Positive Input
—	4	ENC_INL	Digital Encoder Left-Channel Audio Input
5	—	ENC_INL-	Digital Encoder Left-Channel Audio Negative Input
—	5, 7	N.C.	No Connection. Not internally connected.
6	—	ENC_INR+	Digital Encoder Right-Channel Audio Positive Input
—	6	ENC_INR	Digital Encoder Right-Channel Audio Input
7	—	ENC_INR-	Digital Encoder Right-Channel Audio Negative Input
8	8	VCR_INR	VCR SCART Right-Channel Audio Input
9	9	VCR_INL	VCR SCART Left-Channel Audio Input
10	10	TV_INR	TV SCART Right-Channel Audio Input
11	11	TV_INL	TV SCART Left-Channel Audio Input
12	12	GNDAUD	Audio Ground
13	13	AUD_BIAS	Audio Input Bias Voltage. Bypass AUD_BIAS with a 47µF capacitor and a 0.1µF capacitor to GNDAUD.
14	14	V_{AUD}	Audio Supply. Connect to a +5V supply. Bypass with a 10µF aluminum electrolyte capacitor in parallel with a 0.47µF low-ESR ceramic capacitor to GNDAUD.
15	15	VCR_OUTR	VCR SCART Right-Channel Audio Output
16	16	VCR_OUTL	VCR SCART Left-Channel Audio Output
17	17	RF_MONO_OUT	RF Modulator Mono Audio Output
18	18	TV_OUTL	TV SCART Left-Channel Audio Output
19	19	TV_OUTR	TV SCART Right-Channel Audio Output
20	20	V_{12}	+12V Supply. Bypass V_{12} with a 10µF capacitor in parallel with a 0.1µF capacitor to ground.
21	21	TV_SS	TV SCART Bidirectional Slow-Switch Signal
22	22	VCR_SS	VCR SCART Bidirectional Slow-Switch Signal
23	23	SET	Filter Cutoff Frequency Set Input. Connect 100kΩ resistor from SET to ground.
24, 36	24, 36	V_{VID}	Video and Digital Supply. Connect to a +5V supply. Bypass with a 0.01µF capacitor to GNDVID. V_{VID} also serves as a digital supply for the I^2C interface.
25	25	VCRIN_FS	VCR SCART Fast-Switching Input
26	26	ENCIN_FS	Digital Encoder Fast-Switching Input
27	27	TVOUT_FS	TV SCART Fast-Switching Output. This signal is used to switch the TV to its RGB inputs for on-screen display purposes.
28	28	GNDVID	Video Ground

Audio/Video Switch for Dual SCART Connectors

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4397D	MAX4397S		
29	29	RF_CVBS_OUT	RF Modulator Composite Video Output. Internally biased at 1V.
30	30	TV_Y/CVBS_OUT	TV SCART Luma/Composite Video Output. Internally biased at 1V.
31	31	TV_R/C_OUT	TV SCART Red/Chroma Video Output. Internally biased at 1V for Red video signal and 2.2V for Chroma video signal.
32	32	TV_G_OUT	TV SCART Green Video Output. Internally biased at 1V.
33	33	TV_B_OUT	TV SCART Blue Video Output. Internally biased at 1V.
34	34	VCR_Y/CVBS_OUT	VCR SCART Luma/Composite Video Output. Internally biased at 1V.
35	35	VCR_R/C_OUT	VCR SCART Red/Chroma Video Output. Internally biased at 1V for Red video signals and 2.2V for Chroma video signal.
37	37	TV_R/C_IN	TV SCART Red/Chroma Video Input. Internally biased at 1.2V for Red video signals, or 1.9V for Chroma video signals.
38	38	TV_Y/CVBS_IN	TV SCART Luma/Composite Video Input. Internally biased at 1.2V.
39	39	VCR_Y/CVBS_IN	VCR SCART Luma/Composite Video Input. Internally biased at 1.2V.
40	40	VCR_R/C_IN	VCR SCART Red/Chroma Video Input. Internally biased at 1.2V for Red video signals and 1.9V for Chroma video signals.
41	41	VCR_G_IN	VCR SCART Green Video Input. Internally biased at 1.2V.
42	42	VCR_B_IN	VCR SCART Blue Video Input. Internally biased at 1.2V.
43	43	ENC_Y/CVBS_IN	Digital Encoder Luma/Composite Video Input. Internally biased at 1.2V.
44	44	ENC_R/C_IN	Digital Encoder Red/Chroma Video Input. Internally biased at 1.2V for Red video signals, or 1.9V for Chroma video signals.
45	45	ENC_G_IN	Digital Encoder Green Video Input. Internally biased at 1.2V.
46	46	ENC_B_IN	Digital Encoder Blue Video Input. Internally biased at 1.2V.
47	47	ENC_Y_IN	Digital Encoder Luma Video Input. Internally biased at 1.2V.
48	48	ENC_C_IN	Digital Encoder Chroma Video Input. Internally biased at 1.9V.
EP	EP	GNDAUD	Exposed Paddle. Solder to the circuit board ground (GNDAUD) for proper thermal and electrical performance.

Detailed Description

The MAX4397 is a switch matrix that routes audio and video signals between different ports using the I²C interface. The ports consist of the MPEG decoder output, and two SCART connectors for the TV and VCR. Per EN50049 and IEC 933, the encoder can only input a signal to the SCART connector, while TV and VCR SCART connectors are bidirectional.

The MAX4397 circuitry consists of four major sections: the video section, the audio section, the slow- and fast-switching section, and the digital interface.

The video section consists of clamp and bias circuitry, input buffers, reconstruction filters, a switch matrix, a Y/C mixer, and output buffers. All video inputs are AC-coupled through a 0.1µF capacitor to set an acceptable DC level using clamp or bias networks. The bidirectional Red/Chroma outputs can be connected to ground using I²C control to make them terminations when Red/Chroma is an input (see the *Video Inputs* section).

The audio section features an input buffer, a switching matrix, volume- or gain-control circuitry, and output drivers. The audio inputs are AC-coupled through a 0.1µF capacitor. Only the audio encoder inputs of the MAX4397D are different from the MAX4397S. The MAX4397S has a single-ended audio encoder input while the audio encoder input for the MAX4397D is differential. The TV output audio path has volume control from -56dB to +6dB in 2dB steps, while the VCR output audio path has volume control from -6dB to +6dB in 6dB steps. The MAX4397 can be configured to switch inputs during a zero-crossing function to reduce clicks.

Audio/Video Switch for Dual SCART Connectors

The slow-switching feature allows for bidirectional, tri-level, slow-switching input and output signals at pin VCR_SS and TV_SS, respectively. The slow-switching signals from the VCR set the aspect ratio or video source of the TV screen. See the *Slow Switching* section.

Fast switching consists of two inputs from the encoder and VCR, and one output to the TV to insert an on-screen display (OSD). Fast switching is used to route video signals from the VCR or from the encoder to the TV. In addition, the fast-switching output can be configured to a high or low voltage. Fast switching is controlled through the I²C interface.

The digital block contains the 2-wire interface circuitry, control, and status registers. The MAX4397 can be configured through an I²C-compatible interface. DEV_ADDR sets the I²C-compatible address.

SCART Video Switching

The MAX4397 switches video signals between an MPEG decoder, TV SCART, and VCR SCART. The video switch includes reconstruction filters, multiplexed video amplifiers, and a Y/C mixer driver for an RF modulator. See Figure 1 for the functional diagram of the video section. While the SCART connector supports RGB, S-video, and Composite video formats, RGB, and S-video typically share a bidirectional set of SCART connector pins.

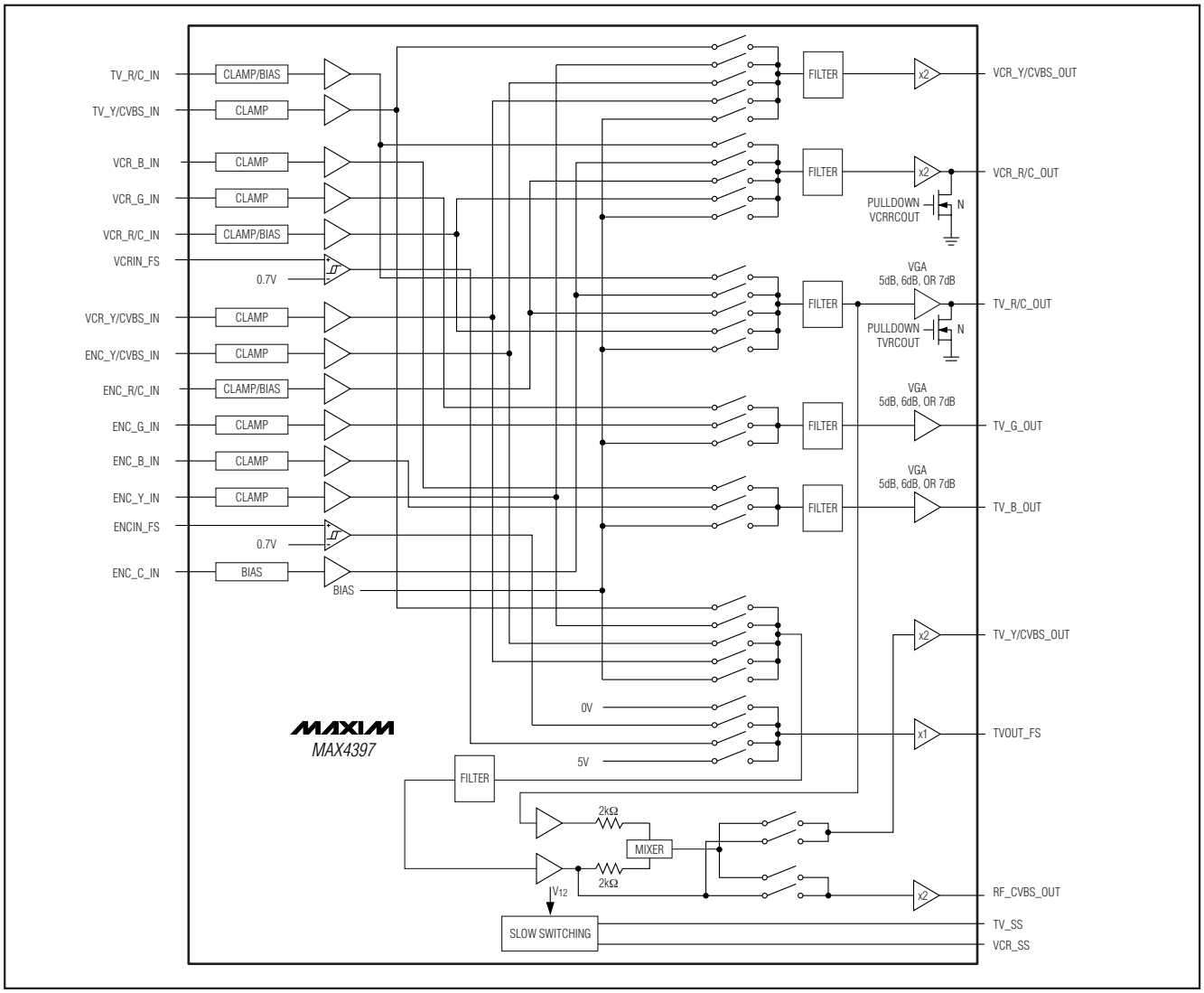


Figure 1. MAX4397 Video Section Functional Diagram

Audio/Video Switch for Dual SCART Connectors

Video Inputs

All video inputs are AC-coupled with an external 0.1µF capacitor. Either a clamp or bias circuit sets the DC input level of the video signals. The clamp circuit positions the sync tip of the Composite (CVBS), the Component RGB, or the S-Video Luma signal. If the signal does not have a sync tip, then the clamp positions the minimum of the signal at the clamp voltage. The bias circuitry is used to position the S-video Chroma signal at midlevel of the Luma (Y) signal. On the video inputs that can receive either a Chroma or a Red video signal, the bias or clamp circuit is selected through I²C. See Tables 3–12 for loading register details.

The MPEG decoder and VCR uses the RGB format and fast switching to insert an on-screen display (OSD), usually text, onto the TV. The MAX4397 supports RGB as an input from either the VCR or the MPEG decoder and as an output only to the TV. The Red video signal of the RGB format and the Chroma video signal of the S-VHS format share the same SCART connector pin. Therefore, RGB and S-video signals cannot be present at the same time. Loop-through is possible with a Composite video signal but not with RGB signals because the RGB SCART pins are used for both input and output.

In SCART, there is the possibility of a bidirectional use of the Red/Chroma pin. When using the Red/Chroma pin as an input port, terminate the Red/Chroma output with a 75Ω resistor to ground. Thus, a ground state is provided by an active pulldown to GNDVID on the Red/Chroma output to support the bidirectional Chroma or Red I/O, turning the output source resistors into terminations (see Figure 2). The active pulldown also provides the “Mute Output” function, and disables the deselected video outputs. The “Mute Output” state is the default power-on state for video.

For high-quality home video, the MPEG decoder, VCR, and TV use the S-video format. The MAX4397 supports S-video signals as an input from the VCR, the MPEG decoder, and the TV, and also as a separately switchable output to the TV and VCR. Because S-video support was not included in the original specifications of the SCART connector, the Luma (Y) signal of S-video and the CVBS signal share the same SCART connector pins. If S-video is present, then a Composite signal must be created from the Y and C signals to drive the RF_CVBS_OUT pin. For S-video, loop-through is not possible since the Chroma SCART port is used for both input and output.

The MAX4397 supports Composite video (CVBS) format, with inputs from the VCR, MPEG decoder, and TV. Full loop-through is possible to the TV and VCR only, since the MPEG decoder SCART connector has separate input and output pins for the CVBS format.

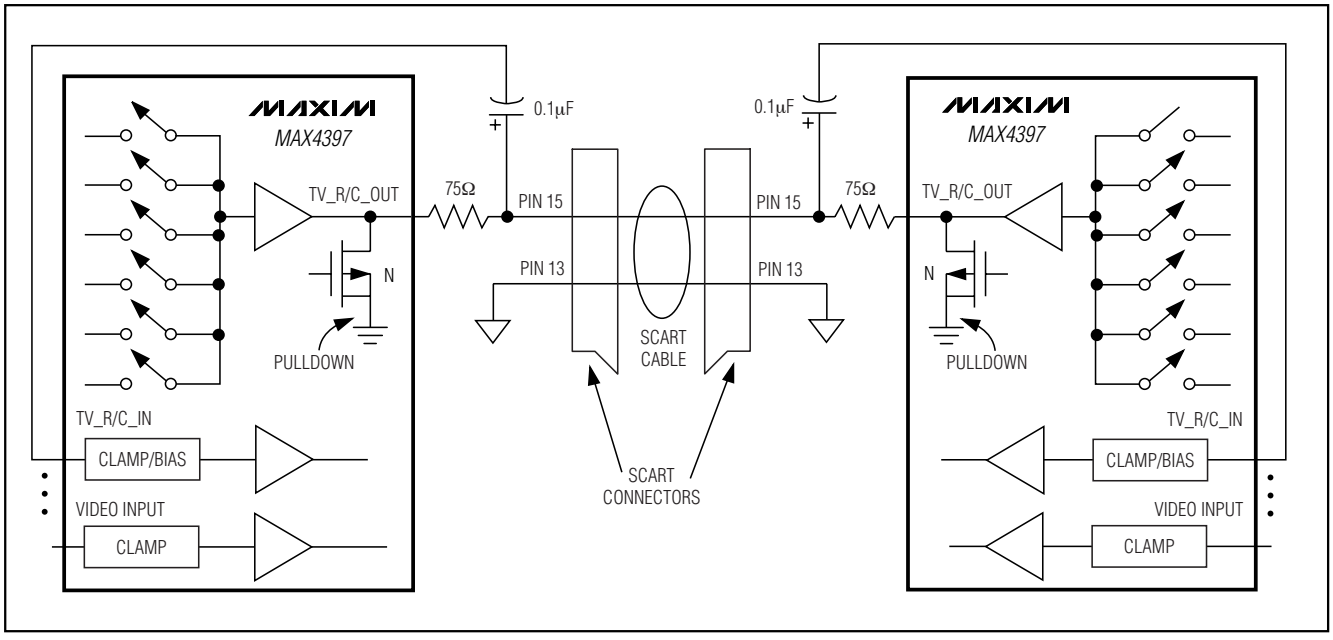


Figure 2. Bidirectional SCART Pins

Audio/Video Switch for Dual SCART Connectors

Video Outputs

The DC level at the video outputs is controlled so that coupling capacitors are not required, and all of the video outputs are capable of driving a DC-coupled, 150Ω, back-terminated coax load with respect to ground.

In a typical television input circuit (see Figure 3) the video output driver on the SCART chip only needs to source current. Users should note that, while the SCART specification states 75Ω impedance, in practice, typical SCART chip implementations assume 75Ω input resistance to ground (and source current from the video output stage).

Since some televisions and VCRs use the horizontal sync height for automatic gain control, the MAX4397 accurately reproduces the sync height to within ±2%.

Slow Switching

The MAX4397 supports the IEC 933-1, Amendment 1, tri-level slow switching that selects the aspect ratio for the display (TV). Under I²C-compatible control, the MAX4397 sets the slow-switching output voltage level. Table 1 shows the valid input levels of the slow-switching signal and the corresponding operating modes of the display device.

Two bidirectional ports are available for slow-switching signals for the TV and VCR. The slow-switching input status is continuously read and stored in the register 0Eh. The slow-switching outputs can be set to a logic level or high impedance by writing to registers 07h and 09h. See Tables 8 and 10 for details.

Fast Switching

The VCR or MPEG decoder outputs a fast-switching signal to the display device or TV to insert on-screen display (OSD). The fast-switching signal can also be set to a constant high or low output signal through the I²C interface. The fast-switching output can be set through writing to register 07h.

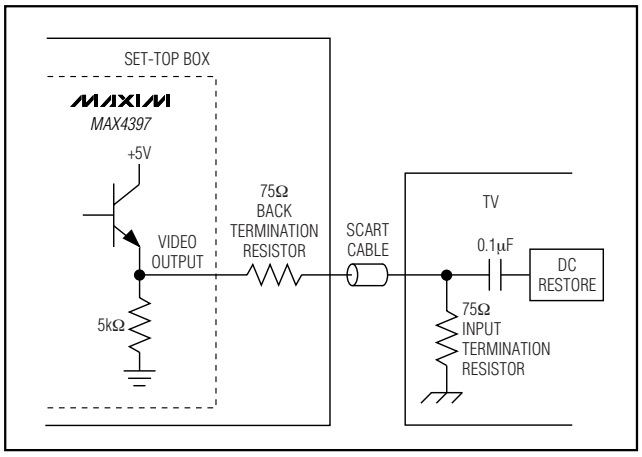


Figure 3. Typical TV Input Circuit

Y/C Mixer

The MAX4397 includes an on-chip mixer to produce Composite video (CVBS) when S-video (Y and C) is present. The Composite video drives the RF_CVBS_OUT output pin. The circuit sums Y and C signals to obtain the CVBS component. A +6dB output buffer drives RF_CVBS_OUT.

Video Reconstruction Filter

The encoder DAC outputs need to be lowpass-filtered to reject the out-of-band noise. The MAX4397 integrates the reconstruction filter. The filter is fourth order, which is composed of two Sallen-Key biquad in cascade, implementing a Butterworth-type transfer function. The internal reconstruction filters feature a 6MHz cutoff frequency, and -35dB minimum attenuation at 27MHz. Note that the SET pin is used to set the accuracy of the filter cutoff frequency. Connect a 100kΩ resistor from SET to ground.

SCART Audio Switching

Audio Inputs

All audio inputs for the MAX4397S are single-ended and are AC-coupled. The MAX4397D audio inputs are singled-ended and AC-coupled except for the audio encoder input, which is differential DC-coupled.

The audio block has three stereo audio inputs from the TV, the VCR, and the MPEG decoder SCART. Each input has a 100kΩ resistor connected to an internally generated voltage equal to 0.23 x V_{12}, except for the encoder input of the MAX4397D, where the DC bias is fixed externally.

Table 1. Slow-Switching Modes

SLOW-SWITCHING SIGNAL VOLTAGE (V)	MODE
0 to 2	Display device uses an internal source such as a built-in tuner to provide a video signal
4.5 to 7.0	Display device uses a video signal from the SCART connector and sets the display to 16:9 aspect ratio
9.5 to 12.6	Display device uses a signal from the SCART connector and sets the display to 4:3 aspect ratio

Audio/Video Switch for Dual SCART Connectors

Audio Outputs

Both right and left channels have a stereo output for the TV and VCR SCART. The monaural output, which is a mix of the TV right and left channels, drives the RF modulator, RF_MONO_OUT. The monaural mixer, a resistor summer, attenuates the amplitude of each of the two signals by 6dB. A 12.54dB gain block follows the monaural mixer. If the left and right audio channels were completely uncorrelated, then a 9.54dB gain block is used. See Figures 4 and 5 for the functional diagram of the audio section.

Clickless Switching

The TV channel incorporates a zero-crossing detect (ZCD) circuit that minimizes click noise due to abrupt signal level changes that occur when switching between audio signals at an arbitrary moment.

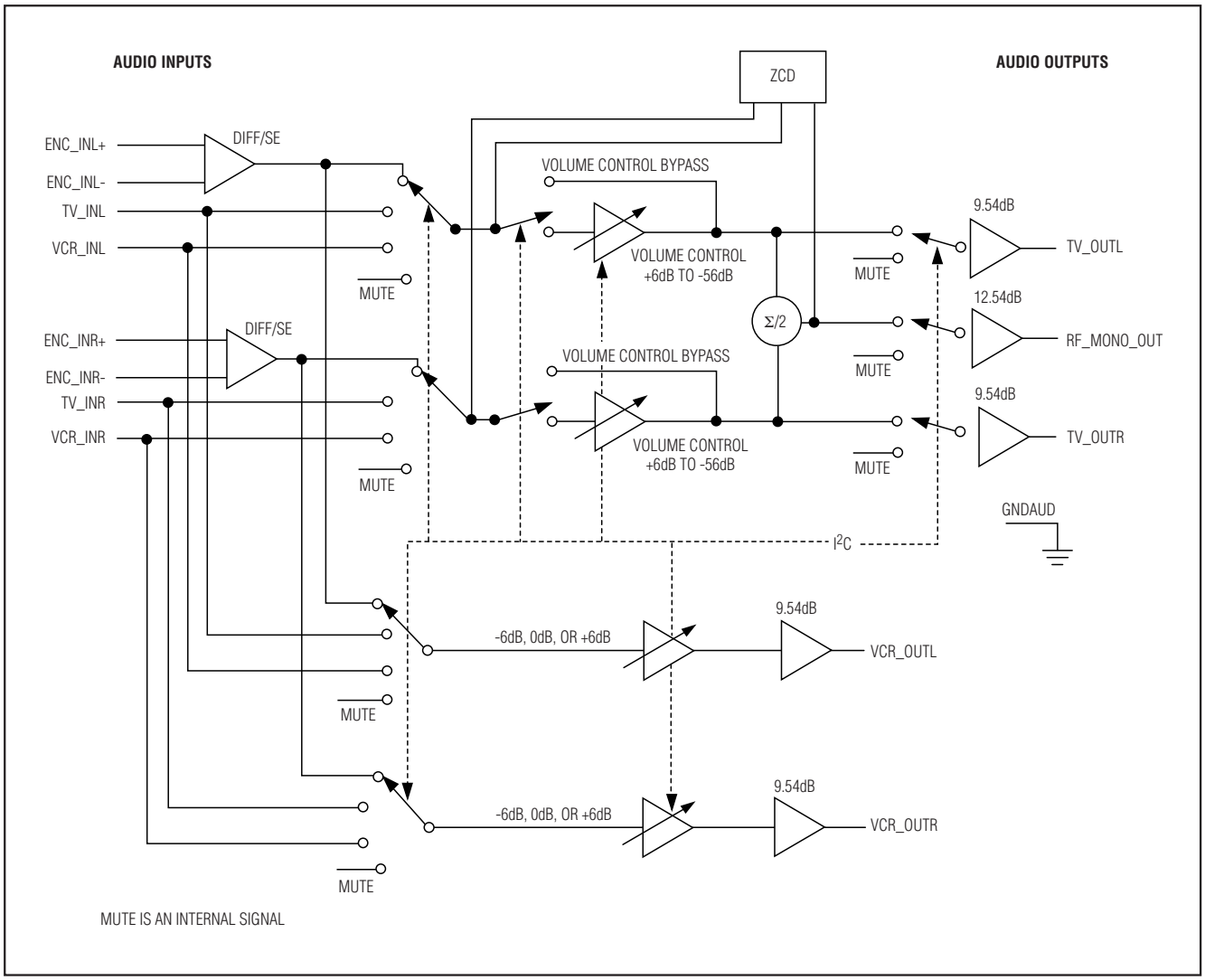


Figure 4. MAX4397D Audio Section Functional Diagram

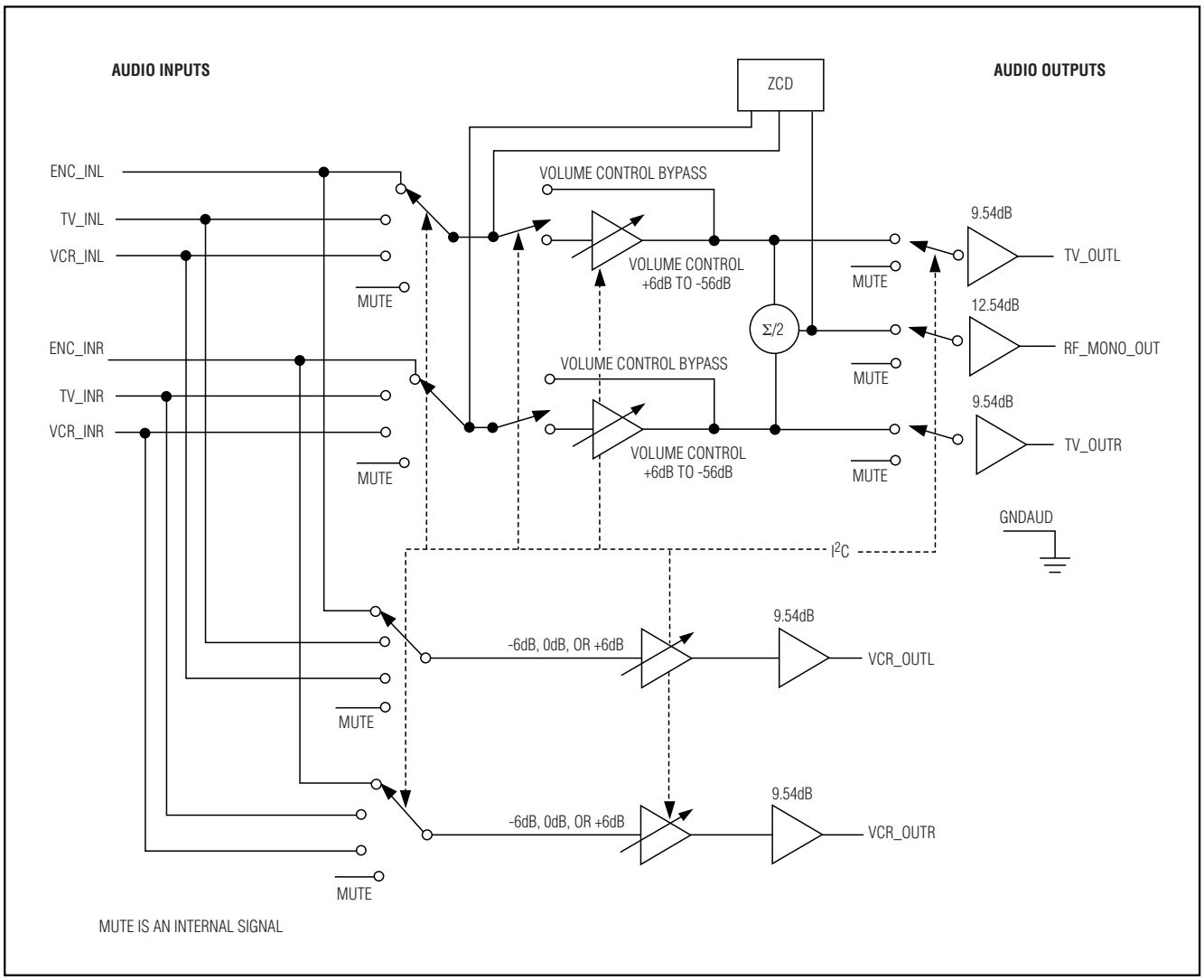


Figure 5. MAX4397S Audio Section Features Singled-Ended Encoder Input

To implement the zero-crossing function when switching audio signals, set the ZCD bit by loading register 00h through the I²C-compatible interface (if the ZCD bit is not already set). Then set the mute bit low by loading register 00h. Next, wait for a sufficient period of time for the audio signal to cross zero. This period is a function of the audio signal path's low-frequency 3dB corner (f_{L3dB}). Thus, if f_{L3dB} = 1kHz, the time period to wait for a zero-crossing detect is $^1/_2$kHz or 0.5ms.

Next, set the appropriate TV switches using register 01h. Finally, clear the mute bit (while leaving the ZCD bit high) using register 00h. The MAX4397 switches the signal out of mute at the next zero crossing.

To implement the zero-cross function for TV volume changes, or for TV and phono volume bypass switching, simply ensure the ZCD bit in register 00h is set.

Audio/Video Switch for Dual SCART Connectors

Volume Control

The TV channel volume control ranges from -56dB to +6dB in 2dB steps. The VCR volume control settings are programmable for -6dB, 0dB, and +6dB. These gain levels are referenced to the application inputs, where some dividers are present. With the ZCD bit set, the TV volume control switches only at zero-crossings, thus minimizing click noise. The TV outputs can bypass the volume control. Likewise, the monaural output signal can be processed by the TV volume control or it can bypass the volume control.

Digital Section

Serial Interface

The MAX4397 uses a simple 2-wire serial interface requiring only two standard microprocessor port I/O lines. The fast-mode I²C-compatible serial interface allows communication at data rates up to 400kbps or 400kHz. Figure 6 shows the timing diagram of the signals on the 2-wire interface.

The two bus lines (SDA and SCL) must be at logic-high when the bus is not in use. The MAX4397 is a slave device and must be controlled by a master device. Pullup resistors from the bus lines to the supply are required when push-pull circuitry is not driving the lines.

The logic level on the SDA line can only change when the SCL line is low. The start and stop conditions occur when SDA toggles low/high while the SCL line is high (see Figure 6). Data on SDA must be stable for the duration of the setup time ($t_{SU,DAT}$) before SCL goes high. Data on SDA is sampled when SCL toggles high with data on SDA stable for the duration of the hold time ($t_{HD,DAT}$). Note that data is transmitted in an 8-bit byte. A total of nine clock cycles are required to transfer a byte to the MAX4397. The device acknowledges the successful receipt of the byte by pulling the SDA line low during the 9th clock cycle.

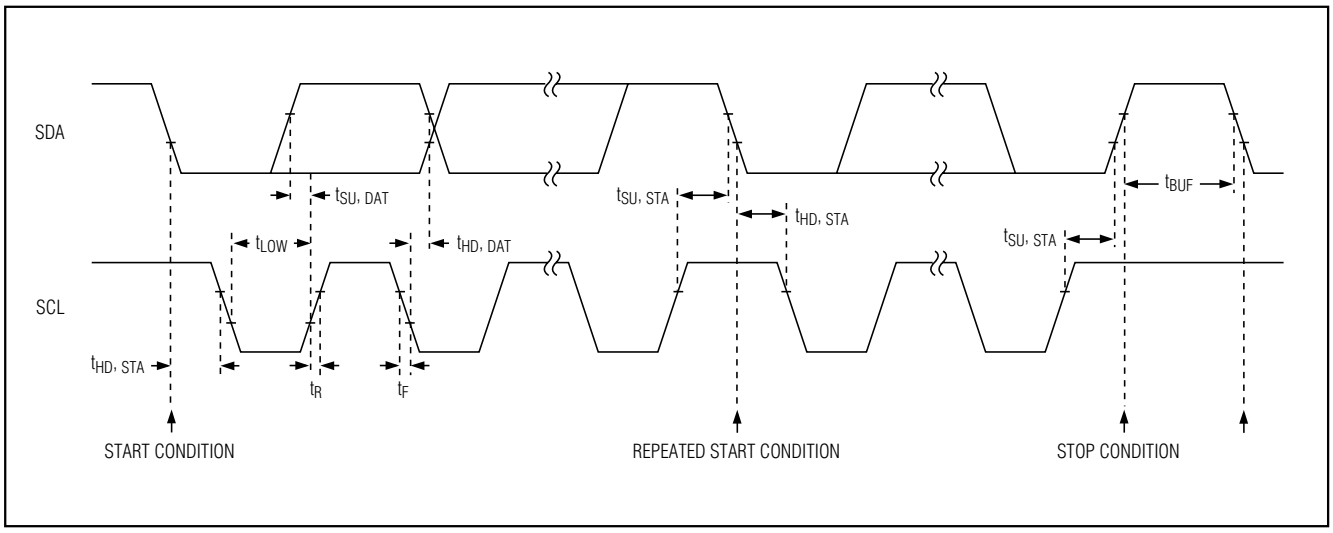


Figure 6. SDA and SCL Signal Timing Diagram

Data Format of the I²C Interface

Write Mode

S	Slave Address (Write address)	A	Register Address	A	Data	A	P

Read Mode

S	Slave Address (Write address)	A	Register Address	A	Sr	Slave Address (Read address)	A	Data	NA	P

S = Start Condition, A = Acknowledge, NA = Not Acknowledge, Sr = Repeat Start Condition, P = Stop Condition

I²C Compatibility

The MAX4397 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs. SDA has an open drain that pulls the bus line to a logic-low during the 9th clock pulse. Figure 7 shows a typical I²C interface application. The communication protocol supports the standard I²C 8-bit communications. The MAX4397 address is compatible with the 7-bit I²C addressing protocol only; 10-bit format is not supported.

Digital Inputs and Interface Logic

The I²C-compatible, 2-wire interface has logic levels defined as V_{IL} = 0.8V and V_{IH} = 2.0V. All of the inputs include Schmitt-trigger buffers to accept low-transition interfaces. The digital inputs are compatible with 3V CMOS logic levels.

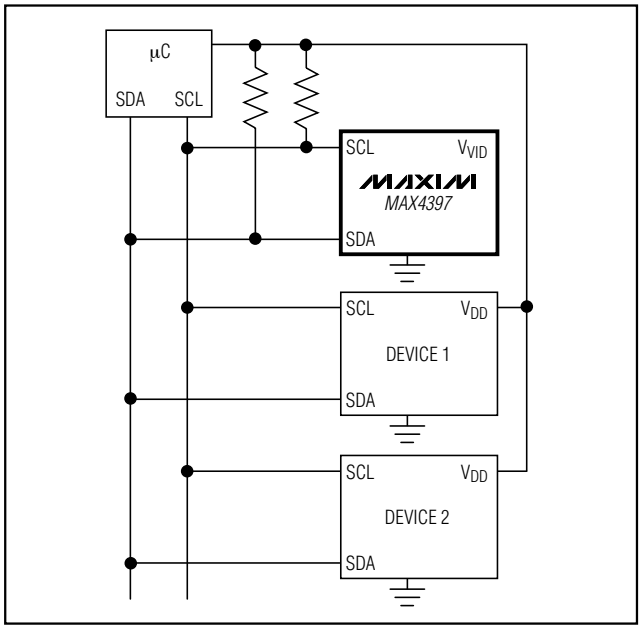


Figure 7. Typical I²C Interface Application

Programming

Connect DEV_ADDR to ground to set the MAX4397 write and read address as shown in Table 2.

Table 2. Slave Address Programming

ADDRESS PIN STATE	WRITE ADDRESS	READ ADDRESS
V_{VID}	96h	97h
GNDVID	94h	95h

Data Register Writing and Reading

Program the SCART video and audio switches by writing to registers 00h through 0Dh. Registers 00h through 0Eh can also be read, allowing read-back of data after programming and facilitating system debugging. The status register is read-only and can be read from address 0Eh. See Tables 3–12 for register programming information.

Applications Information

Hot-Plug of SCART Connectors

The MAX4397 features high-ESD protection on all SCART inputs and outputs, and requires no external transient-voltage suppressor (TVS) devices to protect against floating chassis discharge. Some set-top boxes have a floating chassis problem in which the chassis is not connected to earth ground. As a result, the chassis can charge up to 500V. When a SCART cable is connected to the SCART connector, the charged chassis can discharge through a signal pin. The equivalent circuit is a 2200pF capacitor charged to 311V connected through less than 0.1Ω to a signal pin. The MAX4397 is soldered on the PC board when it experiences such a discharge. Therefore, the current spike flows through the ESD protection diodes and is absorbed by the supply bypass capacitors, which have high capacitance and low ESR.

To better protect the MAX4397 against excess voltages during the cable discharge condition, place an additional 75Ω resistor in series with all inputs and outputs to the SCART connector. For harsh environments where ±15kV protection is needed, the MAX4385E and MAX4386E single and quad high-speed op amps feature the industry's first integrated ±15kV ESD protection on video inputs and outputs.

Audio/Video Switch for Dual SCART Connectors

Power Supplies and Bypassing

The MAX4397 features single 5V and 12V supply operation and requires no negative supply. The +12V supply V_{12} is for the SCART switching function. For pin V_{12}, place all bypass capacitors as close as possible with a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. Connect all V_{AUD} pins together to +5V and bypass with a 10µF electrolytic capacitor in parallel with a 0.47µF low-ESR ceramic capacitor to audio ground. Bypass V_{AUD} pins with a 0.1µF capacitor to audio ground. Bypass AUD_BIAS to audio ground with a 10µF electrolytic in parallel with a 0.1µF ceramic capacitor.

Bypass V_{DIG} with a 0.1µF ceramic capacitor to digital ground. Bypass each V_{VID} to video ground with a 0.1µF ceramic capacitor. Connect V_{VID} in series with a 200nH ferrite bead to the +5V supply.

Layout and Grounding

For optimal performance, use controlled-impedance traces for video signal paths and place input termination resistors and output back-termination resistors close to the MAX4397. Avoid routing video traces parallel to high-speed data lines.

The MAX4397 provides separate ground connections for video, audio, and digital supplies. For best performance, use separate ground planes for each of the ground returns and connect all three ground planes together at a single point. Refer to the MAX4397 evaluation kit for a proven circuit board layout example.

Table 3. Data Format for Write Mode

REGISTER ADDRESS (HEXADECIMAL)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	TV volume bypass	ZCD	TV volume control					TV audio output mute
01h	VCR volume control		Not used	Not used	VCR audio selection		TV audio selection	
02h	Not used							
03h	Not used							
04h	Not used							
05h	Not used							
06h	TV_R/C_IN clamp	RGB gain		TV G and B video switch		TV video switch		
07h	Not used	RF_CVBS_ OUT switch	TV_Y/ CVBS_OUT switch	TV fast blank (fast switching)		TV_R/C_OUT ground	Set function TV	
08h	VCR_R/ C_IN clamp	Not used	Not used	Not used	ENC_R/ C_IN clamp	VCR video switch		
09h	Not used	Not used	Not used	Not used	Not used	VCR_R/C_OUT ground	Set function VCR	
0Ah	Not used							
0Bh	Not used							
0Ch	Not used							
0Dh	VCR_Y/ CVBS_OUT enable	VCR_R/ C_OUT enable	TV_R/C_OUT enable	TV_G_OUT enable	TV_B_OUT enable	TV_Y/ CVBS_OUT enable	TVOUT _FS enable	RF_CVBS_ OUT enable

Table 4. Data Format for Read Mode

REGISTER ADDRESS (HEXADECIMAL)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0Eh	Thermal SHDN	Power-on reset	Not used		VCR slow switch input		TV slow switch input	

Table 5. Register 00h: TV Audio control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Audio Mute								0	Off
								1	On (power-on default)
TV Volume Control			0	0	0	0	0		+6dB gain
			0	0	0	0	1		+4dB gain
			0	0	0	1	0		+2dB gain
			0	0	0	1	1		0dB gain (power-on default)
			0	0	1	0	0		-2dB gain
			0	0	1	0	1		-4dB gain
			1	1	1	1	0		-54dB gain
			1	1	1	1	1		-56dB gain
TV Zero-Crossing Detector		0							Off
		1							On (power-on default)
TV Volume Bypass	0								TV audio passes through volume control (power-on default)
	1								TV audio bypasses volume control

Table 6. Register 01h: TV/VCR Audio Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Input Source for TV Audio							0	0	Encoder audio
							0	1	VCR audio
							1	0	TV audio
							1	1	Mute (power-on default)
Input Source for VCR Audio					0	0			Encoder audio
					0	1			VCR audio
					1	0			TV audio
					1	1			Mute (power-on default)
VCR Volume Control	0	0							0dB gain (power-on default)
	0	1							+6dB gain
	1	0							-6dB gain
	1	1							0dB gain

Audio/Video Switch for Dual SCART Connectors

Table 7. Register 06h: TV Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for TV Video									**TV_Y/CVBS_OUT**	**TV_R/C_OUT**
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	TV_R/C_IN
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
Input Sources for TV_G_OUT and TV_B_OUT									**TV_G_OUT**	**TV_B_OUT**
				0	0				ENC_G_IN	ENC_B_IN
				0	1				VCR_G_IN	VCR_B_IN
				1	0				Mute	Mute
				1	1				Mute (power-on default)	Mute (power-on default)
RGB Gain		0	0						6dB (power-on default)	
		0	1						7dB	
		1	0						5dB	
		1	1						5dB	
TV_R/C_IN Clamp/Bias	0								DC restore clamp active at input (power-on default)	
	1								Chrominance bias applied at input	

Table 8. Register 07h: TV Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set TV Function Switching							0	0	Low (<2V), internal source (power-on default)
							0	1	Medium (4.5V to 7V), external SCART source with 16:9 aspect ratio
							1	0	High impedance
							1	1	High (>9.5V), external SCART source with 4:3 aspect ratio
TV_R/C_OUT Ground						0			Normal operation, pulldown on TV_R/C_OUT is off (power-on default)
						1			Ground, pulldown on TV_R/C_OUT is on, the output amplifier driving TV_R/C_OUT is turned off
Fast Blank (Fast Switching)				0	0				0V (power-on default)
				0	1				Same level as ENC_FB_IN
				1	0				Same level as VCR_FB_IN
				1	1				V_{VID}
TV_Y/CVBS_OUT Switch			0						Composite video from the Y/C mixer is output
			1						The TV_Y/CVBS_OUT signal selected in register 06h is output (power-on default)
RF_CVBS_OUT Switch		0							Composite video from the Y/C mixer is output (power-on default)
		1							The TV_Y/CVBS_OUT signal selected in register 06h is output

Table 9. Register 08h: VCR Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for VCR Video									**VCR_Y/CVBS_OUT**	**VCR_R/C_OUT**
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	TV_R/C_IN
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
VCR_R/C_IN Clamp/Bias	0								DC restore clamp active at input (power-on default)	
	1								Chrominance bias applied at input	
ENC_R/C_IN Clamp/Bias					0				DC restore clamp active at input (power-on default)	
					1				Chrominance bias applied at input	

Audio/Video Switch for Dual SCART Connectors

Table 10. Register 09h: VCR Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set VCR Function Switching							0	0	Low (<2V), internal source (power-on default)
							0	1	Medium (4.5V to 7V), external SCART source with 16:9 aspect ratio
							1	0	High impedance
							1	1	High (>9.5V), external SCART source with 4:3 aspect ratio
VCR_R/C_OUT ground						0			Normal operation, pulldown on VCR_R/C_OUT is off (power-on default)
						1			Ground, pulldown on VCR_R/C_OUT is on, the output amplifier driving VCR_R/C_OUT is turned off

Table 11. Register 0Dh: Output Enable

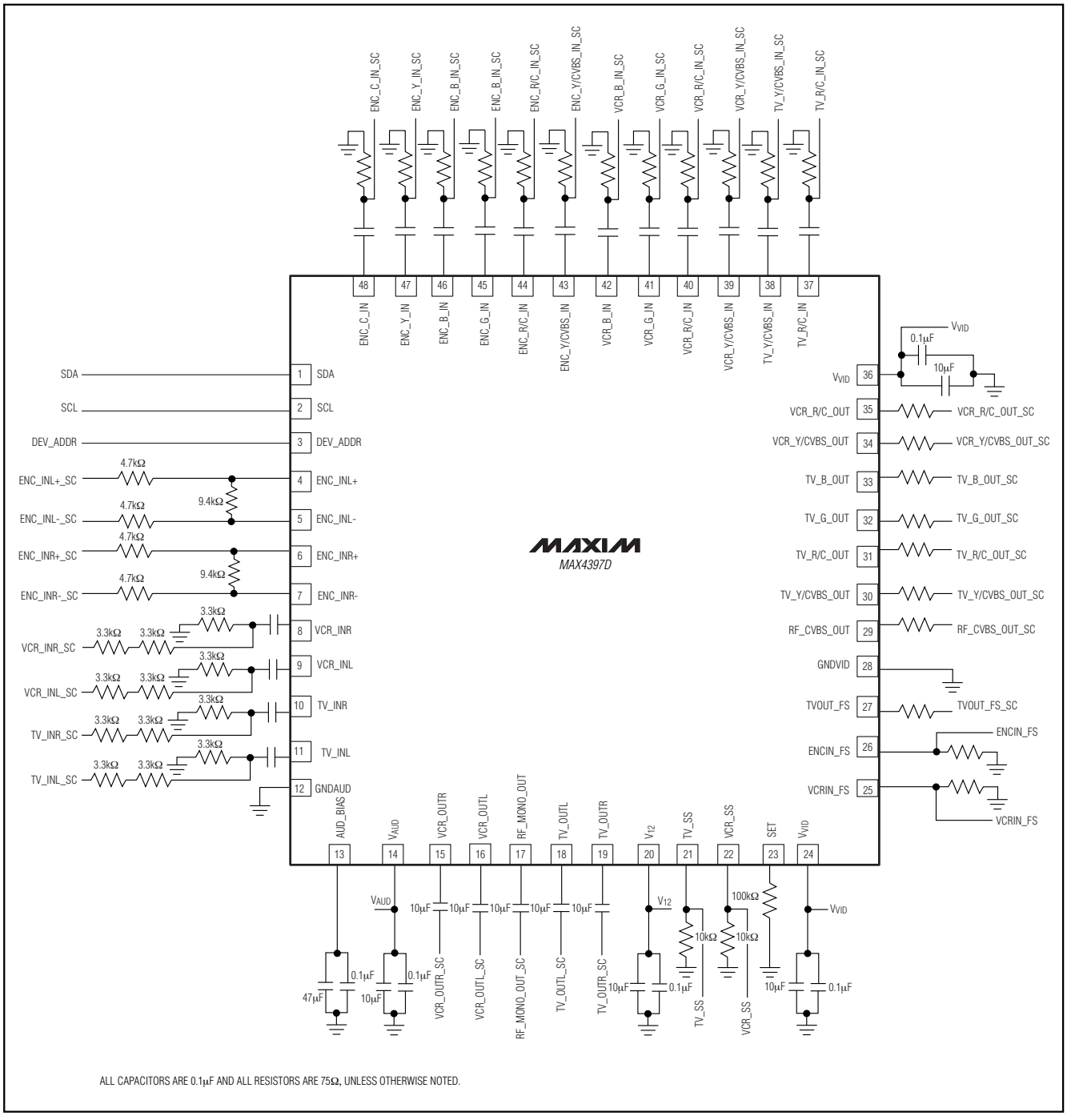
DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
RF_CVBS_OUT								0	Off (power-on default)
								1	On
TVOUT_FS							0		Off (power-on default)
							1		On
TV_Y/CVBS_OUT						0			Off (power-on default)
						1			On
TV_B_OUT					0				Off (power-on default)
					1				On
TV_G_OUT				0					Off (power-on default)
				1					On
TV_R/C_OUT			0						Off (power-on default)
			1						On
VCR_R/C_OUT		0							Off (power-on default)
		1							On
VCR_Y/CVBS_OUT	0								Off (power-on default)
	1								On

Table 12. Register 0Eh Status

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Slow Switch Input							0	0	0 to 2V, internal source
							0	1	4.5V to 7V, external source with 16:9 aspect ratio
							1	0	Not used
							1	1	9.5V to 12.6V, external source with 4:3 aspect ratio
VCR Slow Switch Input					0	0			0 to 2V, internal source
					0	1			4.5V to 7V, external source with 16:9 aspect ratio
					1	0			Not used
					1	1			9.5V to 12.6V, external source with 4:3 aspect ratio
Power-On Reset		0							V_{VID} is too low for digital logic to operate
		1							V_{VID} is high enough for digital logic to operate
Thermal Shutdown	0								The part is in thermal shutdown
	1								The temperature is below the TSHD limit

Audio/Video Switch for Dual SCART Connectors

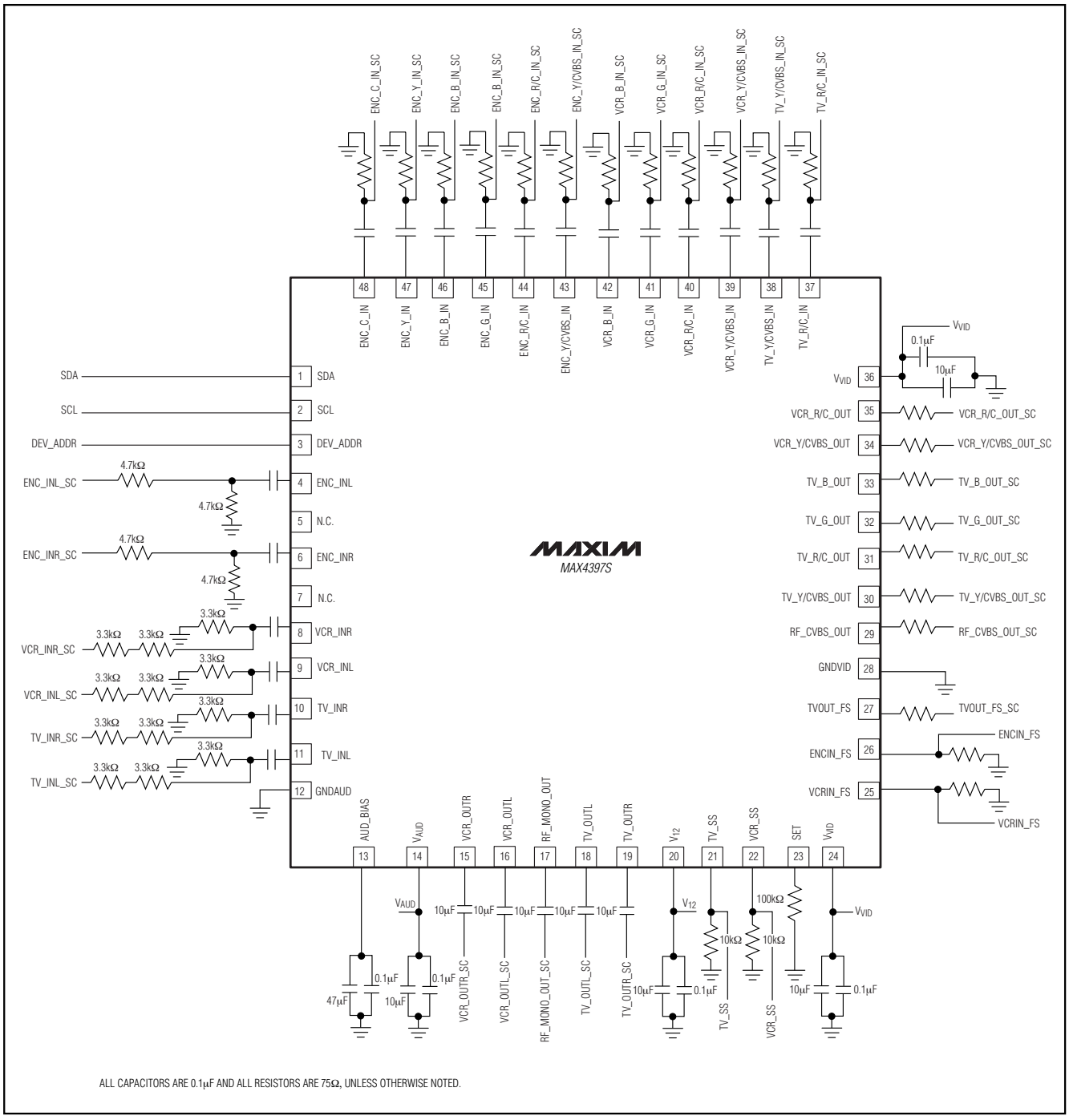
Typical Application Circuits



ALL CAPACITORS ARE 0.1µF AND ALL RESISTORS ARE 75Ω, UNLESS OTHERWISE NOTED.

Audio/Video Switch for Dual SCART Connectors

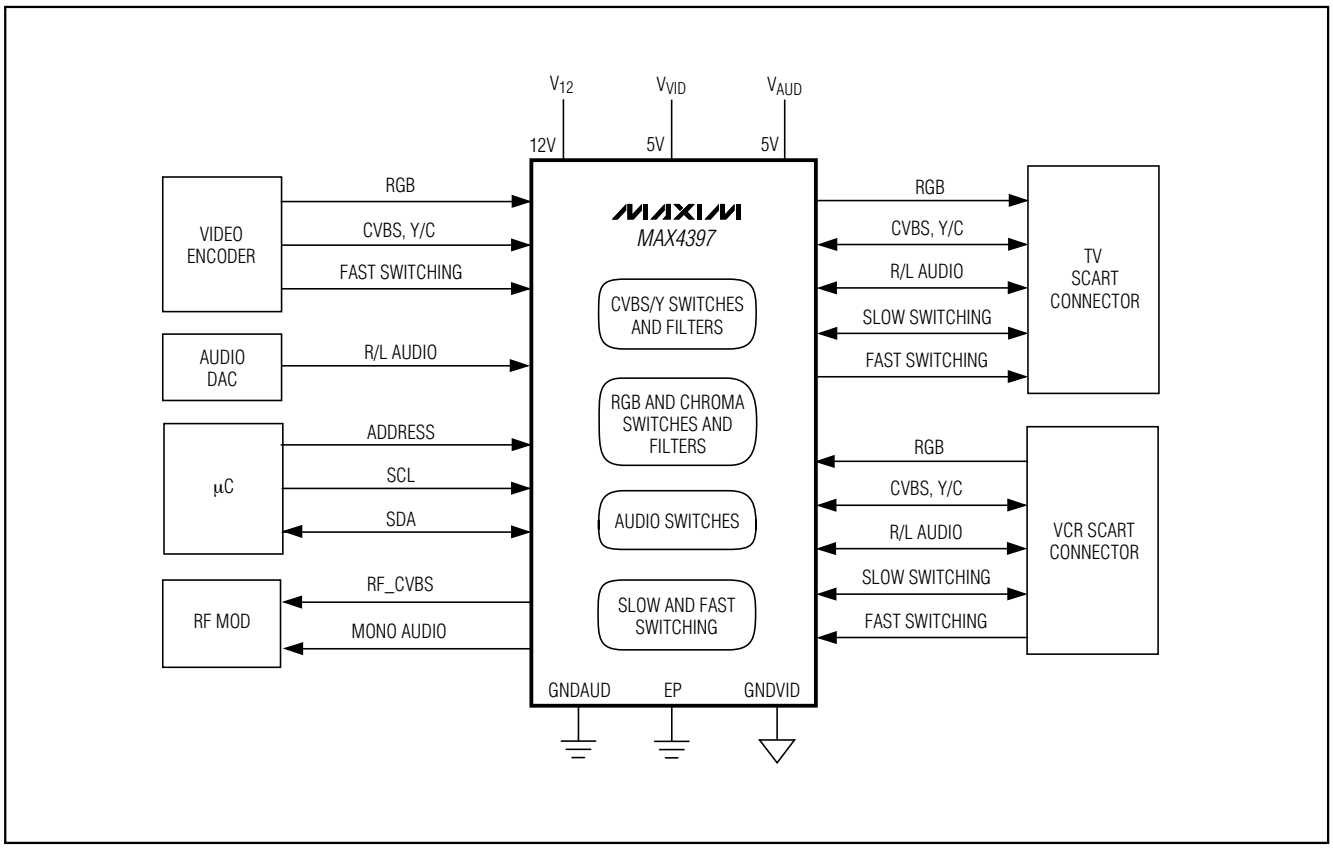
Typical Application Circuits (continued)



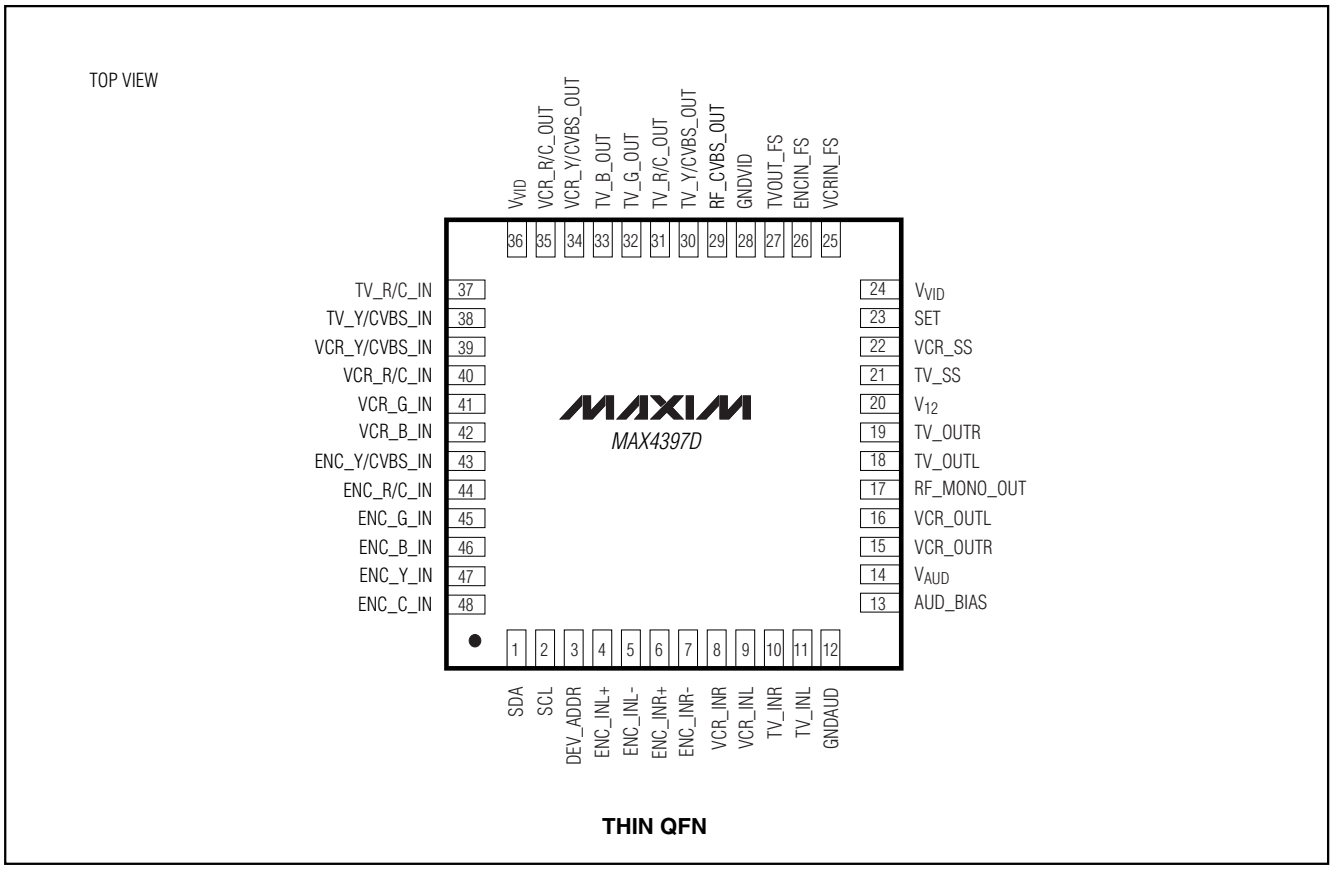
ALL CAPACITORS ARE 0.1µF AND ALL RESISTORS ARE 75Ω, UNLESS OTHERWISE NOTED.

Audio/Video Switch for Dual SCART Connectors

System Block Diagram



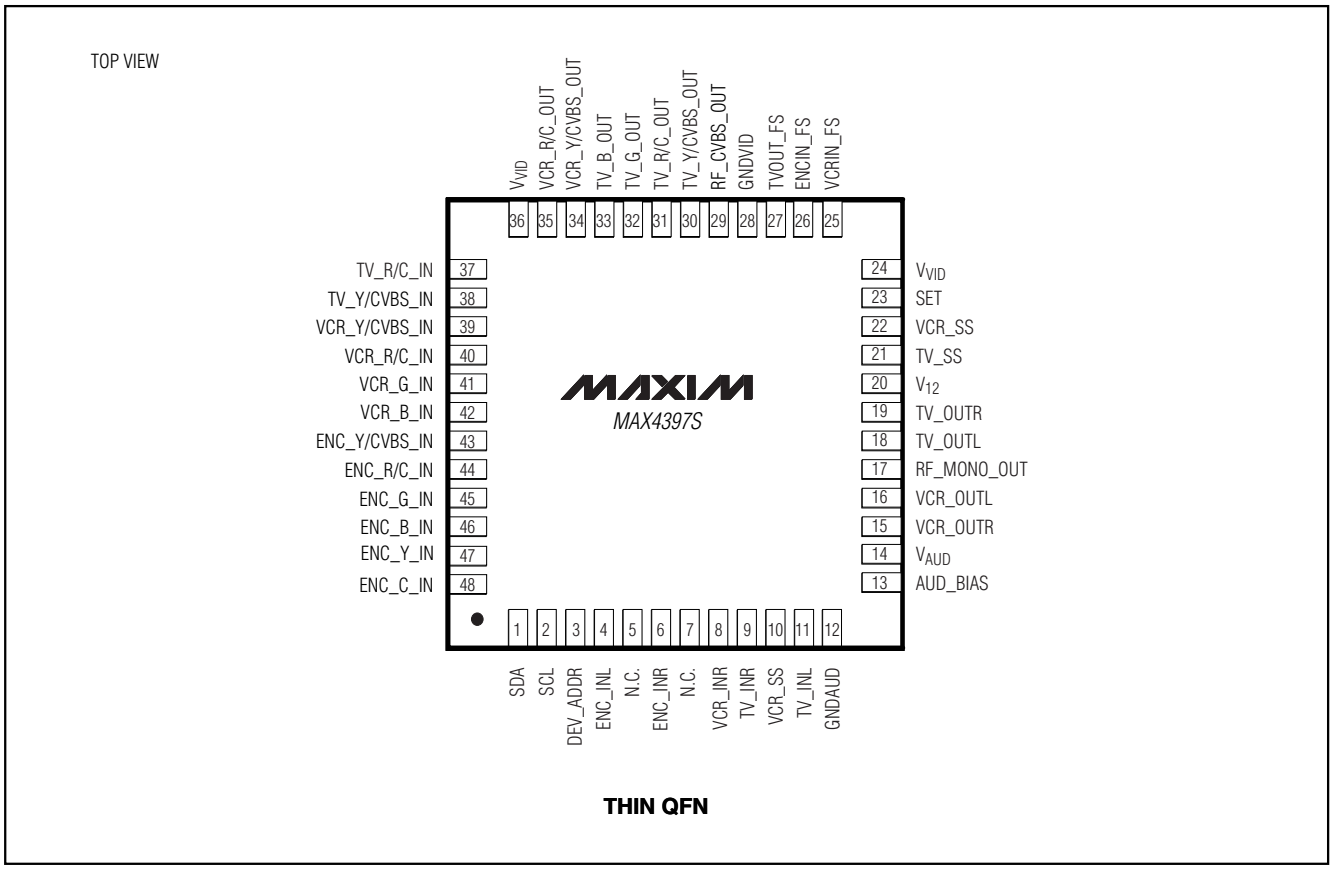
Pin Configurations



THIN QFN

Audio/Video Switch for Dual SCART Connectors

Pin Configurations (continued)



THIN QFN

Chip Information

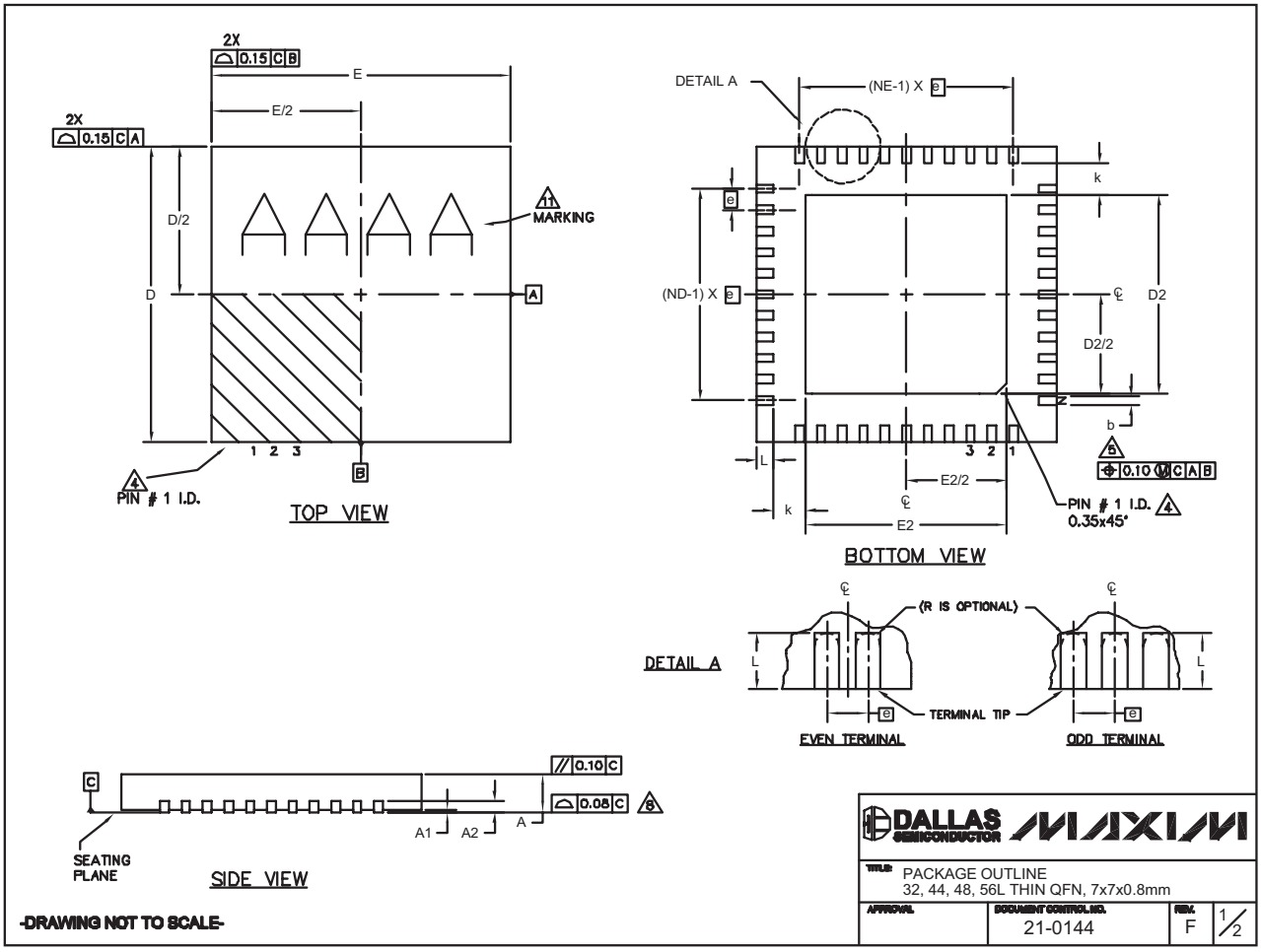
TRANSISTOR COUNT: 13,265

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



Audio/Video Switch for Dual SCART Connectors

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. F | 2/2

Revision History

Pages changed at Rev 2: 1, 13-17, 20, 21, 25, 26, 30

Pages changed at Rev 3: 1, 17, 26, 29, 30

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