19-1148; Rev 0; 11/96

MAXIM

Quad, Low-Voltage, SPST Analog Switches with Enable

General Description

The MAX4536/MAX4537/MAX4538 are quad, low-voltage, single-pole/single-throw (SPST) analog switches with a common enable pin. They are pin compatible with the industry-standard 74HC4316. The MAX4536 has four normally open (NO) switches, and the MAX4537 has four normally closed (NC) switches. The MAX4538 has two NO switches and two NC switches.

These switches operate from a +2V to +12V single supply, or from ±2V to ±6V dual supplies. On-resistance (200Ω max) is matched between switches to 4Ω (max) and is flat (10Ω max) over the specified signal range. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply or dual ±5V supplies.

Applications

Battery-Operated Equipment

Low-Voltage Data Acquisition

Test Equipment

Avionics

Portable Equipment

Audio-Signal Routing

Networking

Features

- **Pin Compatible with 74HC4316**
- **±2.0V to ±6V Dual Supplies**
  +2.0V to +12V Single Supply
- **Four Separately Controlled SPST Switches with Common Enable**
- **100Ω Signal Paths with Dual ±5V Supplies**
  200Ω Signal Paths with Single +4.5V Supply
- **Rail-to-Rail Signal Handling**
- **t_{ON} and t_{OFF} = 100ns and 80ns at ±4.5V Supply**
- **Less than 1µW Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Small Packages: PDIP, QSOP, Narrow SO**

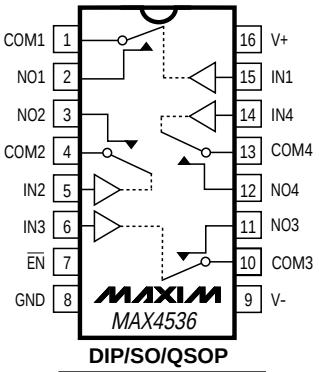
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4536CPE	0°C to +70°C	16 Plastic DIP
MAX4536CSE	0°C to +70°C	16 Narrow SO
MAX4536CEE	0°C to +70°C	16 QSOP
MAX4536C/D	0°C to +70°C	Dice*
MAX4536EPE	-40°C to +85°C	16 Plastic DIP
MAX4536ESE	-40°C to +85°C	16 Narrow SO
MAX4536EEE	-40°C to +85°C	16 QSOP

Ordering Information continued at end of data sheet.

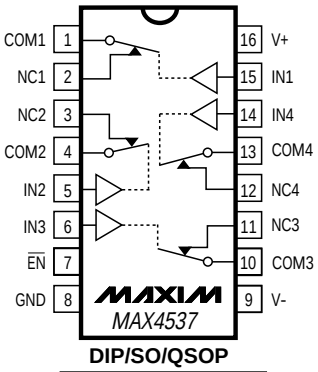
**Contact factory for availability.*

Pin Configurations/Functional Diagrams/Truth Tables



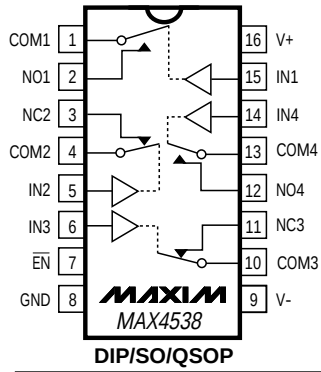
DIP/SO/QSOP

MAX4536		
$\overline{EN}$	IN_	SWITCH_
0	0	OFF
0	1	ON
1	X	OFF



DIP/SO/QSOP

MAX4537		
$\overline{EN}$	IN_	SWITCH_
0	0	ON
0	1	OFF
1	X	OFF



DIP/SO/QSOP

MAX4538			
$\overline{EN}$	IN_	SWITCHES 1, 4	SWITCHES 2, 3
0	0	OFF	ON
0	1	ON	OFF
1	X	OFF	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Quad, Low-Voltage, SPST Analog Switches with Enable

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +13.0V
V- .....-13.0V to +0.3V
V+ to V-.....-0.3V to +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal.....±10mA
Peak Current into Any Terminal
(pulsed at 1ms,10% duty cycle).....±20mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 8.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX453_C_ E .....0°C to +70°C
MAX453_E_ E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NC_, NO_, COM_, $\overline{EN}$, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.
Note 2: All leads are soldered or welded to PC boards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±5V Dual Supplies

(V+ = 4.5V to 5.5V, V- = -4.5V to -5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	V-		V+	V
COM_ NO_, COM_ NC_ On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		55	100	Ω
			C, E			125	
COM_ NO_, COM_ NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		1	4	Ω
			C, E			6	
COM_ NO_, COM_ NC_ On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 5.0V, V- = -5.0V, $V_{COM_}$ = -3.0V, 0, +3.0V, $I_{COM_}$ = 1mA	+25°C		4	10	Ω
			C, E			15	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ∓4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Note 7)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ∓4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Note 7)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ±4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		1.4	2.4	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.8	1.4		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—±5V Dual Supplies (continued)

(V+ = 4.5V to 5.5V, V- = -4.5V to -5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V (Figure 1)	+25°C		35	100	ns
			C, E			125	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V (Figure 1)	+25°C		15	50	ns
			C, E			60	
Break-Before-Make Time Delay (MAX4538 Only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5.5V, V- = -5.5V (Figure 2)	+25°C	5	15		ns
Charge Injection (Figure 3)	Q	C_L = 1.0nF, $V_{NO_}$ = 0V, R_S = 0Ω	+25°C		1	5	pC
NO_, NC_ Off-Capacitance (Figure 6)	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz	+25°C		2		pF
COM_ Off-Capacitance (Figure 6)	$C_{COM_(OFF)}$	$V_{COM_}$ = GND, f = 1MHz	+25°C		2		pF
COM_ On-Capacitance (Figure 7)	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = GND, f = 1MHz	+25°C		6		pF
Off-Isolation (Note 8, Figure 4)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 1MHz	+25°C		-65		dB
Channel-to-Channel Crosstalk (Note 9, Figure 5)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 1MHz	+25°C		-75		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E	-6		6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	
V- Supply Current	I-	V- = -5.5V	+25°C	-1	0.05	1	µA
			C, E	-10		10	

ELECTRICAL CHARACTERISTICS—+5V Single Supply

(V+ = 4.5V to 5.5V, V- = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	0		V+	V
COM_ -NO_, COM_ -NC_ On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		90	200	Ω
			C, E			225	
COM_ -NO_, COM_ -NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		2	8	Ω
			C, E			10	
NO_, NC_ Off-Leakage Current (Notes 7, 10)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V, $V_{N_}$ = +4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Notes 7, 10)	$I_{COM_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V, $V_{N_}$ = +4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Note 7, 10)	$I_{COM_(ON)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V,	+25°C	-2	0.01	2	nA
			C, E	-20		20	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		1.4	2.4	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.8	1.4		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 4.5V (Figure 1)	+25°C		50	100	ns
			C, E		20	125	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 4.5V (Figure 1)	+25°C			80	ns
			C, E			100	
Break-Before-Make Time Delay	t_{BBM}	MAX4538, $V_{COM_}$ = 3V, V+ = 5.5V (Figure 2)	+25°C	5	25		ns
Charge Injection (Figure 3) (Note 4)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

ELECTRICAL CHARACTERISTICS—+3V Single Supply

(V+ = 2.7V to 3.6V, V- = 0V, V_{INH} = 2.0V, V_{INL} = 0.5V, $V_{\overline{EN}}$ = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	0		V+	V
COM_ -NO_, COM_ -NC_ On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1.5V, $I_{COM_}$ = 0.1mA	+25°C		210	500	Ω
			C, E			600	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		0.9	2.0	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.5	0.9		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 4)							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V (Figure 1)	+25°C		80	250	ns
			C, E			300	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V (Figure 1)	+25°C		40	100	ns
			C, E			120	
Break-Before-Make Time Delay	t_{BBM}	MAX4538, $V_{COM_}$ = 1.5V, V+ = 3.6V (Figure 2)	+25°C	10	40		ns
Charge Injection (Figure 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	+25°C			3	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

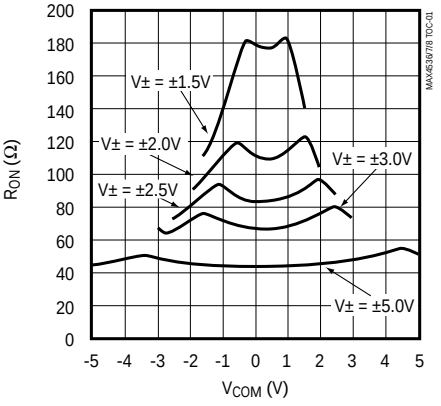
Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: Guaranteed by design.
Note 5: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 6: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog-signal range.
Note 7: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 8: Off-isolation = $20\log_{10}$ [$V_{COM_}$ / ($V_{NC_}$ or $V_{NO_}$)], $V_{COM_}$ = output, $V_{NC_}$ or $V_{NO_}$ = input to off switch.
Note 9: Between any two switches.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad, Low-Voltage, SPST Analog Switches with Enable

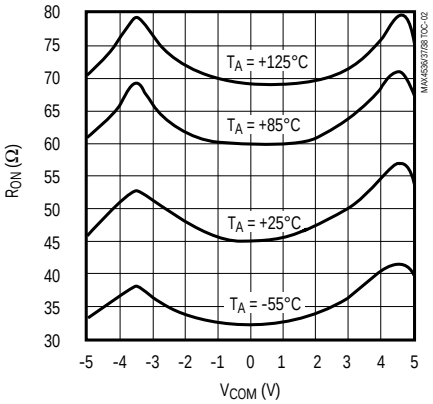
Typical Operating Characteristics

(V+ = +5V, V- = -5V GND = 0V, T_A = +25°C, unless otherwise noted.)

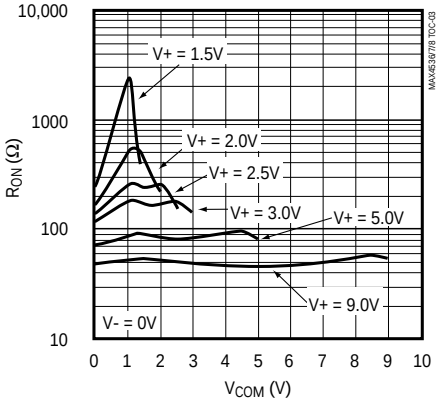
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



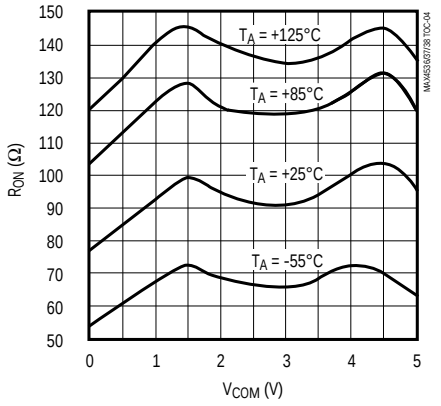
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



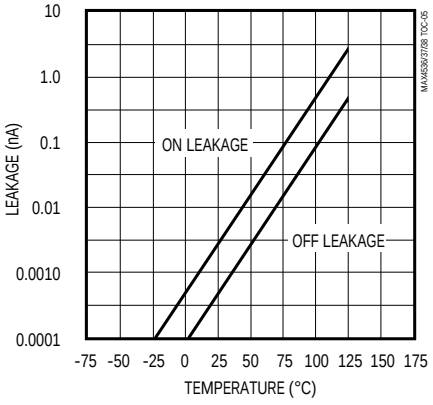
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



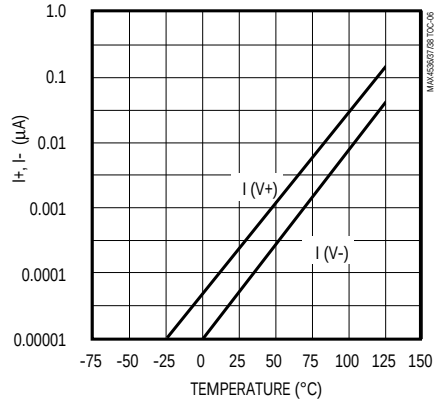
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



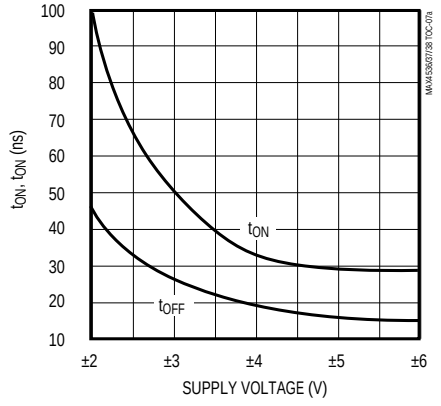
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



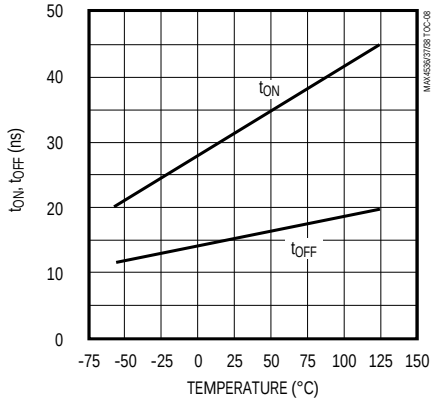
POWER-SUPPLY CURRENT vs. TEMPERATURE



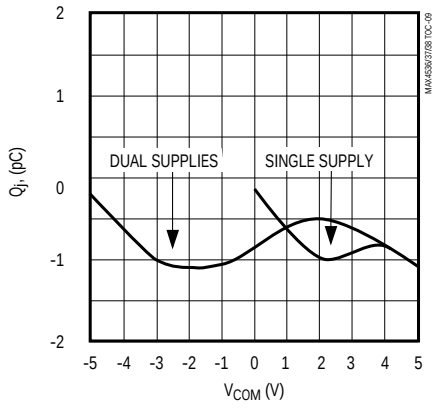
ON/OFF TIME vs. SUPPLY VOLTAGE (DUAL SUPPLIES)



ON/OFF TIME vs. TEMPERATURE



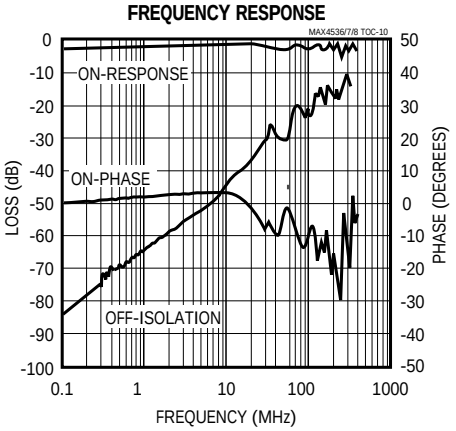
CHARGE INJECTION vs. V_{COM}



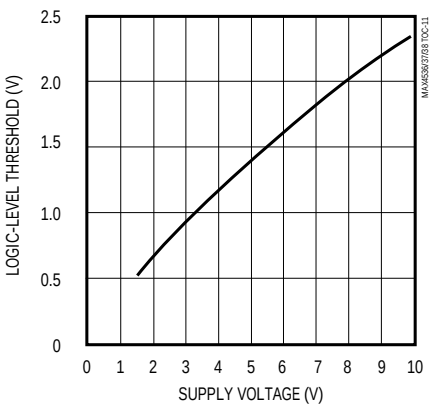
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V GND = 0V, T_A = +25°C, unless otherwise noted.)

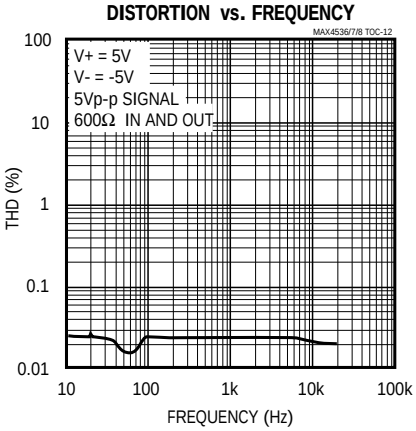
FREQUENCY RESPONSE



LOGIC-LEVEL THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 4, 10, 13	COM1–COM4	Analog Switch Common* Terminals
2, 3, 11, 12	NO1–NO4, or NC1–NC4	Analog Switch Normally Open* or Normally Closed* Terminals (see *Truth Tables*)
5, 6, 14, 15	IN1–IN4	Logic-Control Digital Inputs. Control each switch (see *Truth Tables*), except when $\overline{EN}$ is high.
7	$\overline{EN}$	Disable Logic Input. Connect logic high to $\overline{EN}$ to disable (open) all switches.
8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
9	V-	Negative Analog Supply-Voltage Input. Connect V- to GND for single-supply operation.
16	V+	Positive Analog and Digital Supply-Voltage Input. Internally connected to substrate.

**NO_/NC_ and COM_ pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.*

Quad, Low-Voltage, SPST Analog Switches with Enable

Applications Information

Power-Supply Considerations

Overview

The MAX4536/MAX4537/MAX4538 construction is typical of most CMOS analog switches. These devices have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin, and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-. These reverse-biased ESD diodes leak during normal operation, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog switches' gates. This drive signal is the only connection between the logic supplies and the analog supplies. V+, and V- have ESD-protection diodes to GND. The logic-level inputs have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level thresholds are CMOS/TTL-compatible when V+ is +5V. The threshold increases slightly as V+ is raised. When V+ reaches +12V, the level threshold is about 3.1V, above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4536/MAX4537/MAX4538 operate with bipolar supplies between ±2.0V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4536/MAX4537/MAX4538's V+ to +3V and then connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs in excess of the absolute maximum ratings can damage the part and/or external circuits.**

CAUTION: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or +12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4536/MAX4537/MAX4538. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single Supplies

The MAX4536/MAX4537/MAX4538 operate from single supplies between +2.0V and +12V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -44dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

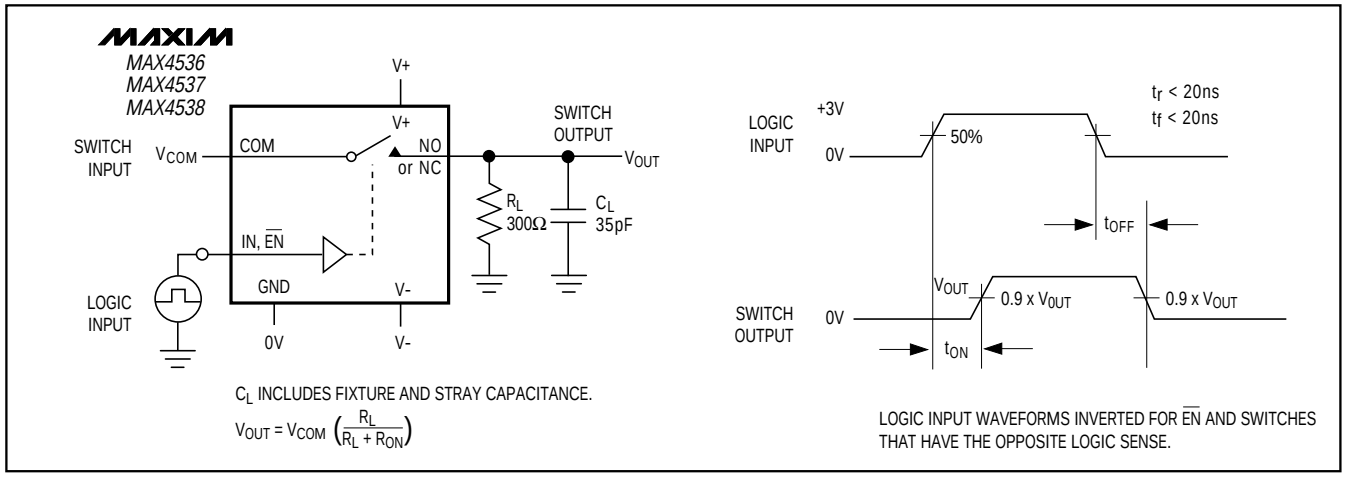


Figure 1. Switching Time

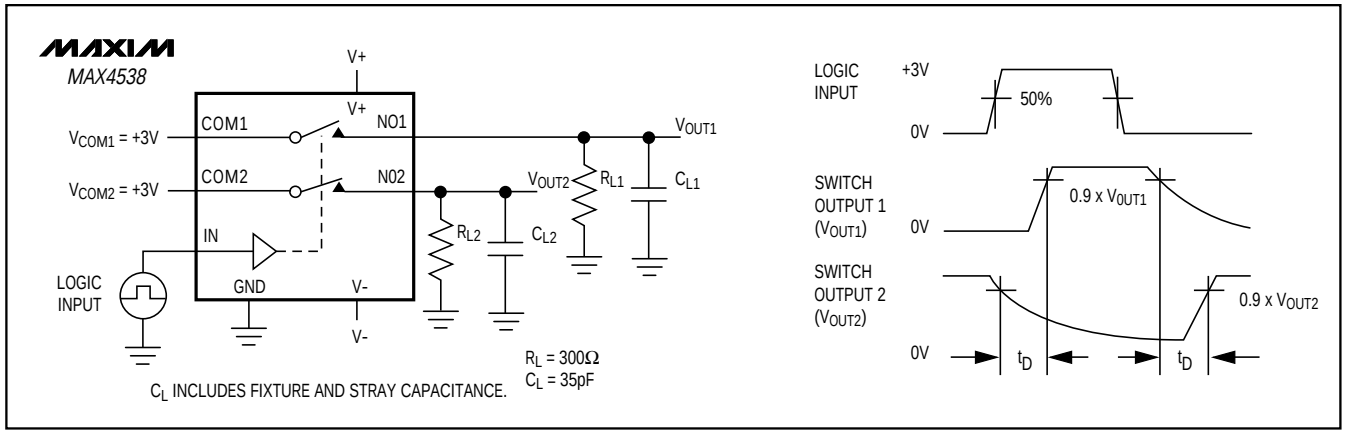


Figure 2. Break-Before-Make Interval (MAX4538 only)

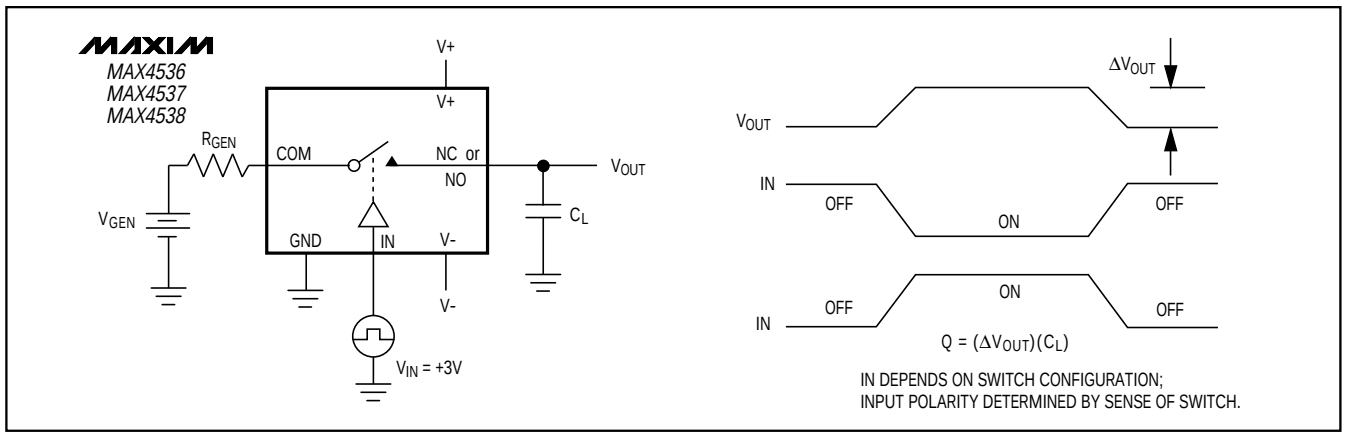


Figure 3. Charge Injection

Quad, Low-Voltage, SPST Analog Switches with Enable

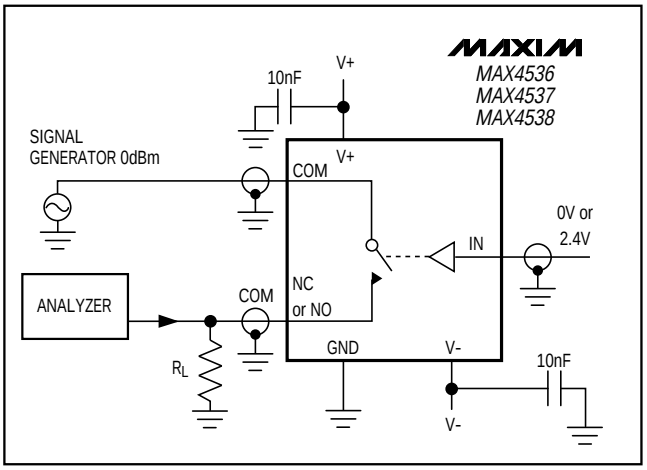


Figure 4. Off Isolation

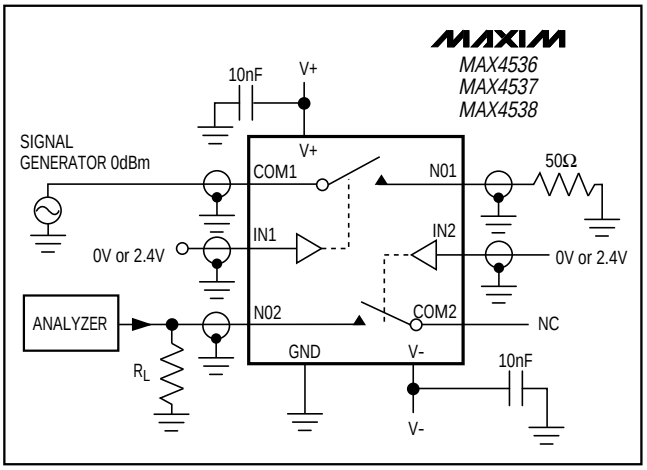


Figure 5. Crosstalk

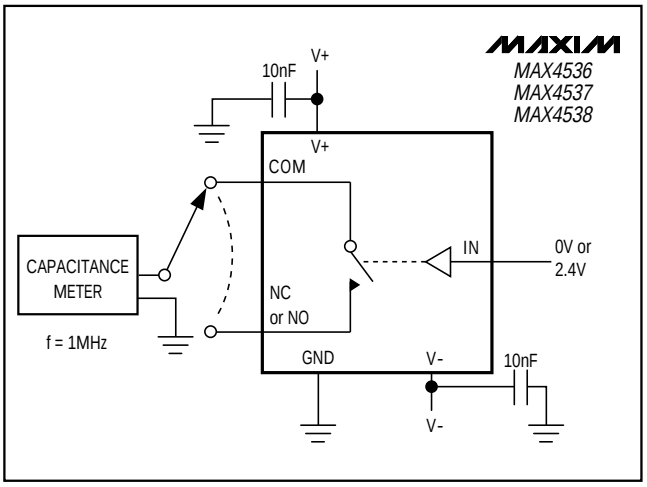


Figure 6. Channel-Off Capacitance

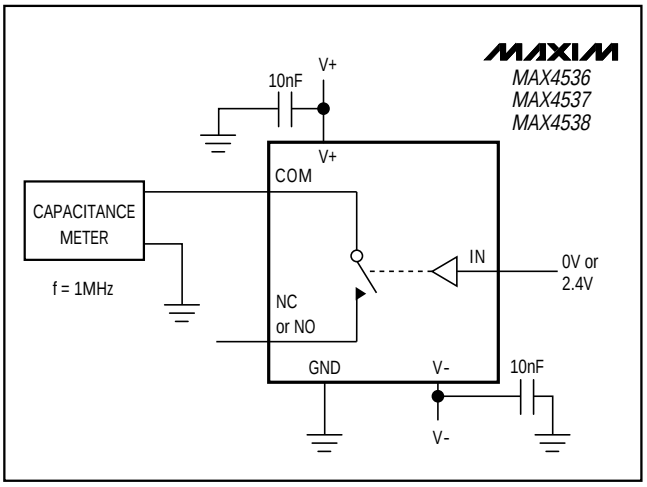


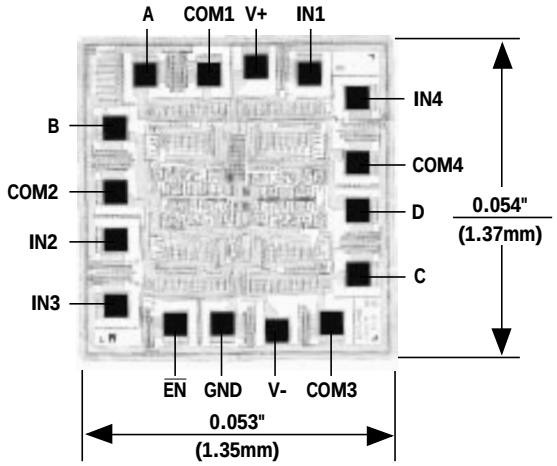
Figure 7. Channel-On Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4537CPE	0°C to +70°C	16 Plastic DIP
MAX4537CSE	0°C to +70°C	16 Narrow SO
MAX4537CEE	0°C to +70°C	16 QSOP
MAX4537C/D	0°C to +70°C	Dice*
MAX4537EPE	-40°C to +85°C	16 Plastic DIP
MAX4537ESE	-40°C to +85°C	16 Narrow SO
MAX4537EEE	-40°C to +85°C	16 QSOP
MAX4538CPE	0°C to +70°C	16 Plastic DIP
MAX4538CSE	0°C to +70°C	16 Narrow SO
MAX4538CEE	0°C to +70°C	16 QSOP
MAX4538C/D	0°C to +70°C	Dice*
MAX4538EPE	-40°C to +85°C	16 Plastic DIP
MAX4538ESE	-40°C to +85°C	16 Narrow SO
MAX4538EEE	-40°C to +85°C	16 QSOP

**Contact factory for availability.*

Chip Topography



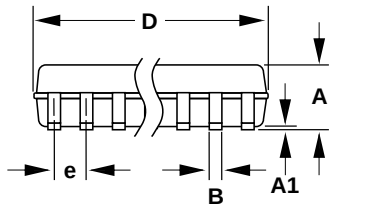
MAX4536		MAX4537		MAX4538	
PIN	**NAME**	**PIN**	**NAME**	**PIN**	**NAME**
A	NO1	A	NC1	A	NO1
B	NO2	B	NC2	B	NC2
C	NO3	C	NC3	C	NC3
D	NO4	D	NC4	D	NO4

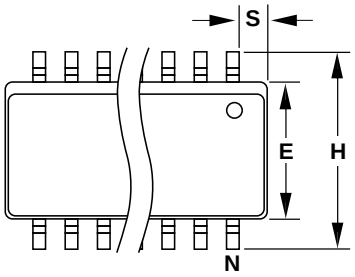
TRANSISTOR COUNT: 121

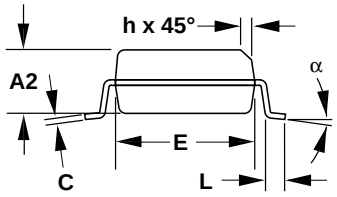
SUBSTRATE IS INTERNALLY CONNECTED TO V+

Quad, Low-Voltage, SPST Analog Switches with Enable

Package Information





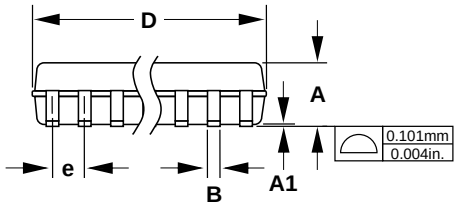


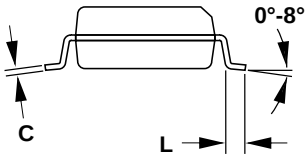
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
α	0°	8°	0°	8°

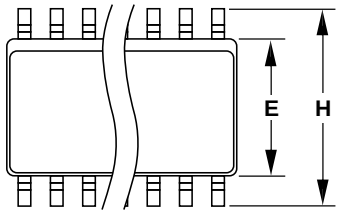
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

QSOP QUARTER SMALL-OUTLINE PACKAGE







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

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