19-3175; Rev 1; 7/04

MAXIM

High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

General Description

The MAX5069 is a high-frequency, current-mode, pulse-width modulation (PWM) controller (with dual MOSFET drivers) that integrates all the building blocks necessary for implementing AC-DC or DC-DC fixed-frequency power supplies. Isolated or nonisolated push-pull and half/full-bridge power supplies are easily constructed using either primary- or secondary-side regulation. Current-mode control with leading-edge blanking simplifies control-loop design and a programmable internal slope-compensation circuit stabilizes the current loop when operating at duty cycles above 50%.

An input undervoltage lockout (UVLO) programs the input-supply startup voltage and ensures proper operation during brownout conditions.

A single external resistor programs the oscillator frequency from 50kHz to 2.5MHz. The MAX5069A/D provide a SYNC input for synchronization to an external clock. The maximum FET-driver duty cycle for the MAX5069 is 50%. Programmable dead time allows additional flexibility in optimizing magnetic design and overcoming parasitic effects. Programmable hiccup current limit provides additional protection under severe faults.

The MAX5069 is specified over the -40°C to +125°C automotive temperature range and is available in a 16-pin thermally enhanced TSSOP-EP package. Refer to the MAX5068 data sheet for single FET-driver applications.

Warning: The MAX5069 is designed to work with high voltages. Exercise caution.

Applications

Universal-Input AC Power Supplies

Isolated Telecom Power Supplies

Networking System Power Supplies

Server Power Supplies

Industrial Power Conversion

Selector Guide appears at end of data sheet.

Features

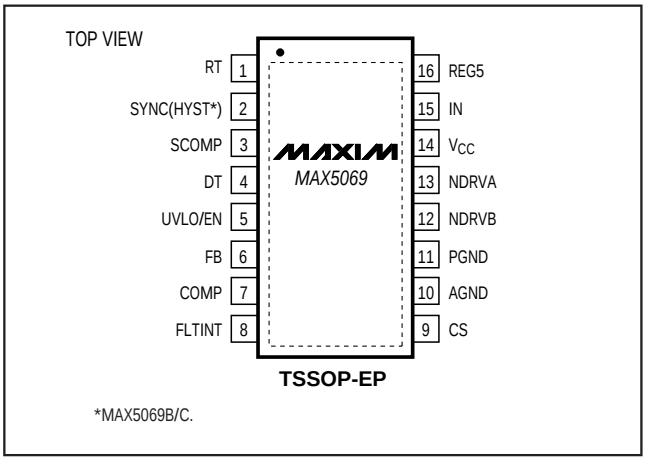
- **Current-Mode Control with 47µA (typ) Startup Current**
- **Oscillator Frequency Programmable to 2.5MHz**
- **Resistor-Programmable ±4.5% Accurate Switching Frequency**
- **Dual Gate-Drive Output for Half/Full-Bridge or Push-Pull Applications**
- **Rectified 85VAC to 265VAC, or 36VDC to 72VDC Input (MAX5069A/B)**
- **Input Directly Driven from 10.8V to 24V (MAX5069C/D)**
- **Programmable Dead Time and Slope Compensation**
- **Programmable Startup Voltage (UVLO)**
- **Programmable UVLO Hysteresis (MAX5069B/C)**
- **Frequency Synchronization Input (MAX5069A/D)**
- **-40°C to +125°C Automotive Temperature Range**
- **16-Pin Thermally Enhanced TSSOP-EP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5069AAUE	-40°C to +125°C	16 TSSOP-EP*
MAX5069BAUE	-40°C to +125°C	16 TSSOP-EP*
MAX5069CAUE	-40°C to +125°C	16 TSSOP-EP*
MAX5069DAUE	-40°C to +125°C	16 TSSOP-EP*

**EP = Exposed pad.*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

IN to PGND .....-0.3V to +30V
IN to AGND.....-0.3V to +30V
V_{CC} to PGND.....-0.3V to +13V
V_{CC} to AGND.....-0.3V to +13V
FB, COMP, CS, HYST, SYNC, REG5 to AGND .....-0.3V to +6V
UVLO/EN, RT, DT, SCOMP, FLTINT to AGND .....-0.3V to +6V
NDRVA, NDRVB to PGND.....-0.3V to (V_{CC} + 0.3V)
AGND to PGND.....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP-EP (derate 21.3mW/°C above +70°C)...1702mW
Operating Temperature Range.....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V for the MAX5069C/D, V_{IN} = +23.6V for the MAX5069A/B at startup, then reduces to +12V, C_{IN} = C_{REG5} = 0.1µF, C_{VCC} = 1µF, R_{RT} = 100kΩ, NDRV_ = floating, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT/STARTUP							
Bootstrap UVLO Wake-Up Level	V_{SUVR}	V_{IN} rising, MAX5069A/B		19.68	21.6	23.60	V
Bootstrap UVLO Shutdown Level	V_{SUVF}	V_{IN} falling, MAX5069A/B		9.05	9.74	10.43	V
UVLO/EN Wake-Up Threshold	V_{ULR2}	UVLO/EN rising		1.205	1.230	1.255	V
UVLO/EN Shutdown Threshold	V_{ULF2}	UVLO/EN falling			1.18		V
HYST FET On-Resistance	$R_{DS(ON)_H}$	MAX5069B/C only, sinking 50mA, $V_{UVLO/EN}$ = 0V			10		Ω
HYST FET Leakage Current	I_{LEAK_H}	$V_{UVLO/EN}$ = 2V, V_{HYST} = 5V			3		nA
IN Supply Current In Undervoltage Lockout	I_{START}	V_{IN} = +19V, $V_{UVLO/EN}$ < V_{ULF2}			47	90	µA
IN Range	V_{IN}			10.8		24.0	V
INTERNAL SUPPLIES (V_{CC} and REG5)							
V_{CC} Regulator Set Point	V_{CCSP}	V_{IN} = +10.8V to +24V, V_{CC} sourcing 1µA to 25mA		7.0		10.5	V
REG5 Output Voltage	V_{REG5}	I_{REG5} = 0 to 1mA		4.85	5.00	5.15	V
REG5 Short-Circuit Current Limit	I_{REG5_SC}				18		mA
IN Supply Current After Startup	I_{IN}	V_{IN} = +24V	f_{SW} = 1.25MHz		7		mA
			f_{SW} = 100kHz		3		
Shutdown Supply Current	I_{VIN_SD}					90	µA
GATE DRIVER (NDRVA, NDRVB)							
Driver Output Impedance	$Z_{OUT(LOW)}$	NDRVA/NDRVB sinking 100mA			2	4	Ω
	$Z_{OUT(HIGH)}$	NDRVA/NDRVB sourcing 25mA			3	6	
Driver Peak Output Current	I_{NDRV}	Sinking			1000		mA
		Sourcing			650		
PWM COMPARATOR							
Comparator Offset Voltage	V_{OS_PWM}	V_{COMP} > V_{CS}		1.30	1.60	2.00	V
Comparator Propagation Delay	t_{PD_PWM}	V_{CS} = 0.1V			40		ns
Minimum On-Time	$t_{ON(MIN)}$	Includes t_{CS_BLANK}			110		ns
CURRENT-LIMIT COMPARATOR							
Current-Limit Trip Threshold	V_{CS}			298	314	330	mV

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS Input Bias Current	I_{B_CL}	V_{CS} = 0V	0		+2	µA
CS Blanking Time	t_{CS_BLANK}			70		ns
Propagation Delay from Comparator Input to NDRV_	t_{PD_CL}	50mV overdrive		40		ns
IN CLAMP VOLTAGE						
IN Clamp Voltage	V_{IN_CLAMP}	IN sinking 2mA (Note 2)	24.0	26.0	29.0	V
ERROR AMPLIFIER (FB, COMP)						
Voltage Gain	A_V	R_{COMP} = 100kΩ to AGND		80		dB
Unity-Gain Bandwidth	BW	R_{COMP} = 100kΩ to AGND, C_{LOAD} = 100pF to AGND		5		MHz
Phase Margin	PM	R_{COMP} = 100kΩ to AGND, C_{LOAD} = 100pF to AGND		65		Degrees
FB Input Offset Voltage	V_{OS_FB}				3	mV
COMP Clamp Voltage	V_{COMP}	High	2.6		3.8	V
		Low	0.4		1.1	
Error-Amplifier Output Current	I_{COMP}	Sinking or sourcing	0.5			mA
Reference Voltage	V_{REF}	+25°C ≤ T_A ≤ +125°C (Note 3)	1.215	1.230	1.245	V
		-40°C ≤ T_A ≤ +125°C (Note 3)	1.205	1.230	1.242	
Input Bias Current	I_{B_EA}			100	300	nA
COMP Short-Circuit Current	I_{COMP_SC}			12		mA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature	T_{SD}			+170		°C
Thermal Hysteresis	T_{HYST}			25		°C
OSCILLATOR SYNC INPUT (MAX5069A/D only)						
SYNC High-Level Voltage	V_{IH_SYNC}		2.4			V
SYNC Low-Level Voltage	V_{IL_SYNC}				0.4	V
SYNC Input Bias Current	I_{B_SYNC}			10		nA
Maximum SYNC Frequency	f_{SYNC}	f_{OSC} = 2.5MHz (Note 4)	3.125			MHz
SYNC High-Level Pulse Width	t_{SYNC_HI}		30			ns
SYNC Low-Level Pulse Width	t_{SYNC_LO}		30			ns
DIGITAL SOFT-START						
Soft-Start Duration	t_{SS}	(Note 5)		2047		Cycles
Reference-Voltage Step	V_{STEP}			9.7		mV
Reference-Voltage Steps During Soft-Start				127		Steps
OSCILLATOR						
Oscillator Frequency Range	f_{OSC}	f_{OSC} = (10^{11} / R_{RT})	50		2500	kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V for the MAX5069C/D, V_{IN} = +23.6V for the MAX5069A/B at startup, then reduces to +12V, C_{IN} = C_{REG5} = 0.1µF, C_{VCC} = 1µF, R_{RT} = 100kΩ, NDRV_ = floating, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NDRV_ Switching Frequency	f_{SW}	$f_{SW} = 10^{11} / (2 \times R_{RT})$		25		1250	kHz
RT Voltage	V_{RT}	40kΩ < R_{RT} < 500kΩ			2.0		V
Oscillator Accuracy		T_A = +25°C	f_{OSC} ≤ 500kHz	-2.5		+2.5	%
			f_{OSC} > 500kHz	-4		+4	
		T_A = -40°C to +125°C	f_{OSC} ≤ 500kHz	-4.5		+4.5	
			f_{OSC} > 500kHz	-6		+6	
Maximum Duty Cycle	D_{MAX}	DT connected to REG5			100		%
DEAD-TIME CONTROL (DT)							
Dead Time	t_{DT}	R_{DT} = 24.9kΩ			60		ns
Dead-Time Disable Voltage	$V_{DT_DISABLE}$			V_{REG5} - 0.5V			V
Dead-Time Regulation Voltage	V_{DT}				1.23		V
INTEGRATING FAULT PROTECTION (FLTINT)							
FLTINT Source Current	I_{FLTINT}	V_{FLTINT} = 0V			60		µA
FLTINT Shutdown Threshold	V_{FLTINT_SD}	V_{FLTINT} rising			2.8		V
FLTINT Restart Threshold	V_{FLTINT_RS}	V_{FLTINT} falling			1.6		V
SLOPE COMPENSATION							
Slope Compensation	V_{SLOPE}	C_{SLOPE} = 100pf, RT = 110kΩ			15		mV/µs
Slope-Compensation Range	V_{SLOPER}			0		90	mV/µs
Slope-Compensation Voltage Range	V_{SCOMP}			0		2.7	V

Note 1: The MAX5069 is 100% tested at T_A = +25°C. All limits over temperature are guaranteed by design.

Note 2: The MAX5069A/B are intended for use in universal-input power supplies. The internal clamp circuit is used to prevent the bootstrap capacitor (C1 in Figure 1) from charging to a voltage beyond the absolute maximum rating of the device when UVLO/EN is low. The maximum current to V_{IN} (hence to clamp) when UVLO is low (device is in shutdown) must be externally limited to 2mA. Clamp currents higher than 2mA may result in clamp voltages higher than 30V, thus exceeding the absolute maximum rating for V_{IN}. For the MAX5069C/D, do not exceed the 24V maximum operating voltage of the device.

Note 3: Reference voltage (V_{REF}) is measured with FB connected to COMP (see the *Functional Diagram*).

Note 4: The SYNC frequency must be at least 25% higher than the programmed oscillator frequency.

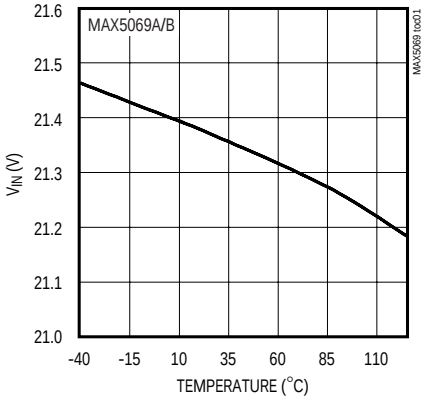
Note 5: The internal oscillator clock cycle.

High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

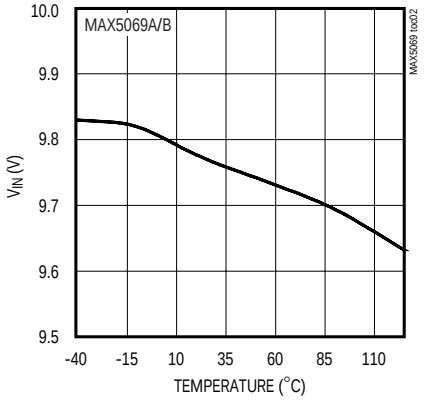
Typical Operating Characteristics

(V_{IN} = +23.6V for MAX5069A/B at startup, then reduces to +12V, V_{IN} = +12V for the MAX5069C/D, C_{IN} = C_{REG5} = 0.1µF, C_{VCC} = 1µF, R_{RT} = 100kΩ, NDRV_ = floating, V_{FB} = 0V, V_{COMP} = floating, V_{CS} = 0V, T_A = +25°C, unless otherwise noted.)

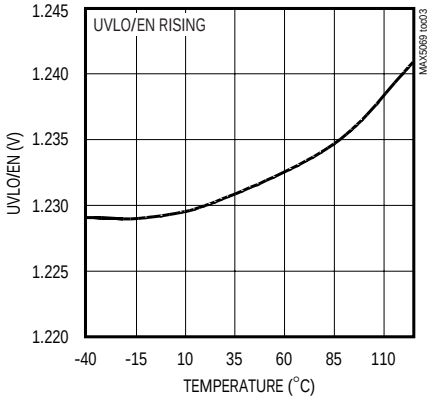
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE



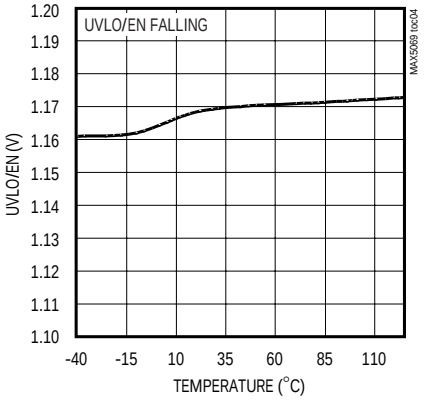
BOOTSTRAP UVLO SHUTDOWN LEVEL vs. TEMPERATURE



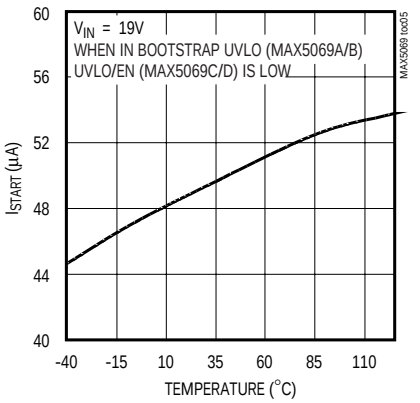
UVLO/EN WAKE-UP THRESHOLD vs. TEMPERATURE



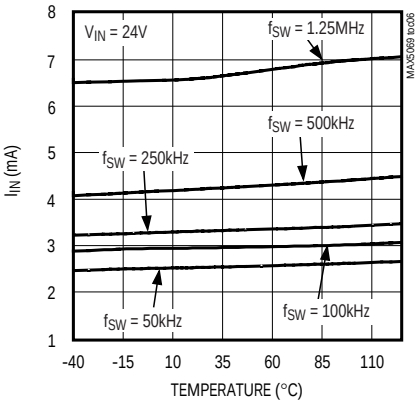
UVLO/EN SHUTDOWN THRESHOLD vs. TEMPERATURE



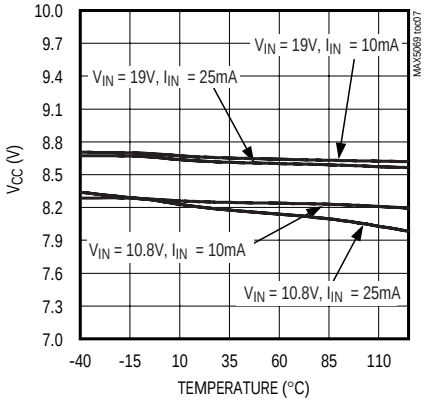
V_{IN} SUPPLY CURRENT IN UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



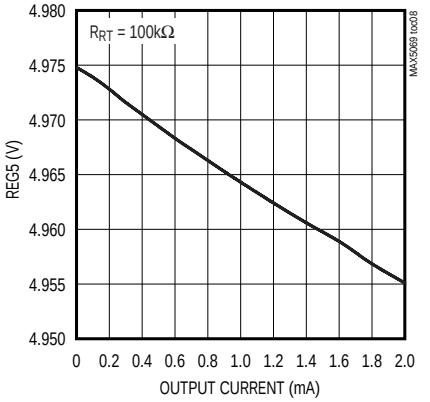
V_{IN} SUPPLY CURRENT AFTER STARTUP vs. TEMPERATURE



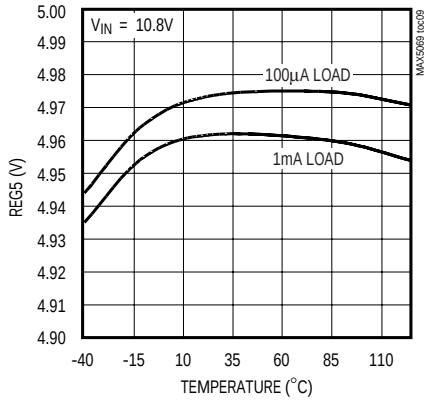
V_{CC} vs. TEMPERATURE



REG5 OUTPUT VOLTAGE vs. OUTPUT CURRENT



REG5 vs. TEMPERATURE

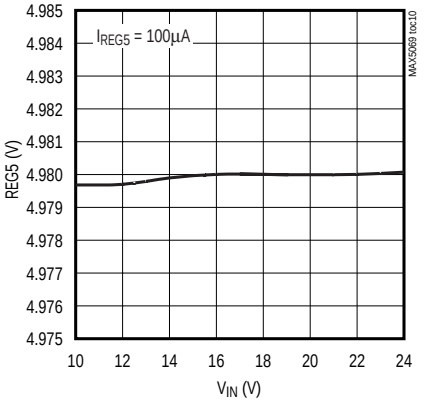


High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

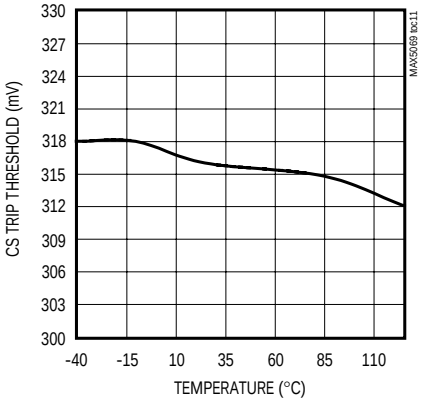
Typical Operating Characteristics (continued)

(V_{IN} = +23.6V for MAX5069A/B at startup, then reduces to +12V, V_{IN} = +12V for the MAX5069C/D, C_{IN} = C_{REG5} = 0.1µF, C_{VCC} = 1µF, R_{RT} = 100kΩ, NDRV_ = floating, V_{FB} = 0V, V_{COMP} = floating, V_{CS} = 0V, T_A = +25°C, unless otherwise noted.)

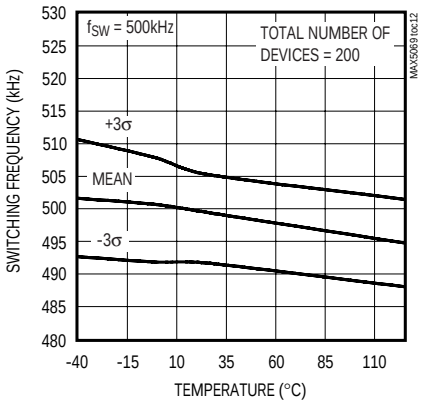
REG5 OUTPUT VOLTAGE vs. V_{IN}



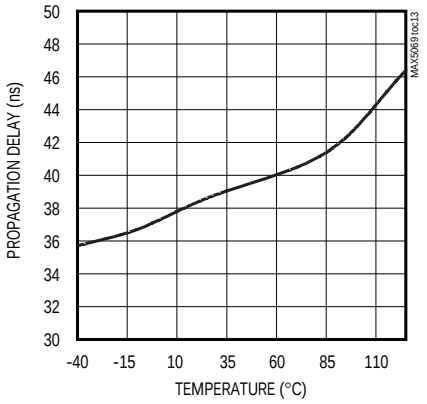
CS TRIP THRESHOLD vs. TEMPERATURE



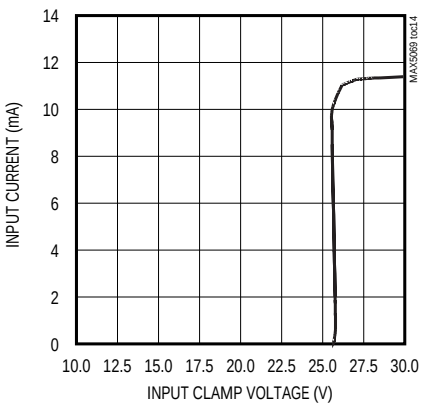
SWITCHING FREQUENCY vs. TEMPERATURE



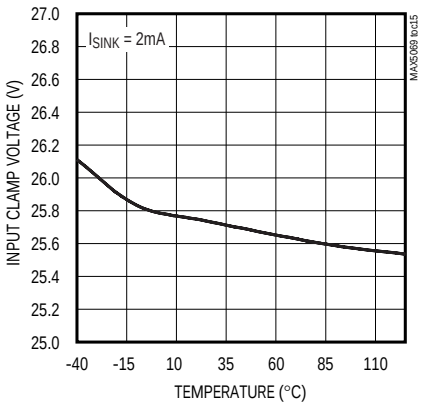
PROPAGATION DELAY FROM CS COMPARATOR INPUT TO NDRV vs. TEMPERATURE



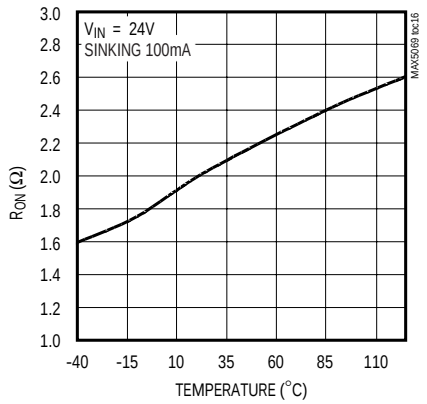
INPUT CURRENT vs. INPUT CLAMP VOLTAGE



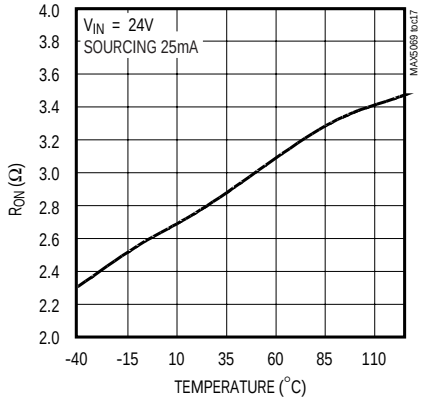
INPUT CLAMP VOLTAGE vs. TEMPERATURE



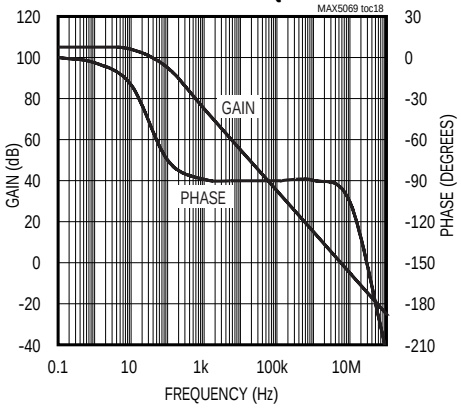
NDRVA/NDRVB OUTPUT IMPEDANCE vs. TEMPERATURE



NDRVA/NDRVB OUTPUT IMPEDANCE vs. TEMPERATURE



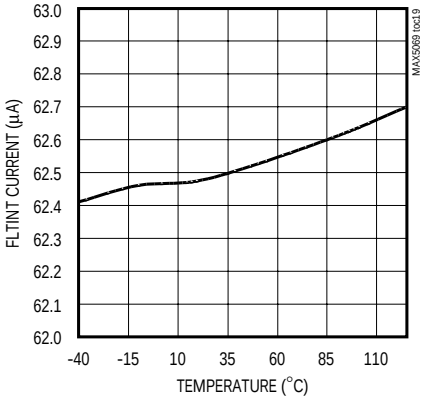
ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



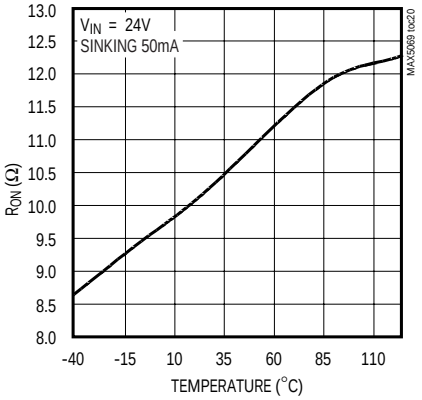
Typical Operating Characteristics (continued)

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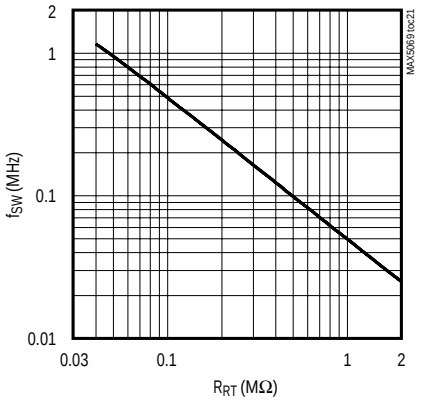
FLTINT CURRENT vs. TEMPERATURE



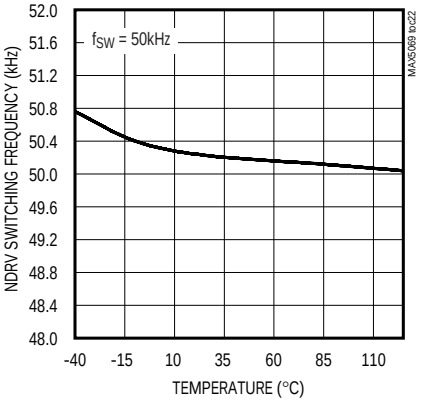
HYST R_{ON} vs. TEMPERATURE



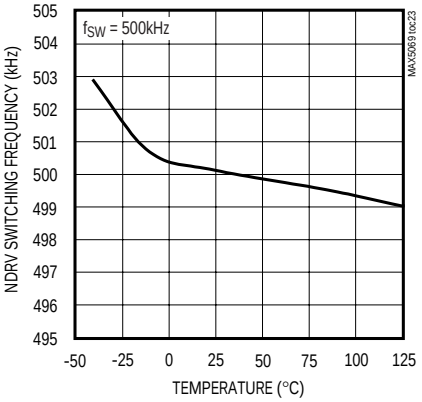
NDRVA SWITCHING FREQUENCY (f_{SW}) vs. R_{RT}



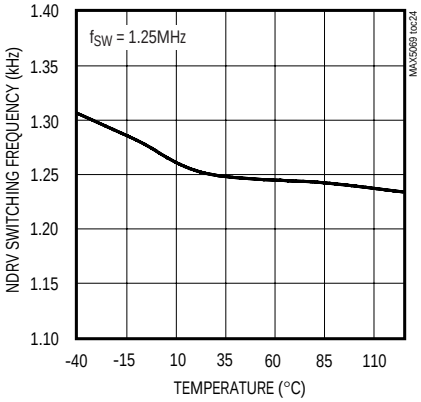
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



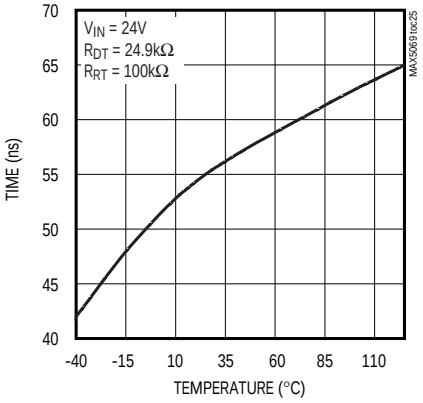
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



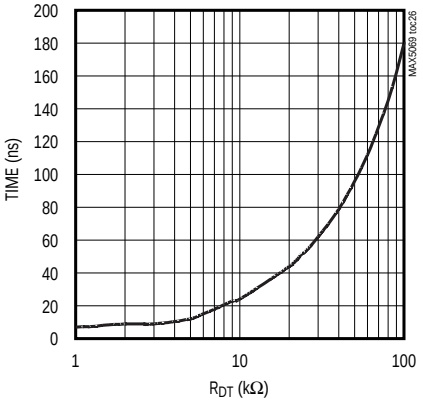
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



DEAD TIME vs. TEMPERATURE



DEAD TIME vs. R_{DT}



High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

Pin Description

PIN		NAME	FUNCTION
MAX5069A MAX5069D	MAX5069B MAX5069C		
1	1	RT	Oscillator-Timing Resistor. Connect a resistor from RT to AGND to set the internal oscillator frequency.
2	—	SYNC	External-Clock Sync Input. Connect SYNC to AGND when not using an external clock.
—	2	HYST	Hysteresis Input
3	3	SCOMP	Slope-Compensation Capacitor Connection
4	4	DT	Dead-Time Resistor Connection. Connect a resistor from DT to AGND to program the output dead time. Connect to REG5 for NDRVA and NDRVB maximum 50% duty cycle.
5	5	UVLO/EN	Externally Programmable Undervoltage Lockout. UVLO/EN programs the input start voltage. Connect UVLO/EN to AGND to disable the output.
6	6	FB	Error-Amplifier Inverting Input
7	7	COMP	Error-Amplifier Output
8	8	FLTINT	Fault-Integration Input. A capacitor connected to FLTINT charges with an internal 60µA current source during persistent current-limit faults. Switching terminates when V_{FLTINT} is 2.8V. An external resistor connected in parallel discharges the capacitor. Switching resumes when V_{FLTINT} drops to 1.6V.
9	9	CS	Current-Sense Resistor Connection
10	10	AGND	Analog Ground. Connect to PGND.
11	11	PGND	Power Ground. Connect to AGND through a ground plane.
12	12	NDRVB	Gate-Driver Output B. Connect NDRVB to the gate of the external N-channel FET.
13	13	NDRVA	Gate-Driver Output A. Connect NDRVA to the gate of the external N-channel FET.
14	14	V_{CC}	9V Linear-Regulator Output. Decouple V_{CC} with a minimum 1µF ceramic capacitor to AGND; also internally connected to the FET drivers.
15	15	IN	Power-Supply Input. IN provides power for all internal circuitry except the gate driver. Decouple IN with 0.1µF to AGND (see the *Typical Operating Circuit*).
16	16	REG5	5V Linear-Regulator Output. Decouple REG5 to AGND with 0.1µF ceramic capacitor.
EP	EP	PAD	Exposed Paddle. Connect to GND.

Detailed Description

The MAX5069 is a current-mode, dual MOSFET driver, PWM controller designed for isolated and nonisolated push-pull or half-/full-bridge power-supply applications. A bootstrap UVLO with a programmable hysteresis, very low startup, and low operating current result in high-efficiency universal-input power supplies. In addition to the internal bootstrap UVLO, the device also offers programmable input startup and turn-off voltages, programmed through the UVLO/EN pin.

The MAX5069 includes a cycle-by-cycle current limit that turns off the gate drive to the external MOSFET during an overcurrent condition. The MAX5069 integrating fault protection reduces average power dissipation during persistent fault conditions (see the *Integrating Fault Protection* section).

The MAX5069 features a very accurate, wide-range, programmable oscillator that simplifies and optimizes the design of the magnetics. The MAX5069A/B are well suited for universal-input (rectified 85VAC to 265VAC) or telecom (-36VDC to -72VDC) power supplies. The MAX5069C/D are well suited for low-input voltage (10.8VDC to 24VDC) power supplies.

The MAX5069 high-frequency, universal input, offline/telecom, current-mode PWM controller integrates all the building blocks necessary for implementing AC-DC and DC-DC fixed-frequency power supplies. Push-pull and half-/full-bridge isolated or nonisolated power supplies are easily constructed using either primary- or secondary-side regulation. Current-mode control with leading-edge blanking simplifies control-loop design and the programmable slope compensation stabilizes the current loop when operating both FET drivers at a combined 100% duty cycle.

An input UVLO programs the input-supply startup voltage and ensures proper operation during brownout conditions. An external voltage-divider programs the supply startup voltage. The MAX5069B/C feature a programmable UVLO hysteresis. The MAX5069A/B feature an additional internal bootstrap UVLO with large hysteresis that requires a minimum startup voltage of 23.6V. The MAX5069A/D start up from a minimum voltage of 10.8V. Internal digital soft-start reduces output-voltage overshoot at startup.

A single external resistor programs the switching frequency of each MOSFET driver from 25kHz to 1.25MHz. The MAX5069A/D provide a SYNC input for synchronization to an external clock. The maximum FET driver duty cycle for each driver is limited to 50%. Programmable dead time allows additional flexibility in optimizing magnetic design and overcoming parasitic effects. Integrating fault protection ignores transient overcurrent conditions for a set length of time. The length of time is programmed by an external capacitor. The internal thermal-shutdown circuit protects the device should the junction temperature exceed +170°C.

Power supplies designed with the MAX5069A/B use a high-value startup resistor, R1, which charges a reservoir capacitor, C1 (Figure 1). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 47µA of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across R1 even at the high end of the universal AC input voltage (265VAC).

The MAX5069 includes a cycle-by-cycle current limit that turns off the gates to both external MOSFETs during an overcurrent condition. When using the MAX5069A/B in the bootstrap mode (if the power-supply output is shorted), the tertiary winding voltage drops below the 9.74V threshold, causing the UVLO to turn off the gate to the external power MOSFETs. This reinitiates a startup sequence with soft-start.

Current-Mode Control

The MAX5069 offers a current-mode control operation feature, such as leading-edge blanking with a dual internal path that only blanks the sensed current signal applied to the input of the PWM controller. The current-limit comparator monitors CS at all times and provides cycle-by-cycle current limit without being blanked. The leading-edge blanking of the CS signal prevents the PWM comparator from prematurely terminating the on cycle. The CS signal contains a leading-edge spike that results from the MOSFET's gate charge current, and the capacitive and diode reverse-recovery current of the power circuit. Since this leading-edge spike is normally lower than the current-limit comparator threshold, current limiting is provided under all conditions.

Use the MAX5069 in push-pull and half-/full-bridge applications where a large duty cycle is desired. The large duty cycle results in much lower operating primary RMS currents through the MOSFET switches, and in most cases it results in a smaller inductor and output filter capacitor. The MAX5069 adjusted slope compensation allows for easy stabilization of the inner current loop.

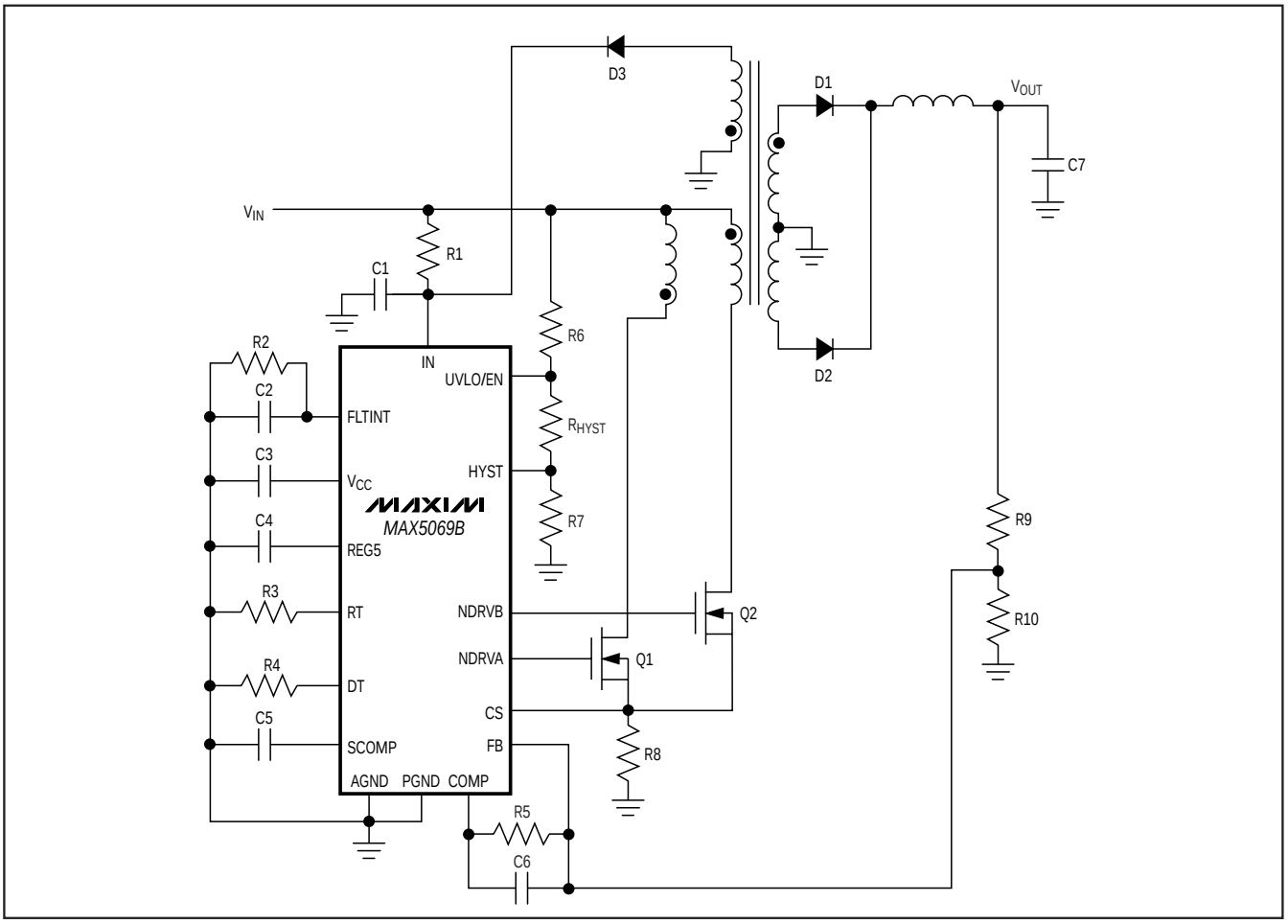


Figure 1. Nonisolated Power Supply with Programmable Input Supply Voltage

Undervoltage Lockout

The MAX5069 features an input voltage UVLO/EN function to enable the PWM controller before any operation can begin. The MAX5069A/D shut down if the voltage at UVLO/EN falls below its 1.18V threshold. The MAX5069B/C also incorporate a UVLO hysteresis input to set the desired turn-off voltage.

MAX5069A/D UVLO Adjustment

The MAX5069A/D have an input voltage UVLO/EN with a 1.231V threshold. Before any operation can commence, the UVLO/EN voltage must exceed the 1.231V threshold. The UVLO circuit keeps the PWM comparator, ILIM comparator, oscillator, and output drivers shutdown to reduce current consumption (see the *Functional Diagram)*.

Calculate R6 in Figure 2 by using the following formula:

$$R6 = \left(\frac{V_{ON}}{V_{ULR2}} - 1 \right) \times R7$$

where V_{ULR2} is the UVLO/EN's 1.231V rising threshold and V_{ON} is the desired startup voltage. Choose an R7 value in the 20kΩ range.

After a successful startup, the MAX5069A/D shut down if the voltage at UVLO/EN drops below its 1.18V falling threshold.

MAX5069B/C UVLO with Programmable Hysteresis

In addition to programmable undervoltage lockout during startup, the MAX5069B/C incorporate a UVLO/EN

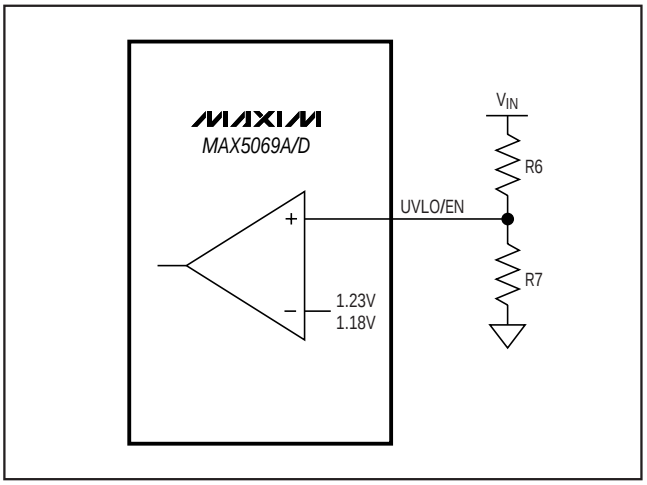


Figure 2. Setting the MAX5069A/D Undervoltage Lockout Threshold

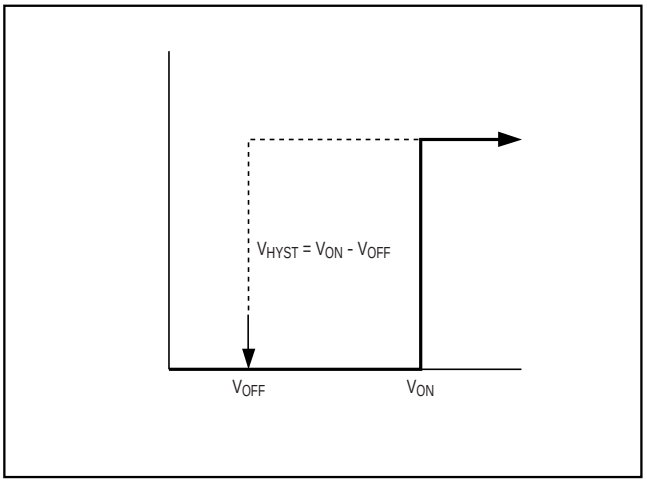


Figure 3. MAX5069 Hysteresis

hysteresis that allows the user to set a voltage (V_{OFF}) to disable the controller (see Figure 3).

At the beginning of the startup sequence, UVLO/EN is below the 1.23V threshold, and Q1 turns on connecting R_{HYST} to GND (Figure 4). Once the UVLO 1.23V threshold is crossed, Q1 turns off, resulting in the series combination of R6, R_{HYST}, and R7, placing the MAX5069 in normal operating condition.

Calculate the turn-on voltage (V_{ON}) by using the following formula:

$$R6 = \left(\frac{V_{ON}}{V_{ULR2}} - 1\right) \times R_{HYST}$$

where V_{ULR2} is the UVLO/EN's 1.23V rising threshold.

Choose an R_{HYST} value in the 20kΩ range.

The MAX5069 turns off when the MAX5069 UVLO/EN falls below the 1.18V falling threshold. The turn-off voltage (V_{OFF}) is then defined as:

$$R7 = R6 / \left(\frac{V_{OFF}}{V_{ULF2}} - 1\right) - R_{HYST}$$

where V_{ULF2} is the 1.18V UVLO/EN falling threshold.

Bootstrap Undervoltage Lockout (MAX5069A/B)

In addition to the externally programmable UVLO function offered by the MAX5069, the MAX5069A/B feature an additional internal bootstrap UVLO for use in high-voltage power supplies (see the *Functional Diagram*). This allows the device to bootstrap itself during initial power-up. The MAX5069A/B start when V_{IN} exceeds the bootstrap UVLO threshold of 23.6V.

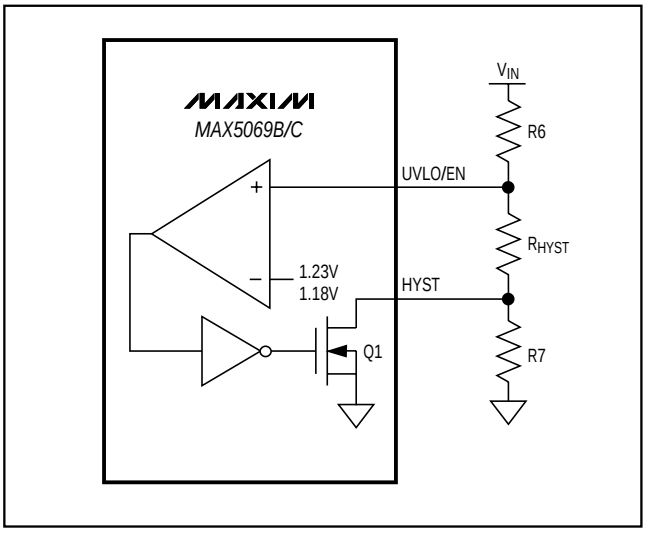


Figure 4. Setting the MAX5069B/C Turn-On/Turn-Off Voltages

During startup, the UVLO circuit keeps the PWM comparator, ILIM comparator, oscillator, and output drivers shut down to reduce current consumption. Once V_{IN} reaches 23.6V, the UVLO circuit turns on both the PWM and ILIM comparators, as well as the oscillator, and allows the output driver to switch. If V_{IN} drops below 9.7V, the UVLO circuit shuts down the PWM comparator, ILIM comparator, oscillator, and output drivers, returning the MAX5069A/B to the startup mode.

High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

MAX5069A/B Startup Operation

Normally, V_{IN} is derived from the tertiary winding of the transformer. However, at startup there is no energy delivered through the transformer; hence, a special bootstrap sequence is required. Figure 5 shows the voltages on V_{IN} and V_{CC} during startup. Initially, both V_{IN} and V_{CC} are 0V. After the input voltage is applied, C1 charges through the startup resistor, R1, to an intermediate voltage (see Figure 1). At this point, the internal regulator begins charging C3 (see Figure 5). Only 47µA of the current supplied by R1 is used by the MAX5069A/B. The remaining input current charges C1 and C3. The charging of C3 stops when the V_{CC} voltage reaches approximately 9.5V. The voltage across C1 continues rising until it reaches the wake-up level of 23.6V. Once V_{IN} exceeds the bootstrap UVLO threshold, NDRVA/NDRVB begin switching the MOSFETs and energy is transferred to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 9.74V (the bootstrap UVLO lower threshold), startup ends and sustained operation commences.

If V_{IN} drops below 9.74V before startup is complete, the device goes back to low-current UVLO. If this occurs, increase the value of C1 to store enough energy to allow for the voltage at the tertiary winding to build up.

Startup Time Considerations for Power Supplies Using the MAX5069A/B

The V_{IN} bypass capacitor, C1, supplies current immediately after wakeup (see Figure 1). The size of C1 and the connection configuration of the tertiary winding determine the number of cycles available for startup. Large values of C1 increase the startup time and also supply extra gate charge for more cycles during initial startup. If the value of C1 is too small, V_{IN} drops below 9.74V because NDRVA/NDRVB do not have enough time to switch and build up sufficient voltage across the tertiary output that powers the device. The device goes back into UVLO and does not start. Use low-leakage capacitors for C1 and C3.

Generally, offline power supplies keep typical startup times to less than 500ms, even in low-line conditions (85VAC input for universal offline applications or 36VDC for telecom applications). Size the startup resistor, R1, to supply both the maximum startup bias of the device (90µA) and the charging current for C1 and C3. The bypass capacitor, C3, must charge to 9.5V, and C1 must charge to 24V, within the desired time period of 500ms. Because of the internal soft-start time of the MAX5069, C1 must store enough charge to deliver current to the device for at least 2047 oscillator clock cycles. To calculate the approximate amount of capacitance required, use the following formula:

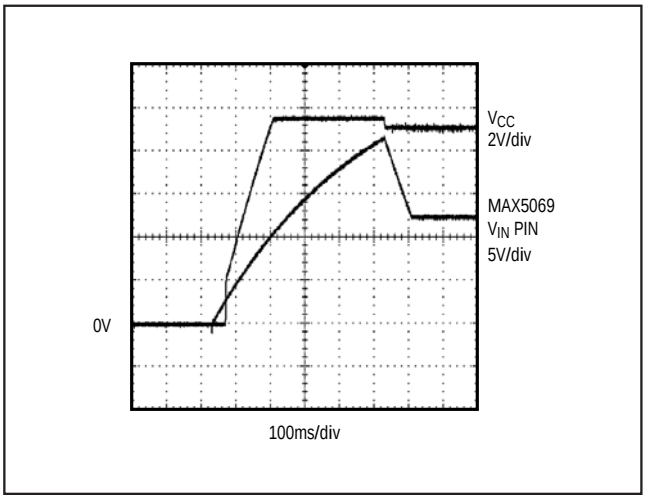


Figure 5. V_{IN} and V_{CC} During Startup When Using the MAX5069 in Bootstrapped Mode (See Figure 1)

$$I_g = Q_{gtot} \times f_{SW}$$

$$C1 = \frac{(I_{IN} + I_g) \times t_{SS}}{V_{HYST}}$$

where I_{IN} is the MAX5069's internal supply current after startup (3.3mA, typ), Q_{gtot} is the total gate charge for Q1 and Q2, f_{SW} is the MAX5069's programmed output switching frequency, V_{HYST} is the bootstrap UVLO hysteresis (12V), and t_{SS} is the internal soft-start time (2047 clock cycles x 1 / f_{OSC}).

Example: I_g = (16nC) (250kHz) ≅ 4mA

f_{OSC} = 500kHz

t_{SS} = 2047 x (1 / f_{OSC}) = 4.1ms

$$C1 = \frac{(3.3mA + 4mA)\ (4.1ms)}{12V} = 2.5\mu F$$

Use a 4.7µF ceramic capacitor for C1.

Assuming C1 > C3, calculate the value of R1 as follows:

$$I_{C1} \cong \frac{V_{SUVR} \times C1}{500ms}$$

$$R1 \cong \frac{V_{IN(MIN)} - 0.5 \times V_{SUVR}}{I_{C1} + I_{START}}$$

where V_{SUVR} is the bootstrap UVLO wakeup level (23.6V max), $V_{IN(MIN)}$ is the minimum input supply voltage for the application (36V for telecom), and I_{START} is the V_{IN} supply current at startup (90µA, max).

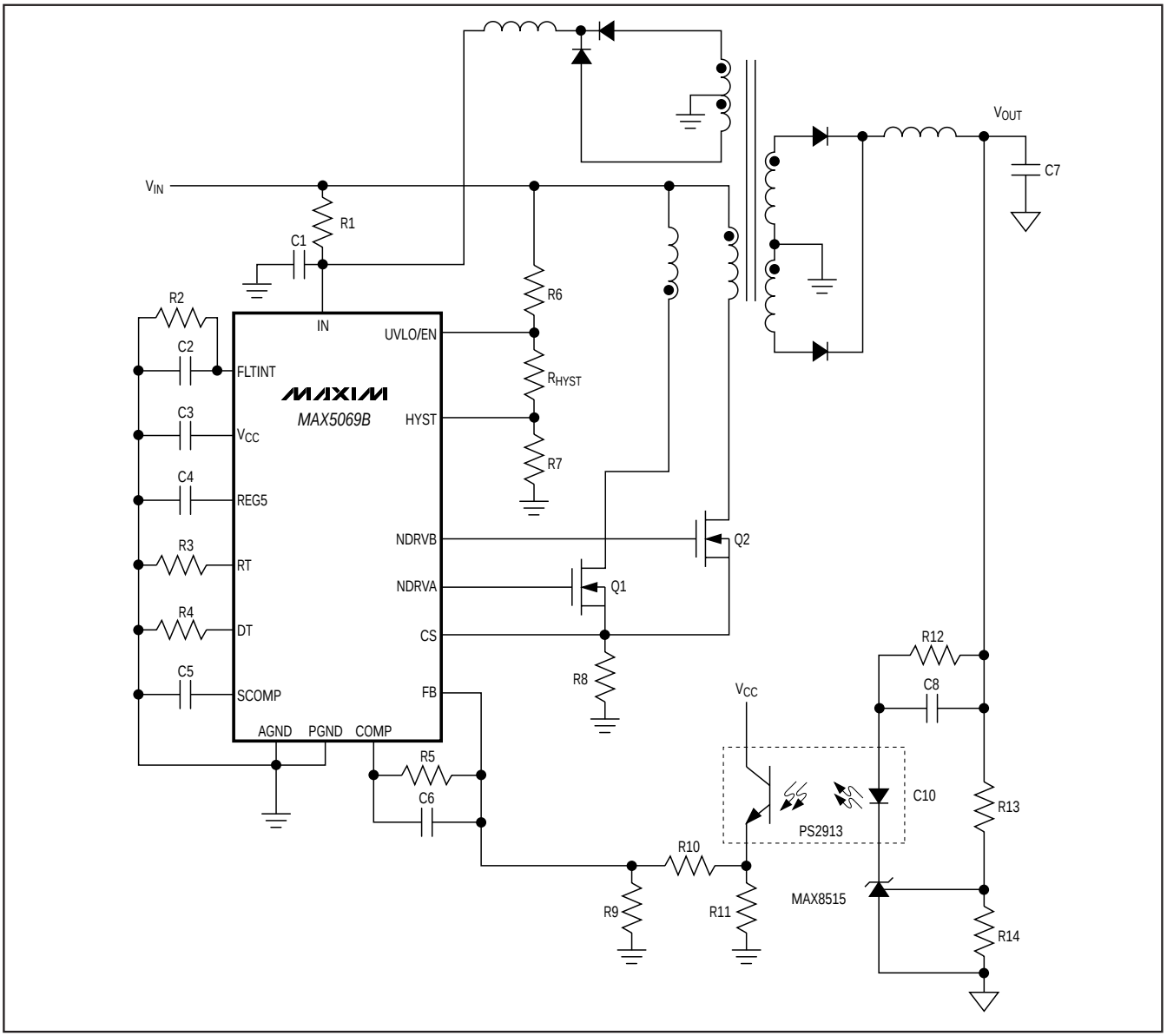


Figure 6. Secondary-Side, Regulated, Isolated Power Supply

For example:

$$I_{C1} = \frac{24V \times 4.7\mu F}{500ms} = 225\mu A$$

$$R1 \cong \frac{36V - 12V}{225\mu A + 90\mu A} = 76k\Omega$$

To minimize power loss on this resistor, choose a higher value for R1 than the one calculated above (if a longer startup time can be tolerated).

The above startup method applies to a circuit similar to the one shown in Figure 1. In this circuit, the tertiary winding has the same phase as the secondary windings. Thus, the voltage on the tertiary winding at any given time is proportional to the output voltage. The minimum discharge time of C1 from 22V to 10V must be greater than the soft-start time (t_{SS}).

High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

Oscillator/Switching Frequency

Use an external resistor at RT to program the MAX5069 internal oscillator frequency from 50kHz to 2.5MHz. The MAX5069 NDRVA/NDRVB switching frequency is one half of the programmed oscillator frequency with a maximum 50% duty cycle.

Use the following formula to calculate the internal oscillator frequency:

$$f_{osc} = \frac{10^{11}}{R_{RT}}$$

where f_{OSC} is the oscillator frequency and R_{RT} is a resistor connected from RT to AGND.

Choose the appropriate resistor at RT to calculate the desired switching frequency (f_{SW}):

$$R_{RT} = \frac{10^{11}}{2f_{SW}}$$

For the maximum 50% duty cycle at NDRVA/NDRVB, connect DT to REG5.

Dual N-Channel MOSFET Switch Driver

The MAX5069 drives two external N-channel MOSFETs in push-pull isolated power supplies. Each MOSFET driver operates with a maximum 50% duty cycle. The NDRV_ outputs are supplied by the internal regulator (V_{CC}), which is internally set to approximately 9.5V. For the universal input voltage range, the MOSFETs used must be able to withstand at least twice the DC level of the high-line input voltage. Both NDRVA and NDRVB can source and sink in excess of 650mA and 1000mA peak current, respectively.

Dead-Time Control

In typical push-pull designs, it is desirable to add some extra delay between the turning off of one MOSFET and the turning on of the next MOSFET (Figure 7). The extra time ensures that the first MOSFET is fully off when the other MOSFET starts to turn on. This prevents both MOSFETs from being on simultaneously, thus avoiding shorting out the transformer's primary. The MAX5069 allows the dead-time delay required to turn on the NDRVB FET after the NDRVA FET turns off. The dead time can be programmed to a minimum of 30ns to 1 / (0.5 x f_{SW}). Connect a resistor between DT and AGND to set the desired dead time. Calculate the dead time using the following formula:

$$\text{Dead time} = \frac{60}{29.4} \times R_{DT}(\text{ns})$$

where R_{DT} is in kΩ and the dead time is in ns.

External Synchronization (MAX5069A/D)

The MAX5069A/D can be synchronized using an external clock at the SYNC input. For proper frequency synchronization, the SYNC's input frequency must be at least 25% higher than the MAX5069A/D programmed internal oscillator frequency. Connect SYNC to AGND when not using an external clock.

Integrating Fault Protection

The integrating fault-protection feature allows transient overcurrent conditions to be ignored for a programmable amount of time, giving the power supply time to behave like a current source to the load. For example, this can occur under load-current transients when the control loop requests maximum current to keep the output voltage from going out of regulation. Program the fault-integration time by connecting an external suitably sized capacitor to the FLTINT. Under sustained overcurrent faults, the voltage across this capacitor ramps up towards the FLTINT shutdown threshold (typically 2.8V). Once the threshold is reached, the power supply shuts down. A high-value bleed resistor connected in parallel with the FLTINT capacitor allows it to discharge towards the restart threshold (typically 1.6V). Once this threshold is reached, the supply restarts with a new soft-start cycle.

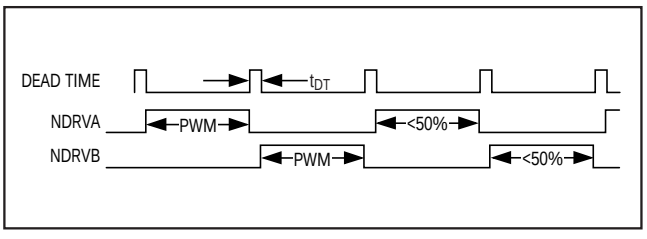


Figure 7. MAX5069 Dead-Time Timing Diagram

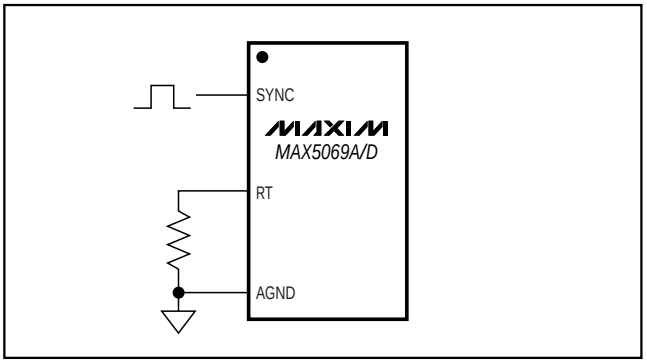


Figure 8. External Synchronization of the MAX5069A/D

Note that cycle-by-cycle current limiting is provided at all times by CS with a threshold of 314mV (typ). The fault-integration circuit forces a 60µA current onto FLTINT each time that the current-limit comparator is tripped (see the *Functional Diagram*). Use the following formula to calculate the value of the capacitor necessary for the desired shutdown time of the circuit:

$$C_{FLTINT} \cong \frac{I_{FLTINT} \times t_{SH}}{2.8V}$$

where I_{FLTINT} = 60µA, t_{SH} is the desired fault-integration time during which current-limit events from the current-limit comparator are ignored. For example, a 0.1µF capacitor gives a fault-integration time of 4.7ms.

This is an approximate formula. Some testing may be required to fine-tune the actual value of the capacitor. To calculate the recovery time, use the following formula:

$$R_{FLTINT} \cong \frac{t_{RT}}{0.595 \times C_{FLTINT}}$$

where t_{RT} is the desired recovery time.

Choose $t_{RT} = 10 \times t_{SH}$. Typical values for t_{SH} range from a few hundred microseconds to a few milliseconds.

Soft-Start

The MAX5069 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after UVLO is deasserted. The voltage applied to the noninverting node of the amplifier ramps from 0 to 1.23V in 2047 oscillator clock cycles (soft-start timeout period). Unlike other devices, the MAX5069 reference voltage to the internal amplifier is soft-started. This method results in superior control of the output voltage under heavy- and light-load conditions.

Internal Regulators

Two internal linear regulators power the MAX5069 internal and external control circuits. V_{CC} powers the external N-channel MOSFETs and is internally set to approximately 9.5V. The REG5 5V regulator has a 1mA sourcing capability and may be used to provide power to external circuitry. Bypass V_{CC} and REG5 with 1µF and 0.1µF high quality capacitors, respectively. Use lower value ceramics in parallel to bypass other unwanted noise signals. Bootstrapped operation requires startup through a bleed resistor. Do not excessively load the regulators while the MAX5069 is in the power-up mode. Overloading the outputs may cause the MAX5069 to fail upon startup.

Error Amplifier

The MAX5069 includes an internal error amplifier that can regulate the output voltage in the case of a nonisolated power supply (Figure 1). Calculate the output voltage using the following equation:

$$V_{OUT} = \left(1 + \frac{R9}{R10}\right) \times V_{REF}$$

where V_{REF} = 1.23V. The amplifier's noninverting input internally connects to a digital soft-start reference voltage. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

Slope Compensation

The MAX5069 uses an internal-ramp generator for slope compensation. The internal-ramp signal resets at the beginning of each cycle and slews at the rate programmed by the external capacitor connected at SCOMP and the resistor at RT. Adjust the MAX5069 slew rate up to 90mV/µs using the following equation:

$$SR = \frac{165 \times 10^{-6}}{R_{RT} \times C_{SCOMP}} \ (mV/\mu s)$$

where R_{RT} is the external resistor at RT that sets the oscillator frequency and C_{SCOMP} is the capacitor at SCOMP.

PWM Comparator

The PWM comparator uses the instantaneous current, the error amplifier, and the slope compensation to determine when to switch NDRVA and NDRVB off. In normal operation, the N-channel MOSFETs turns off when:

$$I_{PRIMARY} \times R_{CS} > V_{EA} - V_{OFFSET} - V_{SCOMP}$$

where $I_{PRIMARY}$ is the current through the N-channel MOSFETs, V_{EA} is the output voltage of the internal amplifier, V_{OFFSET} is the 1.6V internal DC offset, and V_{SCOMP} is the ramp function starting at zero and slewing at the programmed slew rate (SR). When using the MAX5069 in a forward-converter configuration, the following conditions must be met to avoid current-loop subharmonic oscillations:

$$\frac{N_S}{N_P} \times \frac{K \times R_{CS} \times V_{OUT}}{L} = SR$$

where K = 0.75 and N_S and N_P are the number of turns on the secondary and primary side of the transformer, respectively. L is the secondary filter inductor. When optimally compensated, the current loop responds to input-voltage transients within one cycle.

High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

Current Limit

The current-sense resistor (R_{CS}), connected between the source of the MOSFET and ground, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 314mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary that flows through the MOSFET at full load.

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET drivers (NDRVA/NDRVB) quickly terminate the current on-cycle. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the corner frequency to a few MHz above the switching frequency.

Applications Information

Layout Recommendations

Keep all PC board traces carrying switching currents as short as possible, and minimize current loops.

For universal AC input design, follow all applicable safety regulations. Offline power supplies may require UL, VDE, and other similar agency approvals. Contact these agencies for the latest layout and component rules.

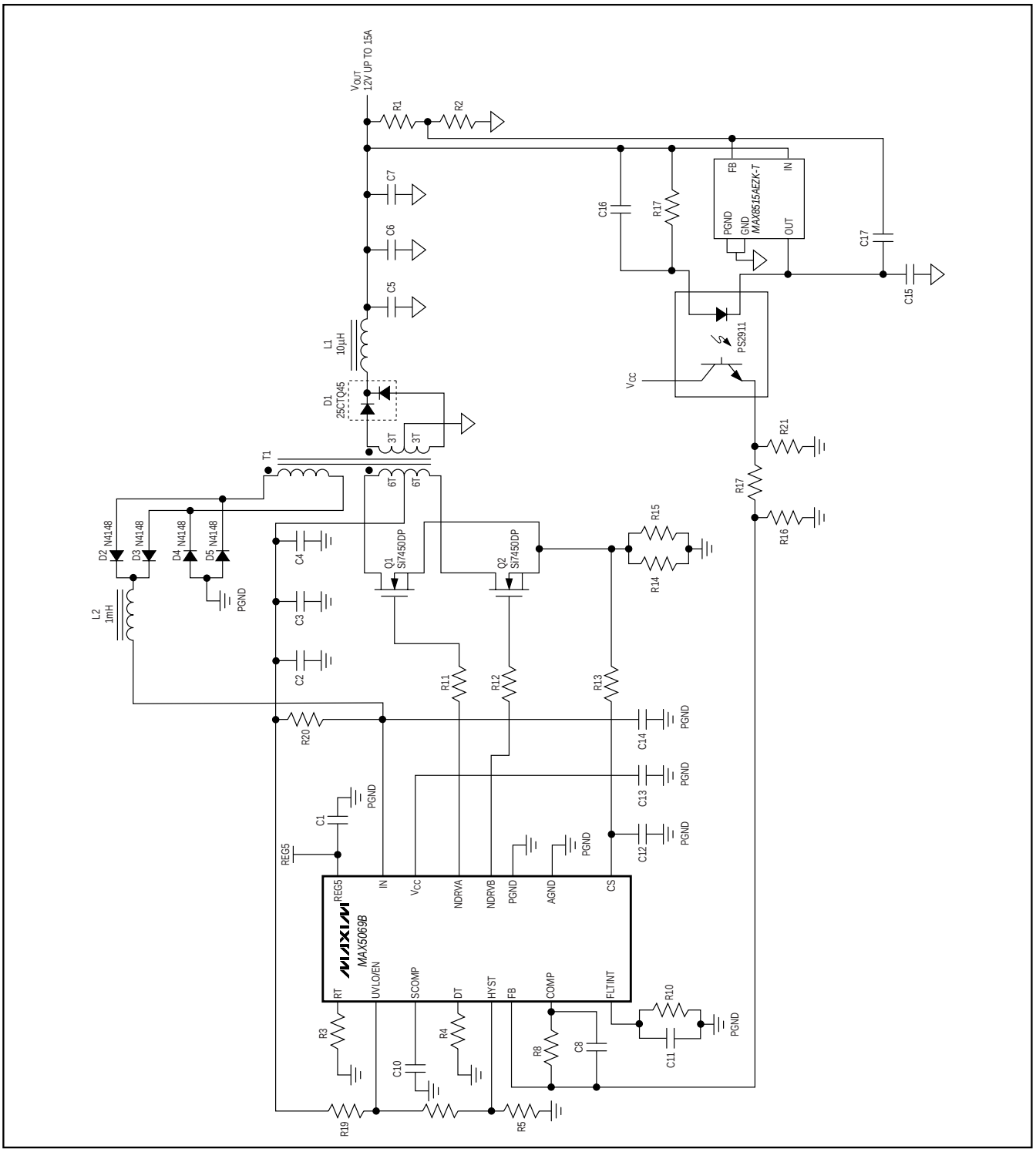
Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET presents a dV/dt source, thus minimize the surface area of the heatsink as much as possible.

To achieve best performance and to avoid ground loops, use a solid ground-plane connection.

Selector Guide

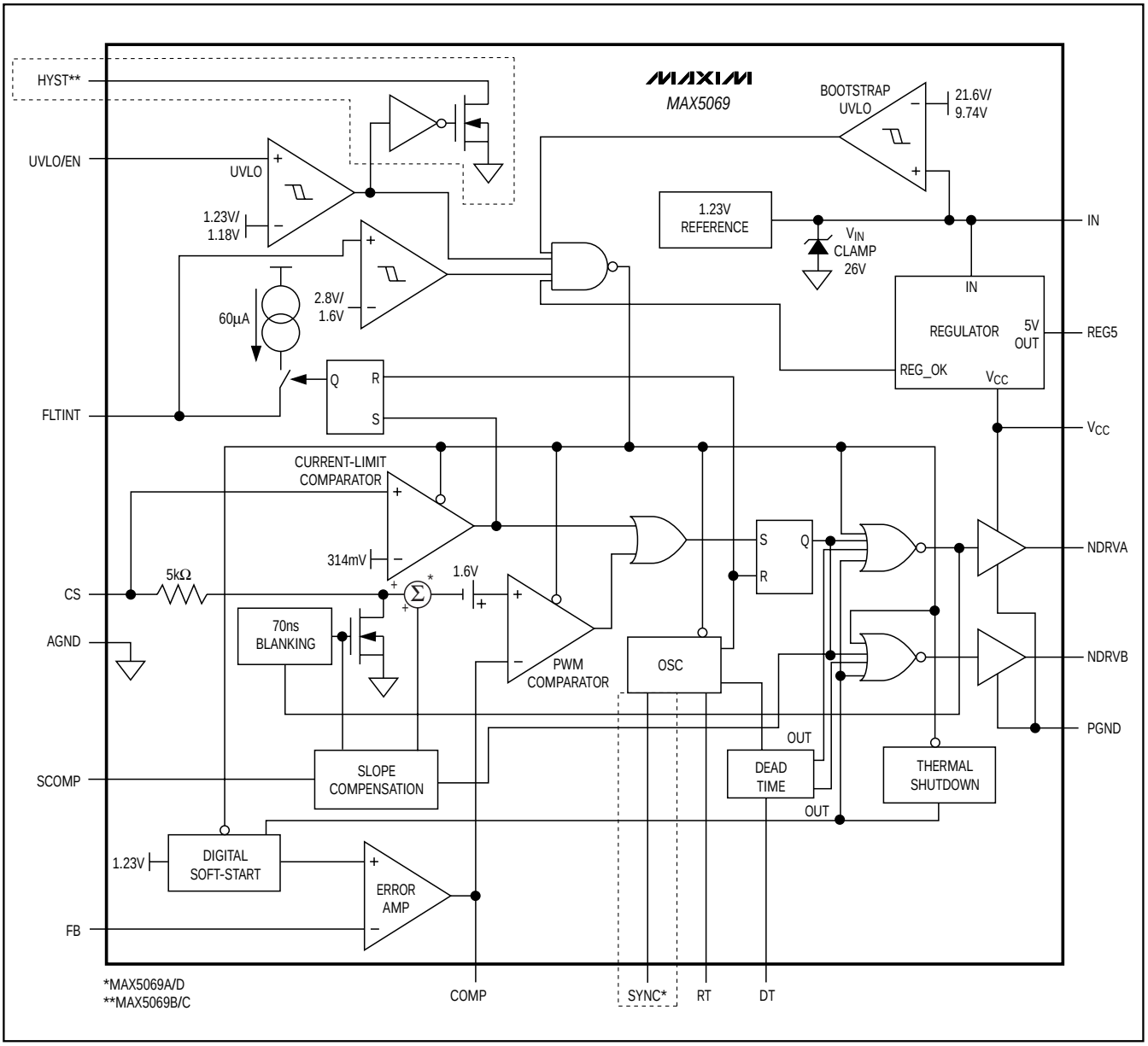
PART	BOOTSTRAP UVLO	STARTUP VOLTAGE (V)	PROGRAMMABLE UVLO HYSTERESIS	OSCILLATOR SYNC
MAX5069A	Yes	23.6	No	Yes
MAX5069B	Yes	23.6	Yes	No
MAX5069C	No	10.8	Yes	No
MAX5069D	No	10.8	No	Yes

Typical Operating Circuit



High-Frequency, Current-Mode PWM Controller with Accurate Oscillator and Dual FET Drivers

Functional Diagram



Chip Information

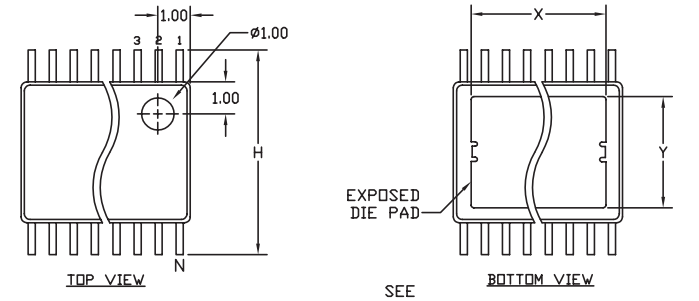
TRANSISTOR COUNT: 4266

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	D	1/1

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