19-1785; Rev 2; 3/11

MAXIM

Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

General Description

The MAX5360/MAX5361/MAX5362 are low-cost, 6-bit digital-to-analog converters (DACs) in miniature 5-pin SOT23 packages with a simple 2-wire serial interface that allows communication with multiple devices. The MAX5360 has an internal +2V reference and operates from a +2.7V to +3.6V supply. The MAX5361 has an internal +4V reference and operates from a +4.5V to +5.5V supply. The MAX5362 operates over the full +2.7V to +5.5V supply range and has an internal reference equal to $0.9 \times V_{DD}$.

The fast-mode I²C-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnect complexity in many applications. Each device is available with one of four factory-preset addresses (see *Selector Guide*).

The MAX5360/MAX5361/MAX5362 also include an output buffer, a low-power shutdown mode, and a power-on reset that ensures the DAC outputs are at zero when power is initially applied. In shutdown mode, the supply current is reduced to less than 1µA and the output is pulled down with a 10kΩ resistor to GND.

The MAX5360/MAX5361/MAX5362 are available in miniature 5-pin SOT23 packages.

Applications

Automatic Tuning (VCO)

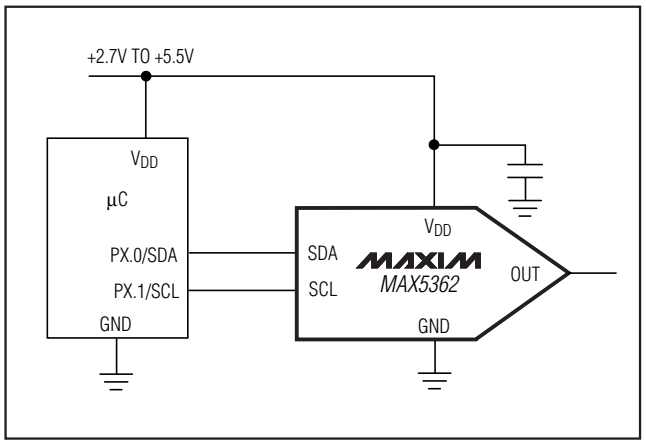
Power Amplifier Bias Control

Programmable Threshold Levels

Automatic Gain Control

Automatic Offset Adjustment

Typical Operating Circuit



Features

- **6-Bit Accuracy in a Tiny 5-Pin SOT23 Package**
- **Wide +2.7V to +5.5V Supply Range (MAX5362)**
- **1µA Shutdown Mode**
- **Buffered Output Drives Resistive Loads**
- **Low Glitch Power-On-Reset to Zero DAC Output**
- **Fast I²C-Compatible Serial Interface**
- **≤-5% Full-Scale Error (MAX5362)**
- **≤1LSB (max) INL/DNL**
- **Low 230µA max Supply Current**

Ordering Information

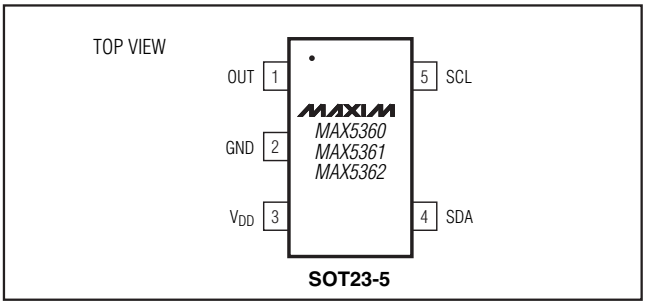
PART	TEMP RANGE	PIN-PACKAGE
MAX5360_EUK_ +T*	-40°C to +85°C	5 SOT23-5
MAX5361_EUK_ +T*	-40°C to +85°C	5 SOT23-5
MAX5362_EUK_ +T*	-40°C to +85°C	5 SOT23-5

**See Selector Guide for address options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Selector Guide

PART	ADDRESS	REFERENCE	TOP MARK
MAX5360LEUK	0x60	+2.0V	ADMM
MAX5360MEUK	0x62	+2.0V	ADMY
MAX5360NEUK	0x64	+2.0V	ADNE
MAX5360PEUK	0x66	+2.0V	ADMO
MAX5361LEUK	0x60	+4.0V	ADMU
MAX5361MEUK	0x62	+4.0V	ADNA
MAX5361NEUK	0x64	+4.0V	ADNG
MAX5361PEUK	0x66	+4.0V	ADMQ
MAX5362LEUK	0x60	0.9 x V_{DD}	ADMW
MAX5362MEUK	0x62	0.9 x V_{DD}	ADNC
MAX5362NEUK	0x64	0.9 x V_{DD}	ADNI
MAX5362PEUK	0x66	0.9 x V_{DD}	ADMS

Pin Configuration



SOT23-5

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT to GND .....-0.3V to (V_{DD} + 0.3V)
SCL, SDA to GND.....-0.3V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range
MAX536__EUK-T .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX5360); V_{DD} = 4.5V to 5.5V (MAX5361); V_{DD} = 2.7V to 5.5V (MAX5362); R_L =10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				6			Bits
Integral Linearity Error	INL	(Note 1)				±1	LSB
Differential Linearity Error	DNL	Guaranteed monotonic (Note 2)				±1	LSB
Offset Error	V_{OS}	Guaranteed monotonic (Note 2)			±1	±25	mV
Offset Error Supply Rejection		MAX5362 (Notes 2, 3)		60			dB
Offset Error Temperature Coefficient		(Note 2)	MAX5360/MAX5361		3		ppm/°C
			MAX5362		1		
Full-Scale Error		Code = 63	MAX5360/MAX5361			10	% of Ideal FS
			MAX5362			5	
Full-Scale Error Supply Rejection		Code = 63, MAX5360/MAX5361 (Note 4)				60	dB
Full-Scale Error Temperature Coefficient		Code = 63	MAX5360/MAX5361		±40		ppm/°C
			MAX5362		±10		
DAC OUTPUT							
Internal Reference (Note 5)	REF	MAX5360		1.8	2	2.2	V
		MAX5361		3.6	4	4.4	
		MAX5362		0.85× V_{DD}	0.9× V_{DD}	0.95× V_{DD}	
Output Load Regulation		Code = 63, 0 to 100µA			0.5		LSB
		Code = 0, 0 to -100µA			0.5		
Output Resistance		V_{OUT} = 0 to V_{DD}, power-down mode			10		kΩ
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative			0.4		V/µs
Output Settling Time		To 1/2LSB, 50kΩ and 50pF load (Note 6)			20		µs
Digital Feedthrough		Code = 0, all digital inputs from 0 to V_{DD}			2		nVs
Digital-Analog Glitch Impulse		Code 31 to 32			40		nVs
Wake-Up Time		From software shutdown			50		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX5360); V_{DD} = 4.5V to 5.5V (MAX5361); V_{DD} = 2.7V to 5.5V (MAX5362); R_L =10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX5360		2.7		3.6	V
		MAX5361		4.5		5.5	
		MAX5362		2.7		5.5	
Supply Current	I_{DD}	No load, all digital inputs at 0 or V_{DD}, code = 63			150	230	µA
		Shutdown mode				1	
DIGITAL INPUTS (SCL, SDA)							
Input Low Voltage	V_{IL}					0.3 × V_{DD}	V
Input High Voltage	V_{IH}			0.7 × V_{DD}			V
Input Hysteresis	V_{hys}				0.05 × V_{DD}		V
Input Capacitance	C_{IN}	(Note 7)			10		pF
Input Leakage Current	I_i					±10	µA
Pulse Width of Spike Suppressed	t_{SP}			0		50	ns
DIGITAL OUTPUT (SDA) (open drain)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0	0.4	V
		I_{SINK} = 6mA			0	0.6	
Output Fall Time	t_{of}	V_{IH} min to V_{IL} max, bus capacitance 10pF to 400pF	I_{SINK} = 3mA			250	ns
			I_{SINK} = 6mA			250	

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX5360); V_{DD} = 4.5V to 5.5V (MAX5361); V_{DD} = 2.7V to 5.5V (MAX5362); R_L =10kΩ, C_L = 50pF, T_A = T_{MAX} to T_{MIN}, Figure 3, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs

Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

TIMING CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX5360); V_{DD} = 4.5V to 5.5V (MAX5361); V_{DD} = 2.7V to 5.5V (MAX5362); R_L =10kΩ, C_L = 50pF, T_A = T_{MAX} to T_{MIN}, Figure 3, unless otherwise noted. Typical values are T_A = +25°C.)

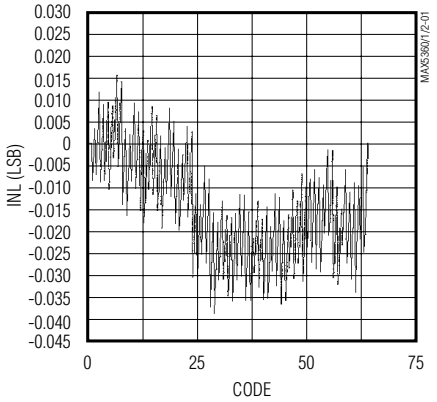
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_r				300	ns
Fall Time of Both SDA and SCL Signals	t_f				300	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF

Note 1: Guaranteed from code 1 to code 63.
Note 2: The offset value extrapolated from the range over which the INL is guaranteed.
Note 3: MAX5362, tested at V_{DD} = 5V ±10%.
Note 4: MAX5360, tested at V_{DD} = 3V ±10%; MAX5361, tested at V_{DD} = 5V ±10%.
Note 5: Actual output voltage at full scale is 63/64 × V_{REF}.
Note 6: Output settling time is measured by taking the code from code 1 to code 63, and from code 63 to code 1.
Note 7: Guaranteed by design.

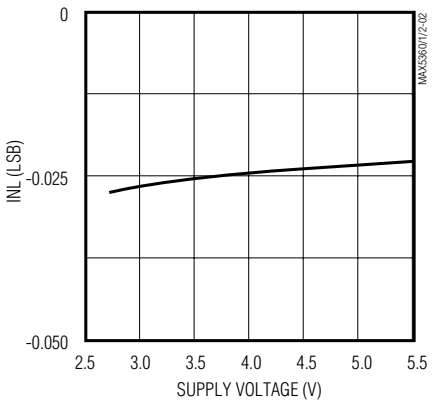
Typical Operating Characteristics

(V_{DD} = 3V (MAX5360), V_{DD} = 5V (MAX5361/MAX5362), T_A = +25°C, unless otherwise noted.)

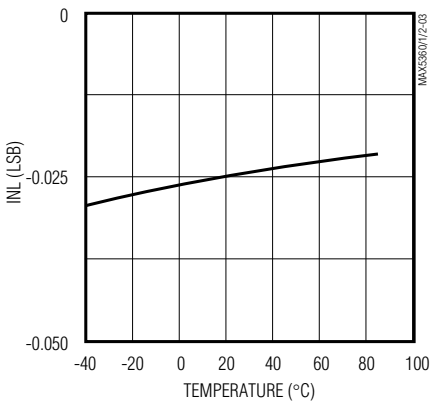
INTEGRAL NONLINEARITY vs. CODE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



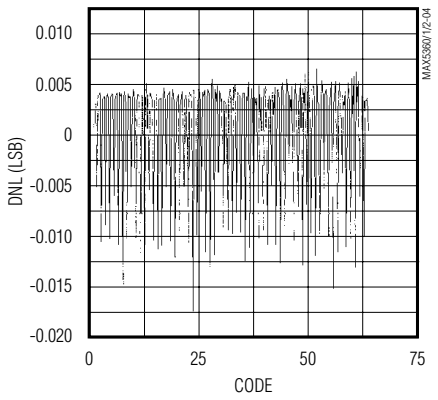
INTEGRAL NONLINEARITY vs. TEMPERATURE



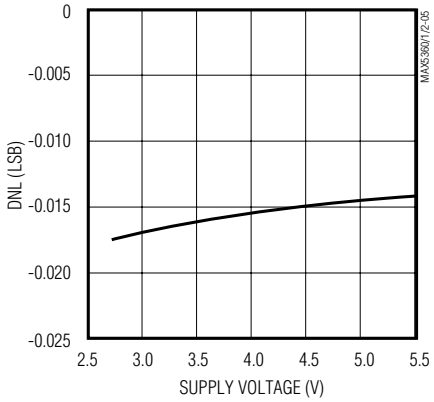
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX5360), V_{DD} = 5V (MAX5361/MAX5362), T_A = +25°C, unless otherwise noted.)

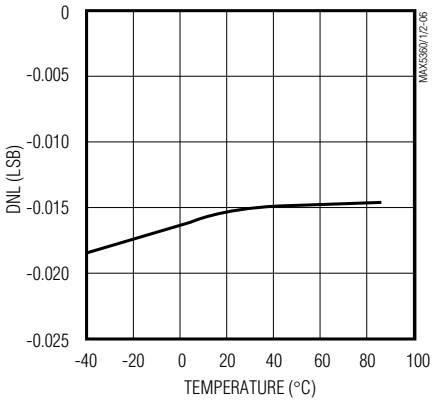
DIFFERENTIAL NONLINEARITY vs. CODE



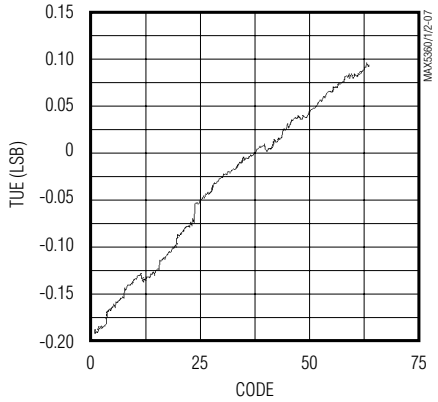
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



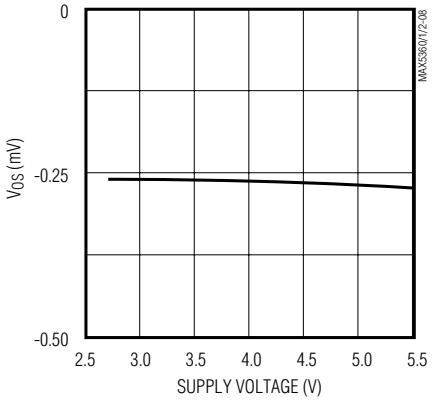
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



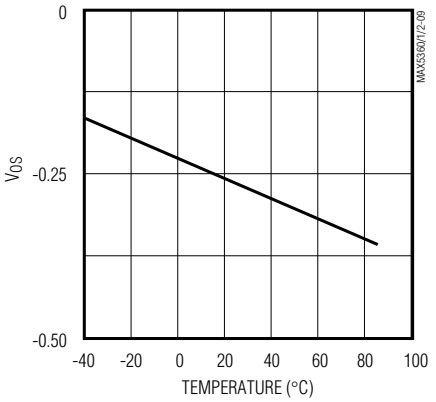
TOTAL UNADJUSTED ERROR vs. CODE



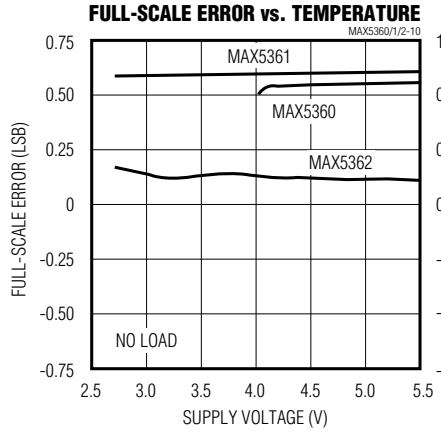
OFFSET ERROR vs. SUPPLY VOLTAGE



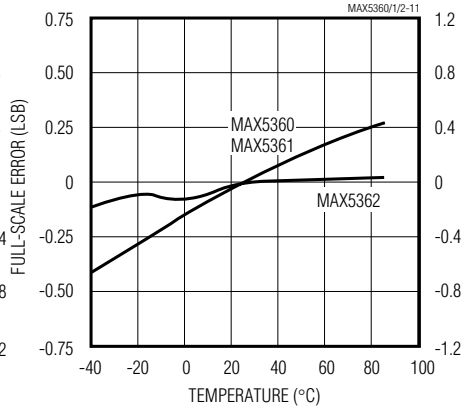
OFFSET ERROR vs. TEMPERATURE



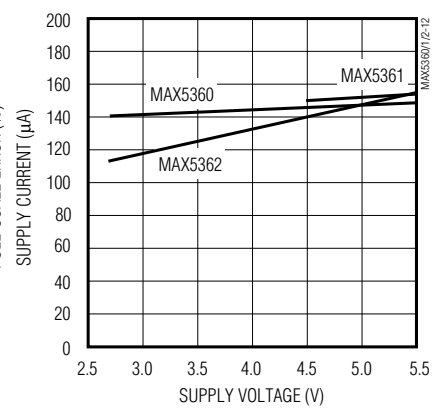
FULL-SCALE ERROR vs. TEMPERATURE



FULL-SCALE ERROR vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

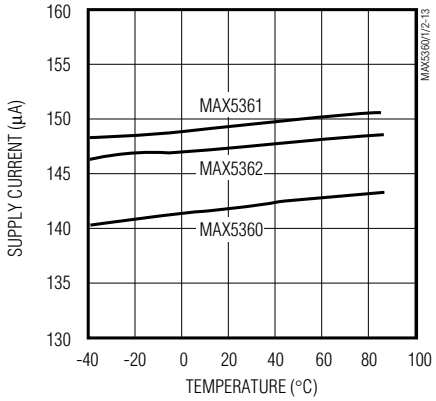


Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

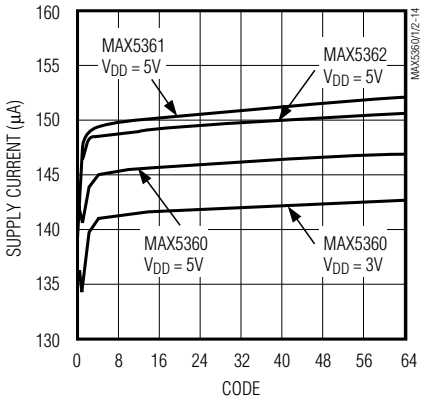
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX5360), V_{DD} = 5V (MAX5361/MAX5362), T_A = +25°C, unless otherwise noted.)

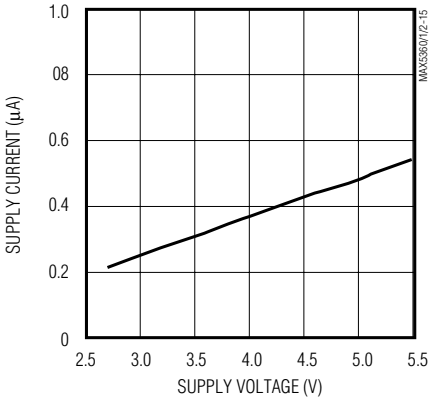
SUPPLY CURRENT vs. TEMPERATURE



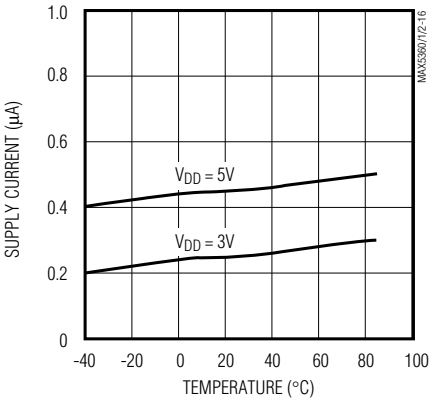
SUPPLY CURRENT vs. CODE



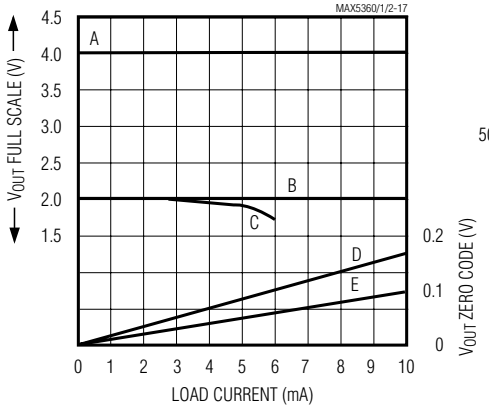
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

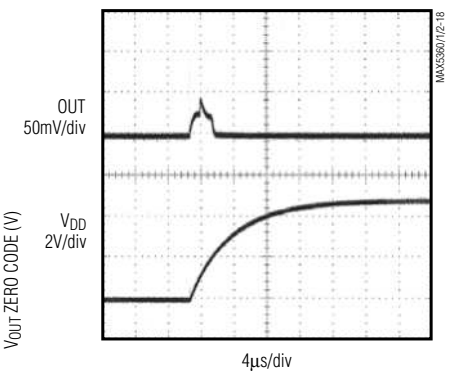


OUTPUT LOAD REGULATION



A: MAX5361/MAX5362, V_{DD} = 4.5V, FULL-SCALE OR SOURCIN
B: MAX5360, FULL-SCALE, V_{DD} = 2.7V SINKING, V_{DD} = 5V SO
C: MAX5360, FULL-SCALE, V_{DD} = 2.7V, SOURCING
D: ZERO CODE, V_{DD} = 2.7V, SINKING
E: ZERO CODE, V_{DD} = 5.5V SINKING

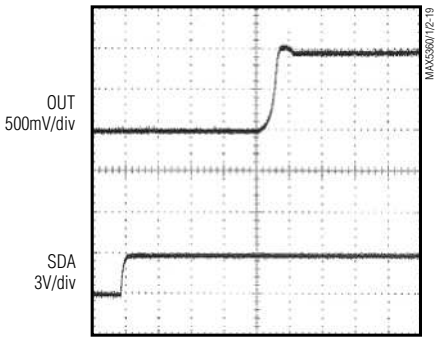
OUTPUT VOLTAGE ON POWER-UP



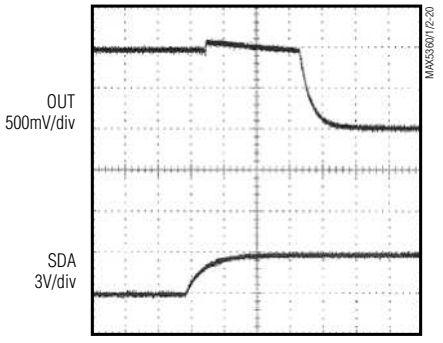
Typical Operating Characteristics (continued)

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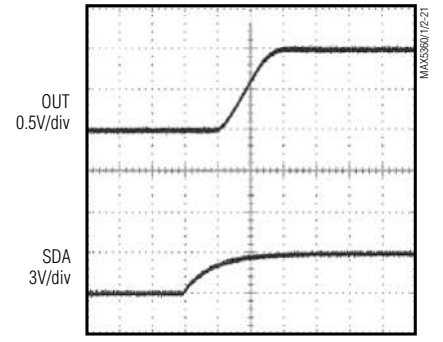
MAX5360 OUTPUT VOLTAGE EXITING SHUTDOWN



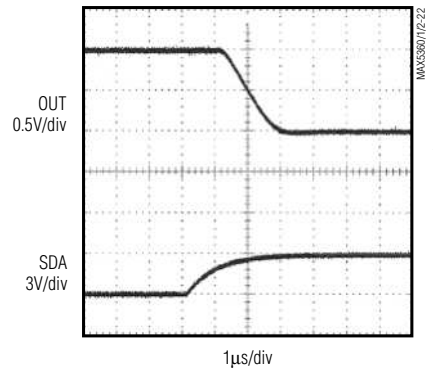
MAX5360 OUTPUT VOLTAGE ENTERING SHUTDOWN



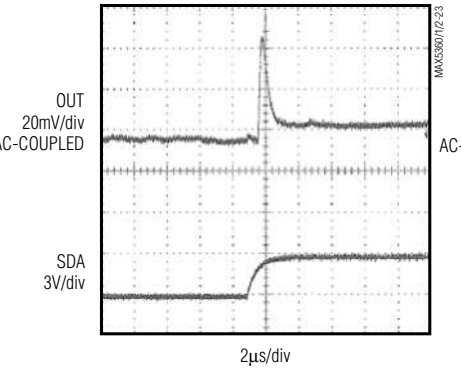
MAX5360 OUTPUT SETTLING FROM 1/4 FS TO 3/4 FS



MAX5360 OUTPUT SETTLING FROM 3/4 FS TO 1/4 FS

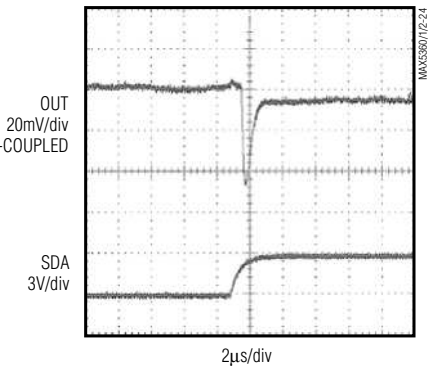


MAX5360 OUTPUT SETTLING 1/4LSB STEP-UP



0 x 7F TO 0 x 80
01111111 TO 10000000

MAX5360 OUTPUT SETTLING 1/4LSB STEP-DOWN



0 x 80 TO 0 x 7F
10000000 TO 01111111

Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Voltage Output
2	GND	Ground
3	V_{DD}	Power-Supply Input
4	SDA	Serial Data Input
5	SCL	Serial Clock Input

Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

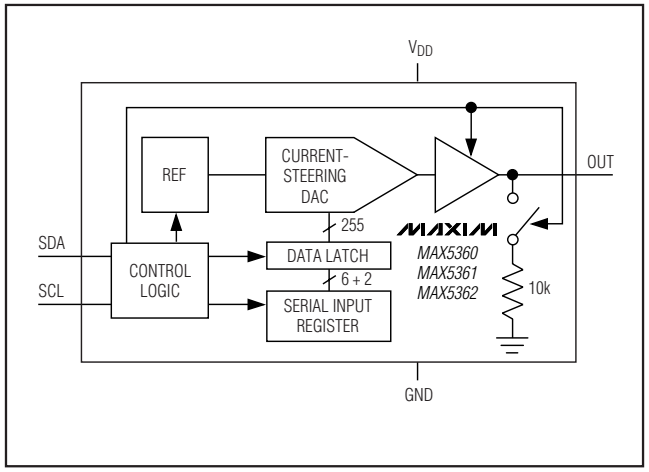


Figure 1. Functional Diagram

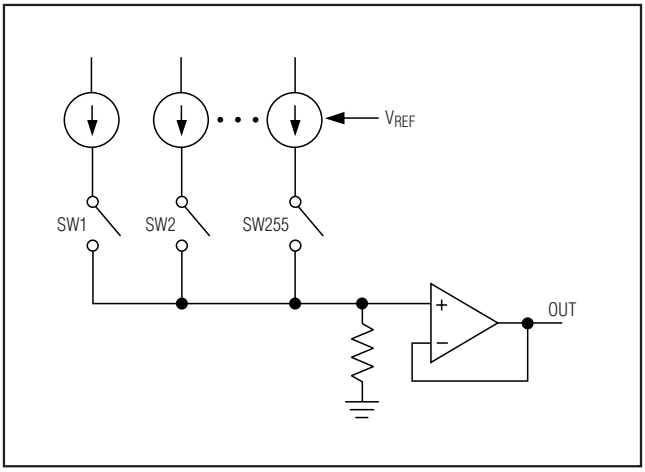


Figure 2. Current-Steering Topology

Table 1. Unipolar Code Current

DAC CODE 6 BITS + 2 SUBBITS	OUTPUT VOLTAGE		
	MAX5360	MAX5361	MAX5362
111111 (00)	2V × (63/64)	4V × (63/64)	0.9 × V_{DD} × (63/64)
100000 (00)	1V	2V	0.9 × V_{DD} / 2
000001 (00)	31mV	62mV	0.9 × V_{DD} / 64
000000 (00)	0	0	0

Detailed Description

The MAX5360/MAX5361/MAX5362 voltage-output, 6-bit DACs offer full 6-bit performance with less than 1LSB integral nonlinearity (INL) error and less than 1LSB differential nonlinearity (DNL) error ensuring monotonic performance. The devices use a simple two-wire, fast-mode I²C-compatible serial interface that operates up to 400kHz. The MAX5360/MAX5361/MAX5362 include an internal reference, an output buffer, and low-current shutdown mode, making them ideal for low-power, highly integrated applications. Figure 1 shows the devices' functional diagram.

Analog Section

The MAX5360/MAX5361/MAX5362 employ a current-steering DAC topology as shown in Figure 2. At the core of the DAC is a reference voltage-to-current converter (V/I) that generates a reference current. This current is mirrored to 255 equally weighted current sources. DAC switches control the outputs of these current mirrors, so only the desired fraction of the total current-mirror currents is steered to the DAC output. The current is then converted to a voltage across a resistor, and this voltage is buffered by the output buffer amplifier.

Output Voltage

Table 1 shows the relationship between the DAC code and the analog output voltage. The 6-bit DAC code is binary unipolar with 1LSB = (V_{REF} / 64). The MAX5360/MAX5361 have a full-scale output voltage of (+2V - 1LSB) and (+4V - 1LSB), respectively, set by the internal references. The MAX5362 has a full-scale output voltage of (0.9 × V_{DD} - 1LSB). Each device accepts 8-bit DAC codes, but the accuracy is guaranteed only for 6 bits.

Output Buffer

The DAC voltage output is an internally buffered unity-gain follower that typically slews at ±0.4V/µs. The output can swing from 0 to full scale. With a 1/4 FS to 3/4 FS output transition, the amplifier outputs typically settle to 1/2LSB in less than 5µs when loaded with 10kΩ in parallel with 50pF. The buffer amplifiers are stable with any combination of resistive loads >10kΩ and capacitive loads <50pF.

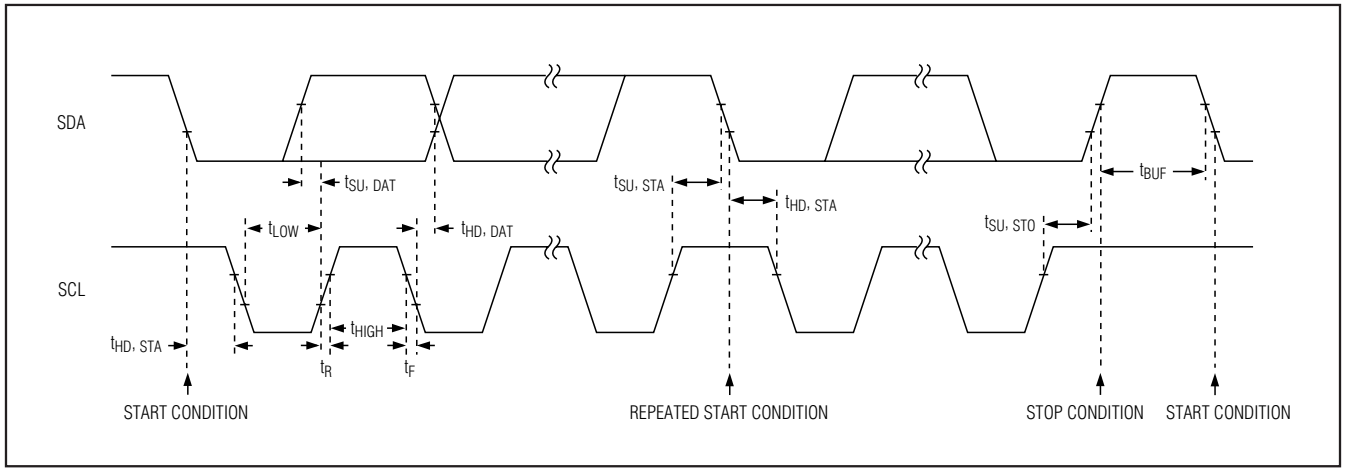


Figure 3. Two-Wire Serial Interface Timing Diagram

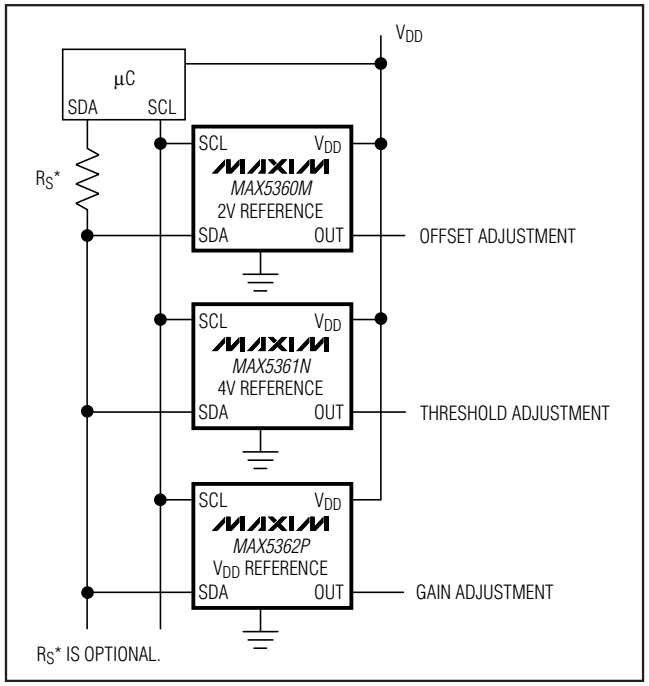


Figure 4. Typical Application Circuit

Power-On Reset

The MAX5360/MAX5361/MAX5362 have a power-on reset circuit to set the DAC's output to 0 when V_{DD} is first applied or when V_{DD} dips below 1.7V. This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. The output glitch on startup is typically <50mV.

Shutdown Mode

The MAX5360/MAX5361/MAX5362 include a software-controlled shutdown mode that reduces the supply current to <1µA. All internal circuitry is disabled and an internal 10kΩ resistor is placed from OUT to GND to ensure 0V at OUT while in shutdown. The device enters shutdown in less than 5µs and exits shutdown in less than 50µs.

Digital Section

Serial interface

The MAX5360/MAX5361/MAX5362 use a simple two-wire serial interface requiring only two I/O lines (two-wire bus) of a standard microprocessor (µP) port. Figure 3 shows the timing diagram for signals on the 2-wire bus.

The two bus lines (SDA and SCL) must be high when the bus is not in use. The MAX5360/MAX5361/MAX5362 are receive-only devices (slaves) and must be controlled by a bus master device. Figure 4 shows a typical application where multiple devices can be connected to the bus provided they have different address settings. External pullup resistors are not necessary on these lines (when driven by push-pull drivers), though the MAX5360/MAX5361/MAX5362 can be used in applications where pullup resistors are required (such as in I^2C systems) to maintain compatibility with existing circuitry. The serial interface operates at SCL rates up to 400kHz. The SDA state is allowed to change only while SCL is low, with the exception of START and STOP conditions as shown in Figure 5. Each transmission consists of a START condition sent by the bus master device, followed by the MAX5360/MAX5361/MAX5362's preset slave address, a power-mode bit, the DAC data (6 bits + 2 subbits), and finally, a STOP

Low-Cost, Low-Power 6-Bit DACs with 2-Wire Serial Interface in SOT23 Package

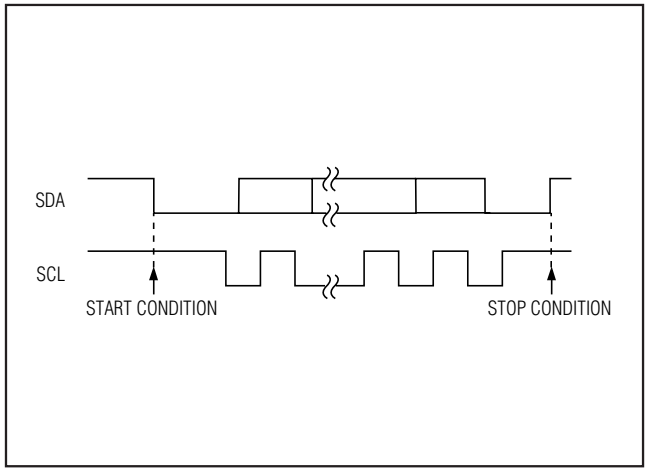


Figure 5. Start and Stop Conditions

condition (Figure 6). The bus is then free for another transmission.

SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer each byte to the MAX5360/MAX5361/MAX5362. Release SDA during the 9th clock cycle as the selected device acknowledges the receipt of the byte, by pulling SDA low during this time. A series resistor on the SDA line may be needed if the master's output is forced high while the selected device acknowledges (Figure 4).

Slave Address

The MAX5360/MAX5361/MAX5362 are available with one of four preset slave addresses. Each address option is identified by the suffix L, M, N, or P added to the part number. The address is defined as the 7 most significant bits (MSBs) sent by the master after a START condition. The address options are 0x60, 0x62, 0x64, and 0x66 (left justified with LSB set to 0). The 8th bit, typically used to define a write or read protocol, sets the device's power mode (SHDN); the device is powered down when SHDN is set to 1. During a device search routine, the MAX5360/MAX5361/MAX5362 acknowledge both options (SHDN = 0 or SHDN = 1) but does not change its power state if a stop condition (or restart) is issued immediately. The second byte (DAC data) must be sent/received for the device to update both power mode and DAC output.

DAC Data

The 6-bit DAC data is decoded as straight binary MSB first with 1LSB = (V_{REF} / 64) and converted into the corresponding analog voltage as shown in Table 1. Two subbits complete the data byte; these 2 bits should be set to zero since they are not tested to guaranteed-monotonic performance.

After receiving the data byte, the MAX5360/MAX5361/MAX5362 acknowledge its receipt and expect a STOP condition, at which point the DAC output is updated. The devices update the output and the power mode only if the second byte is clocked in (SHDN = 0) or out (SHDN = 1) of the device. When SHDN = 1, the master will read all ones when clocking out a data byte. The MAX5360/MAX5361/MAX5362 do not drive SDA except for the acknowledge bit.

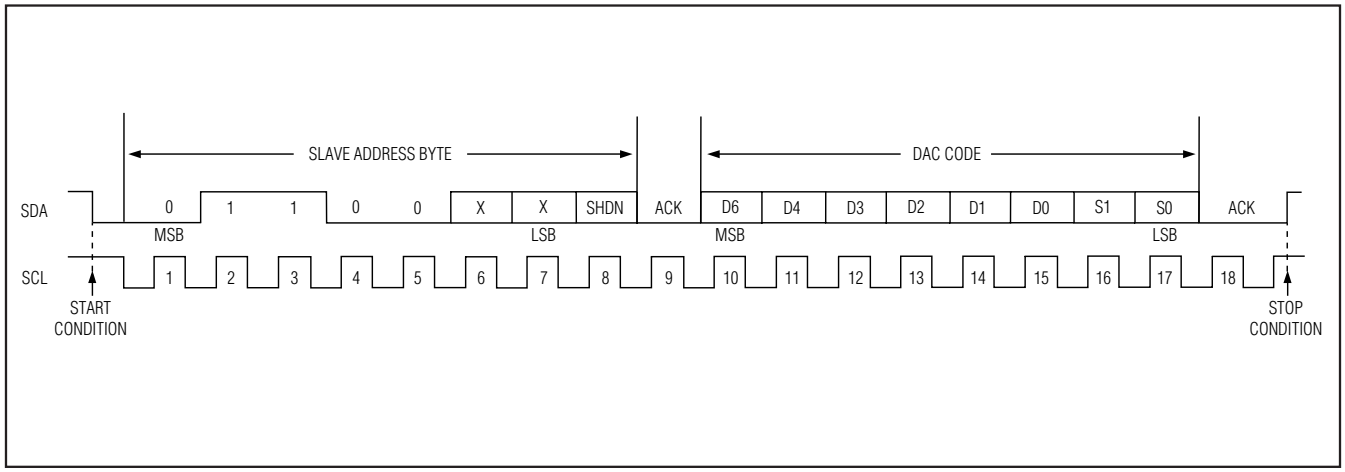


Figure 6. Complete Serial Transmission

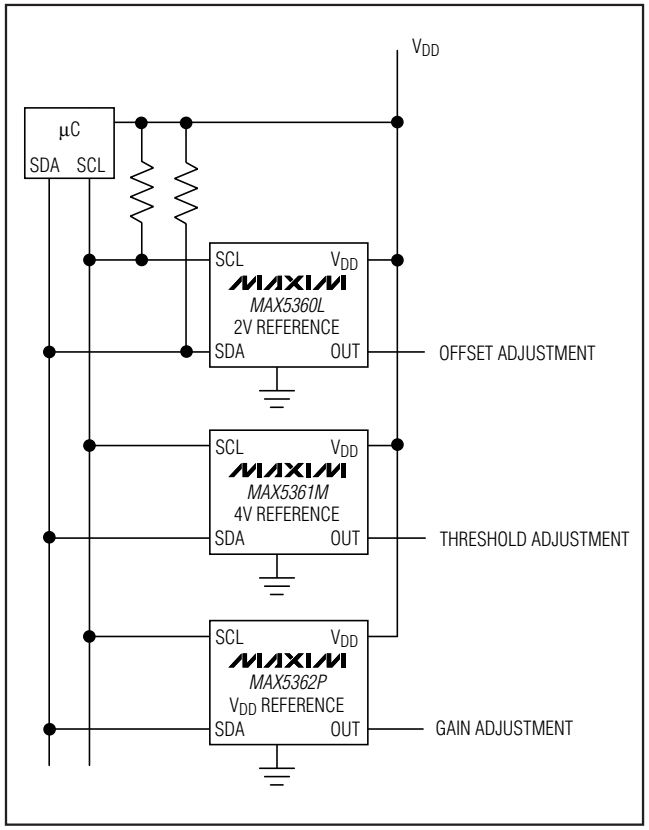


Figure 7. I²C Typical Application

I²C Compatibility

The MAX5360/MAX5361/MAX5362 are compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the 9th clock pulse. Figure 7 shows a typical I²C application. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The MAX5360/MAX5361/MAX5362 address is compatible with the 7-bit I²C addressing protocol only. No 10-bit formats are supported. RESTART protocol is supported, but an immediate STOP condition is necessary to update the DAC.

Applications Information

Digital Inputs and Interface Logic

The serial 2-wire interface has logic levels defined as V_{OL} = 0.3 x V_{DD} and V_{OH} = 0.7 x V_{DD}. All of the inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5360/MAX5361/MAX5362 without additional external logic. The digital inputs are compatible with CMOS logic levels and must not be driven with voltages higher than V_{DD}.

Power-Supply Bypassing and Layout

Careful PC board layout is important for best system performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. Ensure that the ground return from GND to the supply ground is short and low impedance; a ground plane is recommended. Bypass V_{DD} with a 0.1µF to ground as close as possible to the device. If the supply is excessively noisy, connect a 10Ω resistor in series with the supply and V_{DD}, and add additional capacitance

Chip Information

PROCESS: BiCMOS

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Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	21-0057	90-0174

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	3/11	Corrected offset error specification in *Electrical Characteristics* table	2

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