19-3120; Rev 1; 2/07

MAXIM

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs



## General Description

The MAX5510/MAX5511 are single, 8-bit, ultra-low-power, voltage-output, digital-to-analog converters (DACs) offering rail-to-rail buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and consume less than 6µA, making them desirable for low-power and low-voltage applications. A shutdown mode reduces overall current, including the reference input current, to just 0.18µA. The MAX5510/MAX5511 use a 3-wire serial interface that is compatible with SPI™, QSPI™, and MICROWIRE™.

At power-up, the MAX5510/MAX5511 outputs are driven to zero scale, providing additional safety for applications that drive valves or for other transducers that must be off during power-up. The zero-scale outputs enable glitch-free power-up.

The MAX5510 accepts an external reference input. The MAX5511 contains an internal reference and provides an external reference output. Both devices have force-sense-configured output buffers.

The MAX5510/MAX5511 are available in a 4mm x 4mm x 0.8mm, 12-pin, thin QFN package and are guaranteed over the extended -40°C to +85°C temperature range.

For 12-bit compatible devices, refer to the MAX5530/MAX5531 data sheet. For 10-bit compatible devices, refer to the MAX5520/MAX5521 data sheet.

## Applications

Portable Battery-Powered Devices

Instrumentation

Automatic Trimming and Calibration in Factory or Field

Programmable Voltage and Current Sources

Industrial Process Control and Remote Industrial Devices

Remote Data Conversion and Monitoring

Chemical Sensor Cell Bias for Gas Monitors

Programmable Liquid Crystal Display (LCD) Bias

## Selector Guide

| PART | REFERENCE | TOP MARK |
|---|---|---|
| MAX5510ETC | External | AACO |
| MAX5511ETC | Internal | AACP |

*SPI and QSPI are trademarks of Motorola, Inc.*
*MICROWIRE is a trademark of National Semiconductor Corp.*

## Features

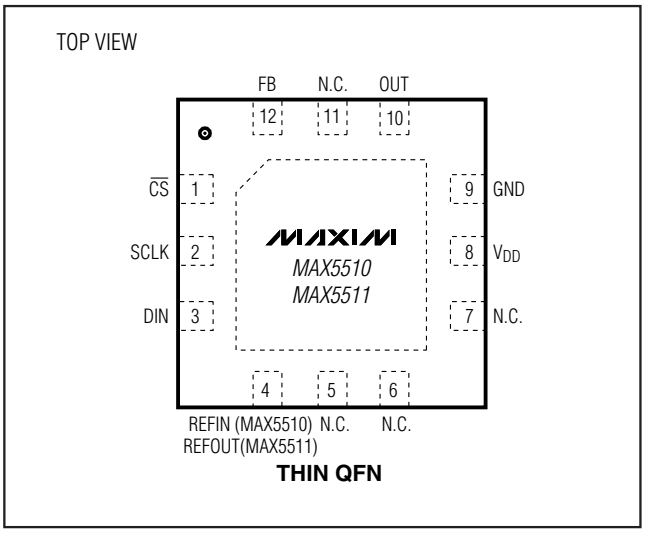
- ♦ **Single +1.8V to +5.5V Supply**
- ♦ **Ultra-Low 6µA Supply Current**
- ♦ **Shutdown Mode Reduces Supply Current to 0.18µA (max)**
- ♦ **Small 4mm x 4mm x 0.8mm Thin QFN Package**
- ♦ **Flexible Force-Sense-Configured Rail-to-Rail Output Buffers**
- ♦ **Internal Reference Sources 8mA of Current (MAX5511)**
- ♦ **Fast 16MHz 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- ♦ **TTL- and CMOS-Compatible Digital Inputs with Hysteresis**
- ♦ **Glitch-Free Outputs During Power-Up**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| **MAX5510**ETC | -40°C to +85°C | 12 Thin QFN-EP* | T1244-4 |
| **MAX5511**ETC | -40°C to +85°C | 12 Thin QFN-EP* | T1244-4 |

**EP = Exposed paddle (internally connected to GND).*

## Pin Configuration






**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.**

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....-0.3V to +6V
OUT to GND .....-0.3V to ($V_{DD}$ + 0.3V)
FB to GND .....-0.3V to ($V_{DD}$ + 0.3V)
SCLK, DIN, $\overline{CS}$ to GND .....-0.3V to ($V_{DD}$ + 0.3V)
REFIN, REFOUT to GND .....-0.3V to ($V_{DD}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
Thin QFN (derate 16.9mW/°C above +70°C).....1349mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature..... +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +1.8V to +5.5V, OUT unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC ACCURACY (MAX5510 EXTERNAL REFERENCE)** | | | | | | |
| Resolution | N | | 8 | | | Bits |
| Integral Nonlinearity (Note 1) | INL | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±0.25 | ±1 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±0.25 | ±1 | |
| Differential Nonlinearity (Note 1) | DNL | Guaranteed monotonic, $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±0.2 | ±1 | LSB |
| | | Guaranteed monotonic, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±0.2 | ±1 | |
| Offset Error (Note 2) | $V_{OS}$ | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±1 | ±20 | mV |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±1 | ±20 | |
| Offset-Error Temperature Drift | | | | ±2 | | µV/°C |
| Gain Error (Note 3) | GE | $V_{DD}$ = 5V, $V_{REF}$ = 4.096V | | ±0.5 | ±1 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.024V | | ±0.5 | ±1 | |
| Gain-Error Temperature Coefficient | | | | ±4 | | ppm/°C |
| Power-Supply Rejection Ratio | PSRR | 1.8V ≤ $V_{DD}$ ≤ 5.5V | | 85 | | dB |
| **STATIC ACCURACY (MAX5511 INTERNAL REFERENCE)** | | | | | | |
| Resolution | N | | 8 | | | Bits |
| Integral Nonlinearity (Note 1) | INL | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±0.25 | ±1 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±0.25 | ±1 | |
| Differential Nonlinearity (Note 1) | DNL | Guaranteed monotonic, $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±0.2 | ±1 | LSB |
| | | Guaranteed monotonic, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±0.2 | ±1 | |
| Offset Error (Note 2) | $V_{OS}$ | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±1 | ±20 | mV |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±1 | ±20 | |
| Offset-Error Temperature Drift | | | | ±2 | | µV/°C |
| Gain Error (Note 3) | GE | $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | ±0.5 | ±1 | LSB |
| | | $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | ±0.5 | ±1 | |
| Gain-Error Temperature Coefficient | | | | ±4 | | ppm/°C |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +1.8V to +5.5V, OUT unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power-Supply Rejection Ratio | PSRR | 1.8V ≤ $V_{DD}$ ≤ 5.5V | | 85 | | dB |
| **REFERENCE INPUT (MAX5510)** | | | | | | |
| Reference-Input Voltage Range | $V_{REFIN}$ | | 0 | | $V_{DD}$ | V |
| Reference-Input Impedance | $R_{REFIN}$ | Normal operation | 4.1 | | | MΩ |
| | | In shutdown | | 2.5 | | GΩ |
| **REFERENCE OUTPUT (MAX5511)** | | | | | | |
| Initial Accuracy | $V_{REFOUT}$ | No external load, $V_{DD}$ = 1.8V | 1.197 | 1.214 | 1.231 | V |
| | | No external load, $V_{DD}$ = 2.5V | 1.913 | 1.940 | 1.967 | |
| | | No external load, $V_{DD}$ = 3V | 2.391 | 2.425 | 2.459 | |
| | | No external load, $V_{DD}$ = 5V | 3.828 | 3.885 | 3.941 | |
| Output-Voltage Temperature Coefficient | $V_{TEMPCO}$ | $T_A$ = -40°C to +85°C (Note 4) | | 12 | 30 | ppm/°C |
| Line Regulation | | $V_{REFOUT}$ < $V_{DD}$ - 200mV (Note 5) | | 2 | 200 | µV/V |
| Load Regulation | | 0 ≤ $I_{REFOUT}$ ≤ 1mA, sourcing, $V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V | | 0.3 | 2 | µV/µA |
| | | 0 ≤ $I_{REFOUT}$ ≤ 8mA, sourcing, $V_{DD}$ = 5V, $V_{REF}$ = 3.9V | | 0.3 | 2 | |
| | | -150µA ≤ $I_{REFOUT}$ ≤ 0, sinking | | 0.2 | | |
| Output Noise Voltage | | 0.1Hz to 10Hz, $V_{REFOUT}$ = 3.9V | | 150 | | $µV_{P-P}$ |
| | | 10Hz to 10kHz, $V_{REFOUT}$ = 3.9V | | 600 | | |
| | | 0.1Hz to 10Hz, $V_{REFOUT}$ = 1.2V | | 50 | | |
| | | 10Hz to 10kHz, $V_{REFOUT}$ = 1.2V | | 450 | | |
| Short-Circuit Current (Note 6) | | $V_{DD}$ = 5V | | 30 | | mA |
| | | $V_{DD}$ = 1.8V | | 14 | | |
| Capacitive Load Stability Range | | (Note 7) | | 0 to 10 | | nF |
| Thermal Hysteresis | | (Note 8) | | 200 | | ppm |
| Reference Power-Up Time (from Shutdown) | | REFOUT unloaded, $V_{DD}$ = 5V | | 5.4 | | ms |
| | | REFOUT unloaded, $V_{DD}$ = 1.8V | | 4.4 | | |
| Long-Term Stability | | | | 200 | | ppm/ 1khrs |
| **DAC OUTPUT (OUT)** | | | | | | |
| Capacitive Driving Capability | $C_L$ | | | 1000 | | pF |
| Short-Circuit Current (Note 6) | | $V_{DD}$ = 5V, $V_{OUT}$ set to full scale, OUT shorted to GND, source current | | | 65 | mA |
| | | $V_{DD}$ = 5V, $V_{OUT}$ set to 0V, OUT shorted to $V_{DD}$, sink current | | | 65 | |
| | | $V_{DD}$ = 1.8V, $V_{OUT}$ set to full scale, OUT shorted to GND, source current | | | 14 | |
| | | $V_{DD}$ = 1.8V, $V_{OUT}$ set to 0V, OUT shorted to $V_{DD}$, sink current | | | 14 | |

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +1.8V to +5.5V, OUT unloaded, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| DAC Power-Up Time | | Coming out of shutdown (MAX5510) | $V_{DD}$ = 5V | | 3 | | ms |
| | | | $V_{DD}$ = 1.8V | | 3.8 | | |
| | | Coming out of standby (MAX5511) | $V_{DD}$ = 1.8V to 5.5V | | 0.4 | | |
| Output Power-Up Glitch | | $C_L$ = 100pF | | | 10 | | mV |
| FB_ Input Current | | | | | 10 | | pA |
| **DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | 4.5V ≤ $V_{DD}$ ≤ 5.5V | | 2.4 | | | V |
| | | 2.7V < $V_{DD}$ ≤ 3.6V | | 2.0 | | | |
| | | 1.8V ≤ $V_{DD}$ ≤ 2.7V | | 0.7 x $V_{DD}$ | | | |
| Input Low Voltage | $V_{IL}$ | 4.5V ≤ $V_{DD}$ ≤ 5.5V | | | | 0.8 | V |
| | | 2.7V < $V_{DD}$ ≤ 3.6V | | | | 0.6 | |
| | | 1.8V ≤ $V_{DD}$ ≤ 2.7V | | | | 0.3 x $V_{DD}$ | |
| Input Leakage Current | $I_{IN}$ | (Note 9) | | | ±0.05 | ±0.5 | µA |
| Input Capacitance | $C_{IN}$ | | | | 10 | | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Voltage-Output Slew Rate | SR | Positive and negative (Note 10) | | | 10 | | V/ms |
| Voltage-Output Settling Time | | 0.1 to 0.9 of full scale to within 0.5 LSB (Note 10) | | | 660 | | µs |
| Output Noise Voltage | | 0.1Hz to 10Hz | $V_{DD}$ = 5V | | 80 | | $µV_{P-P}$ |
| | | | $V_{DD}$ = 1.8V | | 55 | | |
| | | 10Hz to 10kHz | $V_{DD}$ = 5V | | 620 | | |
| | | | $V_{DD}$ = 1.8V | | 476 | | |
| **POWER REQUIREMENTS** | | | | | | | |
| Supply Voltage Range | $V_{DD}$ | | | 1.8 | | 5.5 | V |
| Supply Current (Note 9) | $I_{DD}$ | MAX5510 | $V_{DD}$ = 5V | | 2.6 | 4 | µA |
| | | | $V_{DD}$ = 3V | | 2.6 | 4 | |
| | | | $V_{DD}$ = 1.8V | | 3.6 | 5 | |
| | | MAX5511 | $V_{DD}$ = 5V | | 5.3 | 6.5 | |
| | | | $V_{DD}$ = 3V | | 4.8 | 6.0 | |
| | | | $V_{DD}$ = 1.8V | | 5.4 | 7.0 | |
| Standby Supply Current | $I_{DDSD}$ | (Note 9) | $V_{DD}$ = 5V | | 3.3 | 4.0 | µA |
| | | | $V_{DD}$ = 3V | | 2.8 | 3.4 | |
| | | | $V_{DD}$ = 1.8V | | 2.4 | 3.0 | |
| Shutdown Supply Current | $I_{DDPD}$ | (Note 9) | | | 0.05 | 0.18 | µA |

## TIMING CHARACTERISTICS

($V_{DD}$ = +4.5V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS ($V_{DD}$ = 4.5V TO 5.5V)** | | | | | | |
| Serial Clock Frequency | $f_{SCLK}$ | | 0 | | 16.7 | MHz |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | | 15 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 24 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 24 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 100 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ | | 20 | | | ns |
| SCLK Fall to $\overline{CS}$ Fall Setup | $t_{CSO}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCK Rise Hold Time | $t_{CS1}$ | | 20 | | | ns |

## TIMING CHARACTERISTICS

($V_{DD}$ = +1.8V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS ($V_{DD}$ = 1.8V TO 5.5V)** | | | | | | |
| Serial Clock Frequency | $f_{SCLK}$ | | 0 | | 10 | MHz |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | | 24 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 40 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 40 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 150 | | | ns |
| SCLK Rise to $\overline{CS}$ Rise Hold Time | $t_{CSH}$ | | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ | | 30 | | | ns |
| SCLK Fall to $\overline{CS}$ Fall Setup | $t_{CSO}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCK Rise Hold Time | $t_{CS1}$ | | 30 | | | ns |

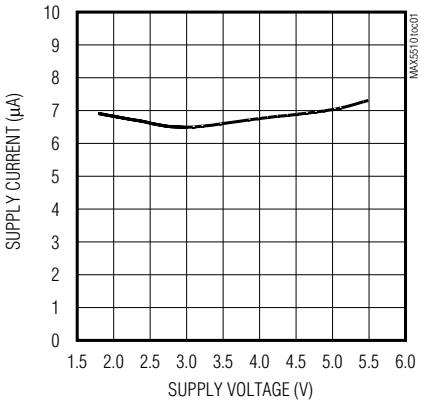
**Note 1:** Linearity is tested within codes 6 to 255.
**Note 2:** Offset is tested at code 6.
**Note 3:** Gain is tested at code 250. FB is connected to OUT.
**Note 4:** Guaranteed by design. Not production tested.
**Note 5:** $V_{DD}$ must be a minimum of 1.8V.
**Note 6:** Outputs can be shorted to $V_{DD}$ or GND indefinitely, provided that the package power dissipation is not exceeded.
**Note 7:** Optimal noise performance is at 2nF load capacitance.
**Note 8:** Thermal hysteresis is defined as the change in the initial +25°C output voltage after cycling the device from $T_{MAX}$ to $T_{MIN}$.
**Note 9:** All digital inputs at $V_{DD}$ or GND.
**Note 10:** Load = 10kΩ in parallel with 100pF, $V_{DD}$ = 5V, $V_{REF}$ = 4.096V (MAX5510) or $V_{REF}$ = 3.9V (MAX5511).

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

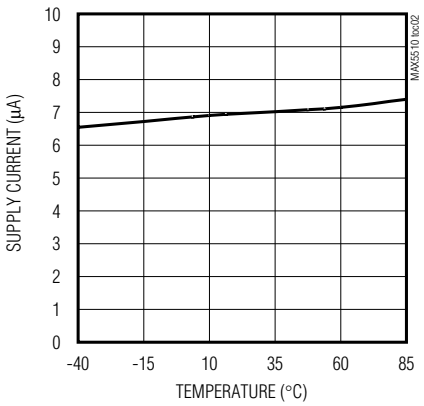
## Typical Operating Characteristics

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5510) or $V_{REF}$ = 3.9V (MAX5511), $T_A$ = +25°C, unless otherwise noted.)

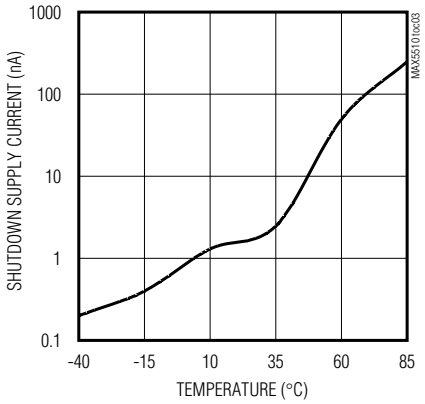
**SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5511)**



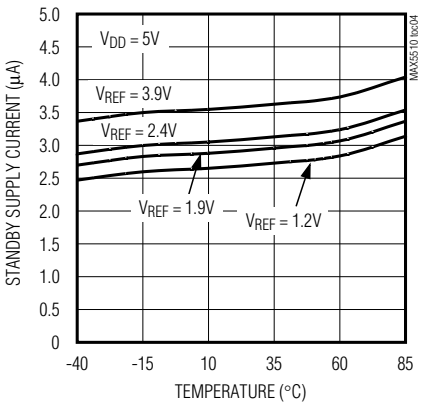

**SUPPLY CURRENT vs. TEMPERATURE (MAX5511)**



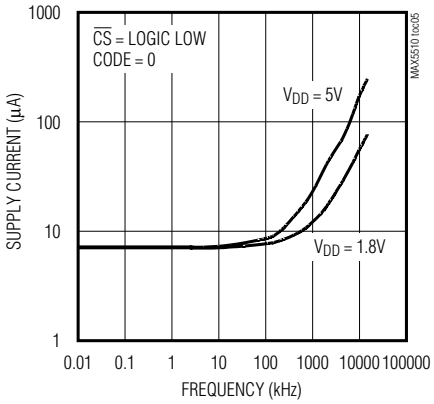

**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5511)**



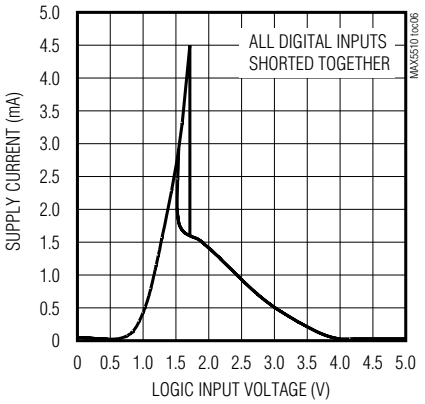

**STANDBY SUPPLY CURRENT vs. TEMPERATURE (MAX5511)**



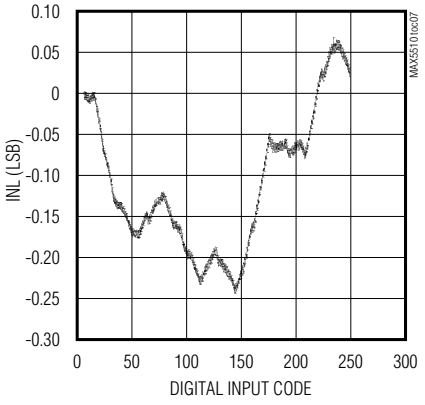

**SUPPLY CURRENT vs. CLOCK FREQUENCY**



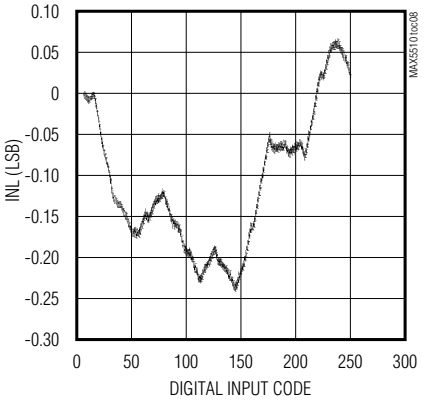

**SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE**



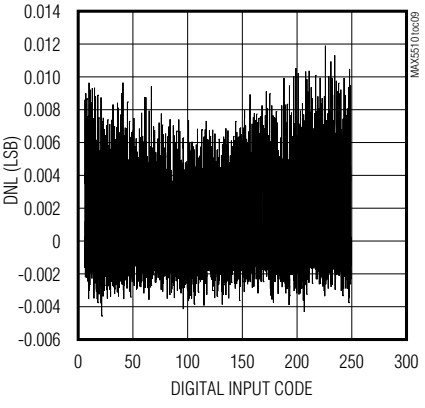

**INL vs. INPUT CODE ($V_{DD}$ = $V_{REF}$ = 1.8V)**




**INL vs. INPUT CODE ($V_{DD}$ = $V_{REF}$ = 5V)**



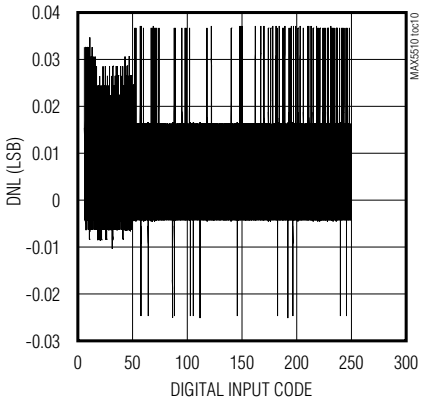

**DNL vs. INPUT CODE ($V_{DD}$ = $V_{REF}$ = 1.8V)**



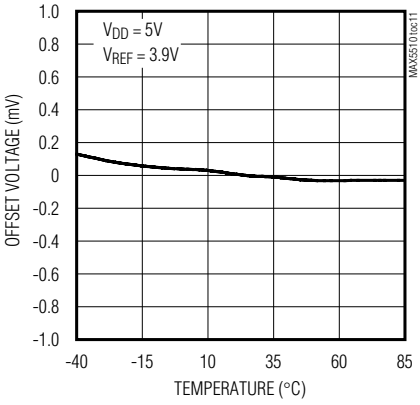
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5510) or $V_{REF}$ = 3.9V (MAX5511), $T_A$ = +25°C, unless otherwise noted.)

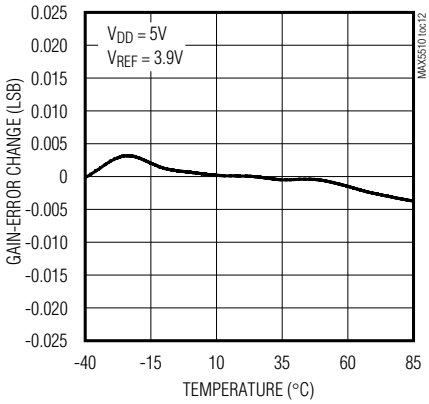
**DNL vs. INPUT CODE ($V_{DD}$ = $V_{REF}$ = 5V)**



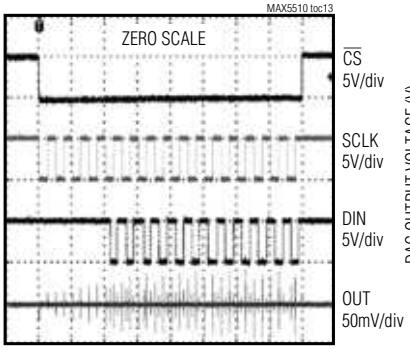

**OFFSET VOLTAGE vs. TEMPERATURE**



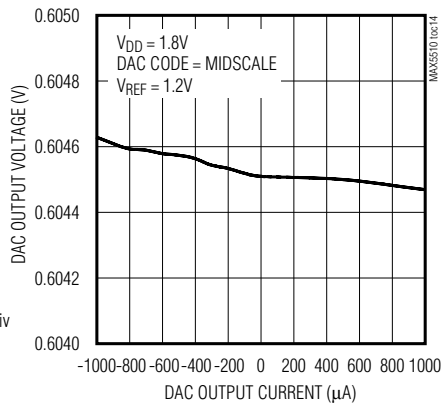

**GAIN-ERROR CHANGE vs. TEMPERATURE**



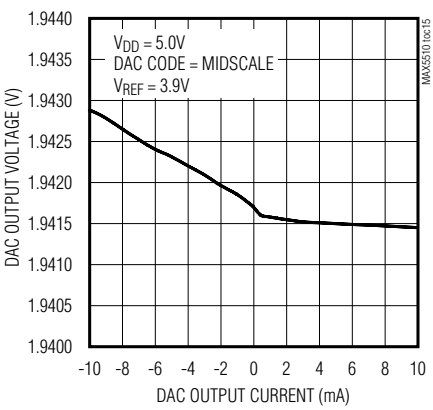

**DIGITAL FEEDTHROUGH RESPONSE (DAC OUTPUT SET TO 0)**



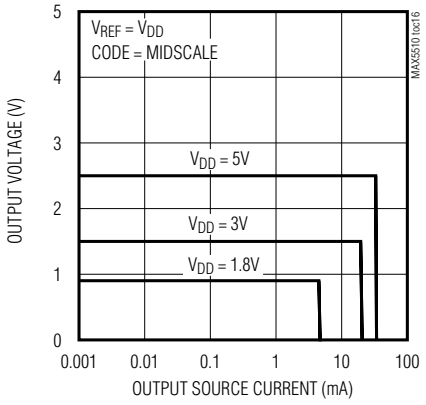

**DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT**



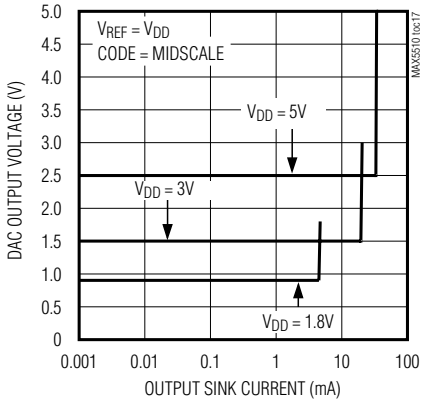

**DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT**



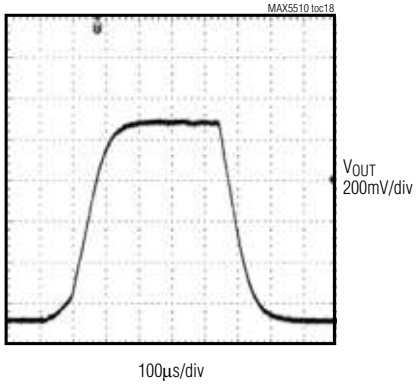

**DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT**




**DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT**




**OUTPUT LARGE-SIGNAL STEP RESPONSE ($V_{DD}$ = 1.8V, $V_{REF}$ = 1.219V)**

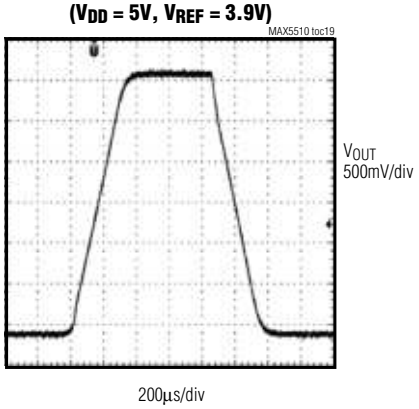


# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

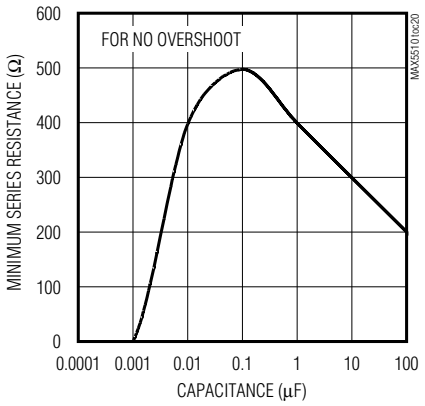
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5510) or $V_{REF}$ = 3.9V (MAX5511), $T_A$ = +25°C, unless otherwise noted.)

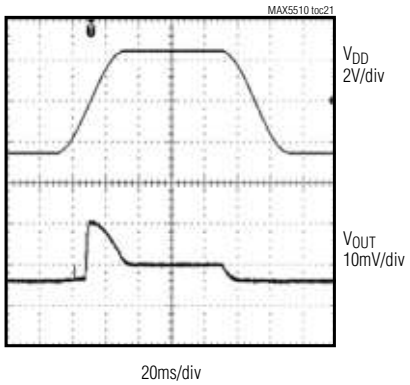
**OUTPUT LARGE-SIGNAL STEP RESPONSE ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**



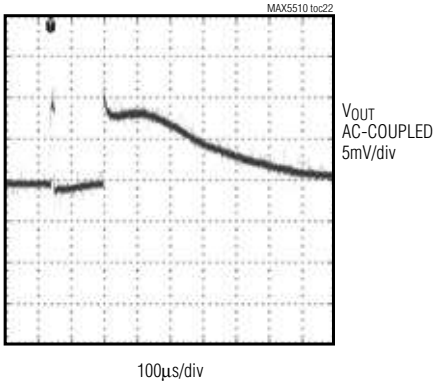

**OUTPUT MINIMUM SERIES RESISTANCE vs. LOAD CAPACITANCE**



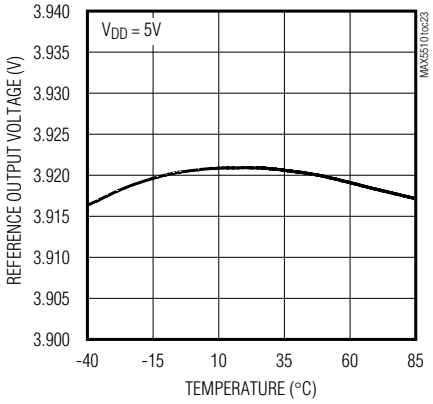

**POWER-UP OUTPUT VOLTAGE GLITCH**



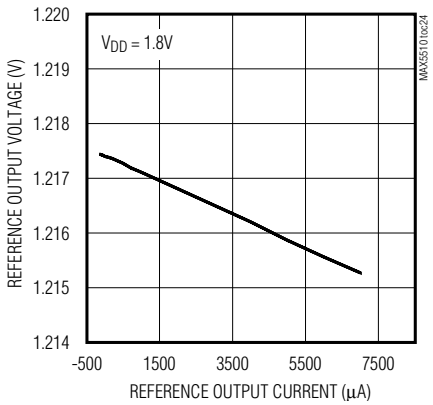

**MAJOR CARRY OUTPUT VOLTAGE GLITCH (CODE 7FFh TO 800h) ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**



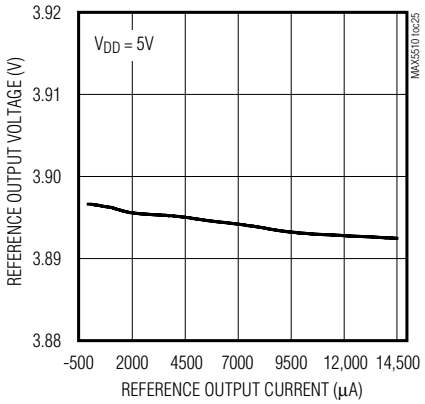

**REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE**



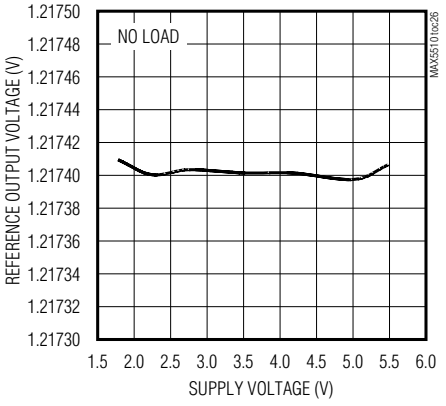

**REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT**



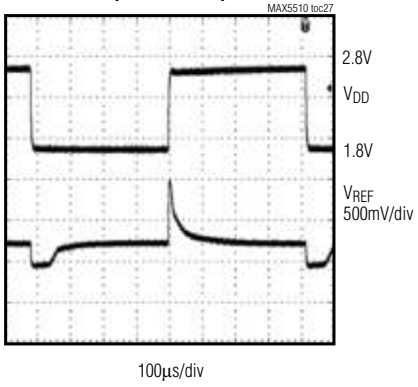

**REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT**




**REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**



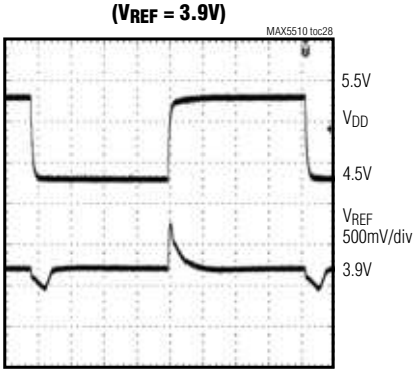

**REFERENCE LINE-TRANSIENT RESPONSE ($V_{REF}$ = 1.2V)**



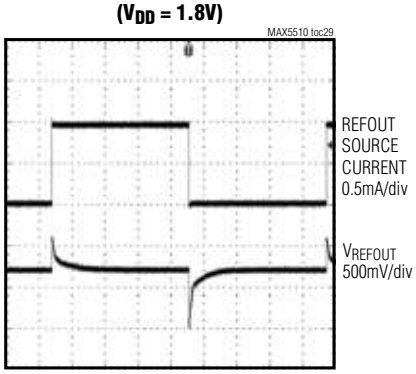
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5.0V, $V_{REF}$ = 4.096V (MAX5510) or $V_{REF}$ = 3.9V (MAX5511), $T_A$ = +25°C, unless otherwise noted.)

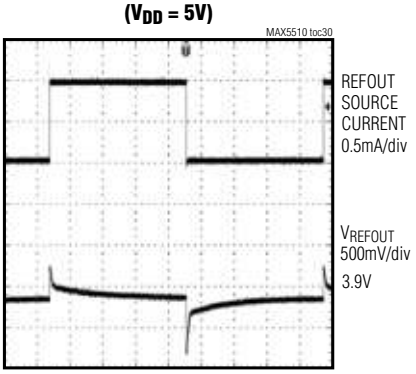
**REFERENCE LINE-TRANSIENT RESPONSE ($V_{REF}$ = 3.9V)**



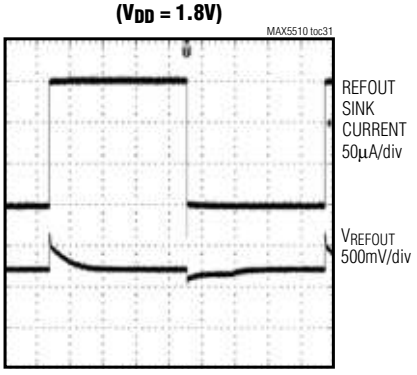

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 1.8V)**



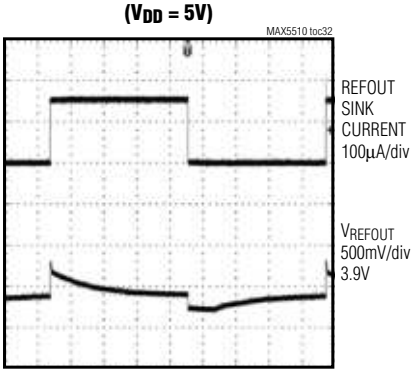

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 5V)**



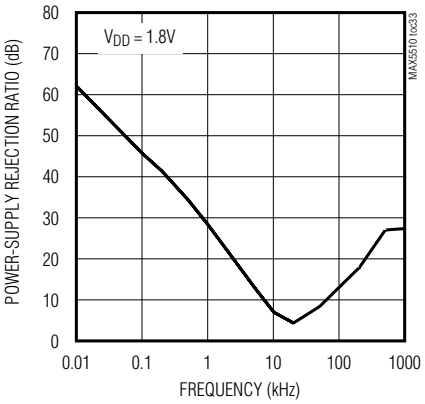

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 1.8V)**



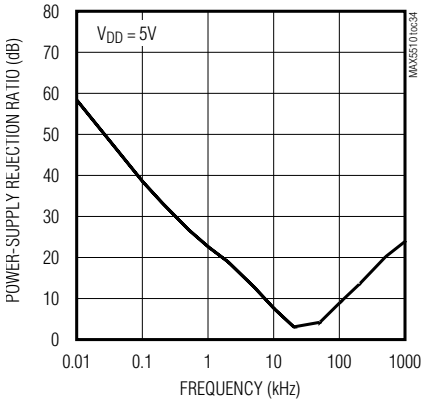

**REFERENCE LOAD TRANSIENT ($V_{DD}$ = 5V)**



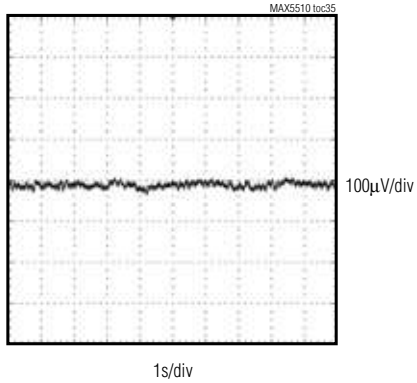

**REFERENCE PSRR vs. FREQUENCY**



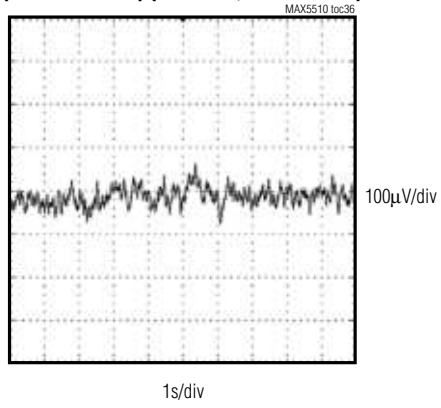

**REFERENCE PSRR vs. FREQUENCY**




**REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) ($V_{DD}$ = 1.8V, $V_{REF}$ = 1.2V)**




**REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) ($V_{DD}$ = 5V, $V_{REF}$ = 3.9V)**

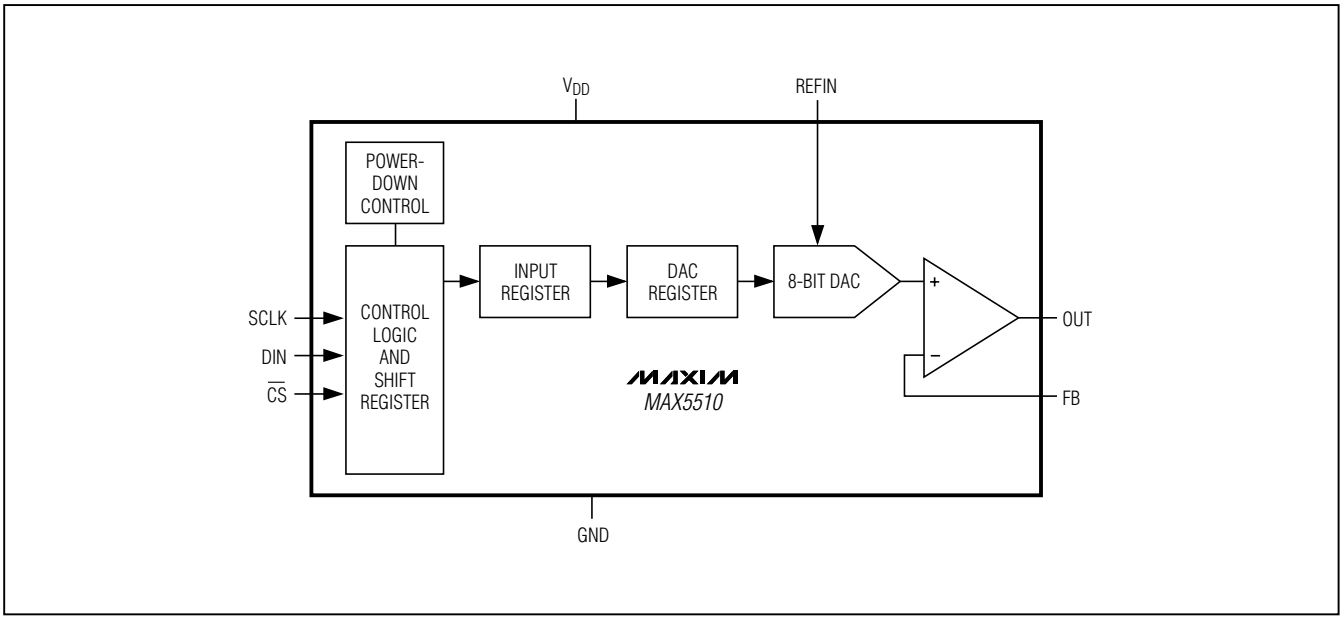


# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

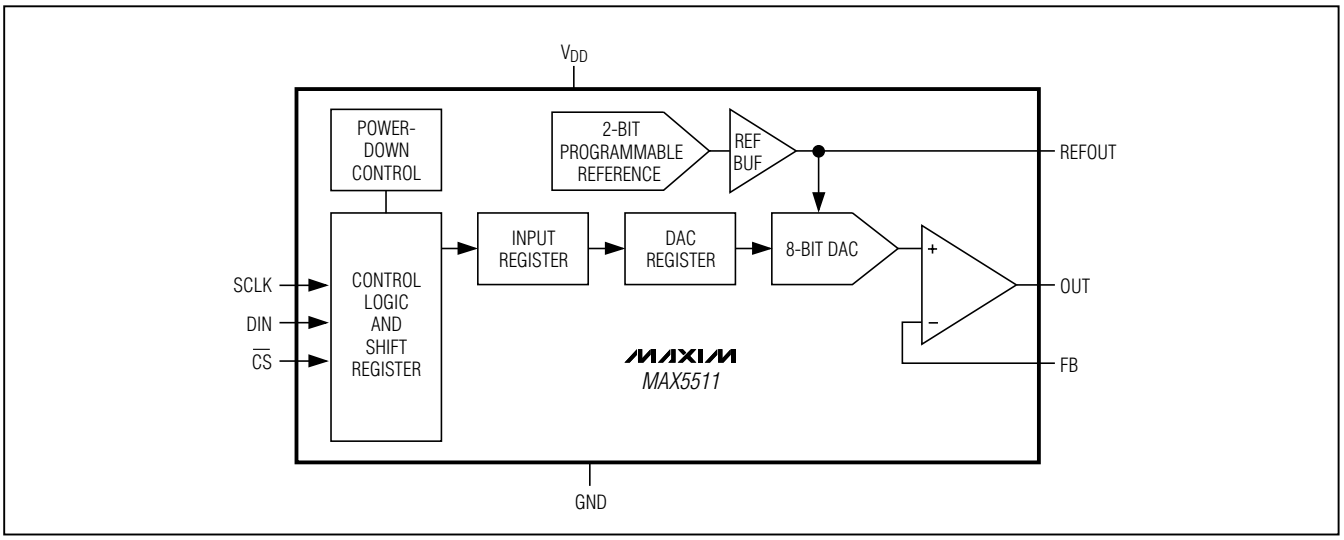
## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX5510 | MAX5511 | | |
| 1 | 1 | $\overline{CS}$ | Active-Low Digital-Input Chip Select |
| 2 | 2 | SCLK | Serial-Interface Clock |
| 3 | 3 | DIN | Serial-Interface Data Input |
| 4 | — | REFIN | Reference Input |
| — | 4 | REFOUT | Reference Output |
| 5, 6, 7, 11 | 5, 6, 7, 11 | N.C. | No Connection. Leave N.C. inputs unconnected (floating), or connect to GND. |
| 8 | 8 | $V_{DD}$ | Power Input. Connect $V_{DD}$ to a 1.8V to 5.5V power supply. Bypass $V_{DD}$ to GND with a 0.1µF capacitor. |
| 9 | 9 | GND | Ground |
| 10 | 10 | OUT | Analog Voltage Output |
| 12 | 12 | FB | Feedback Input |
| EP | EP | Exposed Paddle | Exposed Paddle. Connect EP to GND. |

## MAX5510 Functional Diagram



## MAX5511 Functional Diagram




## Detailed Description

The MAX5510/MAX5511 single, 8-bit, ultra-low-power, voltage-output DACs offer Rail-to-Rail buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and require only 6µA (max) supply current. These devices feature a shutdown mode that reduces overall current, including the reference input current, to just 0.18µA. The MAX5511 includes an internal reference that saves additional board space and can source up to 8mA, making it functional as a system reference. The 16MHz, 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE protocols. When $V_{DD}$ is applied, all DAC outputs are driven to zero scale with virtually no output glitch. The MAX5510/MAX5511 output buffers are configured in force sense allowing users to externally set voltage gains on the output (an output-amplifier inverting input is available). These devices come in a 4mm x 4mm thin QFN package.

### Digital Interface

The MAX5510/MAX5511 use a 3-wire serial interface compatible with SPI, QSPI, and MICROWIRE protocols (Figures 1 and 2).

The MAX5510/MAX5511 include a single, 16-bit, input shift register. Data loads into the shift register through the serial interface. $\overline{CS}$ must remain low until all 16 bits are clocked in. Data loads MSB first, D9–D0. The 16 bits consist of 4 control bits (C3–C0), 8 data bits (D7–D0), and 4 sub-bits. (see Table 1). D7–D0 are the DAC data bits and S3–S0 are the sub-bits. The sub-bits must be set to zero for proper operation. The control bits C3–C0 control the MAX5510/MAX5511, as outlined in Table 2.

Each DAC channel includes two registers: an input register and a DAC register. The input register holds input data. The DAC register contains the data updated to the DAC output.

The double-buffered register configuration allows any of the following:

- Loading the input registers without updating the DAC registers
- Updating the DAC registers from the input registers
- Updating all the input and DAC registers simultaneously

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

## Table 1. Serial Write Data Format

| CONTROL | | | | DATA BITS | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | | | | | | | | | LSB |
| C3 | C2 | C1 | C0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | S3 | S2 | S1 | S0 |

*Sub-bits S3—S0 must be set to zero for proper operation.*

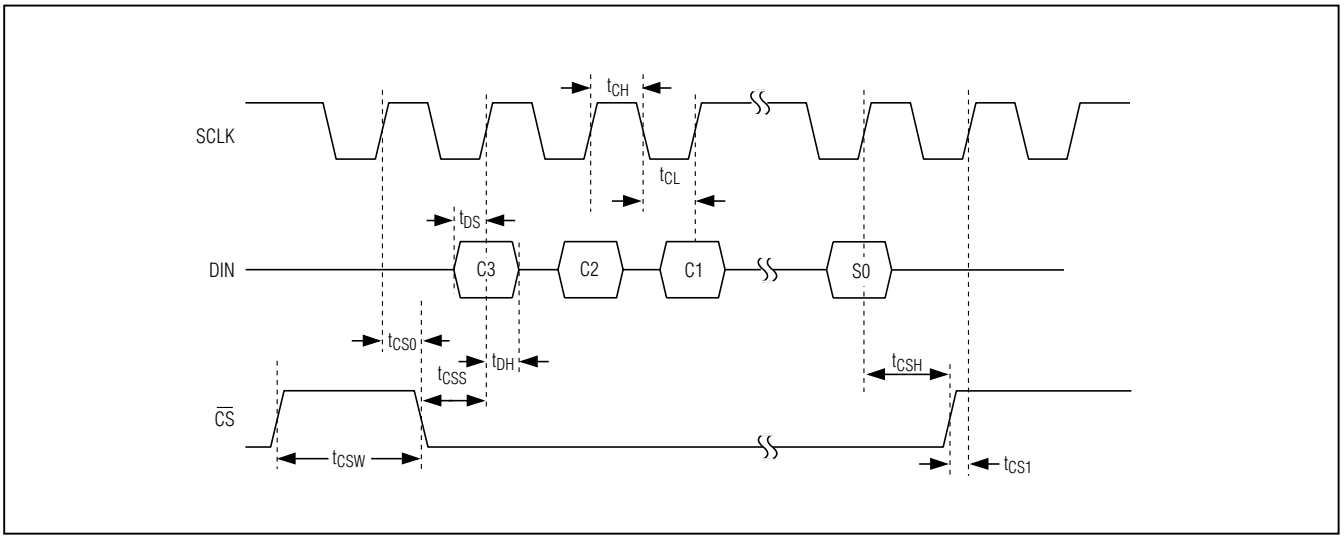



*Figure 1. Timing Diagram*

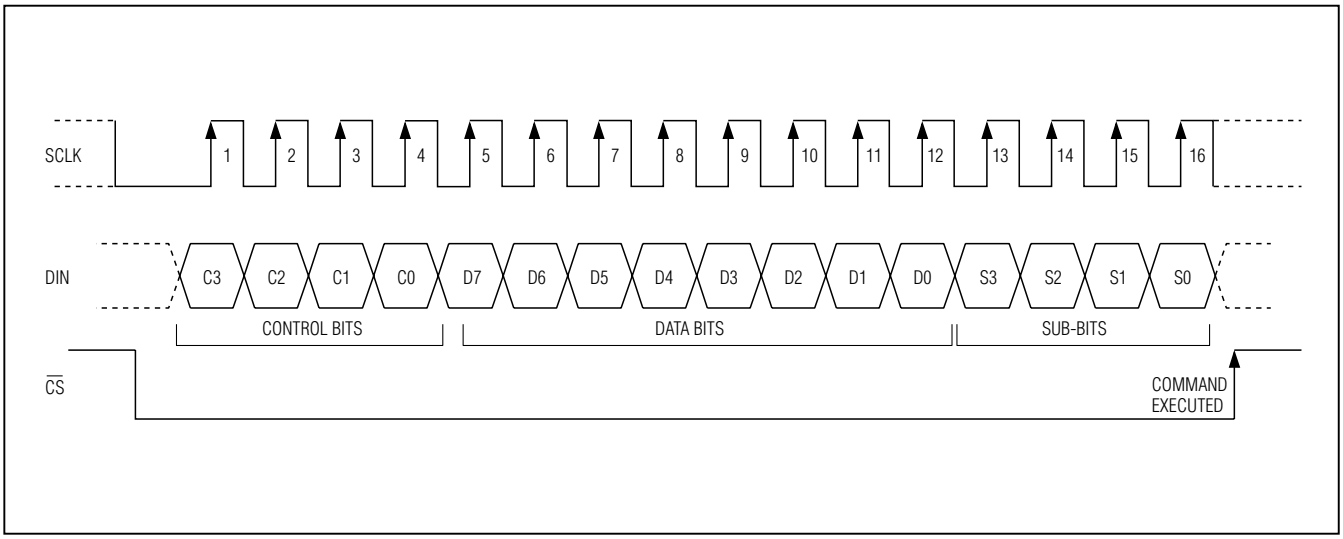



*Figure 2. Register Loading Diagram*

## Table 2. Serial-Interface Programming Commands

| CONTROL BITS | | | | INPUT DATA | SUB-BITS | FUNCTION |
|---|---|---|---|---|---|---|
| C3 | C2 | C1 | C0 | D7–D0 | S3–S0 | |
| 0 | 0 | 0 | 0 | XXXXXXXX | 0000 | No operation; command is ignored. |
| 0 | 0 | 0 | 1 | 8-bit data | 0000 | Load input register from shift register; DAC register unchanged; DAC output unchanged. |
| 0 | 0 | 1 | 0 | — | — | Command reserved; do not use. |
| 0 | 0 | 1 | 1 | — | — | Command reserved; do not use. |
| 0 | 1 | 0 | 0 | — | — | Command reserved; do not use. |
| 0 | 1 | 0 | 1 | — | — | Command reserved; do not use. |
| 0 | 1 | 1 | 0 | — | — | Command reserved; do not use. |
| 0 | 1 | 1 | 1 | — | — | Command reserved; do not use. |
| 1 | 0 | 0 | 0 | XXXX XXXX | 0000 | Load DAC register from input register; DAC output updated; MAX5510 enters normal operation if in shutdown; MAX5511 enters normal operation if in standby or shutdown. |
| 1 | 0 | 0 | 1 | 8-bit data | 0000 | Load input register and DAC register from shift register; DAC output updated; MAX5510 enters normal operation if in shutdown; MAX5511 enters normal operation if in standby or shutdown. |
| 1 | 0 | 1 | 0 | — | — | Command reserved; do not use. |
| 1 | 0 | 1 | 1 | — | — | Command reserved; do not use. |
| 1 | 1 | 0 | 0 | D7, D6, XXXXXX | 0000 | MAX5510 enters shutdown; MAX5511 enters standby*. For the MAX5511, D7 and D6 configure the internal reference voltage (Table 3). |
| 1 | 1 | 0 | 1 | D7, D6, XXXXXX | 0000 | MAX5510/MAX5511 enter normal operation; DAC output reflects existing contents of DAC register. For the MAX5511, D7 and D6 configure the internal reference voltage (Table 3). |
| 1 | 1 | 1 | 0 | D7, D6, XXXXXX | 0000 | MAX5510/MAX5511 enter shutdown; DAC output set to high impedance. For the MAX5511, D7 and D6 configure the internal reference voltage (Table 3). |
| 1 | 1 | 1 | 1 | 8-bit data | 0000 | Load input register and DAC register from shift register; DAC output updated; MAX5510 enters normal operation if in shutdown; MAX5511 enters normal operation if in standby or shutdown. |

*X = Don't care.*

**Standby mode can be entered from normal operation only. It is not possible to enter standby mode from shutdown.*

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

### Power Modes

The MAX5510/MAX5511 feature two power modes to conserve power during idle periods. In normal operation, the device is fully operational. In shutdown mode, the device is completely powered down, including the internal voltage reference in the MAX5511. The MAX5511 also offers a standby mode where all circuitry is powered down except the internal voltage reference. Standby mode keeps the reference powered up while the remaining circuitry is shut down, allowing it to be used as a system reference. Standby mode also helps reduce the wake-up delay by not requiring the reference to power up when returning to normal operation.

### Shutdown Mode

The MAX5510/MAX5511 feature a software-programmable shutdown mode that reduces the typical supply current and the reference input current to 0.18µA (max). Writing an input control word with control bits C[3:0] = 1110 places the device in shutdown mode (Table 2). In shutdown, the MAX5510 reference input and DAC output buffers go high impedance. Placing the MAX5511 into shutdown turns off the internal reference, and the DAC output buffers go high impedance. The serial interface remains active for all devices.

Table 2 shows several commands that bring the MAX5510/MAX5511 back to normal operation. The power-up time from shutdown is required before the DAC outputs are valid.

**Note:** For the MAX5511, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation before entering standby mode.

### Standby Mode (MAX5511 Only)

The MAX5511 features a software-programmable standby mode that reduces the typical supply current to 6µA. Standby mode powers down all circuitry except the internal voltage reference. Place the device in standby mode by writing an input control word with control bits C[3:0] = 1100 (Table 2). The internal reference and serial interface remain active while the DAC output buffers go high impedance. If the MAX5511 is coming out of standby, the power-up time from standby is required before the DAC outputs are valid.

For the MAX5511, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation before entering standby mode. To enter standby from shutdown, issue the command to return to normal operation, followed immediately by the command to go into standby.

Table 2 shows several commands that bring the MAX5511 back to normal operation. When transitioning from standby mode to normal operation, only the DAC power-up time is required before the DAC outputs are valid.

### Reference Input

The MAX5510 accepts a reference with a voltage range extending from 0 to $V_{DD}$. The output voltage ($V_{OUT}$) is represented by a digitally programmable voltage source as:

$$V_{OUT} = (V_{REF} \times N / 256) \times gain$$

where N is the numeric value of the DAC's binary input code (0 to 255), $V_{REF}$ is the reference voltage and gain is the externally set voltage gain for the MAX5510/MAX5511.

In shutdown mode, the reference input enters a high-impedance state with an input impedance of 2.5GΩ (typ).

### Reference Output

The MAX5511 internal voltage reference is software configurable to one of four voltages. Upon power-up, the default reference voltage is 1.214V. Configure the reference voltage using the D6 and D7 data bits (Table 3) when the control bits are as follows: C[3:0] = 1100, 1101, or 1110 (Table 2). $V_{DD}$ must be kept at a minimum of 200mV above $V_{REF}$ for proper operation.

## Table 3. Reference Output Voltage Programming

| D7 | D6 | REFERENCE VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 1.214 |
| 0 | 1 | 1.940 |
| 1 | 0 | 2.425 |
| 1 | 1 | 3.885 |

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

## Applications Information

### 1-Cell and 2-Cell Circuit

See Figure 3 for an illustration of how to power the MAX5510/MAX5511 with either one lithium-ion battery or two alkaline batteries. The low current consumption of the devices makes the MAX5510/MAX5511 ideal for battery-powered applications.

### Programmable Current Source

See the circuit in Figure 4 for an illustration of how to configure the MAX5510 as a programmable current source for driving an LED. The MAX5510 drives a standard NPN transistor to program the current source. The current source ($I_{LED}$) is defined in the equation in Figure 4.

### Voltage Biasing a Current-Output Transducer

See the circuit in Figure 5 for an illustration of how to configure the MAX5510 to bias a current-output transducer. In Figure 5, the output voltage of the MAX5510 is a function of the voltage drop across the transducer added to the voltage drop across the feedback resistor R.

### Self-Biased Two-Electrode Potentiostat Application

See the circuit in Figure 6 for an illustration of how to use the MAX5511 to bias a two-electrode potentiostat on the input of an ADC.

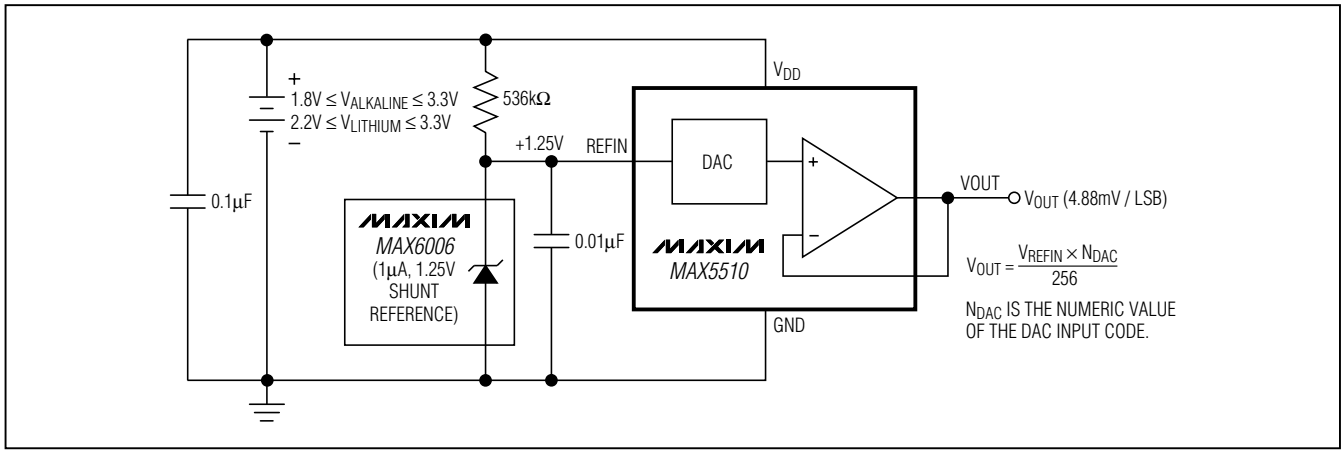



*Figure 3. Portable Application Using Two Alkaline Cells or One Lithium Coin Cell*

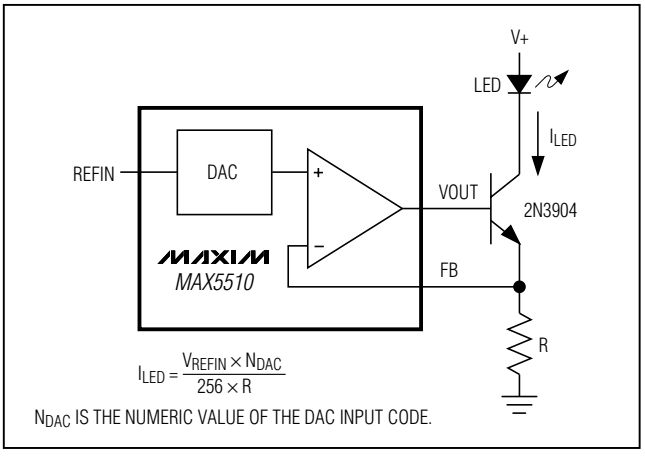



*Figure 4. Programmable Current Source Driving an LED*

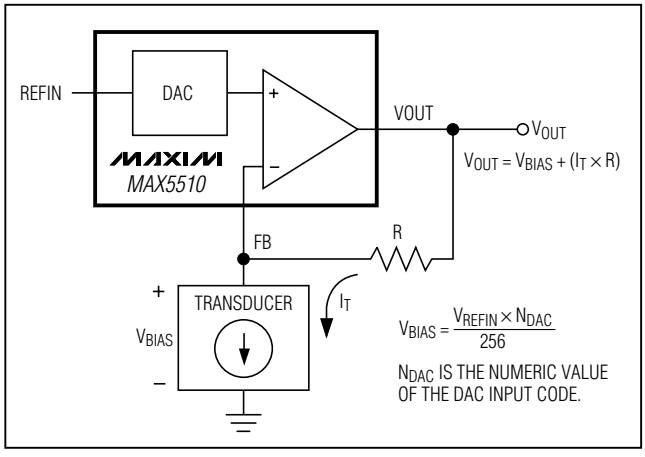



*Figure 5. Transimpedance Configuration for a Voltage-Biased Current-Output Transducer*

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

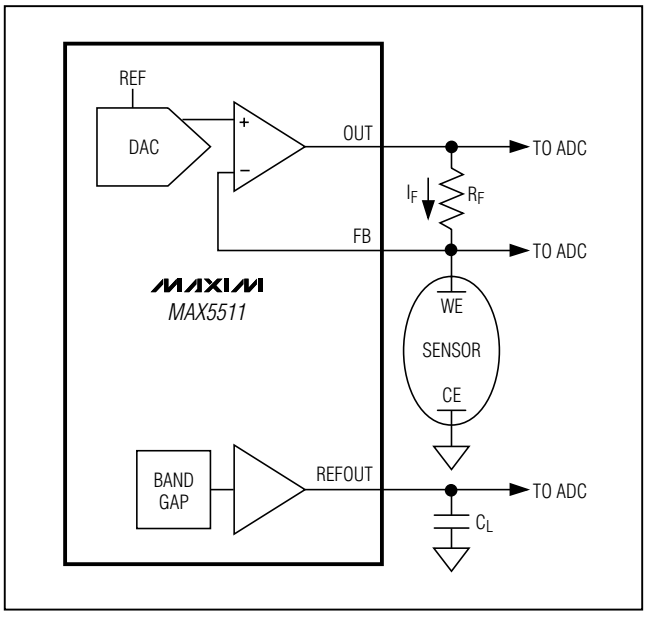



*Figure 6. Self-Biased Two-Electrode Potentiostat Application*

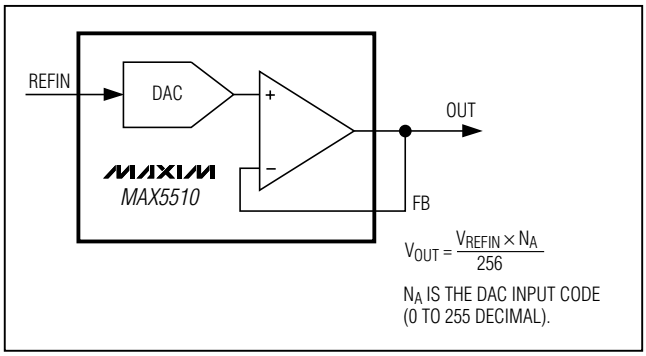



*Figure 7. Unipolar Output Circuit*

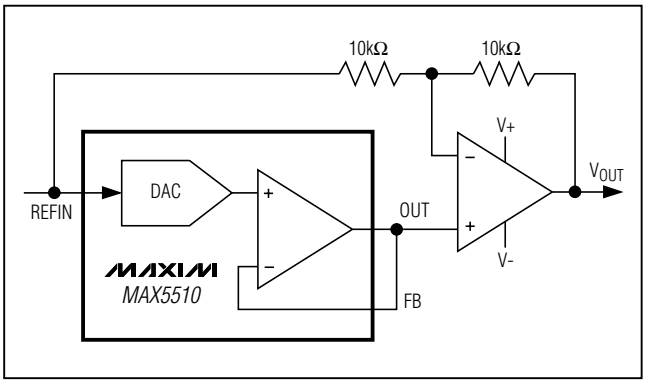



*Figure 8. Bipolar Output Circuit*

### Unipolar Output

Figure 7 shows the MAX5510 in a unipolar output configuration with unity gain. Table 4 lists the unipolar output codes.

### Bipolar Output

The MAX5510 output can be configured for bipolar operation, as shown in Figure 8. The output voltage is given by the following equation:

$$V_{OUT} = V_{REF} \times [(N_A - 128) / 128]$$

where NA represents the numeric value of the DAC's binary input code. Table 5 shows digital codes (offset binary) and the corresponding output voltage for the circuit in Figure 4.

### Configurable Output Gain

The MAX5510/MAX5511 have a force-sense output, which provides a connection directly to the inverting terminal of the output op amp, yielding the most flexibility. The advantage of the force-sense output is that specific gains can be set externally for a given application. The gain error for the MAX5510/MAX5511 is specified in a unity-gain configuration (op-amp output and inverting terminals connected), and additional gain error results from external resistor tolerances. Another advantage of the force-sense DAC is that it allows many useful circuits to be created with only a few simple external components.

## Table 4. Unipolar Code Table (Gain = +1)

| DAC CONTENTS MSB | | LSB | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 0000 | $+V_{REF}$ (255/256) |
| 1000 | 0001 | 0000 | $+V_{REF}$ (129/256) |
| 1000 | 0000 | 0000 | $+V_{REF}$ (128/256) = $+V_{REF}/2$ |
| 0111 | 1111 | 0000 | $+V_{REF}$ (127/256) |
| 0000 | 0001 | 0000 | $+V_{REF}$ (1/256) |
| 0000 | 0000 | 0000 | 0V |

## Table 5. Bipolar Code Table (Gain = +1)

| DAC CONTENTS MSB | | LSB | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 0000 | $+V_{REF}$ (127/128) |
| 1000 | 0001 | 0000 | $+V_{REF}$ (1/128) |
| 1000 | 0000 | 0000 | 0V |
| 0111 | 1111 | 0000 | $-V_{REF}$ (1/128) |
| 0000 | 0001 | 0000 | $-V_{REF}$ (127/128) |
| 0000 | 0000 | 0000 | $-V_{REF}$ (128/128) = $-V_{REF}$ |

An example of a custom fixed gain using the force-sense output of the MAX5510/MAX5511 is shown in Figure 9. In this example R1 and R2 set the gain for $V_{OUT}$.

$$V_{OUT} = [(V_{REFIN} \times N_A) / 256] \times [1 + (R2 / R1)]$$

where $N_A$ represents the numeric value of the DAC input code.

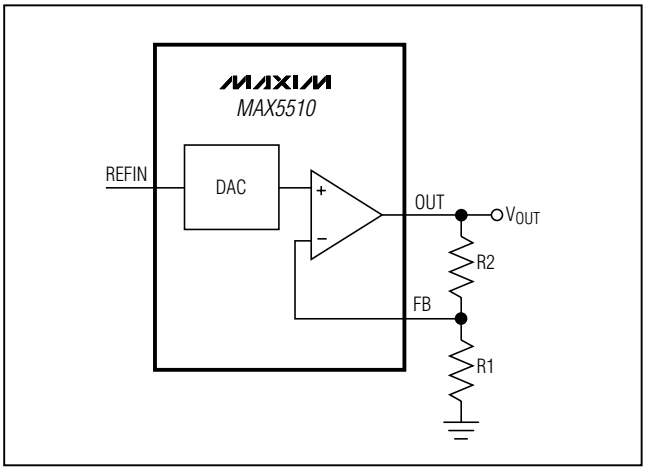



*Figure 9. Separate Force-Sense Outputs Create Unity and Greater-than-Unity DAC Gains Using the Same Reference*

### Power Supply and Bypassing Considerations

Bypass the power supply with a 0.1µF capacitor to GND. Minimize lengths to reduce lead inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation. For the thin QFN package, connect the exposed paddle to ground.

## Layout Considerations

Digital and AC transient signals coupling to GND can create noise at the output. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use printed circuit (PC) boards. Good PC board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines.

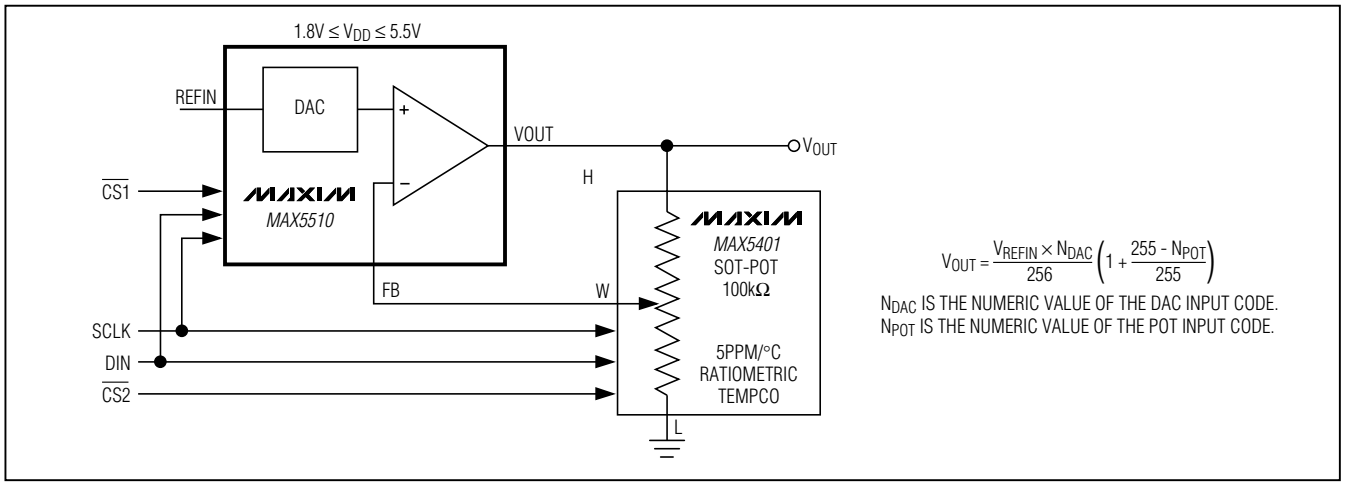



*Figure 10. Software-Configurable Output Gain*

## Revision History

Pages changed at Rev 1: 1, 13, 17, 18

## Chip Information

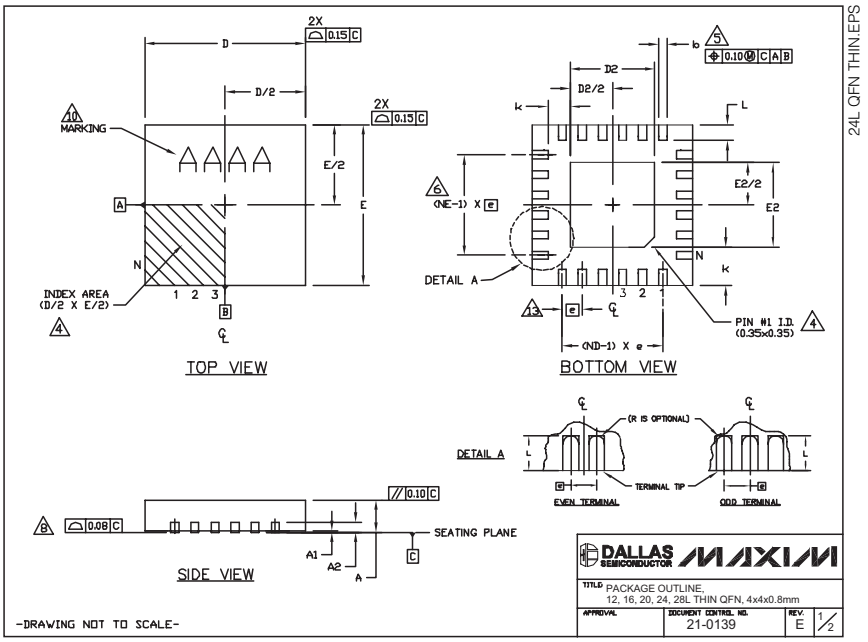
TRANSISTOR COUNT: 10,688

PROCESS: BiCMOS

# +1.8V to +5.5V, Ultra-Low-Power, 8-Bit, Voltage-Output DACs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)




**COMMON DIMENSIONS**

| PKG | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | | 28L 4x4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | | 28 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| JEDEC VAR. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | | WGGE | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | D2 | | | E2 | | | DOWN BONDS ALLOWED |
|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| T1244-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1244-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T1644-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1644-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2044-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2044-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2444-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2444-3 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | YES |
| T2444-4 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | NO |
| T2844-1 | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 | NO |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. E
2/2

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