MAX5723/MAX5724/ MAX5725

Ultra-Small, Octal-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

General Description

The MAX5723/MAX5724/MAX5725 8-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal 3ppm/°C reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5723/MAX5724/MAX5725 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (6mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100kΩ (typ) load to an external reference.

The MAX5723/MAX5724/MAX5725 have a fast 50MHz, 4-wire SPI/QSPI™/MICROWIRE/DSP-compatible serial interface that operates at clock rates up to 50MHz. The DAC output is buffered and has a low supply current of less than 250µA per channel and a low offset error of ±0.5mV (typ). On power-up, the MAX5723/MAX5724/MAX5725 reset the DAC outputs to zero or midscale based on the status of M/$\overline{Z}$ logic input, providing flexibility for a variety of control applications. The internal reference is initially powered down to allow use of an external reference. The MAX5723/MAX5724/MAX5725 allow simultaneous output updates using software LOAD commands or the hardware load DAC logic input ($\overline{LDAC}$).

The MAX5723/MAX5724/MAX5725 feature a programmable watchdog function which can be enabled to monitor the I/O interface for activity and integrity.

A clear logic input ($\overline{CLR}$) allows the contents of the CODE and the DAC registers to be cleared asynchronously and simultaneously sets the DAC outputs to the programmable default value. The MAX5723/MAX5724/MAX5725 are available in a 20-pin TSSOP and an ultra-small, 20-bump WLP package and are specified over the -40°C to +125°C temperature range.

Applications

Programmable Voltage and Current Sources

Gain and Offset Adjustment

Automatic Tuning and Optical Control

Power Amplifier Control and Biasing

Process Control and Servo Loops

Portable Instrumentation

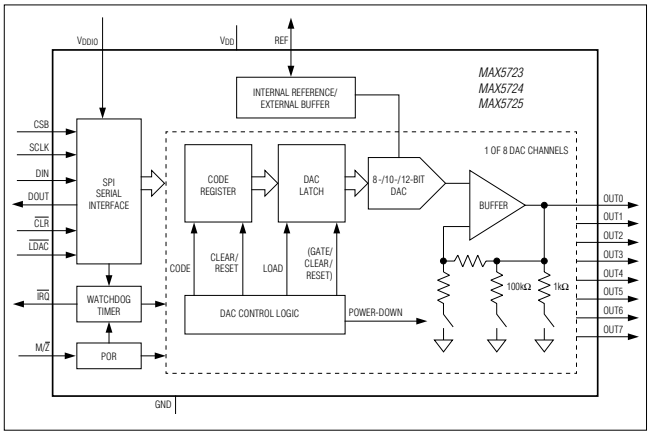
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Benefits and Features

- Eight High-Accuracy DAC Channels
  - 12-Bit Accuracy Without Adjustment
  - ±1 LSB INL Buffered Voltage Output
  - Guaranteed Monotonic Over All Operating Conditions
  - Independent Mode Settings for Each DAC
- Three Precision Selectable Internal References
  - 2.048V, 2.500V, or 4.096V
- Internal Output Buffer
  - Rail-to-Rail Operation with External Reference
  - 4.5µs Settling Time
  - Outputs Directly Drive 2kΩ Loads
- Small 6.5mm x 4.4mm 20-Pin TSSOP or Ultra-Small 2.5mm x 2.3mm 20-Bump WLP Package
- Wide 2.7V to 5.5V Supply Range
- Separate 1.8V to 5.5V V_{DDIO} Power-Supply Input
- Fast 50MHz 4-Wire SPI/QSPI/MICROWIRE/DSP-Compatible Serial Interface
- Programmable Interface Watchdog Timer
- Pin-Selectable Power-On-Reset to Zero-Scale or Midscale DAC Output
- $\overline{LDAC}$ and $\overline{CLR}$ for Asynchronous DAC Control
- Three Selectable Power-Down Output Impedances
  - 1kΩ, 100kΩ, or High Impedance

Functional Diagram



***Ordering Information* appears at end of data sheet.**

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Absolute Maximum Ratings

V_{DD}, V_{DDIO} to GND .....-0.3V to +6V
OUT_, REF to GND .....0.3V to the lower of (V_{DD} + 0.3V) and +6V
SCLK, CSB, $\overline{IRQ}$, M/$\overline{Z}$, $\overline{LDAC}$, $\overline{CLR}$ to GND.....-0.3V to +6V
DIN, DOUT to GND.....-0.3V to the lower of (V_{DDIO} + 0.3V) and +6V
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate at 13.6mW/°C above 70°C).....1084mW
WLP (derate at 21.3mW/°C above 70°C).....1700mW
Maximum Continuous Current into Any Pin ..... ±50mA
Operating Temperature..... -40°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (TSSOP only) (soldering, 10s).....+300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....73.8°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....20°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 2) .....47°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.
Note 2: Visit **www.maximintegrated.com/app-notes/index.mvp/id/1891** for information about the thermal performance of WLP packaging.

Electrical Characteristics

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (Note 4)						
Resolution and Monotonicity	N	MAX5723	8			Bits
		MAX5724	10			
		MAX5725	12			
Integral Nonlinearity (Note 5)	INL	MAX5723	-0.25	±0.05	+0.25	LSB
		MAX5724	-0.5	±0.2	+0.5	
		MAX5725	-1	±0.5	+1	
Differential Nonlinearity (Note 5)	DNL	MAX5723	-0.25	±0.05	+0.25	LSB
		MAX5724	-0.5	±0.1	+0.5	
		MAX5725	-1	±0.2	+1	
Offset Error (Note 6)	OE		-5	±0.5	+5	mV
Offset Error Drift				±10		µV/°C
Gain Error (Note 6)	GE		-1.0	±0.1	+1.0	%FS
Gain Temperature Coefficient		With respect to V_{REF}		±3.0		ppm of FS/°C

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Zero-Scale Error				0		+10	mV
Full-Scale Error		With respect to V_{REF}		-0.5		+0.5	%FS
DAC OUTPUT CHARACTERISTICS							
Output Voltage Range (Note 7)		No load		0		V_{DD}	V
		2kΩ load to GND		0		V_{DD} - 0.2	
		2kΩ load to V_{DD}		0.2		V_{DD}	
Load Regulation		V_{OUT} = V_{FS}/2	V_{DD} = 3V ±10%, $\|I_{OUT}\| \le$ 5mA		300		µV/mA
			V_{DD} = 5V ±10%, $\|I_{OUT}\| \le$ 10mA		300		
DC Output Impedance		V_{OUT} = V_{FS}/2	V_{DD} = 3V ±10%, $\|I_{OUT}\| \le$ 5mA		0.3		Ω
			V_{DD} = 5V ±10%, $\|I_{OUT}\| \le$ 10mA		0.3		
Maximum Capacitive Load Handling	C_L				500		pF
Resistive Load Handling	R_L			2			kΩ
Short-Circuit Output Current		V_{DD} = 5.5V	Sourcing (output shorted to GND)		30		mA
			Sinking (output shorted to V_{DD})		50		
DC Power-Supply Rejection		V_{DD} = 3V ±10% or 5V ±10%			100		µV/V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	Positive and negative			1.0		V/µs
Voltage-Output Settling Time		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5723			2.2		µs
		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5724			2.6		
		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5725			4.5		
DAC Glitch Impulse		Major code transition (code x7FF to x800)			7		nV*s
Channel-to-Channel Feedthrough (Note 8)		Internal reference			3.3		nV*s
		External reference			4.07		
Digital Feedthrough		Midscale code, all digital inputs from 0V to V_{DDIO}			0.2		nV*s
Power-Up Time		Startup calibration time (Note 9)			200		µs
		From power-down			50		µs

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage-Noise Density (DAC Output at Midscale)		External reference	f = 1kHz		90		nV/√Hz
			f = 10kHz		82		
		2.048V internal reference	f = 1kHz		112		
			f = 10kHz		102		
		2.5V internal reference	f = 1kHz		125		
			f = 10kHz		110		
		4.096V internal reference	f = 1kHz		160		
			f = 10kHz		145		
Integrated Output Noise (DAC Output at Midscale)		External reference	f = 0.1Hz to 10Hz		12		μV_{P-P}
			f = 0.1Hz to 10kHz		76		
			f = 0.1Hz to 300kHz		385		
		2.048V internal reference	f = 0.1Hz to 10Hz		14		
			f = 0.1Hz to 10kHz		91		
			f = 0.1Hz to 300kHz		450		
		2.5V internal reference	f = 0.1Hz to 10Hz		15		
			f = 0.1Hz to 10kHz		99		
			f = 0.1Hz to 300kHz		470		
		4.096V internal reference	f = 0.1Hz to 10Hz		16		
			f = 0.1Hz to 10kHz		124		
			f = 0.1Hz to 300kHz		490		
Output Voltage-Noise Density (DAC Output at Full Scale)		External reference	f = 1kHz		114		nV/√Hz
			f = 10kHz		99		
		2.048V internal reference	f = 1kHz		175		
			f = 10kHz		153		
		2.5V internal reference	f = 1kHz		200		
			f = 10kHz		174		
		4.096V internal reference	f = 1kHz		295		
			f = 10kHz		255		
Integrated Output Noise (DAC Output at Full Scale)		External reference	f = 0.1Hz to 10Hz		13		μV_{P-P}
			f = 0.1Hz to 10kHz		94		
			f = 0.1Hz to 300kHz		540		
		2.048V internal reference	f = 0.1Hz to 10Hz		19		
			f = 0.1Hz to 10kHz		143		
			f = 0.1Hz to 300kHz		685		
		2.5V internal reference	f = 0.1Hz to 10Hz		21		
			f = 0.1Hz to 10kHz		159		
			f = 0.1Hz to 300kHz		705		
		4.096V internal reference	f = 0.1Hz to 10Hz		26		
			f = 0.1Hz to 10kHz		213		
			f = 0.1Hz to 300kHz		750		

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Reference Input Range	V_{REF}			1.24		V_{DD}	V
Reference Input Current	I_{REF}	V_{REF} = V_{DD} = 5.5V			55	74	µA
Reference Input Impedance	R_{REF}			75	100		kΩ
REFERENCE OUTPUT							
Reference Output Voltage	V_{REF}	V_{REF} = 2.048V, T_A = +25°C		2.043	2.048	2.053	V
		V_{REF} = 2.5V, T_A = +25°C		2.494	2.500	2.506	
		V_{REF} = 4.096V, T_A = +25°C		4.086	4.096	4.106	
Reference Temperature Coefficient (Note 10)		MAX5725A			±3	±10	ppm/°C
		MAX5723/MAX5724/MAX5725B			±10	±25	
Reference Drive Capacity		External load			25		kΩ
Reference Capacitive Load Handling					200		pF
Reference Load Regulation		I_{SOURCE} = 0 to 500µA			2		mV/mA
Reference Line Regulation					0.05		mV/V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	V_{REF} = 4.096V		4.5		5.5	V
		All other options		2.7		5.5	
I/O Supply Voltage	V_{DDIO}			1.8		5.5	V
Supply Current (Note 11)	I_{DD}	Internal reference	V_{REF} = 2.048V		1.6	2	mA
			V_{REF} = 2.5V		1.7	2.1	
			V_{REF} = 4.096V		2.0	2.5	
		External reference	V_{REF} = 3V		1.6	2.0	
			V_{REF} = 5V		1.9	2.5	
Power-Down Mode Supply Current	I_{PD}	All DACs off, internal reference ON			140		µA
		All DACs off, internal reference OFF, T_A = -40°C to +85°C			0.7	2	
		All DACs off, internal reference OFF, T_A = +125°C			2	4	
Digital Supply Current	I_{DDIO}	Static logic inputs, all outputs unloaded				1	µA
DIGITAL INPUT CHARACTERISTICS (SCLK, DIN, CSB, $\overline{LDAC}$, $\overline{CLR}$, M/$\overline{Z}$)							
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DDIO}, all inputs except M/$\overline{Z}$ (Note 11)			±0.1	±1	µA
		V_{IN} = 0V or V_{DD}, for M/$\overline{Z}$ (Note 11)					

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}	(All inputs except M/$\overline{Z}$)	2.2V < V_{DDIO} < 5.5V	0.7 x V_{DDIO}			V
			1.8V < V_{DDIO} < 2.2V	0.8 x V_{DDIO}			V
		2.7V < V_{DD} < 5.5V (for M/$\overline{Z}$)		0.7 x V_{DD}			
Input Low Voltage	V_{IL}	(All inputs except M/$\overline{Z}$)	2.2V < V_{DDIO} < 5.5V			0.3 x V_{DDIO}	V
			1.8V < V_{DDIO} < 2.2V			0.2 x V_{DDIO}	V
		2.7V < V_{DD} < 5.5V (for M/$\overline{Z}$)				0.3 x V_{DD}	
Input Capacitance (Note 10)	C_{IN}					10	pF
Hysteresis Voltage	V_H				0.15		V
DIGITAL OUTPUT ($\overline{IRQ}$)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.2	V
Output Inactive Leakage	I_{OFF}				±0.1	±1	µA
Output Inactive Capacitance (Note 10)	C_{OFF}					10	pF
DIGITAL OUTPUT (DOUT)							
Output High Voltage	V_{OH}	V_{DDIO} > 2.5V, I_{SOURCE} = 3mA		V_{DDIO} - 0.2			V
		V_{DDIO} > 1.8V, I_{SOURCE} = 2mA		V_{DDIO} - 0.2			
Output Low Voltage	V_{OL}	V_{DDIO} > 2.5V, I_{SINK} = 3mA				0.2	V
		V_{DDIO} > 1.8V, I_{SINK} = 2mA				0.2	
Output Short-Circuit Current	I_{OSS}	I_{SINK}, I_{SOURCE}			±100		mA
Output Three-State Leakage	I_{OZ}				±0.1	±1	µA
Output Three-State Capacitance	C_{OZ}				10		pF
WATCHDOG TIMER CHARACTERISTICS							
Watchdog Timer Period	t_{WDOSC}	V_{DD} = 3V, T_A = +25°C		0.95	1	1.05	ms
Watchdog Timer Period Supply Drift		V_{DD} = 2.7V to 5.5V, T_A = +25°C			0.6		%/V
Watchdog Timer Period Temperature Drift		V_{DD} = 3V			0.0375		%/°C

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SPI TIMING CHARACTERISTICS							
SCLK Frequency	f_{SCLK}	2.7V < V_{DDIO} < 5.5V	Write mode	0		50	MHz
			Read mode, strobing on 1 SCLK	0		25	
			Read mode, strobing on ½ SCLK	0		12.5	
		1.8V < V_{DDIO} < 2.7V	Write mode	0		33	
			Read mode, strobing on 1 SCLK	0		20	
			Read mode, strobing on ½ SCLK	0		10	
SCLK Period	t_{SCLK}	2.7V < V_{DDIO} < 5.5V, write mode		20			ns
		1.8V < V_{DDIO} < 2.7V, write mode		30			
SCLK Pulse Width High	t_{CH}			8			ns
SCLK Pulse Width Low	t_{CL}			8			ns
CSB Fall to SCLK Fall Setup Time	t_{CSS0}	To first SCLK falling edge	2.7V < V_{DDIO} < 5.5V	8			ns
			1.8V < V_{DDIO} < 2.7V	12			
CSB Fall to SCLK Fall Hold Time	t_{CSH0}	Applies to inactive SCLK falling edge preceding the first SCLK falling edge		0			ns
CSB Rise to SCLK Fall Hold Time	t_{CSH1}	Applies to the 24th SCLK falling edge		0			ns
CSB Rise to SCLK Fall	t_{CSA}	Applies to the 24th SCLK falling edge, aborted sequence		12			ns
SCLK Fall to CSB Fall	t_{CSF}	Applies to 24th SCLK falling edge		100			ns
CSB Pulse Width High	t_{CSPW}			20			ns
DIN to SCLK Fall Setup Time	t_{DS}			5			ns
DIN to SCLK Fall Hold Time	t_{DH}			4.5			ns
$\overline{CLR}$ Pulse Width Low	t_{CLPW}			20			ns
$\overline{CLR}$ Rise to CSB Fall	t_{CSC}	Required for command to be executed		20			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDPW}			20			ns
$\overline{LDAC}$ Fall to SCLK Fall Hold	t_{LDH}	Applies to 24th SCLK falling edge		20			ns
SCLK Fall to DOUT Transition	t_{DOT}	DPHA = 0, C_{LOAD} = 20pF	2.7V < V_{DDIO} < 5.5V			35	ns
			1.8V < V_{DDIO} < 2.7V			40	
SCLK Rise to DOUT Transition	t_{DOT}	DPHA = 1, C_{LOAD} = 20pF	2.7V < V_{DDIO} < 5.5V			35	ns
			1.8V < V_{DDIO} < 2.7V			40	

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 5.5V, V_{DDIO} = 1.8V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Fall to DOUT Hold	t_{DOH}	DPHA = 0, C_{LOAD} = 0pF		2			ns
SCLK Rise to DOUT Hold	t_{DOH}	DPHA = 1, C_{LOAD} = 0pF		2			ns
CSB Fall to DOUT Fall	t_{DOE}	Enable time, C_{LOAD} = 20pF				20	ns
CSB Rise to DOUT Hi-Z	t_{DOZ}	Disable time	2.7V < V_{DDIO} < 5.5V			20	ns
			1.8V < V_{DDIO} < 2.7V			40	

Note 3: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at T_A = +25°C.

Note 4: DC performance is tested without load, V_{REF} = V_{DD}.

Note 5: Linearity is tested with unloaded outputs to within 20mV of GND and V_{DD}.

Note 6: Gain and offset calculated from measurements made with V_{REF} = V_{DD} at codes 30 and 4065 for MAX5725, codes 8 and 1016 for MAX5724, and codes 2 and 254 for MAX5723.

Note 7: Subject to zero- and full-scale error limits and V_{REF} settings.

Note 8: Measured with all other DAC outputs at midscale with one channel transitioning 0 to full scale.

Note 9: On power-up, the device initiates an internal 200µs (typ) calibration sequence. All commands issued during this time will be ignored.

Note 10: Guaranteed by design.

Note 11: All channels active at V_{FS}, unloaded. Static logic inputs with V_{IL} = V_{GND} and V_{IH} = V_{DDIO} for all inputs.

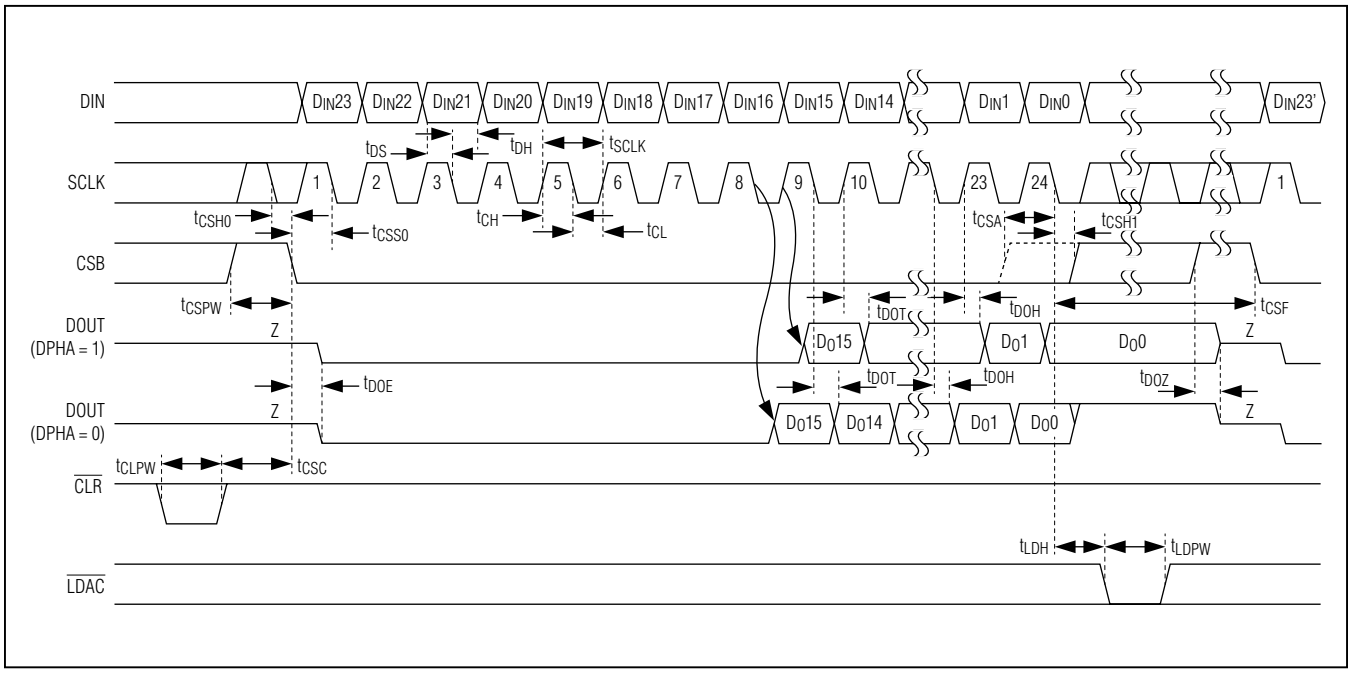
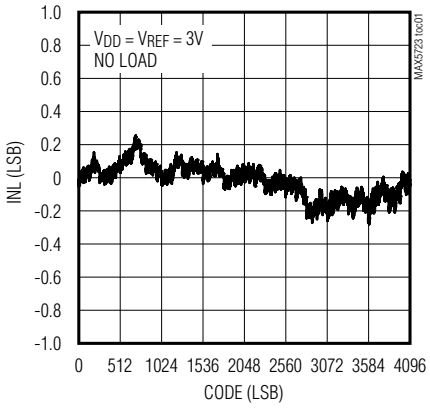


Figure 1. SPI Serial Interface Timing Diagram

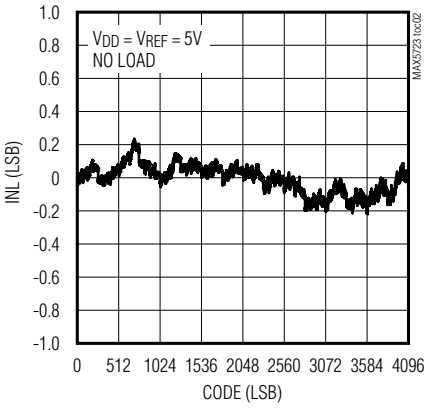
Typical Operating Characteristics

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

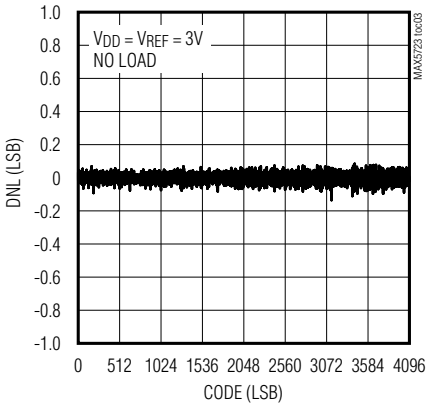
INL vs. CODE



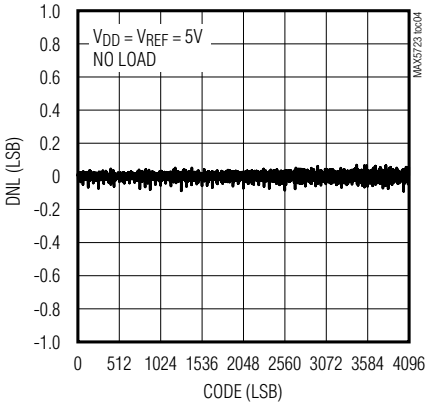
INL vs. CODE



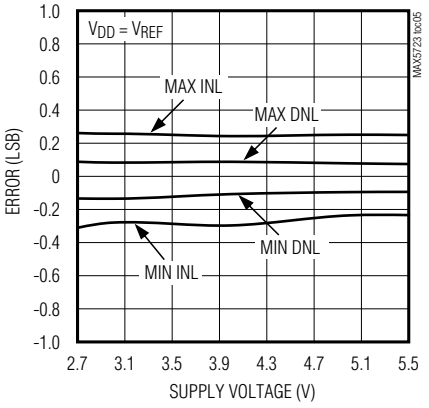
DNL vs. CODE



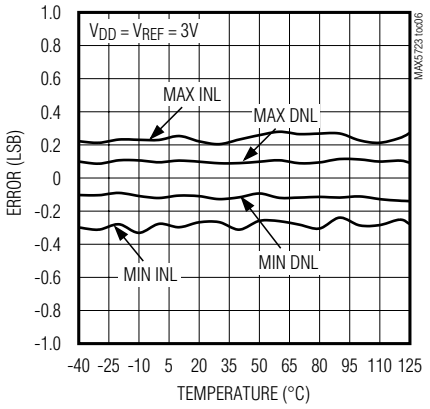
DNL vs. CODE



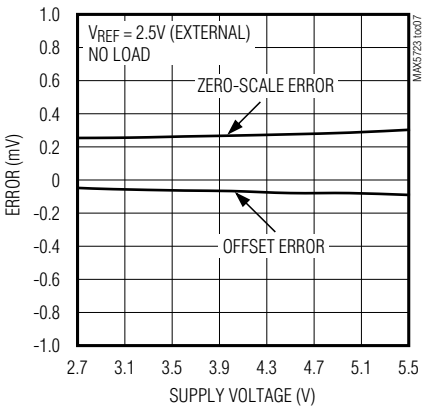
INL AND DNL vs. SUPPLY VOLTAGE



INL AND DNL vs. TEMPERATURE



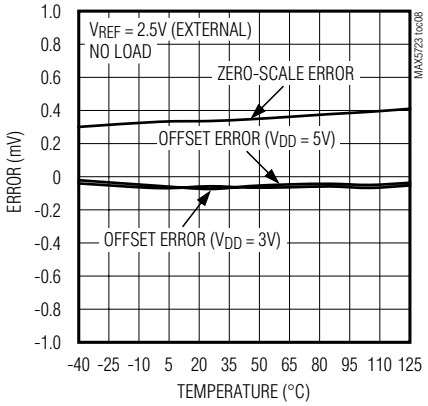
OFFSET AND ZERO-SCALE ERROR vs. SUPPLY VOLTAGE



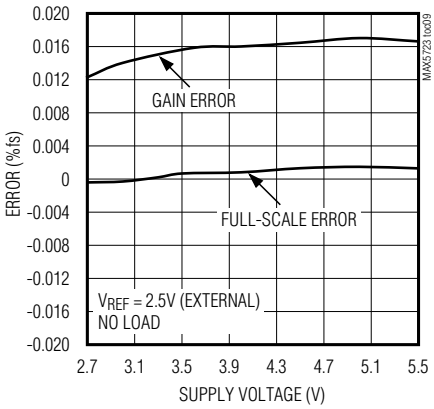
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

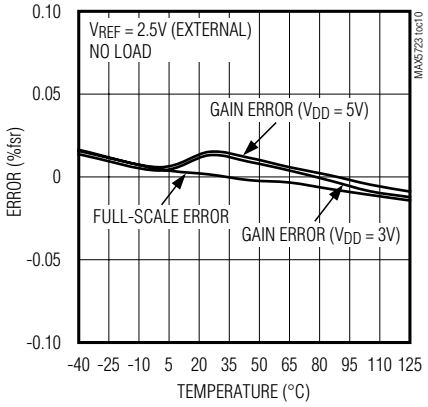
OFFSET AND ZERO-SCALE ERROR vs. TEMPERATURE



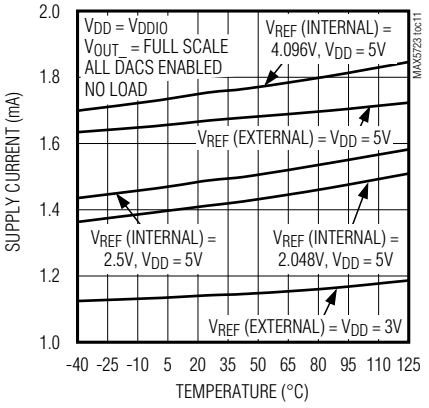
FULL-SCALE ERROR AND GAIN ERROR vs. SUPPLY VOLTAGE



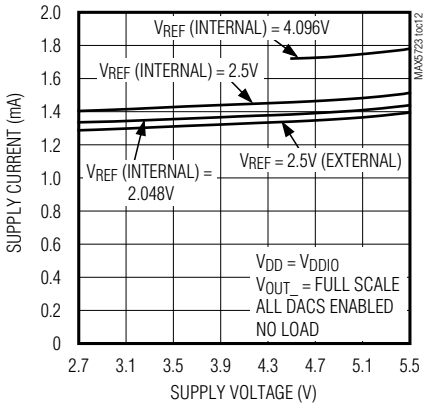
FULL-SCALE ERROR AND GAIN ERROR vs. TEMPERATURE



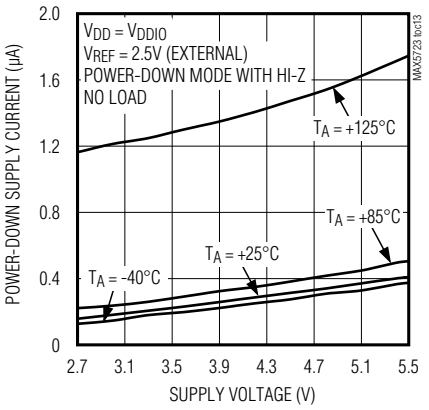
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



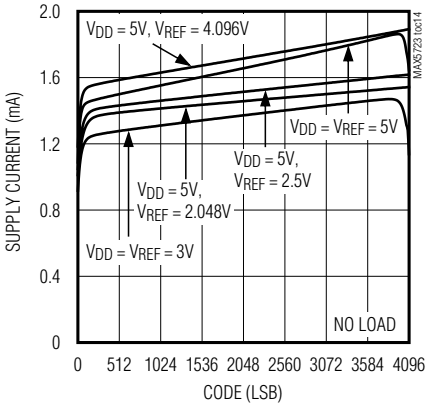
POWER-DOWN MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



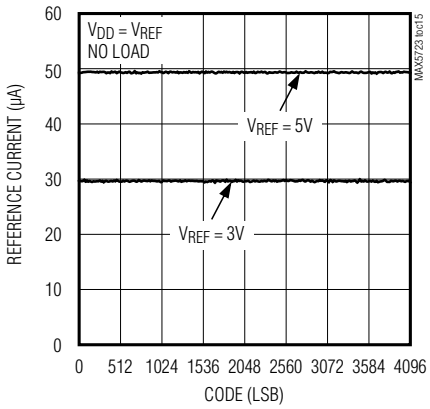
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

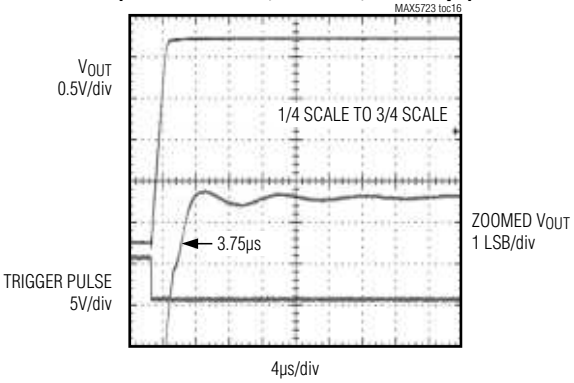
IVDD vs. CODE



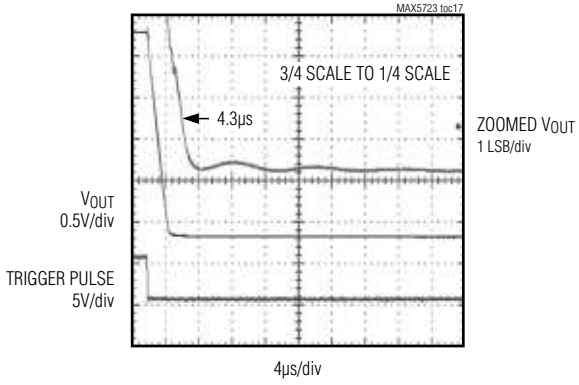
IREF (EXTERNAL) vs. CODE



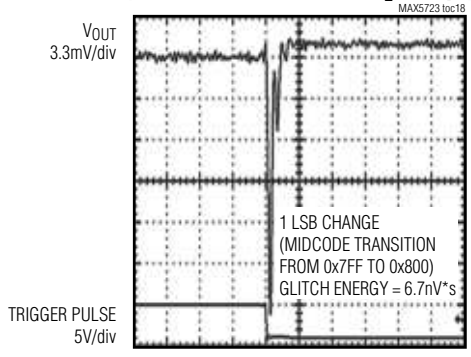
SETTLING TO ±1 LSB
(VDD = VREF = 5V, RL = 2kΩ, CL = 200pF)



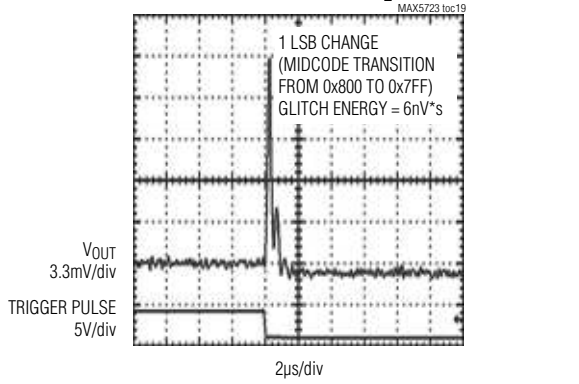
SETTLING TO ±1 LSB
(VDD = VREF = 5V, RL = 2kΩ, CL = 200pF)



MAJOR CODE TRANSITION GLITCH ENERGY
(VDD = VREF = 5V, RL = 2kΩ, CL = 200pF)



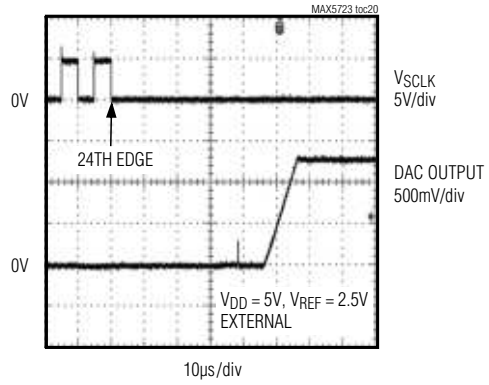
MAJOR CODE TRANSITION GLITCH ENERGY
(VDD = VREF = 5V, RL = 2kΩ, CL = 200pF)



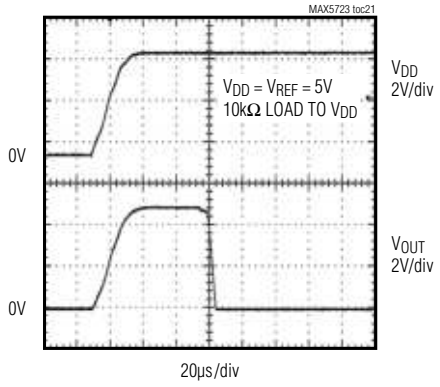
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

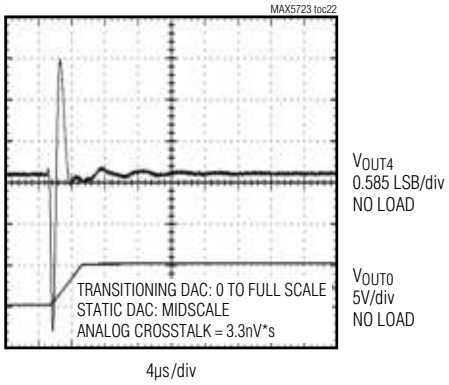
V_{OUT} vs. TIME TRANSIENT EXITING POWER-DOWN



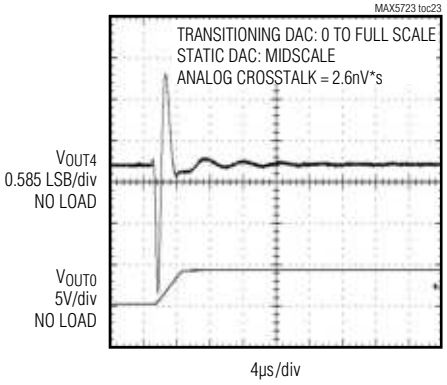
POWER-ON RESET TO 0V



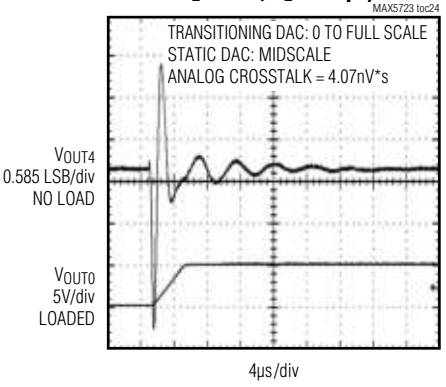
CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = V_{REF} = 5V, T_A = +25°C, NO LOAD)



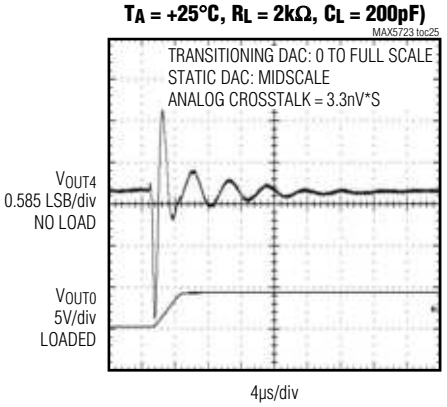
CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = 5V, V_{REF} = 4.096V, T_A = +25°C, NO LOAD)



CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = V_{REF} = 5V, T_A = +25°C, R_L = 2kΩ, C_L = 200pF)



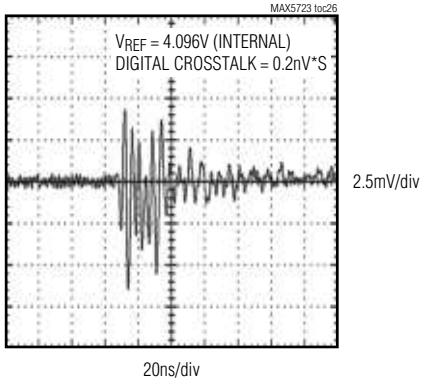
CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = 5V, V_{REF} = 4.096V (INTERNAL), T_A = +25°C, R_L = 2kΩ, C_L = 200pF)



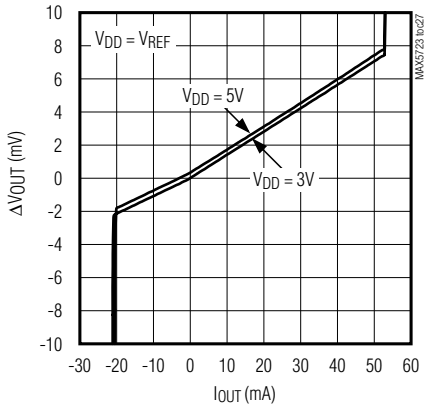
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

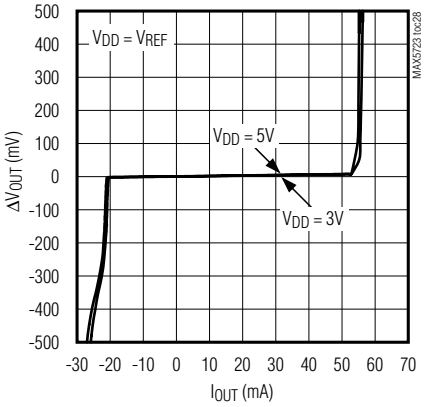
DIGITAL FEEDTHROUGH
(V_{DD} = V_{REF} = 5V, R_L = 10kΩ)



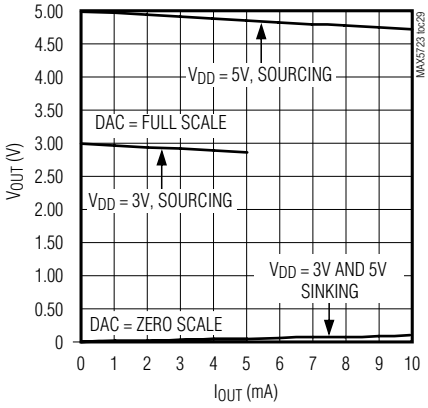
OUTPUT LOAD REGULATION



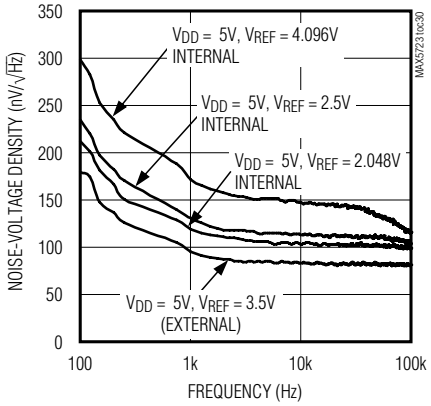
OUTPUT CURRENT LIMITING



HEADROOM AT RAILS
vs. OUTPUT CURRENT (V_{DD} = V_{REF})



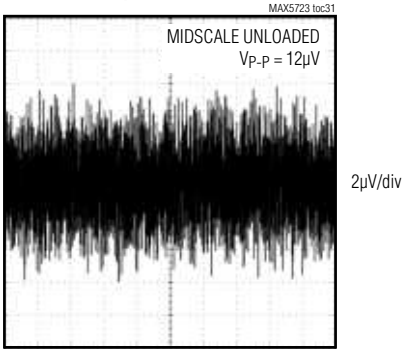
NOISE-VOLTAGE DENSITY vs. FREQUENCY
(DAC AT MIDSCALE)



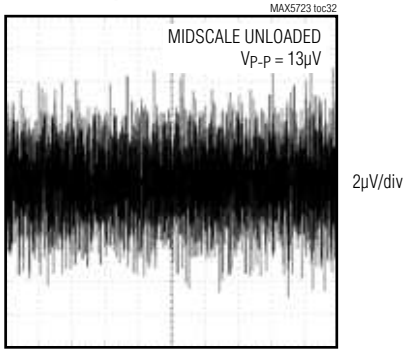
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

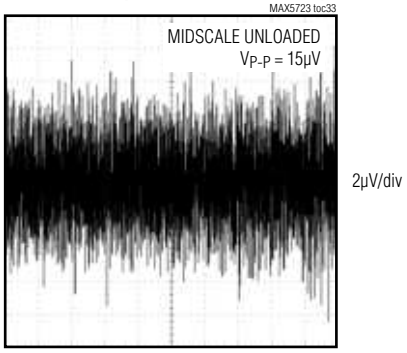
0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 4.5V)



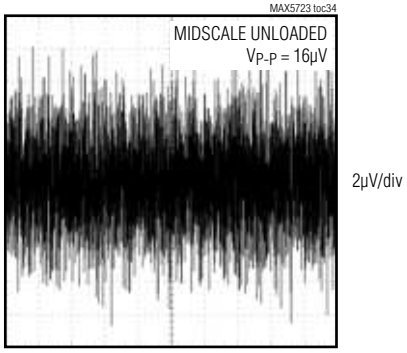
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 2.048V)



0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 2.5V)



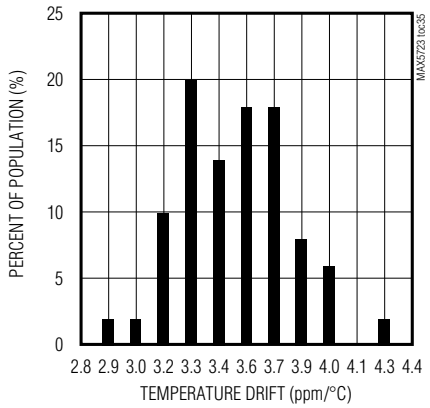
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 4.096V)



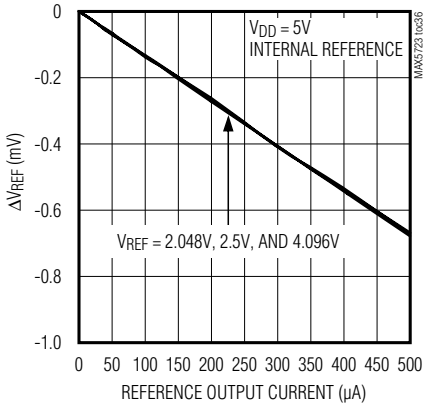
Typical Operating Characteristics (continued)

(MAX5725, 12-bit performance, T_A = +25°C, unless otherwise noted.)

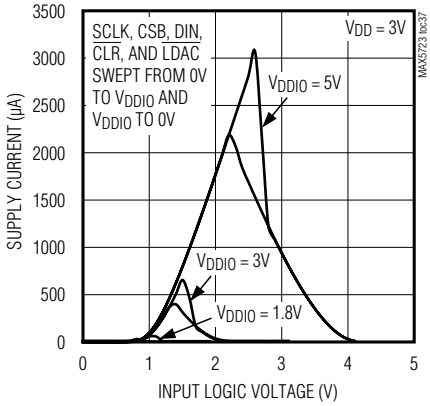
VREF DRIFT vs. TEMPERATURE



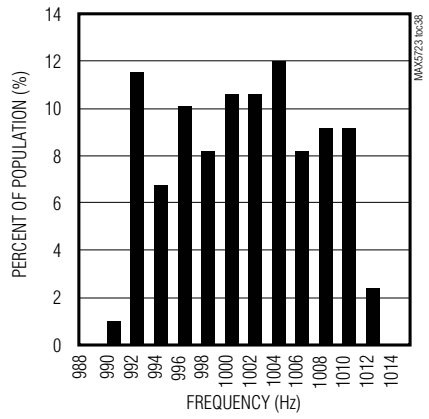
REFERENCE LOAD REGULATION



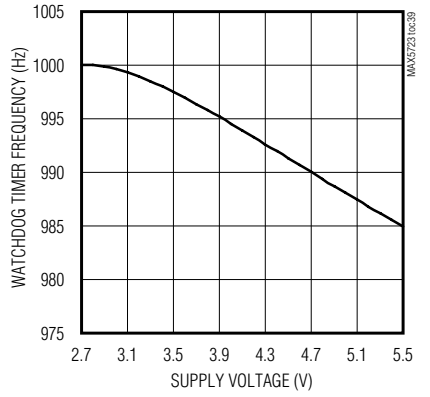
SUPPLY CURRENT vs. SUPPLY VOLTAGE



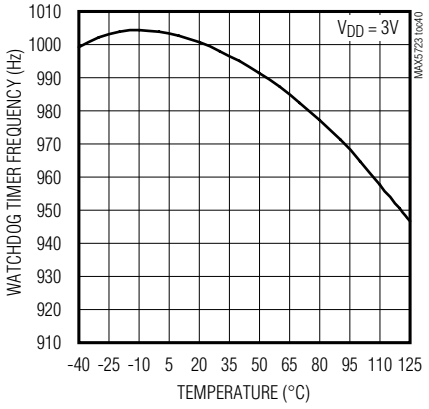
WATCHDOG TIMER PERIOD HISTOGRAM



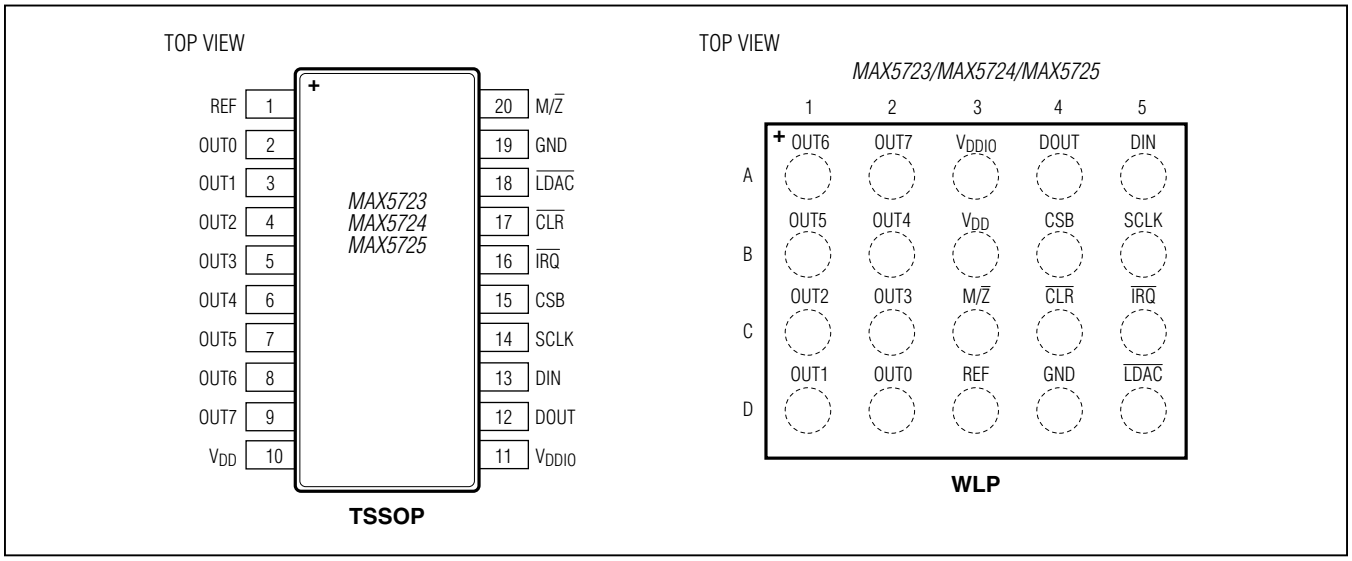
WATCHDOG TIMER FREQUENCY vs. SUPPLY VOLTAGE



WATCHDOG TIMER FREQUENCY vs. TEMPERATURE



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TSSOP	WLP		
1	D3	REF	Reference Voltage Input/Output
2	D2	DAC0	DAC Channel 0 Voltage Output
3	D1	OUT1	DAC Channel 1 Voltage Output
4	C1	OUT2	DAC Channel 2 Voltage Output
5	C2	OUT3	DAC Channel 3 Voltage Output
6	B2	OUT4	DAC Channel 4 Voltage Output
7	B1	OUT5	DAC Channel 5 Voltage Output
8	A1	OUT6	DAC Channel 6 Voltage Output
9	A2	OUT7	DAC Channel 7 Voltage Output
10	B3	V_{DD}	Analog Supply Voltage
11	A3	V_{DDIO}	Digital Supply Voltage
12	A4	DOUT	SPI Serial Data Output
13	A5	DIN	SPI Serial Data Input
14	B5	SCLK	SPI Serial Clock Input
15	B4	CSB	SPI Chip-Select Input
16	C5	$\overline{IRQ}$	Active-Low Open Drain Interrupt Output. $\overline{IRQ}$ low indicates watchdog timeout.
17	C4	$\overline{CLR}$	Active-Low Asynchronous DAC Clear Input
18	D5	$\overline{LDAC}$	Active-Low Asynchronous DAC Load Input
19	D4	GND	Ground
20	C3	M/$\overline{Z}$	DAC Output Reset Selection. Connect M/$\overline{Z}$ to GND for zero-scale and connect M/$\overline{Z}$ to V_{DD} for midscale.

Detailed Description

The MAX5723/MAX5724/MAX5725 are 8-channel, low-power, 8-/10-/12-bit buffered voltage-output DACs. The 2.7V to 5.5V wide supply voltage range and low-power consumption accommodates most low-power and low-voltage applications. The devices present a 100kΩ load to the external reference. The internal output buffers allow rail-to-rail operation. An internal voltage reference is available with software-selectable options of 2.048V, 2.500V, or 4.096V. The devices feature a fast 4-wire SPI/QSPI/MICROWIRE/DSP-compatible serial interface to save board space and reduce the complexity in isolated applications interface. The MAX5723/MAX5724/MAX5725 include a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC outputs to zero scale (M/$\overline{Z}$ = 0) or midscale (M/$\overline{Z}$ = 1), and control logic.

$\overline{CLR}$ is available to asynchronously clear the DAC outputs to a user-programmable default value, independent of the serial interface. $\overline{LDAC}$ is available to simultaneously update selected DACs on one or more devices. The MAX5723/MAX5724/MAX5725 also feature user-configurable interface watchdog, with status indicated by the $\overline{IRQ}$ output.

DAC Outputs (OUT_)

The MAX5723/MAX5724/MAX5725 include internal buffers on all DAC outputs, which provide improved load regulation for the DAC outputs. The output buffers slew at 1V/µs (typ) and drive resistive loads are as low as 2kΩ in parallel with as much as 500pF of capacitance. The analog supply voltage (V_{DD}) determines the maximum output voltage range of the devices since it powers the output buffers. Under no-load conditions, the output buffers drive from GND to V_{DD}, subject to offset and gain errors. With a 2kΩ load to GND, the output buffers drive from GND to within 200mV of V_{DD}. With a 2kΩ load to V_{DD}, the output buffers drive from V_{DD} to within 200mV of GND.

The DAC ideal output voltage is defined by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N}$$

where D = code loaded into the DAC register, V_{REF} = reference voltage, N = resolution.

Internal Register Structure

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers, individual, or multiple DACs as determined by the user command.

Within each DAC channel there is a CODE register followed by a DAC latch register (see the *Detailed Functional Diagram*). The contents of the CODE register hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE_LOAD commands or can upload the current contents of the CODE register using LOAD commands or the $\overline{LDAC}$ logic input.

The contents of both CODE and DAC registers are maintained during power-down states, so that when the DACs are powered on, they return to their previously stored output settings. Any CODE or LOAD commands issued during power-down states continue to update the register contents.

Once the device is powered up, each DAC channel can be independently programmed with a desired RETURN value using the RETURN command. This becomes the value the CODE and DAC registers will use in the event of any watchdog, clear or gate activity, as selected by the DEFAULT command.

Hardware $\overline{CLR}$ operations and SW_CLEAR commands return the contents of all CODE and DAC registers to their user-selected defaults. SW_RESET commands will reset CODE and DAC register contents to their M/$\overline{Z}$ selected initial codes. A SW_GATE state can be used to momentarily hold selected DAC outputs in their DEFAULT positions. The contents of CODE and DAC registers can be manipulated by watchdog timer activity, enabling a variety of safety features.

Internal Reference

The MAX5723/MAX5724/MAX5725 include an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF output for other external circuitry (see the *Typical Operating Circuits*) and can drive loads down to 25kΩ.

External Reference

The external reference input has a typical input impedance of 100kΩ and accepts an input voltage from +1.24V to V_{DD}. Apply an external voltage between REF and GND to use an external reference. The MAX5723/MAX5724/MAX5725 power up and reset to external reference mode. Visit www.maximintegrated.com/products/references for a list of available external voltage-reference devices.

M/$\overline{Z}$ Input

The MAX5723/MAX5724/MAX5725 feature a pin-selectable DAC reset state using the M/$\overline{Z}$ input. Upon a power-on reset, all CODE and DAC data registers are reset to zero scale (M/$\overline{Z}$ = GND) or midscale (M/$\overline{Z}$ = V_{DD}). M/$\overline{Z}$ is referenced to V_{DD} (not V_{DDIO}). In addition, M/$\overline{Z}$ must be valid at the time the device is powered up—connect M/$\overline{Z}$ directly to V_{DD} or GND.

Load DAC ($\overline{LDAC}$) Input

The MAX5723/MAX5724/MAX5725 feature an active-low asynchronous $\overline{LDAC}$ logic input that allows DAC outputs to update simultaneously. Connect $\overline{LDAC}$ to V_{DDIO} or keep $\overline{LDAC}$ high during normal operation when the device is controlled only through the serial interface. Drive $\overline{LDAC}$ low to update the DAC outputs with data from the CODE registers. Holding $\overline{LDAC}$ low causes the DAC registers to become transparent and CODE data is passed through to the DAC registers immediately updating the DAC outputs. A software CONFIG command can be used to configure the $\overline{LDAC}$ operation of each DAC independently.

Clear ($\overline{CLR}$) Input

The MAX5723/MAX5724/MAX5725 feature an asynchronous active-low $\overline{CLR}$ logic input that simultaneously sets all selected DAC outputs to their programmable DEFAULT states. Driving $\overline{CLR}$ low clears the contents of both the CODE and DAC registers and also ignores any on-going SPI command which modifies registers associated with a DAC configured to accept clear operations. To allow a new SPI command, drive $\overline{CLR}$ high, satisfying the t_{CSC} timing requirement. A software CONFIG command can be used to configure the clear operation of each DAC independently.

Watchdog Feature

The MAX5723/MAX5724/MAX5725 feature an interface watchdog timer with programmable timeout duration. This monitors the I/O interface for activity and integrity. If the watchdog is enabled, the host processor must write a valid command to the device within the timeout period to prevent a timeout. If the watchdog is allowed to timeout, selected DAC outputs are returned to the programmable DEFAULT state, protecting the system against control faults.

By default, all watchdog features are disabled; users wishing to activate any watchdog feature must configure the device accordingly. Individual DAC channels can be configured using the CONFIG command to accept the watchdog alarm and to gate, clear, or hold their outputs in response to an alarm. A watchdog refresh event and watchdog behavior upon timeout is defined by a programmable safety level using the WDOG_CONFIG command.

$\overline{IRQ}$ Output

The MAX5723/MAX5724/MAX5725 feature an active-low open-drain interrupt output indicating to the host when a watchdog timeout has occurred.

Interface Power Supply (V_{DDIO})

The MAX5723/MAX5724/MAX5725 feature a separate supply input (V_{DDIO}) for the digital interface (1.8V to 5.5V). Connect V_{DDIO} to the I/O supply of the host processor.

SPI Serial Interface

The MAX5723/MAX5724/MAX5725 4-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSPs. The interface provides three inputs, SCLK, CSB, and DIN. The chip-select input (CSB, active-low) frames the data loaded through the serial data input (DIN). Following a CSB input high-to-low transition, the data is shifted in synchronously and latched into the input register on each falling edge of the serial clock input (SCLK). Each serial operation word is 24-bits long. The DAC data is left justified as shown in Table 1. The serial

Table 1. Format DAC Data Bit Positions

PART	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MAX5723	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X	X
MAX5724	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X
MAX5725	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

input register transfers its contents to the destination registers after loading 24 bits of data on the 24th SCLK falling edge. To initiate a new SPI operation, drive CSB high and then low to begin the next operation sequence, being sure to meet all relevant timing requirements. During CSB high periods, SCLK is ignored, allowing communication to other devices on the same bus. SPI operations consisting of more than 24 SCLK cycles are executed on the 24th SCLK falling edge, using the first three bytes of data available. SPI operations consisting of less than 24 SCLK cycles will not be executed. The content of the SPI operation consists of a command byte followed by a two-byte data word.

The DOUT phase for all SPI_READ commands is determined by the readback command used, allowing the selection of the SCLK DOUT update edge best suited to the digital I/O implementation, maximizing data transfer speed and/or timing margin.

Guaranteed non-zero DOUT hold times allow the microprocessor to strobe DOUT on the same edge as the MAX5723/MAX5724/MAX5725 updates for fastest SPI read mode transfers. For example, if DPHA = 0 is used, the MAX5723/MAX5724/MAX5725 update DOUT in response to SCLK falling edges 8-23, while a microprocessor (µP) with low data hold time requirements can strobe in the DOUT data on SCLK falling edges 9-24. The device supports readback speeds of up to 25MHz for a microprocessor with 5ns data input setup requirements and allowing 35ns for t_{DOT} at V_{DDIO} > 2.7V.

Variable DOUT phase also supports microprocessors with longer data input hold time requirements. For example, if DPHA = 1 is used, the MAX5723/MAX5724/MAX5725 updates DOUT in response to SCLK rising edges 9-24 while the microprocessor can strobe in the DOUT data on SCLK falling edges 9-24. The device supports readback speeds up to 12.5MHz for a µP with 5ns data input setup requirements and allowing 35ns for t_{DOT} (assuming 50% duty cycle SCLK).

For improved readback speed while monitoring device status, the SPI_READ_STATUS command repeats the device status information for multiple bits, allowing polling of the device at maximum interface speeds (up to 50MHz when the readback strobe is placed away from DOUT transition edges). This transfer speed cannot be achieved for other forms of readback using the SPI_READ_DATA command, where more DOUT bus transitions occur.

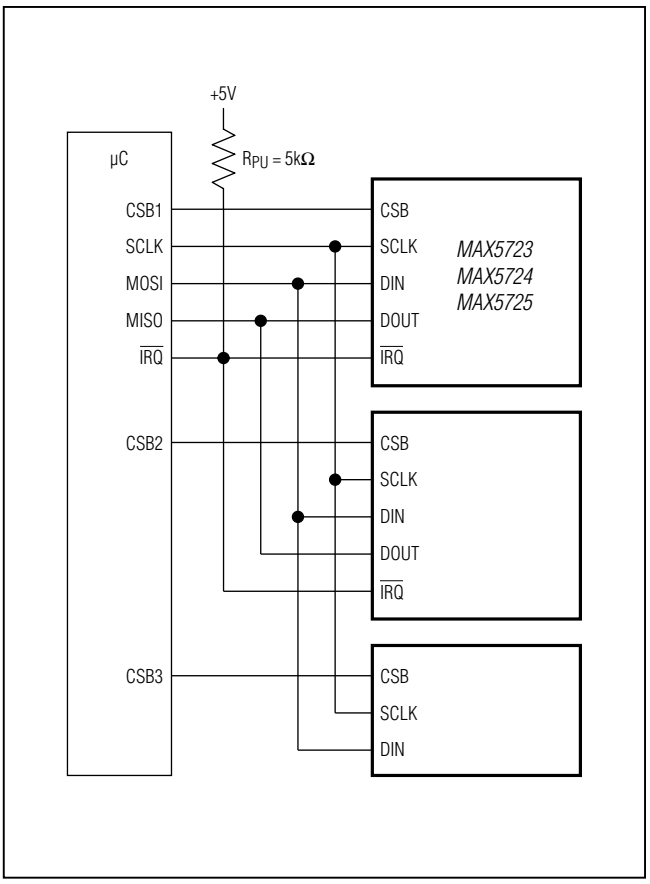


Figure 2. Typical SPI Application Circuit

Figure 1 shows the timing diagram for the complete 4-wire serial interface transmission. The DAC code settings (D) for the MAX5723/MAX5724/MAX5725 are accepted in an offset binary format (see Table 1). Otherwise, the expected data format for each command is listed in Table 2. See Figure 2 for an example of a typical SPI circuit application.

SPI User-Command Register Map

This section lists the user-accessible commands and registers for the MAX5723/MAX5724/MAX5725.

Table 2 provides detailed information about the Command Registers.

Table 2. SPI Commands Summary

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
CONFIGURATION AND SOFTWARE COMMANDS									TIMEOUT SELECTION[11:4]								TIMEOUT SELECTION[3:0]				WD_MASK	Safety Level 00: Low 01: Med 10: High 11: Max		X	
WDOG	0	0	0	1	X	X	X	X																	Updates watchdog settings and safety levels
REF	0	0	1	0	0	REF Power 0= DAC 1=ON	REF Mode 00 = EXT 01 = 2.5V 10 = 2.0V 11 = 4.1V		X															X	Sets the reference operating mode. REF Power (B18): 0 = Internal reference is only powered if at least one DAC is powered 1 = Internal reference is always powered
SW_GATE_CLR	0	0	1	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Removes any existing GATE condition
SW_GATE_SET	0	0	1	1	0	0	0	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Initiates a GATE condition
WD_REFRESH	0	0	1	1	0	0	1	0	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Refreshes the watchdog timer
WD_RESET	0	0	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Reset the watchdog time out alarm status and refreshes the watchdog timer
SW_CLEAR	0	0	1	1	0	1	0	0	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Executes a software clear (all CODE and DAC registers cleared to their DEFAULT values)
SW_RESET	0	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	Executes a software reset (all CODE, DAC, and control registers returned to their power-on reset values)
CONFIG	0	1	0	1	0	0	0	0	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	WDOG Config. 00: DIS 01: GATE 10: CLR 11: HOLD			GATE_ENB	LDAC_ENB	CLEAR_ENB	X	X	Configures selected DAC Watchdog, GATE, LOAD, and CLEAR operations. DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted)

Table 2. SPI Commands Summary (continued)

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
POWER	0	1	0	0	0	0	0	0	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	Power Mode 00 = Normal 01 = PD1kΩ 10 = PD 100kΩ 11 = PD Hi-Z		X	X	X	X	X	X	Sets the Power Mode of the selected DACs (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted)
DEFAULT	0	1	1	0	0	0	0	0	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	Default Values: 000: MZ 001: ZERO 010: MID 011: FULL 100: RETURN 101+: No Effect								Sets the DEFAULT code settings for selected DACs. Note, DACs in RETURN mode programmable RETURN codes. (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted)
DAC COMMANDS																									
RETURNn	0	1	1	1	DAC Selection				RETURN REGISTER DATA[11:4]								RETURN REGISTER DATA[3:0]			X	X	X	X	Writes data to the selected RETURN register(s)
CODEn	1	0	0	0	DAC Selection				CODE REGISTER DATA[11:4]								CODE REGISTER DATA[3:0]			X	X	X	X	Writes data to the selected CODE register(s)
LOADn	1	0	0	1	DAC Selection				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Transfers data from the selected CODE registers to the selected DAC register(s)
CODEn_ LOAD_ALL	1	0	1	0	DAC Selection				CODE REGISTER DATA[11:4]								CODE REGISTER DATA[3:0]			X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating all DAC registers
CODEn_ LOADn	1	0	1	1	DAC Selection				CODE REGISTER DATA[11:4]								CODE REGISTER DATA[3:0]			X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s)
CODE_ALL	1	1	0	0	0	0	0	0	CODE REGISTER DATA[11:4]								CODE REGISTER DATA[3:0]			X	X	X	X	Writes data to all CODE registers

Table 2. SPI Commands Summary (continued)

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
LOAD_ALL	1	1	0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Updates all DAC latches with current CODE register data
CODE_ALL LOAD_ALL	1	1	0	0	0	0	1	0	CODE REGISTER DATA[11:4]								CODE REGISTER DATA[3:0]				X	X	X	X	Simultaneously writes data to the all CODE registers while updating all DAC registers
RETURN_ALL	1	1	0	0	0	0	1	1	RETURN REGISTER DATA[11:4]								RETURN REGISTER DATA[3:0]				X	X	X	X	Writes data to all RETURN registers
SPI_DATA_ REQUEST	1	1	0	1	DAC Selection				INC	DATA SEL [1:0] 00 = DAC 01 = CODE 10 = RET 11 = WDT			X	X	X	X	X	X	X	X	X	X	X	X	Setup data request for readback. INC indicates if the DAC selection is incremented to the next DAC after each SPI_READ _DATA operation DATA SEL[1:0] indicates the data content to be read back
SPI_READ STATUS	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPHA = 0 Readback status
	1	1	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPHA = 1 Readback status
SPI_READ DATA	1	1	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPHA = 0 Readback requested data
	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPHA = 1 Readback requested data
NO OPERATION COMMANDS																									
No Operation	1	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	These commands will have no effect on the device, but will refresh the watchdog timer if safety level is set to low.
	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Reserved Commands: Any commands not specifically listed above are reserved for Maxim internal use only.

RETURNn Command

The RETURN command (B[23:20] = 0111) sets the programmable default RETURN value. This value is used for all future watchdog, clear, and gate operations when RET is selected for the DAC using the DEFAULT command. Issuing this command with DAC_ADDRESS set to all DACs will program the value for all RETURN registers and is equivalent to RETURN_ALL. **Note:** This command is inaccessible when a watchdog timeout has occurred if the watchdog timer is configured for safety level = high or max.

CODEn Command

The CODEn command (B[23:20] = 1000) updates the CODE register contents for the selected DAC(s). Changes to the CODE register content based on this command will not affect DAC outputs directly unless the $\overline{LDAC}$ input is in a low state or the DAC latch has been configured as transparent using the CONFIG command. Issuing this command with DAC_ADDRESS set to all DACs will program the value for all CODE registers and is equivalent to CODE_ALL.

LOADn Command

The LOADn command (B[23:20] = 1001) updates the DAC register content for the selected DAC(s) by uploading the current contents of the selected CODE register(s) into the selected DAC register(s). Channels for which CODE content has not been modified since the last LOAD or $\overline{LDAC}$ operation will not be updated to reduce digital crosstalk. Issuing this command with DAC_ADDRESS set to all DACs will update the contents of all DAC registers and is equivalent to LOAD_ALL.

CODEn_LOADn Command

The CODEn_LOADn command (B[23:20] = 1011) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of the selected DAC(s). Channels for which CODE content has not been modified since the last LOAD or $\overline{LDAC}$ operation will not be updated to reduce digital crosstalk. Issuing this command with DAC_ADDRESS set to all DACs is equivalent to the CODE_ALL_LOAD_ALL (B[23:16] = 1100_0010) command.

CODEn_LOAD_ALL Command

The CODEn_LOAD_ALL command (B[23:20] = 1010) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of all DACs. Channels for which CODE content has not been modified since the last LOAD or $\overline{LDAC}$ operation will not be updated to reduce digital crosstalk. Issuing this command with DAC_ADDRESS set to all DACs will update the CODE and DAC register contents of all DACs and is equivalent to CODE_ALL_LOAD_ALL. Note this command by definition will modify at least one CODE register; to avoid this use the LOAD command with DAC_ADDRESS set to all DACs or the LOAD_ALL command.

Table 3. DAC Selection

B19	B18	B17	B16	DAC SELECTED
0	0	0	0	DAC0
0	0	0	1	DAC1
0	0	1	0	DAC2
0	0	1	1	DAC3
0	1	0	0	DAC4
0	1	0	1	DAC5
0	1	1	0	DAC6
0	1	1	1	DAC7
1	X	X	X	ALL DACs

CODE_ALL Command

The CODE_ALL command (B[23:16] = 1100_0000) updates the CODE register contents for all DACs.

LOAD_ALL Command

The LOAD_ALL command (B[23:16] = 1100_0001) updates the DAC register content for all DACs by uploading the current contents of the CODE registers to the DAC registers.

CODE_ALL_LOAD_ALL Command

The CODE_ALL_LOAD_ALL command (B[23:16] = 1100_0010) updates the CODE register contents for all DACs as well as the DAC register content of all DACs.

RETURN_ALL Command

The RETURN_ALL command (B[23:16] = 1100_0011) updates the RETURN register contents for all DACs.

NO_OP Commands Command

All unused commands in the space (B[23:16] = 1100_01XX or 1100_1XXX) have no effect on the device, but will refresh the watchdog timer (if active) with the safety level set to low.

WDOG Command

The WDOG command (B[23:20] = 0001) updates the watchdog timeout settings and safety levels for the device. Timeout thresholds are selected in 1ms increments (1ms to 4095ms are available). The WD_MASK bit can be used to mask the $\overline{IRQ}$ operation in response to the watchdog status, if WD_MASK = 1, watchdog alarms will not assert $\overline{IRQ}$. The watchdog alarm status (WD bit) can be polled using the available SPI status readback commands regardless of WD_MASK settings. A write to this register will not reset a previously triggered watchdog alarm (use the WD_RESET command for this purpose). The watchdog timer refresh and timeout behavior is defined by the programmable safety level below.

Available safety levels (WL[1:0]):

Low (00): Watchdog timer will refresh with the execution of any valid user mode command or no-op. Any successful slave address acknowledge qualifies to restart the watchdog timer (run to the ninth SCL edge), regardless of the command which follows. Issuing hardware $\overline{CLR}$ or $\overline{LDAC}$ falling edge will also refresh the watchdog timer. A triggered watchdog alarm does not prevent writes to any register. $\overline{LDAC}$ and $\overline{CLR}$ inputs still function after a watchdog timeout event.

Medium (01): A WD_REFRESH command must be executed in order to refresh the watchdog timer. Other commands as well as $\overline{LDAC}$ or $\overline{CLR}$ activity do not refresh the watchdog timer. A triggered watchdog alarm does not prevent writes to any register. $\overline{LDAC}$ and $\overline{CLR}$ inputs still function after a watchdog timeout event.

High (10): A WD_REFRESH command must be executed to refresh the watchdog timer. Other commands as well as $\overline{LDAC}$ or $\overline{CLR}$ activity do not refresh the watchdog timer. A triggered watchdog alarm prevents execution of all POWER, REF, CONFIG, DEFAULT, and RETURN commands. $\overline{LDAC}$ and $\overline{CLR}$ inputs still function after a watchdog timeout event.

Max (11): A WD_REFRESH command must be executed to refresh the watchdog timer. Other commands, as well as $\overline{LDAC}$ or $\overline{CLR}$ activity, do not refresh the watchdog timer. A triggered watchdog alarm prevents execution of all POWER, REF, CONFIG, DEFAULT, and RETURN commands. $\overline{LDAC}$ and $\overline{CLR}$ are gated and do not function after a watchdog timeout event.

Table 4. WDOG Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	X	X	X	X	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	WDM	WL1	WL0	X
WDOG Command				Don't Care				Timeout Selection								Timeout Selection				WD_MASK	WDOG Safety Level: 00: Low 01: Med 10: High 11: Max		Don't Care
Default Value →								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X
Command Byte								Data High Byte								Data Low Byte							

Table 5. Watchdog Safety Level Protection

WATCHDOG SAFETY LEVEL	ANY COMMAND REFRESHES WDT	$\overline{CLR}$/$\overline{LDAC}$ REFRESHES WDT	SW_RESET PLUS WD_RFRS REFRESHES WDT	ALL REGISTERS ACCESSIBLE AFTER WDT TIMEOUT*	$\overline{CLR}$/$\overline{LDAC}$ AFFECT DAC REGISTERS AFTER WDT TIMEOUT*
00 (Low)	X	X	X	X	X
01 (Med)	—	—	X	X	X
10 (High)	—	—	X	—	X
11 (Max)	—	—	X	—	—

**Unless otherwise affected by Watchdog HOLD or $\overline{CLR}$ configurations as set by the CONFIG command. See the CONFIG register definition for details.*

REF Command

The REF command (B[23:20] = 0010) updates the global reference setting used for all DAC channels. If an internal reference mode is selected, bit RF2 (B18) defines the reference power mode. If RF2 is set to zero (default), the reference will be powered down any time all DAC channels are powered down (i.e. the device is in STANDBY mode). If RF2 is set to one, the reference will remain powered even if all DAC channels are powered down, allowing continued operation of external circuitry (note in this mode the low current shutdown state is not available). This command is inaccessible when a watchdog timeout has occurred and the watchdog timer is configured with a safety level of high or max.

SW_GATE_CLR Command

The SW_GATE_CLR command (B[23:0] = 0011_0000_1001_0110_0011_0000) will remove any existing GATE condition initiated by a previous SW_GATE_SET comand.

SW_GATE_SET Command

The SW_GATE_SET command (B[23:0] = 0011_0001_1001_0110_0011_0000) will initiate a GATE condition. Any DACs configured with GTB = 0 (see the *CONFIG Command* section) will have their outputs held at the selected DEFAULT value until the GATE condition is later removed by a subsequent SW_GATE_CLR command. While in gate mode, the CODE and DAC registers continue to function normally and are not reset (unless reset by a watchdog timeout).

WD_REFRESH Command

The WD_REFRESH command (B[23:0] = 0011_0010_1001_0110_0011_0000) will refresh the watchdog timer. This is the only command which will refresh the watchdog timer if the device is configured with a safety level of medium, high, or max. Use this command to prevent the watchdog timer from timing out.

WD_RESET Command

A WD_RESET command (B[23:0] = 0011_0011_1001_0110_0011_0000) will reset the watchdog interrupt (timeout) status and refresh the watchdog timer. Use this command to reset the $\overline{IRQ}$ timeout condition after the watchdog timer has timed out. Any DACs impacted by an existing timeout condition will return to normal operation.

SW_CLEAR Command

A software clear command (B[23:0] = 0011_0100_001_0110_0011_0000) will clear the contents of the CODE and DAC registers to the DEFAULT state for all channels configured with CLB = 0 (see CONFIG command).

SW_RESET Command

A software reset command (B[23:0] = 0011_0101_1001_0110_0011_0000) will reset all CODE, DAC, and configuration registers to their defaults (including POWER, DEFAULT, CONFIG, WDOG, and REF registers), simulating a power-on reset.

Table 6. REF Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	0	RF2	RF1	RF0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
REF Command				Reserved	0 = DAC Controlled 1 = Always ON	REF Mode: 00: EXT 01: 2.5V 10: 2.0V 11: 4.0V		Don't Care								Don't Care							
Default Value →					0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

POWER Command

The POWER command (B[23:20] = 0100) updates the power mode settings of the selected DACs. DACs that are not selected do not update their power settings in response to the command. The new power setting is determined by bits PD[1:0] (B[7:6]) while the affected DAC(s) are selected using B[15:8]). If all DACs are powered down and the RF2 bit is not set, the device enters a STANDBY mode (all analog circuitry is disabled). This command is inaccessible when a watchdog timeout has occurred and the watchdog timer is configured with a safety level of high or max.

Available power modes (PD[1:0]):

Normal (00): DAC channel is active (default).

PD 1kΩ (01): Power down with 1kΩ termination to GND.

PD 100kΩ (10): Power down with 100kΩ termination to GND.

PD Hi-Z (11): Power down with high-impedance output.

Table 7. POWER Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	0	0	7	6	5	4	3	2	1	0	PD1	PD0	X	X	X	X	X	X
POWER Command				Reserved				Multiple DAC Selection								Power Mode: 00 = Normal 01 = 1kΩ 10 = 100kΩ 11 = Hi-Z		Don't Care					
Default Value →								1	1	1	1	1	1	1	1	0	0	X	X	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

CONFIG Command

The CONFIG command (B[23:16] = 0101) updates the watchdog, gate, load, and clear mode settings of the selected DACs. DACs which are not selected do not update their settings in response to the command. The new mode settings to be written are determined by bits B[7:3] while the affected DAC(s) are selected by B[15:8]. This command is inaccessible when a watchdog timeout has occurred and the watchdog timer is configured with a safety level of high or max.

Watchdog Configuration:

WDOG Config settings are written by WC[1:0] (B[7:6]):

DISABLE (WC = 00): Watchdog timeout does not affect the operation of the selected DAC.

GATE (WC = 01): DAC code is gated to DEFAULT value in response to watchdog timeouts. Unless otherwise prohibited by the watchdog safety level, $\overline{LDAC}$, $\overline{CLR}$, and write operations to the CODE and DAC registers are accepted but will not be reflected on the DAC output until the watchdog timeout status is reset.

$\overline{CLR}$ (WC = 10): CODE and DAC register contents are cleared to DEFAULT value in response to watchdog timeouts. All writes to CODE and DAC registers are ignored and $\overline{LDAC}$ or $\overline{CLR}$ input activity has no effect until the watchdog timeout status is reset, regardless of watchdog safety level.

HOLD (WC = 11): DAC code is held at its previously programmed value in response to watchdog timeout. All writes to DAC and CODE registers are ignored and $\overline{LDAC}$ or $\overline{CLR}$ input activity has no effect until the watchdog timeout status is reset, regardless of watchdog safety level.

Note: For the watchdog to timeout and have an impact, the function must first be enabled and configured using the WDOG command.

Gate Configuration:

The DAC GATE setting is written by GTB (B5); GATE operation is as follows:

GTB = 0: Enables software gating function (default), DAC outputs are gated to their DEFAULT settings as long as the device remains in GATE mode (set by SW_GATE_SET and removed by SW_GATE_CLR).

GTB = 1: Disable software gating function, DAC outputs are not impacted by GATE mode.

Load Configuration:

The LDAC_ENB setting is written by LDB (B4); LDAC_ENB operation is as follows:

LDB = 0: DAC latch is operational, enabling $\overline{\text{LDAC}}$ and LOAD functions (default).

LDB = 1: DAC latch is transparent, the CODE register content controls the DAC output directly.

Clear Configuration:

CLEAR_ENB setting is written by CLB (B3); CLEAR_ENB operation is as follows:

CLB = 0: Clear input and command functions impact the DAC (default), clearing CODE and DAC registers to their DEFAULT value.

CLB = 1: Clear input and command functions have no effect on the DAC.

Table 8. CONFIG Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**WC1**	**WC0**	**GTB**	**LDB**	**CLB**	**X**	**X**	**X**
CONFIG Command				Reserved				Multiple DAC Selection								WDOG Config: 00: DISABLE 01: GATE 10: $\overline{\text{CLR}}$ 11: HOLD		GATE_ENB	LDAC_ENB	CLEAR_ENB	Don't Care		
Default Value →								1	1	1	1	1	1	1	1	0	0	0	0	0	X	X	X
Command Byte								Data High Byte								Data Low Byte							

DEFAULT Command

The DEFAULT command (B[23:20] = 0110) selects the default value for selected DACs. DACs which are not selected do not update their default settings in response to the command. These default values are used for all future watchdog, clear, and gate operations. The new default setting is determined by bits DF[2:0] (B[7:5]) while the affected DAC(s) are selected using B[15:8]. This command is inaccessible when a watchdog timeout has occurred and the watchdog timer is configured with a safety level of high or max. Note the selected default values do not apply to resets initiated by SW_RESET commands or supply cycling, both of which return all DACs to the values determined by the M/$\overline{Z}$ input and reset this register to M/$\overline{Z}$ mode.

Available default values (DF[2:0]):

M/$\overline{Z}$ (000): DAC channel defaults to value as selected by the M/$\overline{Z}$ input (default).

ZERO (001): DAC channel defaults to zero scale.

MID (010): DAC channel defaults to midscale.

FULL (011): DAC channel defaults to full scale.

RETURN (100): DAC channel defaults to the value programmed by the RETURN command.

No Effect (101, 110, 111): DAC channel default behavior is unchanged.

Table 9. DEFAULT Command Format

B23	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DF2**	**DF1**	**DF0**	**X**	**X**	**X**	**X**	**X**
DEFAULT Command				Reserved				Multiple DAC Selection								Default Values: 000: M/$\overline{Z}$ 001: ZERO 010: MID 011: FULL 100: RETURN 101+: No Effect			Don't Care				
Default Value →								1	1	1	1	1	1	1	1	0	0	0	X	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

SPI_DATA_REQUEST Command

The SPI_DATA_REQUEST command (B[23:20] = 1101) sets up the data request for future SPI_READ_DATA operations. SPI_READ_DATA is used to fetch the current settings of the internal CODE, DAC, or RETURN registers for each channel or the watchdog configuration (WDOG) settings or the device. The DAC address provided tells the part which channel location data is to be read back by the next SPI_READ_DATA command (see Table 3). Setting the DAC address greater than the number of available DACS will read back channel 0 content.

The INC bit tells the device how the next readback will update the DAC address pointer:

0 = Fix the address pointer (all further readbacks continue at the current address).

1 = Increment the address pointer (further readbacks continue at the next address, with rollover, default).

The SEL[1:0] bits tells the part what type of data is requested:

DAC (00): DAC register data (current DAC latch data, not subject to gating status, default).

CODE (01): CODE register data.

RET (10): RETURN register data.

WDT (11): WDOG register data (DAC selection does not apply).

Table 10. SPI_DATA_REQUEST Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	1	DAC SELECTION				INC	SEL[1:0]		X	X	X	X	X	X	X	X	X	X	X	X	X
SPI_DATA_REQUEST				DAC Selection				Increment	Data Selection 00: DAC 01: CODE 10: RET 11: WDT		Don't Care					Don't Care							
Default Value →				0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

SPI_READ_STATUS Command

The SPI_READ_STATUS command (B[23:18] = 111000 for DPHA = 0, B[23:18] = 111001 for DPHA = 1) reads back the watchdog timer and CLR pin status (intentionally repeated to allow maximum interface speeds) through DOUT.

DIN[18] selects the DOUT Phase (DPHA) to be used (see the SPI Serial Interface Timing Diagram in Figure 1 for details).

WD_STAT indicates a watchdog timeout condition. It reads 0 during normal operation, 1 during a timeout. WD_STAT is not masked by the WD_MASK bit in the WDOG_CONFIG command.

$\overline{CLR}$_STAT indicates the line level of the $\overline{CLR}$ pin. '0' indicates the $\overline{CLR}$ input is or was asserted (grounded) during the current SPI operation. '1' indicates the $\overline{CLR}$ input is not currently asserted (V_{DDIO} level).

Table 11. SPI_READ_STATUS Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SPI_READ_STATUS (DPHA = 0)								DOUT = WD_STAT (Repeated)								DOUT = $\overline{CLR}$_STAT (Repeated)							
1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SPI_READ_STATUS (DPHA = 1)								DOUT = WD_STAT (Repeated)								DOUT = $\overline{CLR}$_STAT (Repeated)							
Command Byte								Data High Byte								Data Low Byte							

SPI_READ_DATA Command

The SPI_READ_DATA command (B[23:18] = 111010 for DPHA = 0, B[23:18] = 111011 for DPHA = 1) reads back the data requested using the SPI_DATA_REQUEST command through DOUT.

DIN[18] selects the DOUT phase (DPHA) to be used (see Figure 1 for details, and the SPI Timing Characteristics in the *Electrical Characteristics* for a complete listing of readback speed capabilities based on the DPHA selection).

The SPI_READ_DATA command provides register and address data as defined by the SPI_DATA_REQUEST configuration SEL bits. SPI_READ_DATA also increments the channel address pointer if configured to do so by the SPI_DATA_REQUEST INC bit, the address readback is the address corresponding to the data returned.

Table 12. SPI_READ_DATA Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SPI_READ_DATA (DPHA = 0, SEL = 00)								DOUT = DAC[11:4]								DOUT = DAC[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 0, SEL = 01)								DOUT = CODE[11:4]								DOUT = CODE[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 0, SEL = 10)								DOUT = RETURN[11:4]								DOUT = RET[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 0, SEL = 11)								DOUT = WDOG[15:8]								DOUT = WDOG[7:1]							0
1	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SPI_READ_DATA (DPHA = 1, SEL = 00)								DOUT = DAC[11:4]								DOUT = DAC[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 1, SEL = 01)								DOUT = CODE[11:4]								DOUT = CODE[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 1, SEL = 10)								DOUT = RETURN[11:4]								DOUT = RET[3:0]				ADDRESS[3:0]			
SPI_READ_DATA (DPHA = 1, SEL = 11)								DOUT = WDOG[15:8]								DOUT = WDOG[7:1]							0
Command Byte								Data High Byte								Data Low Byte							

Applications Information

Power-On Reset (POR)

When power is applied to V_{DD} and V_{DDIO}, the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200µs, typ).

Power Supplies and Bypassing Considerations

Bypass V_{DD} and V_{DDIO} with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5723/MAX5724/MAX5725 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to minimize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5723/MAX5724/MAX5725 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL ≤ 1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL ≥ 1 LSB, the DAC output may still be monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function. The offset error is calculated from two measurements near zero code and near maximum code.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Zero-Scale Error

Zero-scale error is the difference between the DAC output voltage when set to code zero and ground. This includes offset and other die level nonidealities.

Full-Scale Error

Full-scale error is the difference between the DAC output voltage when set to full scale and the reference voltage. This includes offset, gain error, and other die level nonidealities.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

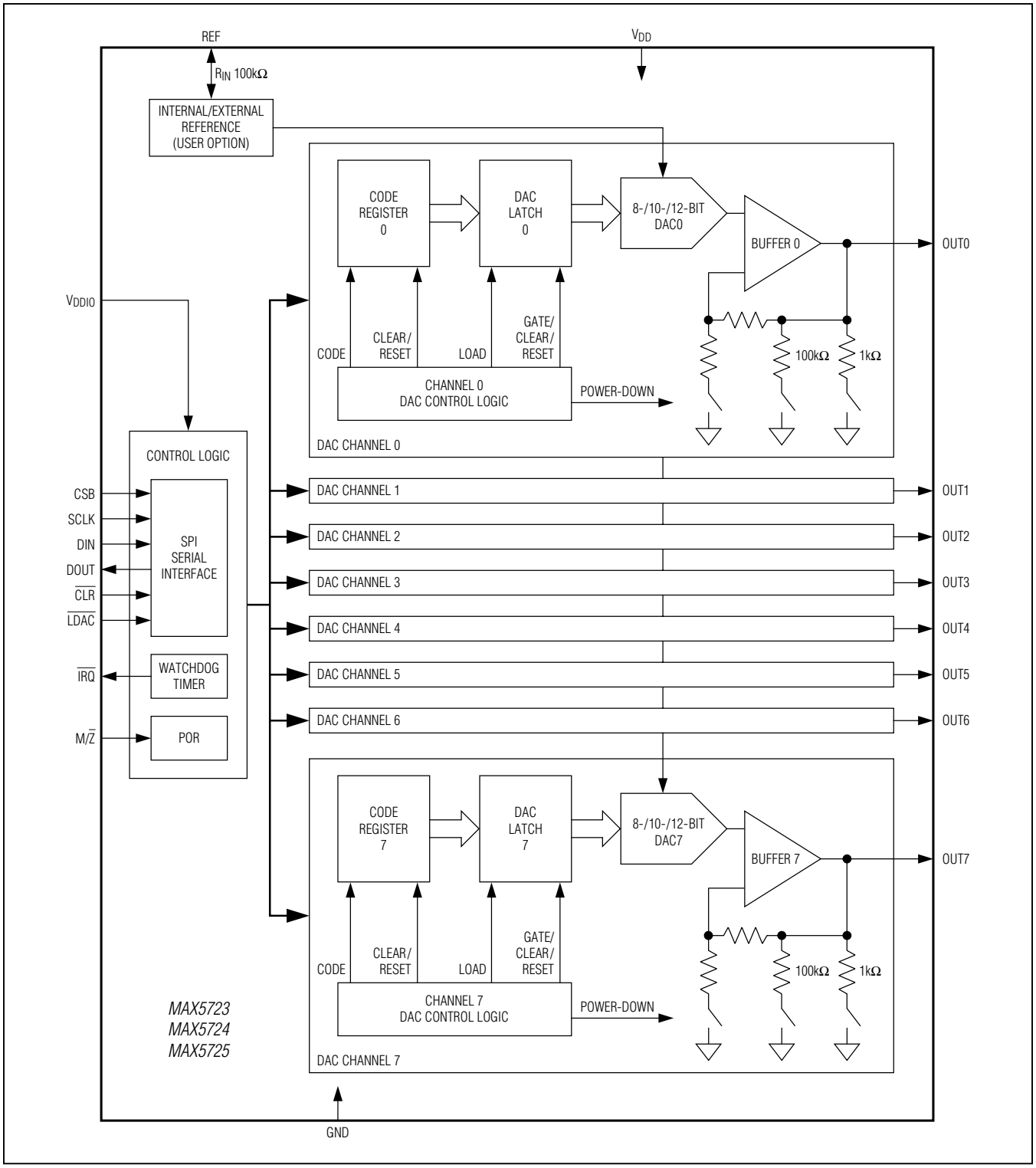
Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

Digital-to-Analog Glitch Impulse

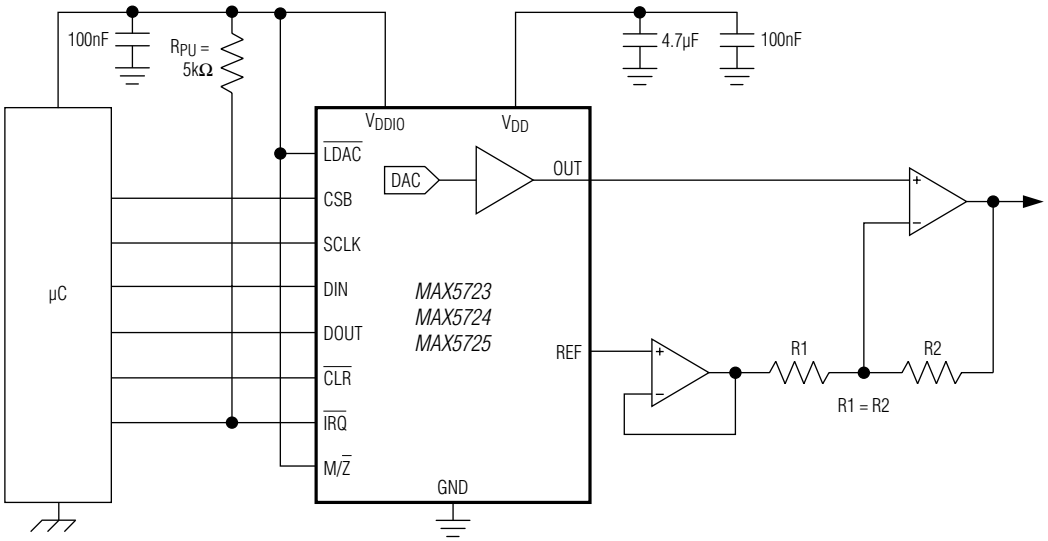
A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse. Although all bits change, larger steps may lead to larger glitch energy.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

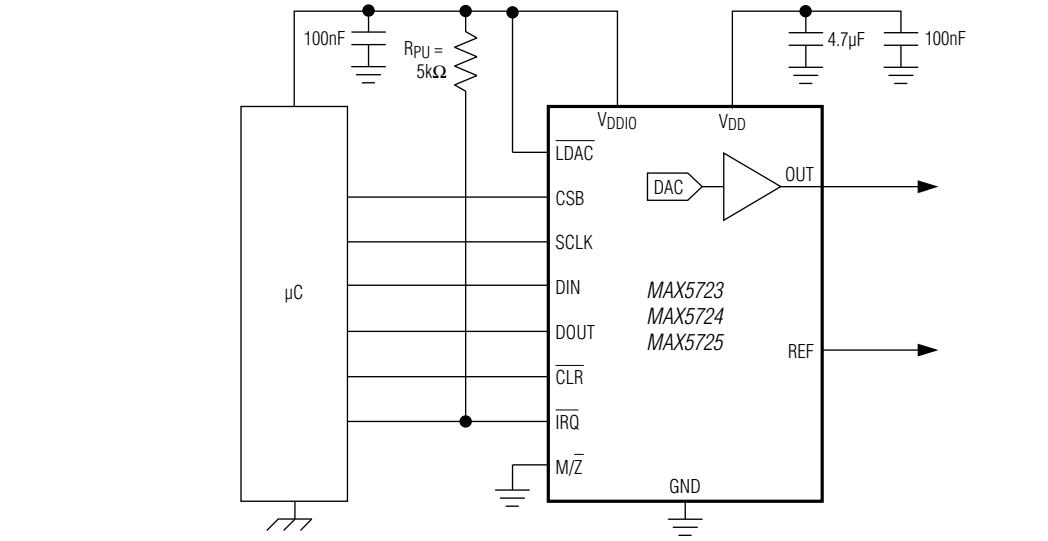
Detailed Functional Diagram



Typical Operating Circuits



NOTE: BIPOLAR OPERATING CIRCUIT, ONE CHANNEL SHOWN



NOTE: UNIPOLAR OPERATING CIRCUIT, ONE CHANNEL SHOWN

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESOLUTION (BIT)
MAX5723AUP+	-40°C to +125°C	20 TSSOP	8
MAX5724AUP+	-40°C to +125°C	20 TSSOP	10
MAX5725AAUP+	-40°C to +125°C	20 TSSOP	12
MAX5725AWP+T	-40°C to +125°C	20 WLP	12
MAX5725BAUP+	-40°C to +125°C	20 TSSOP	12

Note: *All devices are specified over the -40°C to +125°C temperature range.*
+Denotes a lead(Pb)–free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP	U20+1	**21-0066**	**90-0116**
20 WLP	W202C2+1	**21-0059**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/12	Initial release	—
1	11/12	Revised the *Ordering Information*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Configuration, Pin Description,* Figure 1, and the *DAC Outputs (OUT_)*, *CODEn_LOADn Command*, and *Offset Error* sections	3, 5, 8, 10–13, 15–18, 23, 31, 34
2	2/13	Released the MAX5723/MAX5724/MAX5725B, and updated the *Electrical Characteristics* global and Note 3	2–8, 34

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