19-2315; Rev 1; 3/05

MAXIM

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

General Description

The MAX5822 is a dual, 12-bit, voltage-output, digital-to-analog converter (DAC) with an I²C-compatible, 2-wire interface that operates at clock rates up to 400kHz. The device operates from a single 2.7V to 5.5V supply and draws only 115µA at V_{DD} = 3.6V. A power-down mode decreases current consumption to less than 1µA. The MAX5822 features three software-selectable power-down output impedances: 100kΩ, 1kΩ, and high impedance. Other features include internal precision rail-to-rail output buffers and a power-on reset (POR) circuit that powers up the DAC in the 100kΩ power-down mode.

The MAX5822 features a double-buffered I²C-compatible serial interface that allows multiple devices to share a single bus. All logic inputs are CMOS-logic compatible and buffered with Schmitt triggers, allowing direct interfacing to optocoupled and transformer-isolated interfaces. The MAX5822 minimizes digital noise feedthrough by disconnecting the clock (SCL) signal from the rest of the device when an address mismatch is detected.

The MAX5822 is specified over the extended temperature range of -40°C to +85°C and is available in a miniature 8-pin µMAX® package. Refer to the MAX5821 data sheet for the 10-bit version and the MAX5820 data sheet for the 8-bit version.

Applications

Digital Gain and Offset Adjustments

Programmable Voltage and Current Sources

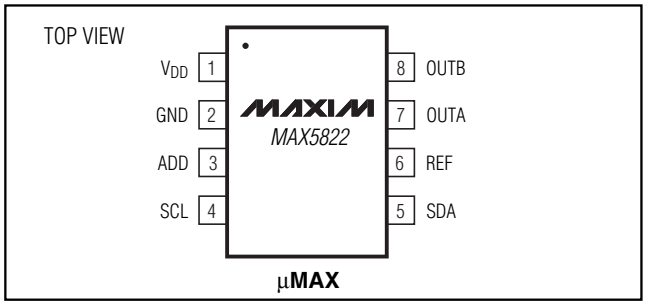
Programmable Attenuation

VCO/Varactor Diode Control

Low-Cost Instrumentation

Battery-Powered Instrumentation

Pin Configuration



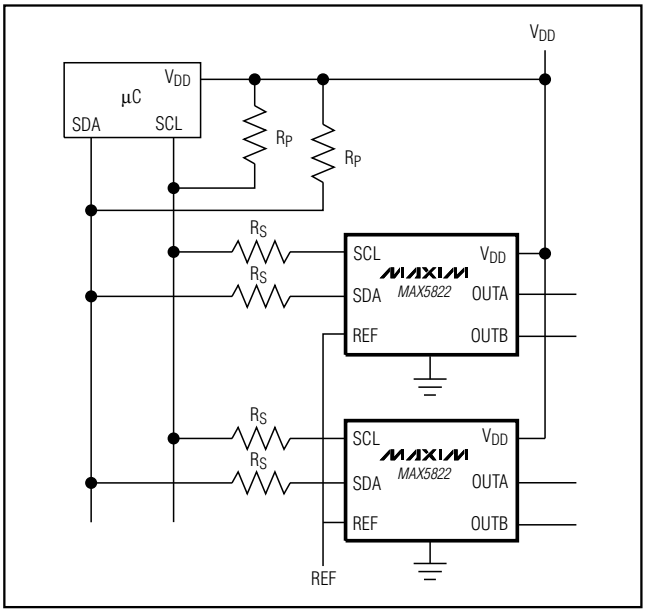
Features

- **Ultra-Low Supply Current**
  115µA at V_{DD} = 3.6V
  135µA at V_{DD} = 5.5V
- **300nA Low-Power Power-Down Mode**
- **Single 2.7V to 5.5V Supply Voltage**
- **Fast 400kHz I²C-Compatible 2-Wire Serial Interface**
- **Schmitt-Trigger Inputs for Direct Interfacing to Optocouplers**
- **Rail-to-Rail Output Buffer Amplifiers**
- **Three Software-Selectable Power-Down Output Impedances**
  100kΩ, 1kΩ, and High Impedance
- **Read-Back Mode for Bus and Data Checking**
- **Power-On Reset to Zero**
- **8-Pin µMAX Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	ADDRESS
MAX5822LEUA	-40°C to +85°C	8 µMAX	0111 00X
MAX5822MEUA	-40°C to +85°C	8 µMAX	1011 00X

Typical Operating Circuit



µMAX is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCL, SDA to GND .....-0.3V to +6V
OUT_, REF, ADD to GND.....-0.3V to V_{DD} + 0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW above +70°C) 362mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (NOTE 2)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 3)		±2	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Code Error	ZCE	Code = 000 hex, V_{DD} = 2.7V		6	40	mV
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = FFF hex		-0.8	-3	%FSR
Gain-Error Tempco				0.26		ppm/°C
Power-Supply Rejection Ratio	PSRR	Code = FFF hex, V_{DD} = 4.5V to 5.5V		58.8		dB
DC Crosstalk				30		µV
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		0		V_{DD}	V
Reference Input Impedance			65	90		kΩ
Reference Current		Power-down mode		0.3	1	µA
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V_{DD}	V
DC Output Impedance		Code = 800 hex		1.2		Ω
Short-Circuit Current		V_{DD} = 5V, V_{OUT} = full scale (short to GND)		42.2		mA
		V_{DD} = 3V, V_{OUT} = full scale (short to GND)		15.1		
Wake-Up Time		V_{DD} = 5V		8		µs
		V_{DD} = 3V		8		
DAC Output Leakage Current		Power-down mode = high impedance, V_{DD} = 5.5V, $V_{OUT_}$ = V_{DD} to GND		±0.1	±1	µA
DIGITAL INPUTS (SCL, SDA)						
Input High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Low Voltage	V_{IL}				0.3 × V_{DD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis			0.05 x V_{DD}			V
Input Leakage Current		Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance				6		pF
DIGITAL OUTPUT (SDA)						
Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Three-State Leakage Current	I_L	Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Three-State Output Capacitance				6		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.5		V/µs
Voltage-Output Settling Time		To 1/2LSB code 400 hex to C00 hex or C00 hex to 400 hex (Note 5)		4	12	µs
Digital Feedthrough		Code = 000 hex, digital inputs from 0 to V_{DD}		0.2		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition (code = 7FF hex to 800 hex and 800 hex to 7FF hex)		12		nV-s
DAC to DAC Crosstalk				2.4		nV-s
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load	I_{DD}	All digital inputs at 0 or V_{DD} = 3.6V		115	205	µA
		All digital inputs at 0 or V_{DD} = 5.5V		135	215	
Power-Down Supply Current	I_{DDPD}	All digital inputs at 0 or V_{DD} = 5.5V		0.3	1	µA
TIMING CHARACTERISTICS (FIGURE 1)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD,STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Repeated START Setup Time	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_r	(Note 5)	0		300	ns
SDA and SCL Receiving Fall Time	t_f	(Note 5)	0		300	ns
SDA Transmitting Fall Time	t_f	(Note 5)	20 + 0.1C_b		250	ns

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

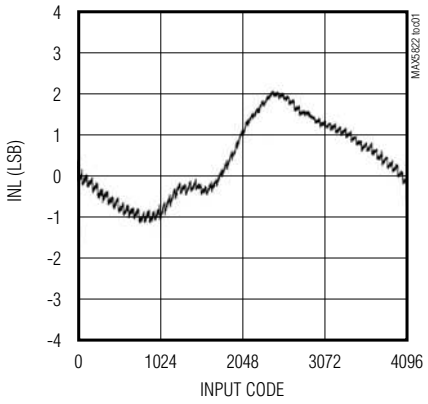
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_b	(Note 5)			400	pF
Maximum Duration of Suppressed Pulse Widths	t_{SP}		0		50	ns

Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by design at T_A = T_{MIN} to T_{MAX}.
Note 2: Static specifications are tested with the output unloaded.
Note 3: Linearity is guaranteed from codes 115 to 3981.
Note 4: Offset and gain error limit the FSR.
Note 5: Guaranteed by design. Not production tested.

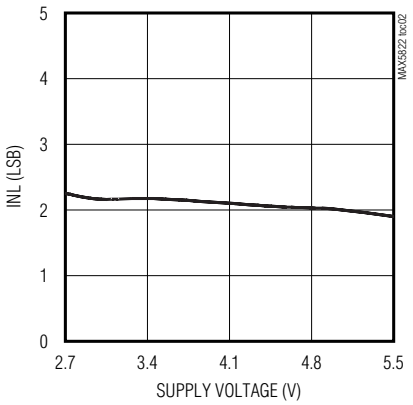
Typical Operating Characteristics

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

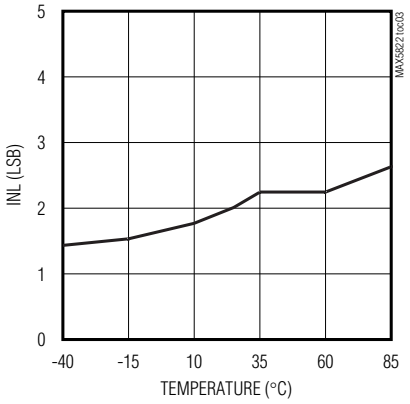
INTEGRAL NONLINEARITY vs. INPUT CODE



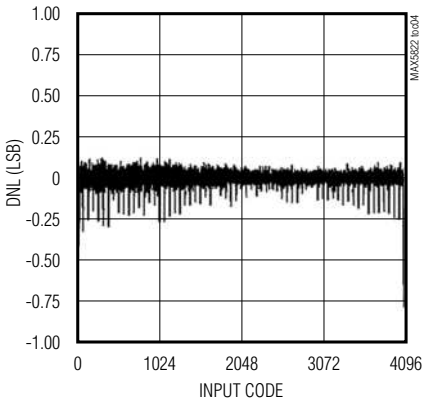
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



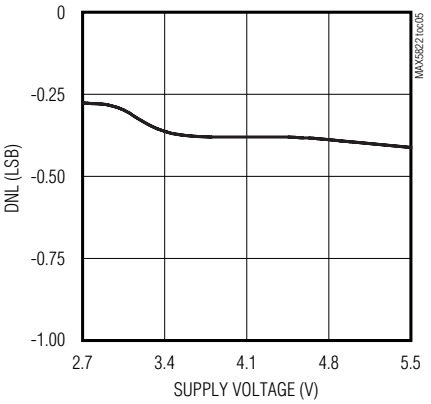
INTEGRAL NONLINEARITY vs. TEMPERATURE



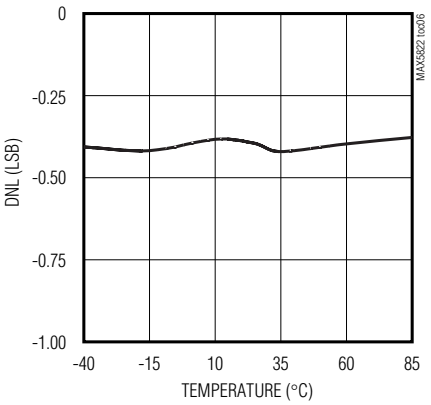
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



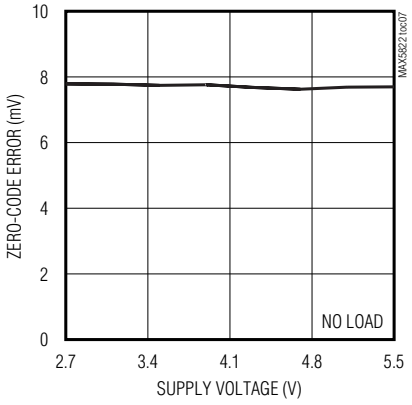
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



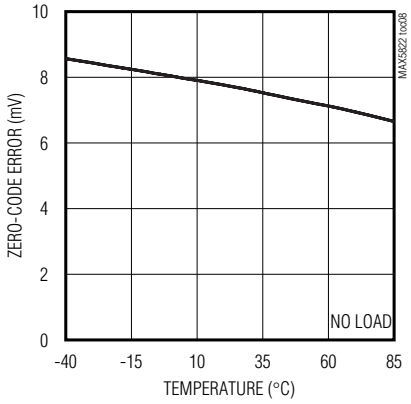
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

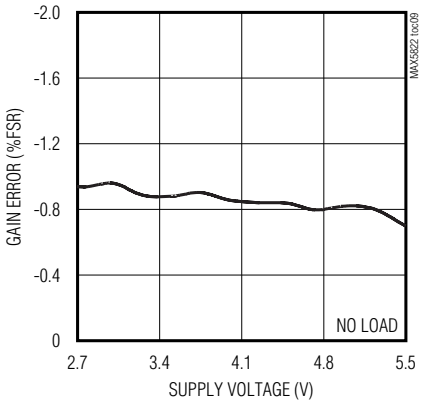
ZERO-CODE ERROR vs. SUPPLY VOLTAGE



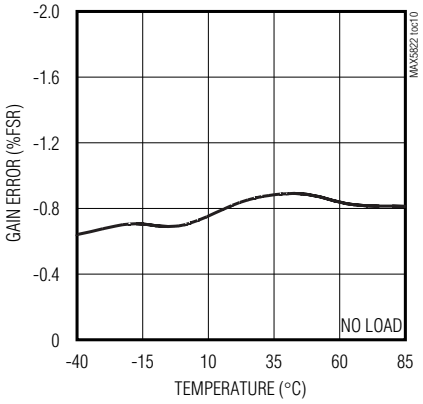
ZERO-CODE ERROR vs. TEMPERATURE



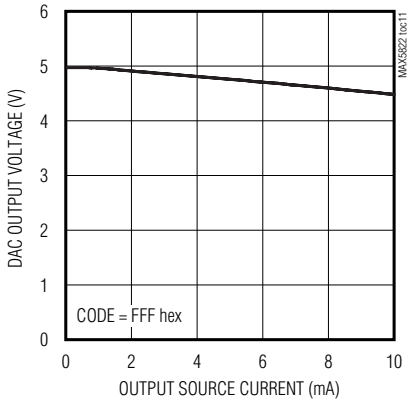
GAIN ERROR vs. SUPPLY VOLTAGE



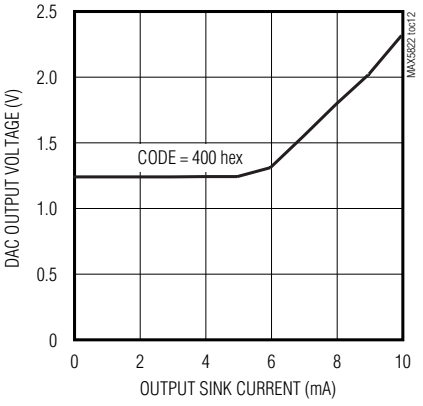
GAIN ERROR vs. TEMPERATURE



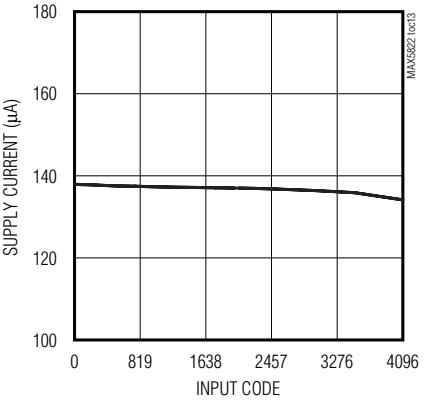
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (NOTE 6)



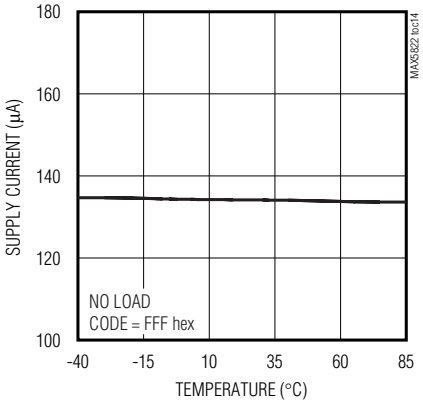
DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT (NOTE 6)



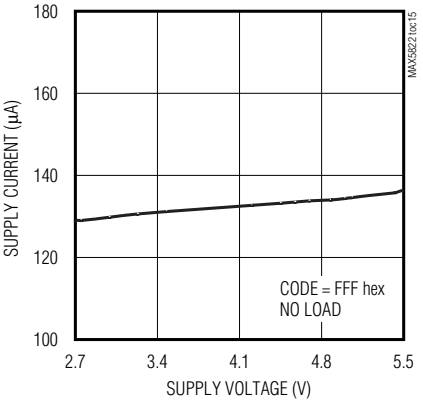
SUPPLY CURRENT vs. INPUT CODE



SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

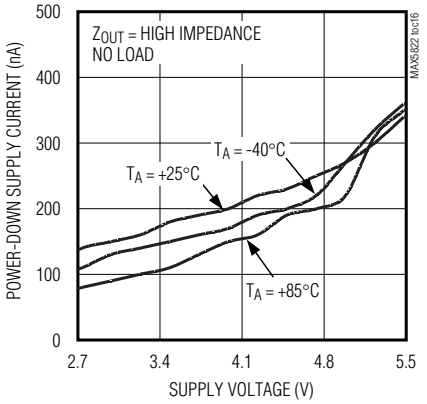


Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

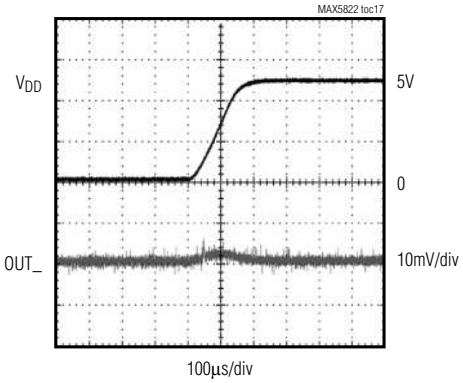
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

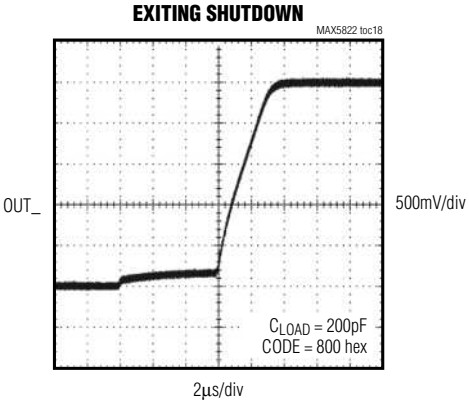
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



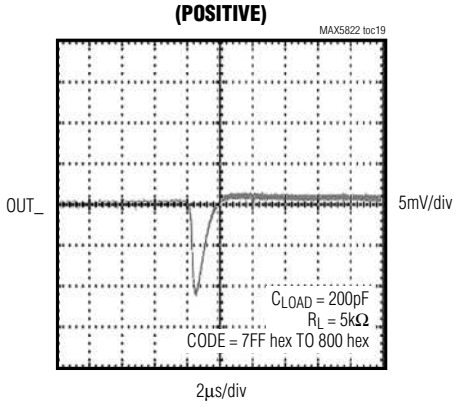
POWER-UP GLITCH



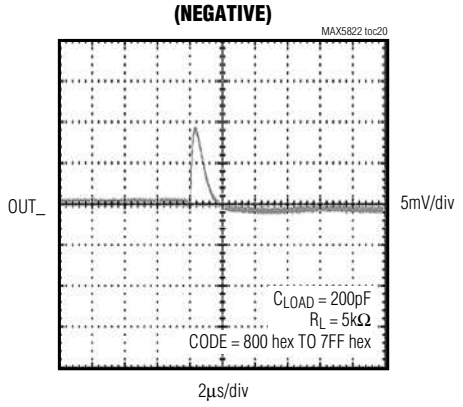
EXITING SHUTDOWN



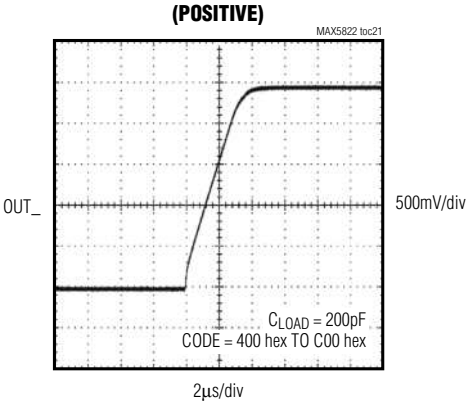
MAJOR-CARRY TRANSITION (POSITIVE)



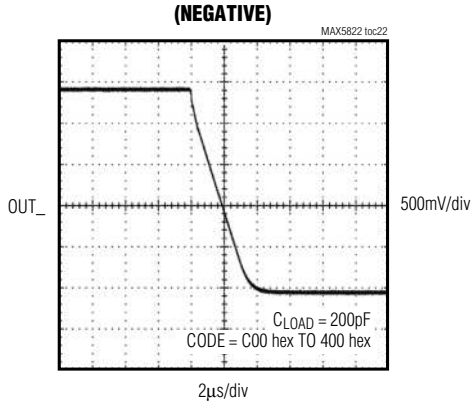
MAJOR-CARRY TRANSITION (NEGATIVE)



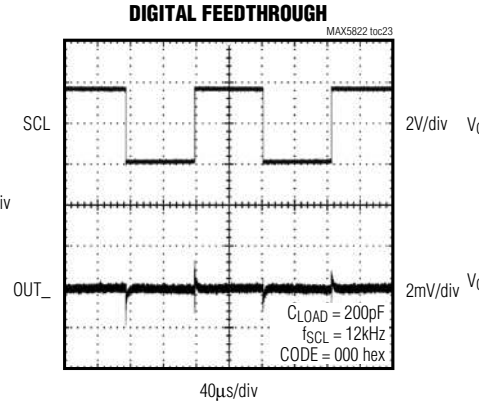
SETTLING TIME (POSITIVE)



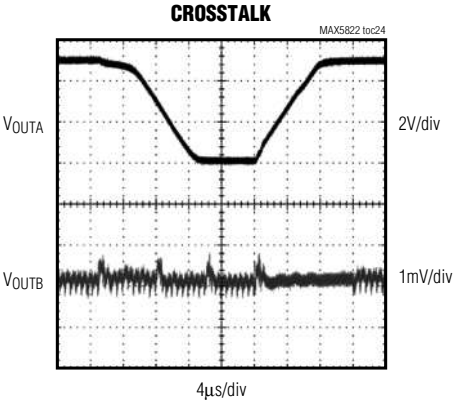
SETTLING TIME (NEGATIVE)



DIGITAL FEEDTHROUGH



CROSSTALK



Note 6: The ability to drive loads greater than 5kΩ is not implied.

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Supply
2	GND	Ground
3	ADD	Address Select. A logic high sets the address LSB to 1; a logic low sets the address LSB to 0.
4	SCL	Serial Clock Input
5	SDA	Bidirectional Serial Data Interface
6	REF	Reference Input
7	OUTA	DAC A Output
8	OUTB	DAC B Output

Detailed Description

The MAX5822 is a dual, 12-bit, voltage-output DAC with an I²C/SMBus™-compatible 2-wire interface. The device consists of a serial interface, power-down circuitry, two input and DAC registers, two 12-bit resistor string DACs, two unity-gain output buffers, and output resistor networks. The serial interface decodes the address and control bits, routing the data to the proper input or DAC register. Data can be directly written to the DAC register, immediately updating the device output, or can be written to the input register without changing the DAC output. Both registers retain data as long as the device is powered.

DAC Operation

The MAX5822 uses a segmented resistor string DAC architecture, which saves power in the overall system and guarantees output monotonicity. The MAX5822's input coding is straight binary, with the output voltage given by the following equation:

$$V_{OUT_} = \frac{V_{REF} \times (D)}{2^N}$$

where N = 12 (bits), and D = the decimal value of the input code (0 to 4095).

Output Buffer

The MAX5822 analog outputs are buffered by precision, unity-gain followers that slew 0.5V/µs. Each buffer output swings rail-to-rail, and is capable of driving 5kΩ in parallel with 200pF. The output settles to ±0.5LSB within 4µs.

Power-On Reset

The MAX5822 features an internal POR circuit that initializes the device upon power-up. The DAC registers are set to zero scale and the device is powered down, with the output buffers disabled and the outputs pulled to GND through the 100kΩ termination resistor. Following power-up, a wake-up command must be initiated before any conversions are performed.

Power-Down Modes

The MAX5822 has three software-controlled, low-power power-down modes. All three modes disable the output buffers and disconnect the DAC resistor strings from REF, reducing supply current draw to 1µA and the reference current draw to less than 1µA. In power-down mode 0, the device output is high impedance. In power-down mode 1, the device output is internally pulled to GND by a 1kΩ termination resistor. In power-down mode 2, the device output is internally pulled to GND by a 100kΩ termination resistor. Table 1 shows the power-down mode command words.

Upon wake-up, the DAC output is restored to its previous value. Data is retained in the input and DAC registers during power-down mode.

Digital Interface

The MAX5822 features an I²C/SMBus-compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). The MAX5822 is SMBus compatible within the range of V_{DD} = 2.7V to 3.6V. SDA and SCL facilitate bidirectional communication between the MAX5822 and the master at rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX5822 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX5822 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or repeated START (S_r) condition and a STOP (P) condition. Each word transmitted over the

SMBus is a trademark of Intel Corporation.

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

Table 1. Power-Down Command Bits

POWER-DOWN COMMAND BITS		MODE/FUNCTION
PD1	PD0	
0	0	Power-up device. DAC output restored to previous value.
0	1	Power-down mode 0. Power down device with output floating.
1	0	Power-down mode 1. Power down device with output terminated with 1kΩ to GND.
1	1	Power-down mode 2. Power down device with output terminated with 100kΩ to GND.

bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX5822 SDA and SCL drivers are open-drain outputs, requiring a pullup resistor to generate a logic-high voltage (see the *Typical Operating Circuit*). Series resistors R_S are optional. These series resistors protect the input stages of the MAX5822 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5822. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *Acknowledge Bit (ACK)* section). The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX5822 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX5822 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 3). This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP conditions.

Repeated START Conditions

A repeated START (S_r) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5822 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

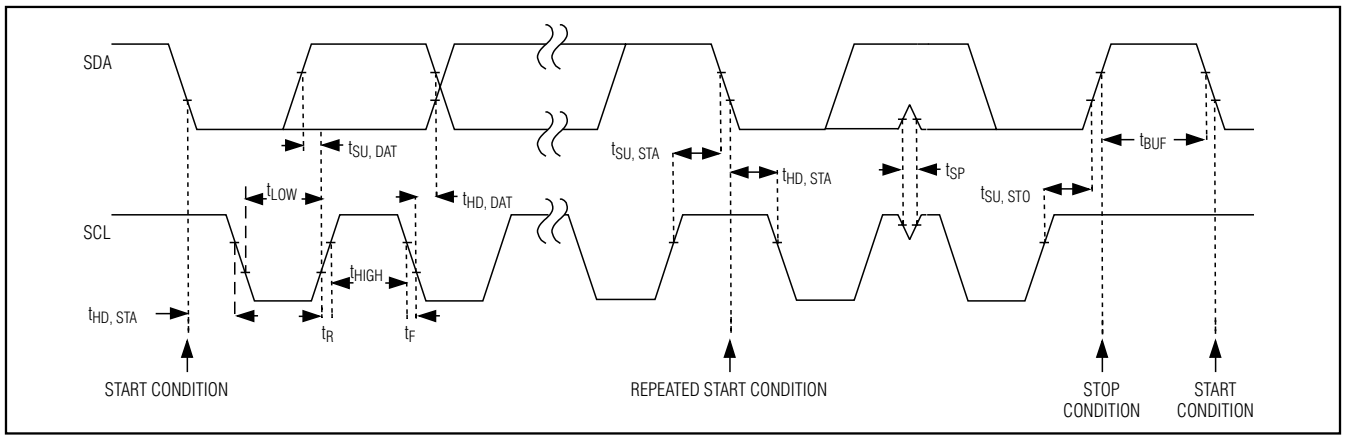


Figure 1. 2-Wire Serial Interface Timing Diagram

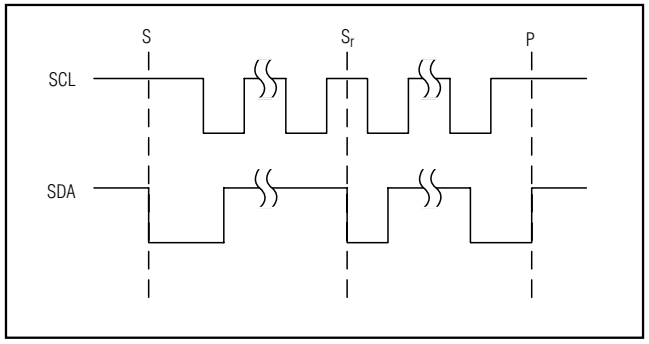


Figure 2. START and STOP Conditions

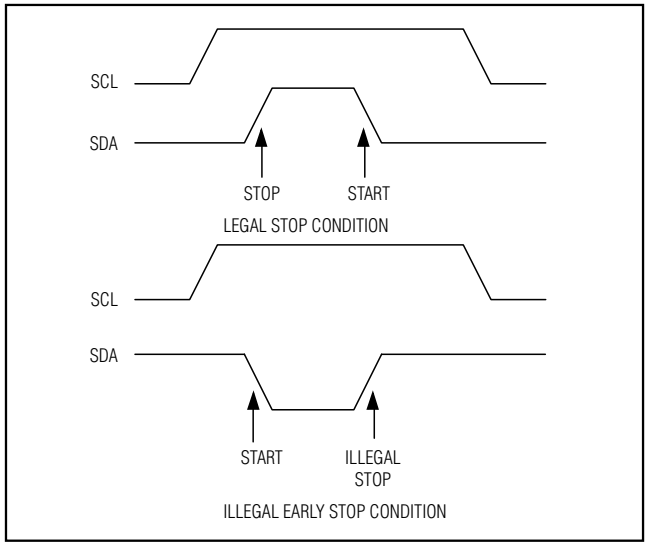


Figure 3. Early STOP Conditions

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device. The MAX5822 generates an ACK when receiving an address or data by pulling SDA low during the ninth clock period. When transmitting data, the MAX5822 waits for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address (Figure 4). When idle, the MAX5822 waits for a START condition followed by its slave address. The serial interface compares each address value bit by bit, allowing the interface to power down immediately, if an incorrect address is detected. The LSB of the address word is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. R/$\overline{\text{W}}$ indicates whether the master is writing to or reading from the MAX5822 (R/$\overline{\text{W}}$ = 0 selects the write condition, R/$\overline{\text{W}}$ = 1 selects the read condition). After receiving the proper address, the MAX5822 issues an ACK by pulling SDA low for one clock cycle.

The MAX5822 has four different factory/user-programmed addresses (Table 2). Address bits A6 through A1 are preset, while A0 is controlled by ADD. Connecting ADD to GND sets A0 = 0. Connecting ADD to V_{DD} sets A0 = 1. This feature allows up to four MAX5822s to share the same bus.

Table 2. MAX5822 I²C Slave Addresses

PART	V_{ADD}	DEVICE ADDRESS (A6...A0)
MAX5822L	GND	0111 000
MAX5822L	V_{DD}	0111 001
MAX5822M	GND	1011 000
MAX5822M	V_{DD}	1011 001

Write Data Format

In write mode (R/$\overline{\text{W}}$ = 0), data that follows the address byte controls the MAX5822 (Figure 5). Bits C3–C0 configure the MAX5822 (Table 3). Bits D11–D0 are DAC data. Input and DAC registers update on the falling edge of SCL during the acknowledge bit. Should the write cycle be prematurely aborted, data is not updated and the write cycle must be repeated. Figure 6 shows two example write data sequences.

Extended Command Mode

The MAX5822 features an extended command mode that is accessed by setting C3–C0 = 1 and D11–D8 = 0. The next data byte writes to the shutdown registers

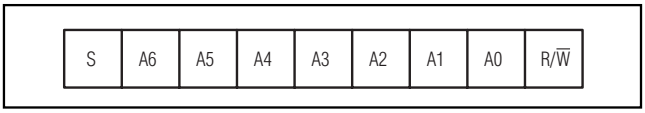


Figure 4. Slave Address Byte Definition

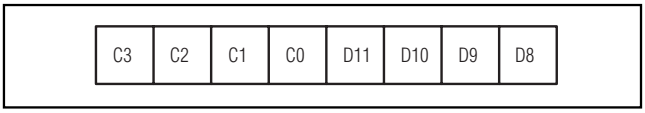


Figure 5. Command Byte Definition

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

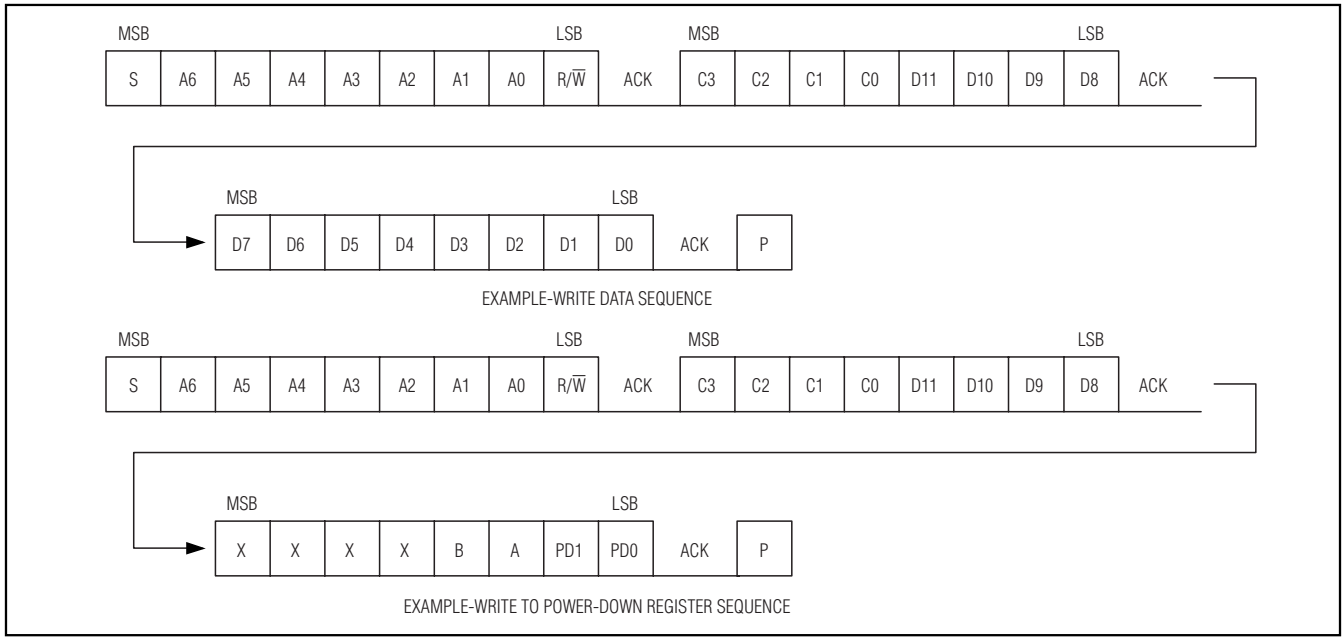


Figure 6. Example Write-Command Sequences

(Figure 7). Setting bits A or B to 1 sets that DAC to the selected power-down mode based on the states of PD0 and PD1 (Table 1). Any combination of the DACs can be controlled with a single write sequence.

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX5822 writes the contents of the DAC register to the bus. The direction of data flow reverses following the address acknowledge by the MAX5822. The device transmits the first byte of data, waits for the master to acknowledge, then transmits the second byte. Figure 8 shows an example-read data sequence.

I²C Compatibility

The MAX5822 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The *Typical Operating Circuit* shows a typical I²C application. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored. The MAX5822 address is compatible with the 7-bit I²C addressing protocol only. No 10-bit address formats are supported.

Digital Feedthrough Suppression

When the MAX5822 detects an address mismatch, the serial interface disconnects the SCL signal from the core circuitry. This minimizes digital feedthrough

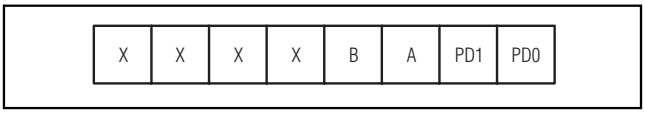


Figure 7. Extended Command Byte Format

caused by the SCL signal on a static output. The serial interface reconnects the SCL signal once a valid START condition is detected.

Applications Information

Digital Inputs and Interface Logic

The MAX5822 2-wire digital interface is I²C/SMBus compatible. The two digital inputs (SCL and SDA) load the digital input serially into the DAC. Schmitt-trigger buffered inputs allow slow-transition interfaces, such as optocouplers to interface directly to the device. The digital inputs are compatible with CMOS logic levels.

Power-Supply Bypassing and Ground Management

Careful PC board layout is important for optimal system performance. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Use a ground plane to ensure that the ground return from GND to the power-supply ground is short and low impedance. Bypass V_{DD} with a 0.1µF capacitor to ground as close to the device as possible.

Table 3. Command Byte Definitions

SERIAL DATA INPUT								FUNCTION
C3	C2	C1	C0	D11	D10	D9	D8	
0	0	0	0	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load DAC A input and DAC registers with new data. Contents of DAC B input registers are transferred to the DAC register. Both outputs are updated.
0	0	0	1	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load DAC B input and DAC registers with new data. Contents of DAC A input registers are transferred to the DAC register. Both outputs are updated simultaneously.
0	1	0	0	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load DAC A input register with new data. DAC outputs remain unchanged.
0	1	0	1	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load DAC B input register with new data. DAC outputs remain unchanged.
1	0	0	0	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Data in all input registers is transferred to respective DAC registers. All DAC outputs are updated simultaneously. New data is loaded into DAC A input register.
1	0	0	1	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Data in all input registers is transferred to respective DAC registers. All DAC outputs are updated simultaneously. New data is loaded into DAC B input register.
1	1	0	0	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load all DACs with new data and update all DAC outputs simultaneously. Both input and DAC registers are updated with new data.
1	1	0	1	DAC DATA	DAC DATA	DAC DATA	DAC DATA	Load all input registers with new data. DAC outputs remain unchanged.
1	1	1	0	X	X	X	X	Update all DAC outputs simultaneously. Device ignores D11–D8. Do not send the data byte.
1	1	1	1	0	0	0	0	Extended command mode. The next word writes to the power-down registers (see the *Extended Command Mode* section).
1	1	1	1	0	0	0	1	Read DAC A data. The device expects an S_r condition followed by an address word with R/$\overline{W}$ = 1.
1	1	1	1	0	0	1	0	Read DAC B data. The device expects an S_r condition followed by an address word with R/$\overline{W}$ = 1.

Dual, 12-Bit, Low-Power, 2-Wire, Serial Voltage-Output DAC

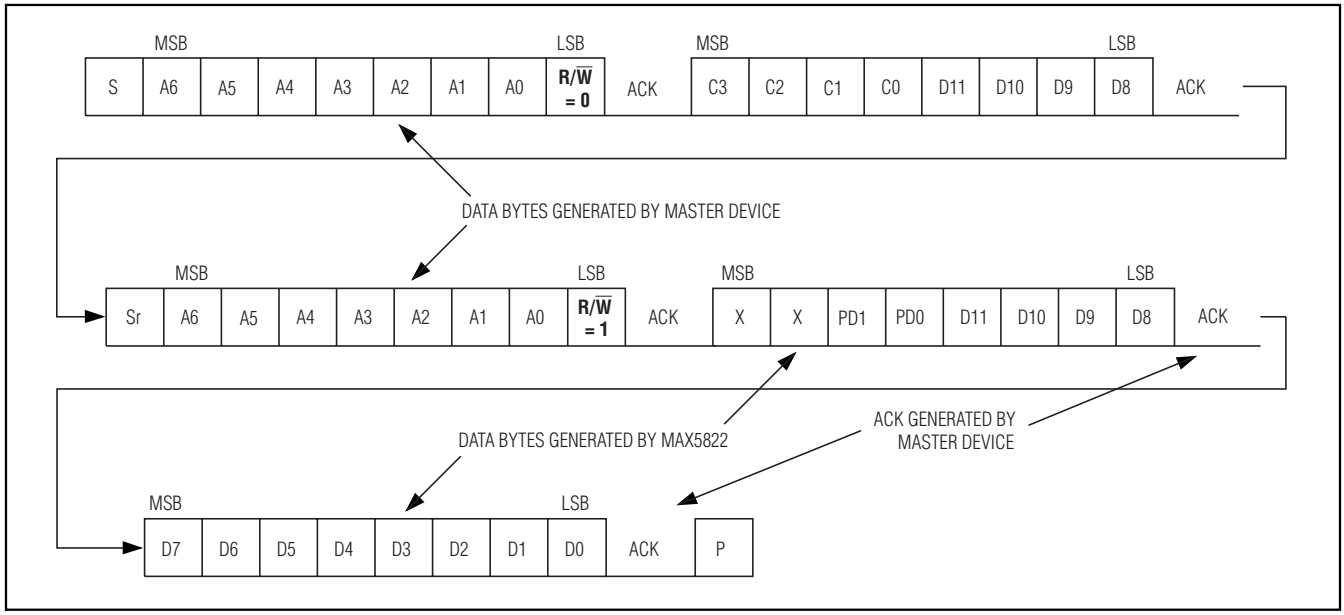
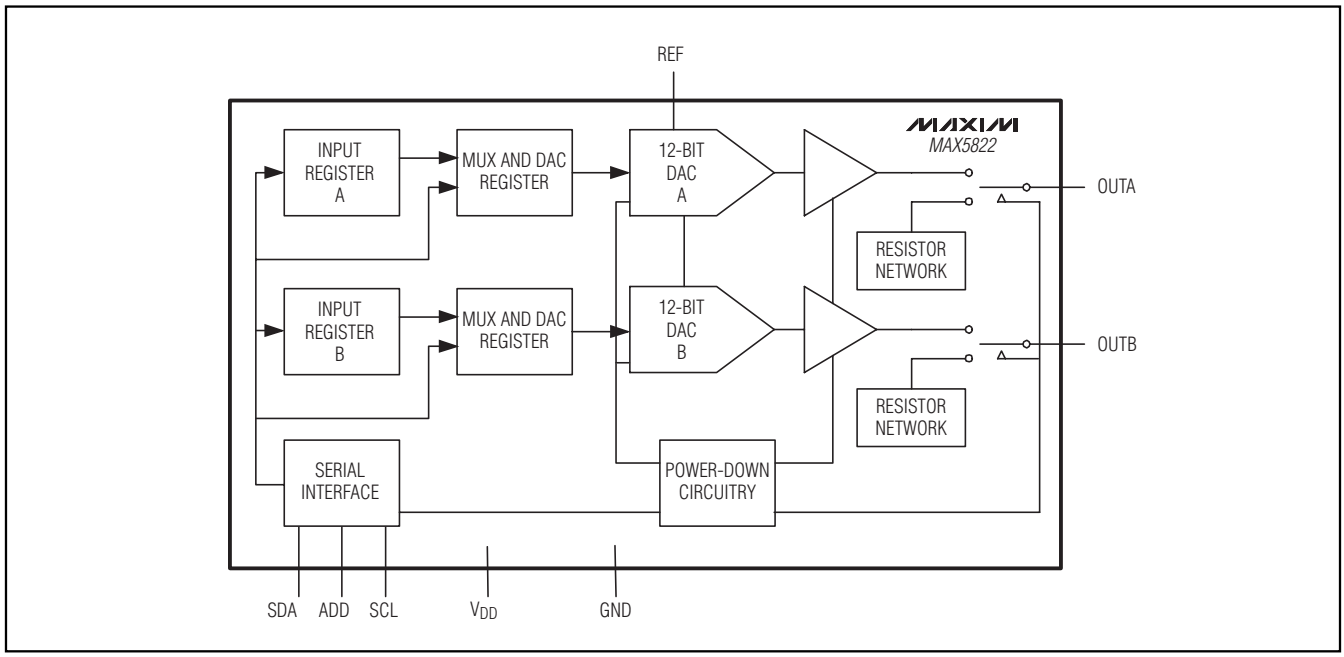


Figure 8. Example Read Word Data Sequence

Functional Diagram



Chip Information

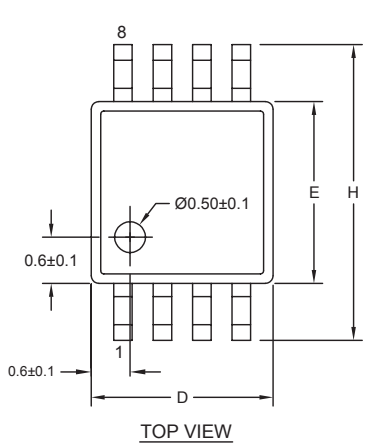
TRANSISTOR COUNT: 11,186

PROCESS: BiCMOS

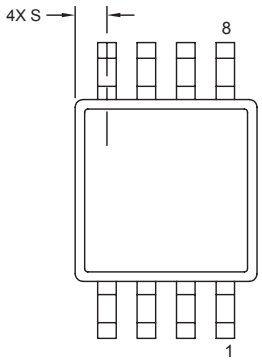
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

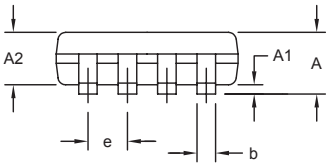


TOP VIEW

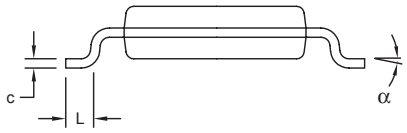


BOTTOM VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

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