19-2945; Rev 3; 3/04

EVALUATION KIT AVAILABLE

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

General Description

The MAX5927/MAX5929 +1V to +13.2V quad hot-swap controllers provide complete protection for multisupply systems. They allow the safe insertion and removal of circuit cards into live backplanes. These devices hot swap multiple supplies ranging from +1V to +13.2V, provided one supply is at or above +2.7V and only one supply is above +11.0V. The input voltage rails (channels) can be configured to sequentially turn-on/off, track each other, or have completely independent operation.

The discharged filter capacitors of the circuit card provide low impedance to the live backplane. High inrush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. The MAX5927/MAX5929 hot-swap controllers prevent such problems by gradually ramping up the output voltage and regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is complete, on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, and provide immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The MAX5929A automatically restarts after a fault condition, while the MAX5929L must be unlatched. The MAX5927 fault management mode is selectable.

The MAX5927/MAX5929 offer a variety of options to reduce external component count and design time. All devices integrate an on-board charge pump to drive the gates of low-cost external N-channel MOSFETs, an adjustable startup timer, and an adjustable current limit. The devices offer integrated features like startup current regulation and current glitch protection to eliminate external timing resistors and capacitors. The MAX5929_L provides an open-drain active-low status output for each channel, the MAX5929_H provides an open-drain active-high status output for each channel, and the MAX5927 status output polarity is selectable.

The MAX5927 is available in a 32-pin thin QFN package and the MAX5929 is available in a 24-pin QSOP package. All devices are specified over the extended temperature range, -40°C to +85°C.

Applications

PCI Express Hot Plug

Hot Plug-In Daughter Cards

RAID

Power-Supply Sequencing/Tracking

Basestation Line Cards

Portable Computer Device Bays (Docking Stations)

Network Switches, Routers, Hubs

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Features

- **Safe Hot Swap for +1V to +13.2V Power Supplies with Any Input Voltage ($V_{IN_}$ ≥ 2.7V and Only One $V_{IN_}$ > 11.0V)**
- **Adjustable Circuit Breaker/Current-Limit Threshold from 25mV to 100mV**
- **Configurable Tracking, Sequencing, or Independent Operation Modes**
- **VariableSpeed/BiLevel Circuit-Breaker Response**
- **Internal Charge Pumps Generate N-Channel MOSFET Gate Drives**
- **Inrush Current Regulated at Startup**
- **Autoretry or Latched Fault Management**
- **Programmable Undervoltage Lockout**
- **Status Outputs Indicate Fault/Safe Condition**

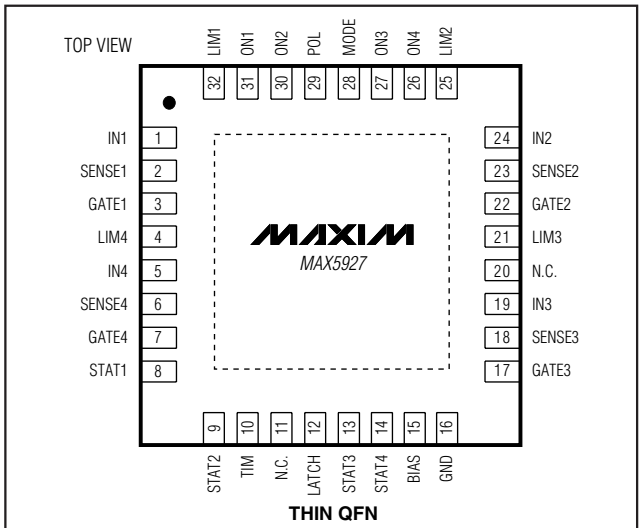
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5927ETJ	-40°C to +85°C	32 Thin QFN-EP
MAX5929LHEEG	-40°C to +85°C	24 QSOP
MAX5929LLEEG	-40°C to +85°C	24 QSOP
MAX5929AHEEG	-40°C to +85°C	24 QSOP
MAX5929ALEEG	-40°C to +85°C	24 QSOP

EP = Exposed paddle.

Selector Guide and Typical Operating Circuit appear at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
IN_ .....-0.3V to +14V
GATE_.....-0.3V to (IN_ + 6V)
BIAS (Note 1) ..... (V_{IN} - 0.3V) to +14V
ON_, STAT_, LIM_ (MAX5927), TIM, MODE, LATCH (MAX5927), POL (MAX5927) (Note 1).....-0.3V to (V_{IN} + 0.3V)
SENSE_.....-0.3V to (IN_ + 0.3V)
Current into Any Pin.....±50mA

Note 1: V_{IN} is the largest of V_{IN1}, V_{IN2}, V_{IN3}, and V_{IN4}.

Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
32-Pin Thin QFN (derate 21.3mW/°C above +70°C) ..1702mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN_}$ = +1V to +13.2V provided at least one supply is larger than or equal to +2.7V and only one supply is > +11.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN1} = 12.0V, V_{IN2} = 5.0V, V_{IN3} = 3.3V, V_{IN4} = 1.0V, $V_{ON_}$ = +3.3V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
IN_ Input Voltage Range	$V_{IN_}$	At least one $V_{IN_}$ ≥ +2.7V and only one $V_{IN_}$ > +11.0V		1.0		13.2	V
Supply Current	I_Q	I_{IN1} + I_{IN2} + I_{IN3} + I_{IN4}, $V_{ON_}$ = 2.7V, $V_{IN_}$ = +13.2V, after STAT_ asserts			2.5	5	mA
CURRENT CONTROL							
Slow-Comparator Threshold ($V_{IN_}$ - $V_{SENSE_}$) (Note 3)	$V_{SC,TH}$	LIM_ = GND, MAX5927/MAX5929 (Note 4)	T_A = +25°C	22.5	25	27.5	mV
			T_A = -40°C to +85°C	21.0		27.5	
		$R_{LIM_}$ = 10kΩ (MAX5927)		80		125	
		$R_{LIM_}$ from LIM_ to GND (MAX5927)		$R_{LIM_}$ x 7.5 x 10^{-6} + 25mV			
Slow-Comparator Response Time (Note 4)	t_{SCD}	1mV overdrive			3		ms
		50mV overdrive			130		µs
Fast-Comparator Threshold ($V_{IN_}$ - $V_{SENSE_}$)	$V_{FC,TH}$				2 x $V_{SC,TH}$		mV
Fast-Comparator Response Time	t_{FCD}	10mV overdrive, from overload condition			200		ns
SENSE_ Input Bias Current	$I_{B\ SENSE_}$	$V_{SENSE_}$ = $V_{IN_}$			0.03	1	µA
MOSFET DRIVER							
Startup Period (Note 5)	t_{START}	R_{TIM} = 100kΩ		8.0	10.8	13.6	ms
		R_{TIM} = 4kΩ (minimum value)		0.30	0.4	0.55	
		TIM floating (default)		5	9	14	

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN_}$ = +1V to +13.2V provided at least one supply is larger than or equal to +2.7V and only one supply is > +11.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN1} = 12.0V, V_{IN2} = 5.0V, V_{IN3} = 3.3V, V_{IN4} = 1.0V, $V_{ON_}$ = +3.3V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Average Gate Current	I_{GATE}	Charging, $V_{GATE_}$ = GND, $V_{IN_}$ = 5V (Note 6)	80	100	125	µA
		Discharging, during startup		100		
		Discharging, normal turn-off or triggered by the slow comparator after startup, $V_{GATE_}$ = 5V, $V_{IN_}$ = 10V, $V_{ON_}$ = 0V	2	3	7	mA
		Discharging, triggered by a fault after startup, $V_{GATE_}$ = 5V, $V_{IN_}$ = 10V, ($V_{IN_}$ - $V_{SENSE_}$) > $V_{FC,TH}$ (Note 7)	30	50	120	
Gate-Drive Voltage	V_{DRIVE}	$V_{GATE_}$ - $V_{IN_}$, $I_{GATE_}$ = 1µA	4.9	5.3	5.6	V
ON COMPARATOR						
ON_ Threshold	$V_{ON_,TH}$	Low to high	0.85	0.875	0.90	V
		Hysteresis		25		mV
ON_ Propagation Delay		10mV overdrive		10		µs
ON_ Voltage Range	$V_{ON_}$	Without false output inversion			V_{IN}	V
ON_ Input Bias Current	$I_{BON_}$	$V_{ON_}$ = V_{IN}		0.03	1	µA
ON_ Pulse Width Low	$t_{UNLATCH}$	To unlatch after a latched fault	100			µs
DIGITAL OUTPUTS (STAT_)						
Output Leakage Current		$V_{STAT_}$ ≤ 13.2V			1	µA
Output Voltage Low	$V_{OL_}$	POL = floating (MAX5927), I_{SINK} = 1mA			0.4	V
UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold	V_{UVLO}	Startup is initiated when this threshold is reached by any $V_{IN_}$ and $V_{ON_}$ > 0.9V (Note 8)	2.25		2.65	V
UVLO Hysteresis	$V_{UVLO,HYST}$			250		mV
UVLO Glitch Filter Reset Time	$t_{D, GF}$	V_{IN} < V_{UVLO} maximum pulse width to reset			10	µs
UVLO to Startup Delay	$t_{D,UVLO}$	Time input voltage must exceed V_{UVLO} before startup is initiated	20	37.5	60	ms
Input Power-Ready Threshold	V_{PWRRDY}	(Note 9)	0.9	0.95	1.0	V
Input Power-Ready Hysteresis	$V_{PWRHYST}$			50		mV
LOGIC AND TIMING						
POL Input Pullup	I_{POL}	POL = GND (MAX5927)	2	4	6	µA
LATCH Input Pullup	I_{LATCH}	LATCH = GND (MAX5927)	2	4	6	µA
MODE Input Voltage	V_{MODE}	MODE floating (default to sequencing mode)	1.0	1.25	1.5	V
Independent Mode Selection Threshold	$V_{INDEP, TH}$	V_{MODE} rising			0.4	V
Tracking Mode Selection Threshold	$V_{TRACK, TH}$	V_{MODE} rising	2.7			V

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

ELECTRICAL CHARACTERISTICS (continued)

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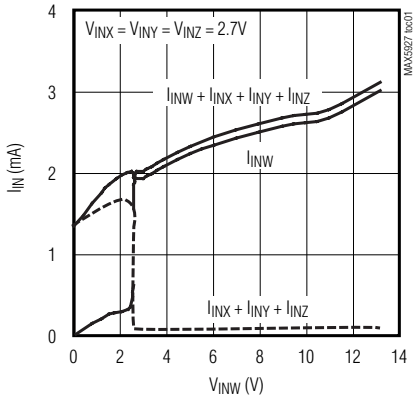
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MODE Input Impedance	R_{MODE}			200		kΩ
Autoretry Delay	t_{RETRY}	Delay time to restart after fault shutdown		64 x t_{START}		ms

Note 2: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: The slow-comparator threshold is adjustable. $V_{SC,TH} = R_{LIM}$ x 7.5µA + 25mV (see the *Typical Operating Characteristics*).
Note 4: The current-limit slow-comparator response time is weighed against the amount of overcurrent—the higher the overcurrent condition, the faster the response time (see the *Typical Operating Characteristics*).
Note 5: The startup period (t_{START}) is the time during which the slow comparator is ignored and the device acts as a current limiter by regulating the sense current with the fast comparator (see the *Startup Period* section).
Note 6: The current available at GATE is a function of V_{GATE} (see the *Typical Operating Characteristics*).
Note 7: After a fault triggered by the fast comparator, the gate is discharged by the strong discharge current.
Note 8: Each channel input while the other inputs are at +1V.
Note 9: Each channel input while any other input is at +3.3V.

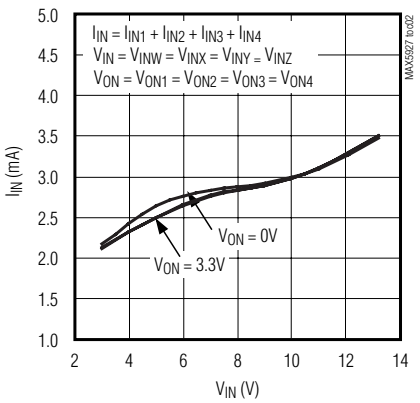
Typical Operating Characteristics

(Typical Operating Circuits, Q1 = Q2 = Q3 = Q4 = Fairchild FDB7090L, V_{IN1} = 12V, V_{IN2} = 5.0V, V_{IN3} = 3.3V, V_{IN4} = 1.0V, T_A = +25°C, unless otherwise noted. Channels 1 through 4 are identical in performance. Where characteristics are interchangeable, channels 1 through 4 are referred to as W, X, Y, and Z.)

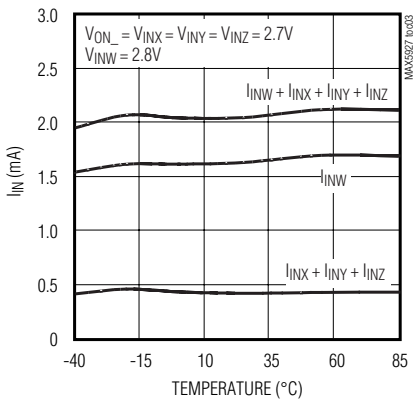
SUPPLY CURRENT vs. INPUT VOLTAGE



TOTAL SUPPLY CURRENT vs. INPUT VOLTAGE



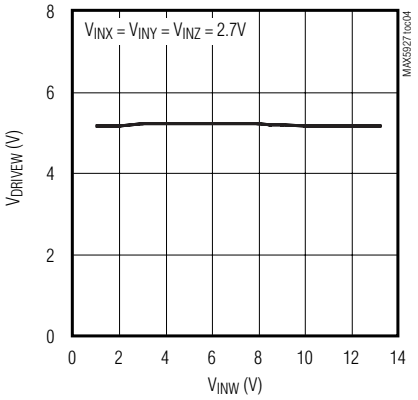
SUPPLY CURRENT vs. TEMPERATURE



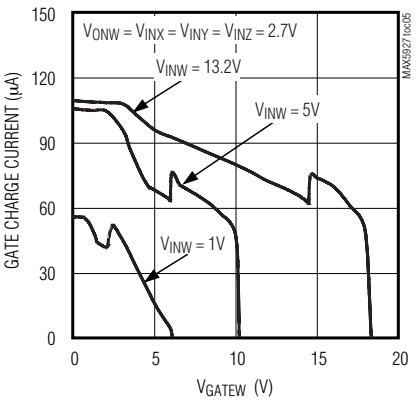
Typical Operating Characteristics (continued)

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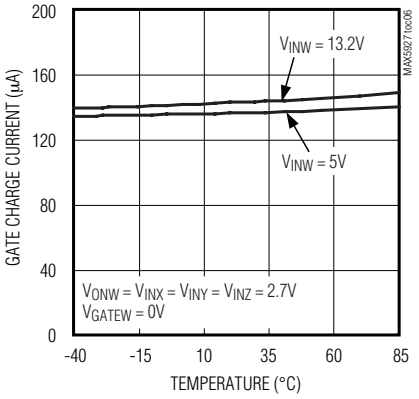
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



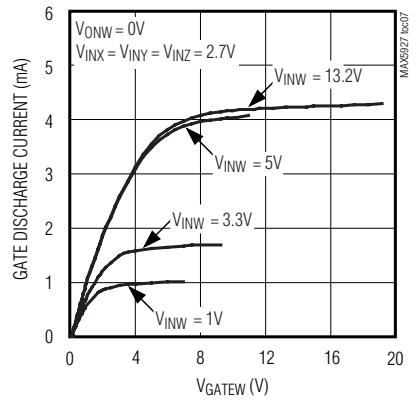
GATE CHARGE CURRENT vs. GATE VOLTAGE



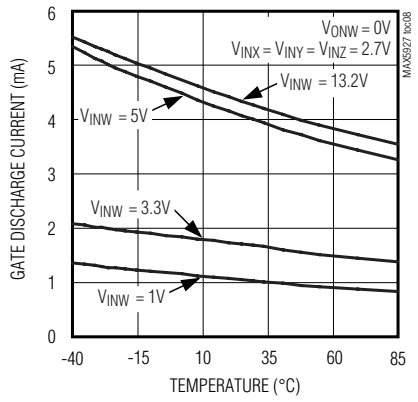
GATE CHARGE CURRENT vs. TEMPERATURE



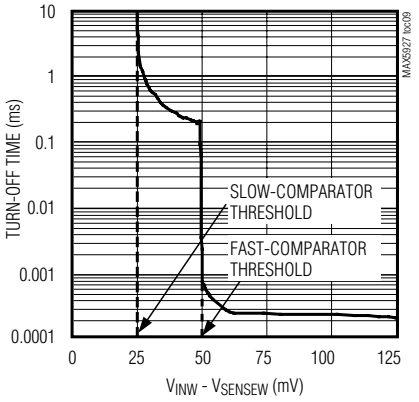
GATE DISCHARGE CURRENT (NORMAL) vs. GATE VOLTAGE



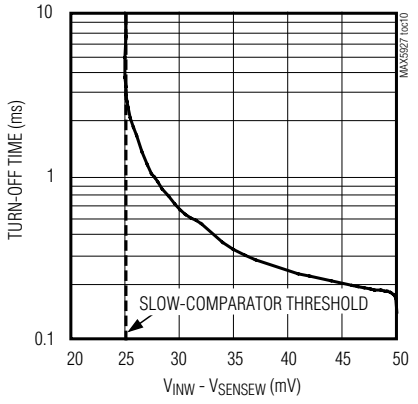
GATE DISCHARGE CURRENT (NORMAL) vs. TEMPERATURE



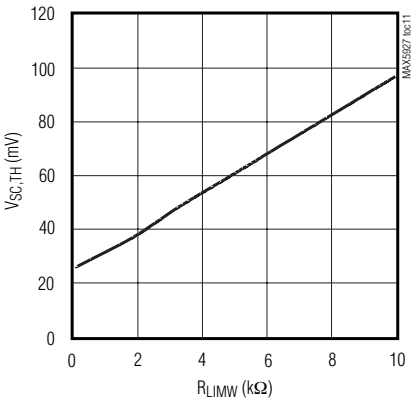
TURN-OFF TIME vs. SENSE VOLTAGE



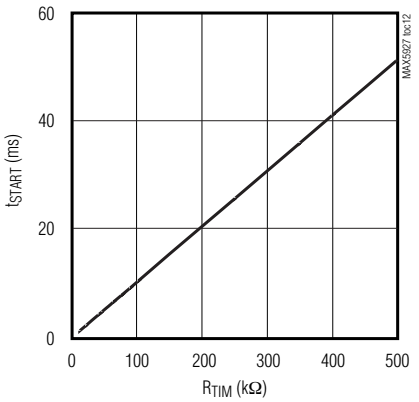
TURN-OFF TIME vs. SENSE VOLTAGE (EXPANDED SCALE)



SLOW-COMPARATOR THRESHOLD vs. R_{LIMW}



STARTUP PERIOD vs. R_{TIM}

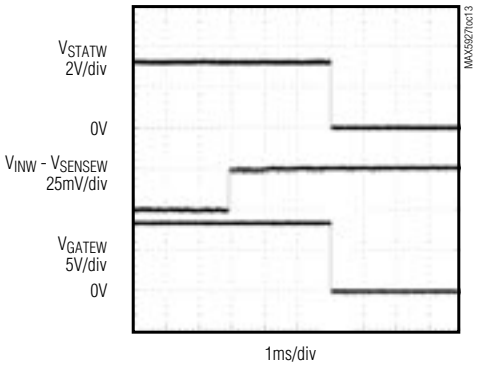


Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

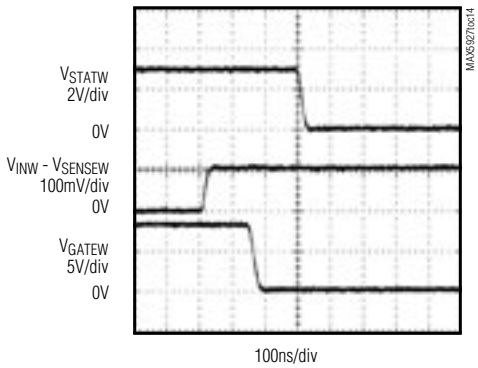
Typical Operating Characteristics (continued)

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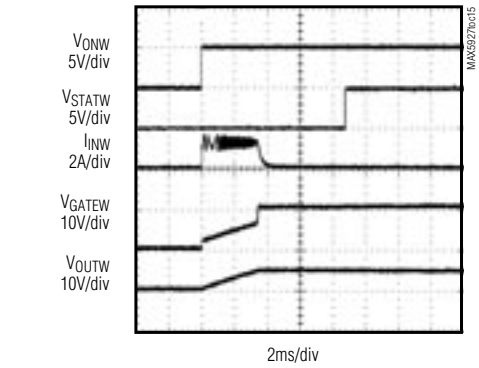
TURN-OFF TIME SLOW-COMPARATOR FAULT



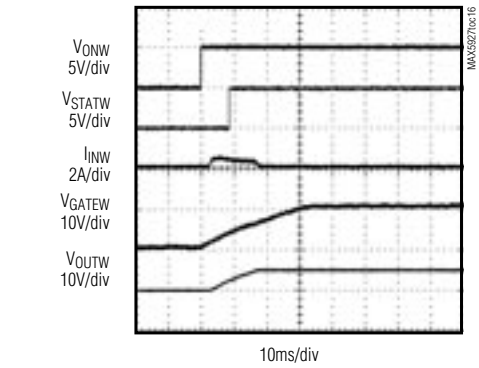
TURN-OFF TIME FAST-COMPARATOR FAULT



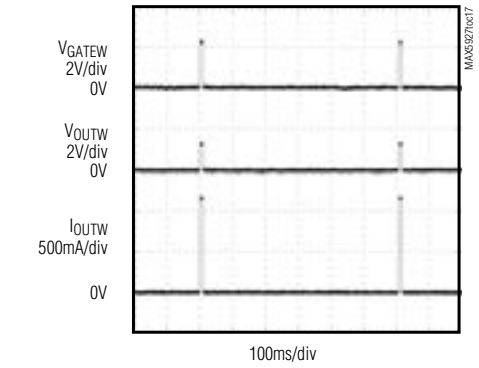
STARTUP WAVEFORMS FAST TURN-ON (C_{GATE} = 0nF, C_{BOARD} = 1000µF)



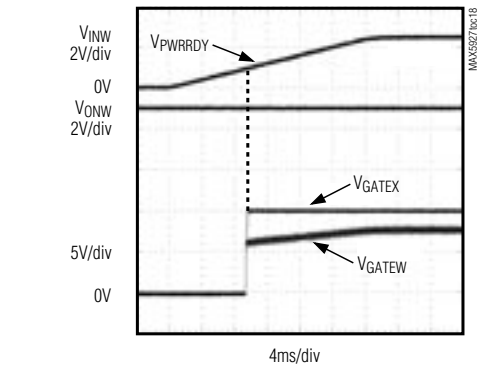
STARTUP WAVEFORMS SLOW TURN-ON (C_{GATE} = 0.22µF, C_{BOARD} = 1000µF)



AUTORETRY DELAY (TIME FLOATING)



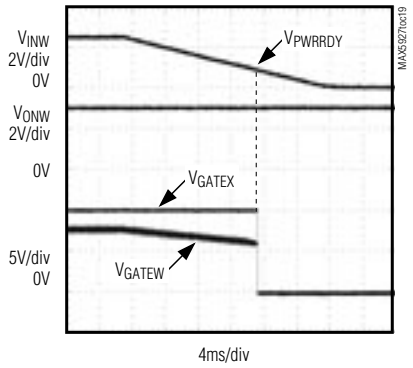
TURN-ON IN VOLTAGE-TRACKING MODE



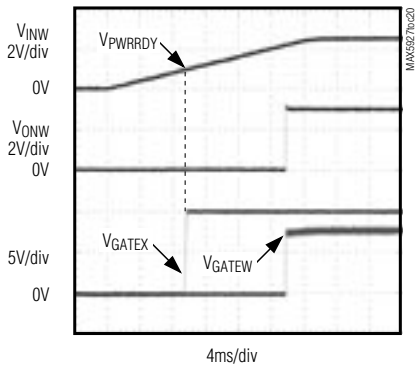
Typical Operating Characteristics (continued)

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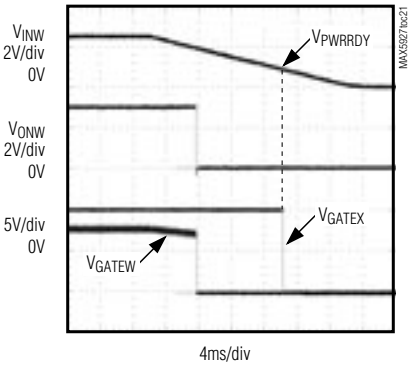
TURN-OFF IN VOLTAGE-TRACKING MODE



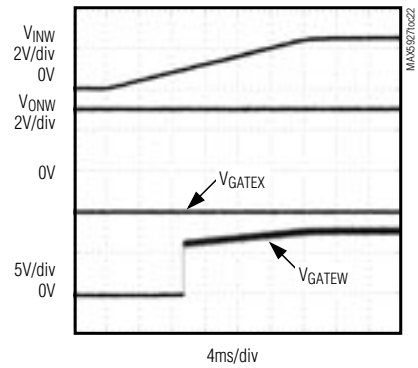
TURN-ON IN POWER-SEQUENCING MODE



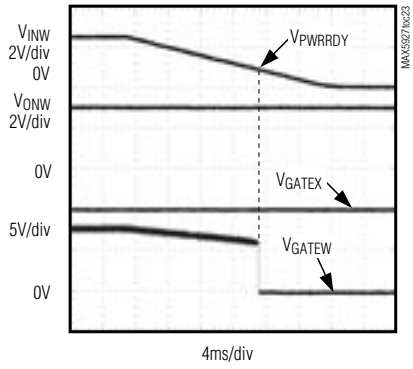
TURN-OFF IN POWER-SEQUENCING MODE



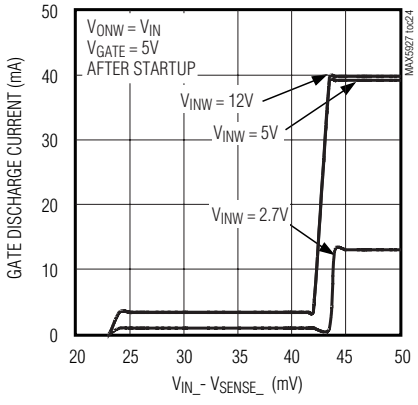
TURN-ON IN INDEPENDENT MODE



TURN-OFF IN INDEPENDENT MODE



STRONG GATE DISCHARGE CURRENT vs. OVERDRIVE



Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

Pin Description

PIN		NAME	FUNCTION
MAX5927	MAX5929		
1	4	IN1	Channel 1 Supply Input. Connect to a supply voltage from 1V to 13.2V and to one end of R_{SENSE1}. Bypass with a 0.1µF capacitor to ground.
2	5	SENSE1	Channel 1 Current-Sense Input. Connect SENSE1 to the drain of an external MOSFET and to one end of R_{SENSE1}.
3	6	GATE1	Channel 1 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
4	—	LIM4	Channel 4 Current-Limit Setting. Connect a resistor from LIM4 to GND to set current-trip level. Connect to GND for the default 25mV threshold. Do not leave open.
5	7	IN4	Channel 4 Supply Input. Connect to a supply voltage from 1V to 13.2V and to one end of R_{SENSE4}. Bypass with a 0.1µF capacitor to ground.
6	8	SENSE4	Channel 4 Current-Sense Input. Connect SENSE4 to the drain of an external MOSFET and to one end of R_{SENSE4}.
7	9	GATE4	Channel 4 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
8	10	STAT1	Open-Drain Status Signal for Channel 1. STAT1 asserts when hot swap is successful and t_{START} has elapsed. STAT1 deasserts if ON1 is low, or if channel 1 is turned off for any fault condition.
9	11	STAT2	Open-Drain Status Signal for Channel 2. STAT2 asserts when hot swap is successful and t_{START} has elapsed. STAT2 deasserts if ON2 is low, or if channel 2 is turned off for any fault condition.
10	12	TIM	Startup Timer Setting. Connect a resistor from TIM to GND to set the startup period. Leave TIM unconnected for the default startup period of 9ms. R_{TIM} must be between 4kΩ and 500kΩ.
11, 20	—	N.C.	No Connection. Not internally connected.
12	—	LATCH	Latch/Autoretry Selection Input. Connect LATCH to GND for autoretry mode after a fault. Leave LATCH open for latch mode.
13	13	STAT3	Open-Drain Status Signal for Channel 3. STAT3 asserts when hot swap is successful and t_{START} has elapsed. STAT3 deasserts if ON3 is low, or if channel 3 is turned off for any fault condition.
14	14	STAT4	Open-Drain Status Signal for Channel 4. STAT4 asserts when hot swap is successful and t_{START} has elapsed. STAT4 deasserts if ON4 is low, or if channel 4 is turned off for any fault condition.
15	15	BIAS	Supply Reference Output. The highest supply is available at BIAS for filtering. Connect a 1nF to 10nF ceramic capacitor from BIAS to GND. No other connections are allowed to this pin.
16	16	GND	Ground
17	17	GATE3	Channel 3 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
18	18	SENSE3	Channel 3 Current-Sense Input. Connect SENSE3 to the drain of an external MOSFET and to one end of R_{SENSE3}.
19	19	IN3	Channel 3 Supply Input. Connect to a supply voltage from 1V to 13.2V and to one end of R_{SENSE3}.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5927	MAX5929		
21	—	LIM3	Channel 3 Current-Limit Setting. Connect a resistor from LIM3 to GND to set current-trip level. Connect to GND for the default 25mV threshold. Do not leave open.
22	20	GATE2	Channel 2 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
23	21	SENSE2	Channel 2 Current-Sense Input. Connect SENSE2 to the drain of an external MOSFET and to one end of R_{SENSE2}.
24	22	IN2	Channel 2 Supply Input. Connect to a supply voltage from 1V to 13.2V and to one end of R_{SENSE2}.
25	—	LIM2	Channel 2 Current-Limit Setting. Connect a resistor from LIM2 to GND to set the current-trip level. Connect to GND for the default 25mV threshold. Do not leave open.
26	23	ON4	On/Off Channel 4 Control Input (see the *Mode* section)
27	24	ON3	On/Off Channel 3 Control Input (see the *Mode* section)
28	1	MODE	Mode Configuration Input. Mode is configured according to Table 1 as soon as one of the IN_ voltages exceeds UVLO and before turning on OUT_ (see the *Mode* section).
29	—	POL	STAT Output Polarity Select (See Table 3 and the *Status Output* Section)
30	2	ON2	On/Off Channel 2 Control Input (See the *Mode* Section)
31	3	ON1	On/Off Channel 1 Control Input (See the *Mode* Section)
32	—	LIM1	Channel 1 Current-Limit Setting. Connect a resistor from LIM1 to GND to set the current-trip level. Connect to GND for the default 25mV threshold. Do not leave open.
EP	—	EP	Exposed Pad. Leave EP floating or connect to GND.

Detailed Description

The MAX5927/MAX5929 are circuit-breaker ICs for hot-swap applications where a line card is inserted into a live backplane. The MAX5927/MAX5929 operate down to 1V provided one of the inputs is above 2.7V. Normally, when a line card is plugged in to a live backplane, the card's discharged filter capacitors provide low impedance that can momentarily cause the main power supply to collapse. The MAX5927/MAX5929 reside either on the backplane or on the removable card to provide inrush current limiting and short-circuit protection. This is achieved by using external N-channel MOSFETs, external current-sense resistors, and on-chip comparators. The startup period and current-limit threshold of the MAX5927/MAX5929 can be adjusted with external resistors. Figure 1 shows the MAX5927/MAX5929 functional diagram.

The MAX5927 offers four programmable current limits, selectable fault management mode, and selectable STAT_ output polarity. The MAX5929 features fixed current limits, and a variety of fault management and STAT_ polarity option combinations.

Mode

The MAX5927/MAX5929 supports three modes of operation: voltage-tracking, power-sequencing, and independent mode. Select the appropriate mode according to Table 1.

Voltage-Tracking Mode

Connect MODE high to enter voltage-tracking mode. While in voltage-tracking mode, all channels turn on and off together. To turn all channels on:

- At least one $V_{IN_}$ must exceed V_{UVLO} (2.45V) for the UVLO to startup delay (37.5ms).
- All $V_{IN_}$ must exceed V_{PWRRDY} (0.95V).
- All $V_{ON_}$ must exceed $V_{ON,TH}$ (0.875V).
- No faults may be present on any channel.

Table 1. Operational Mode Selection

MODE	OPERATION
High (Connect to BIAS)	Voltage tracking
OPEN	Power sequencing
GND	Independent

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

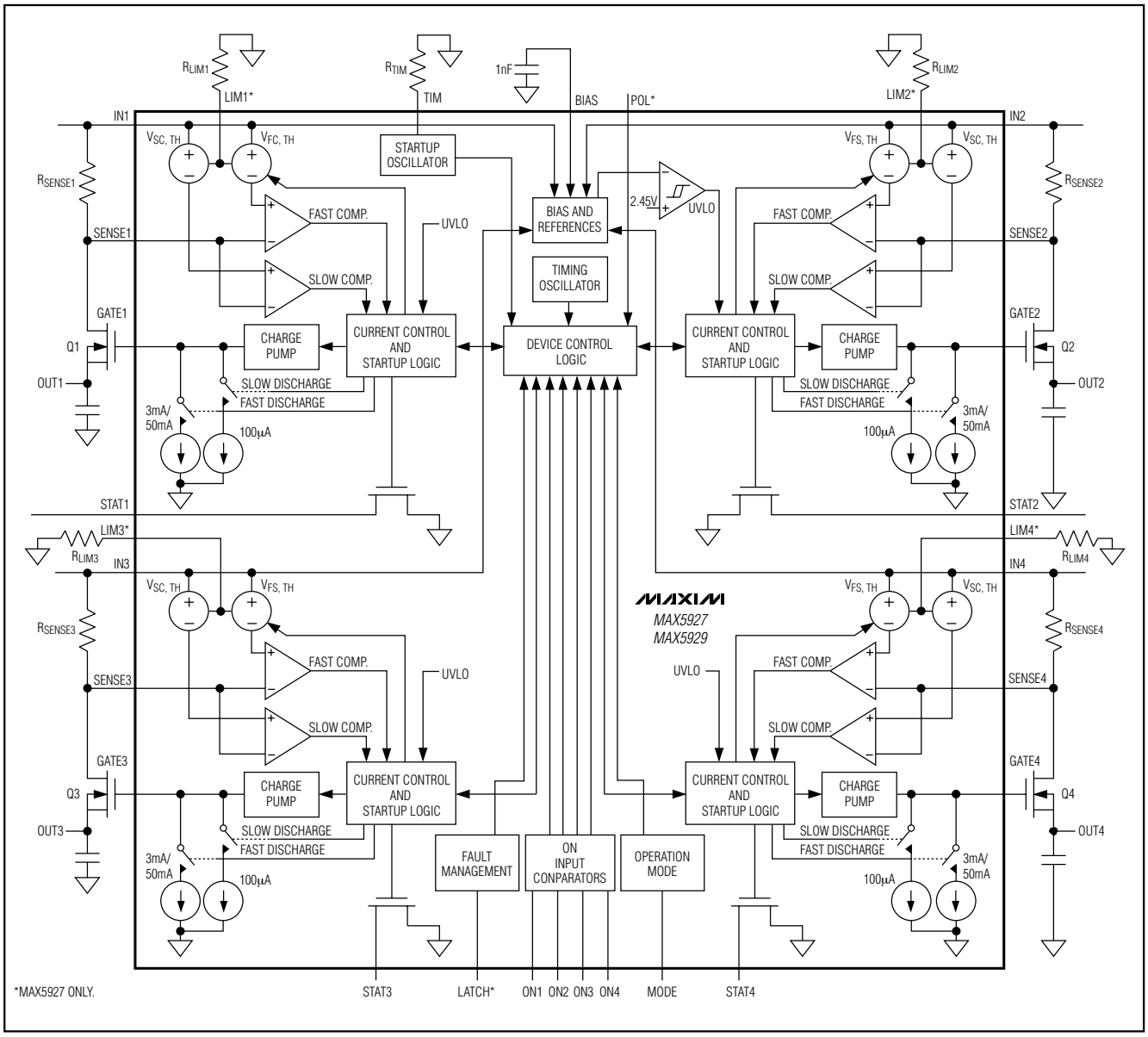


Figure 1. Functional Diagram

The MAX5927/MAX5929 turn off all channels if any of the above conditions are not met. After a fault-latched shutdown, cycle any of the ON_ inputs to unlatch and restart all channels.

Power-Sequencing Mode

Leave MODE floating to enter power-sequencing mode. While in power-sequencing mode, the MAX5927/MAX5929 turn on and off each channel depending on the state of the corresponding $V_{ON_}$. To turn on a given channel:

- At least one $V_{IN_}$ must exceed V_{UVLO} (2.45V) for the UVLO to startup delay (37.5ms).
- All $V_{IN_}$ must exceed V_{PWRRDY} (0.95V).
- The corresponding $V_{ON_}$ must exceed $V_{ON,TH}$ (0.875V).
- No faults may be present on any channel.

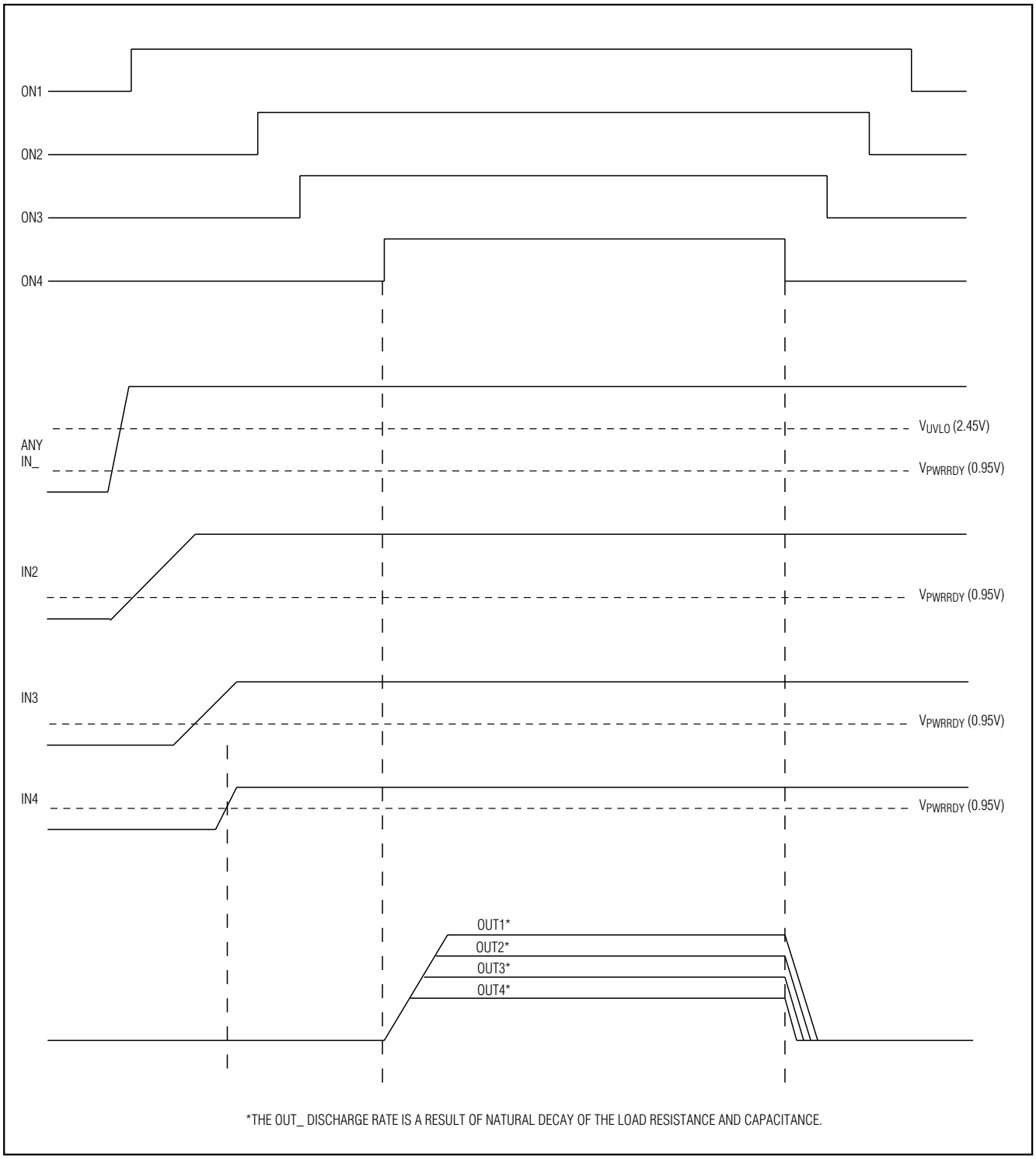
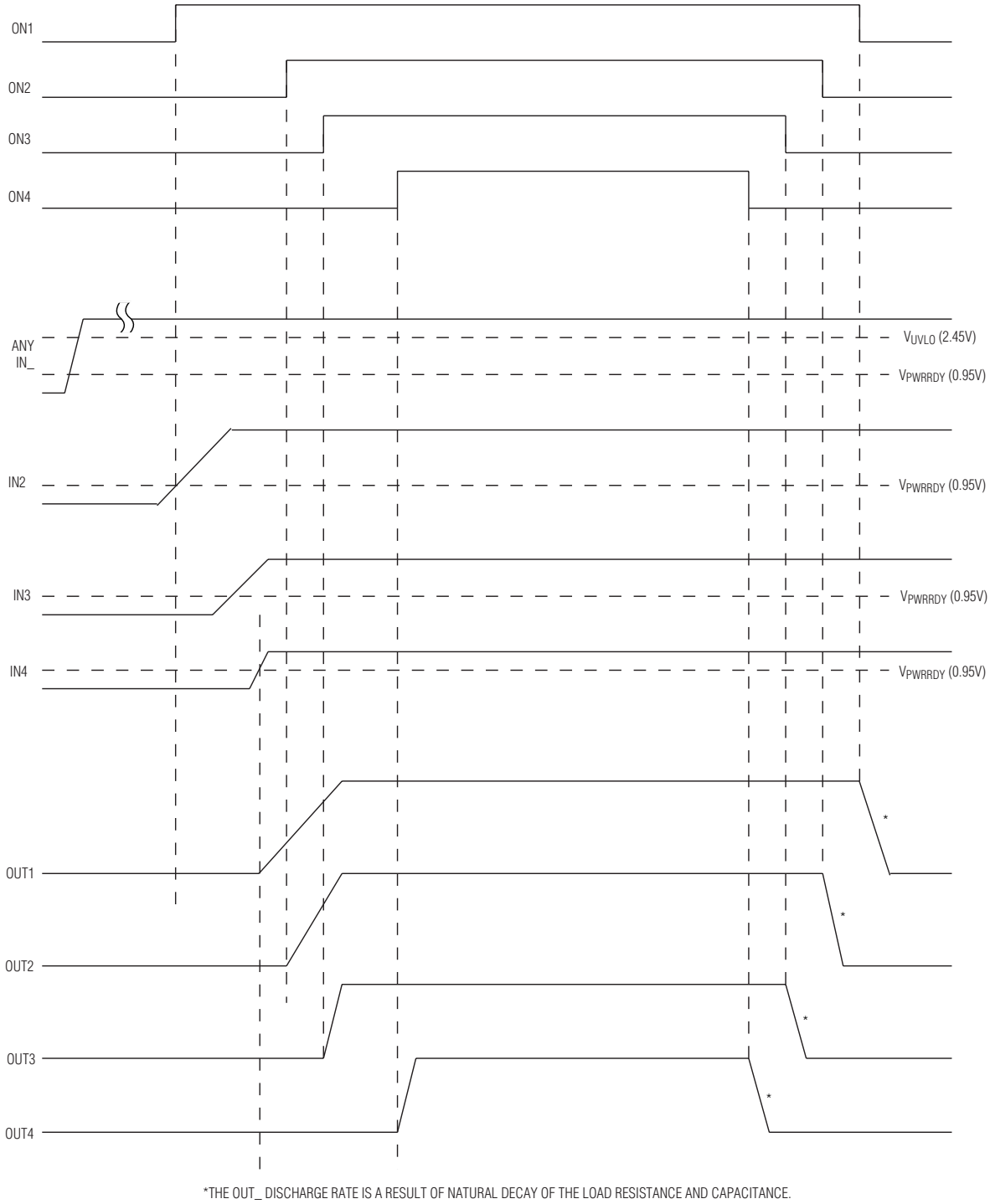


Figure 2. Voltage-Tracking Timing Diagram (Provided $t_{D, UVLO}$ Requirement is Met)



*THE OUT_ DISCHARGE RATE IS A RESULT OF NATURAL DECAY OF THE LOAD RESISTANCE AND CAPACITANCE.

Figure 3. Power-Sequencing Timing Diagram (Provided $t_{D,\ UVLO}$ Requirement is Met)

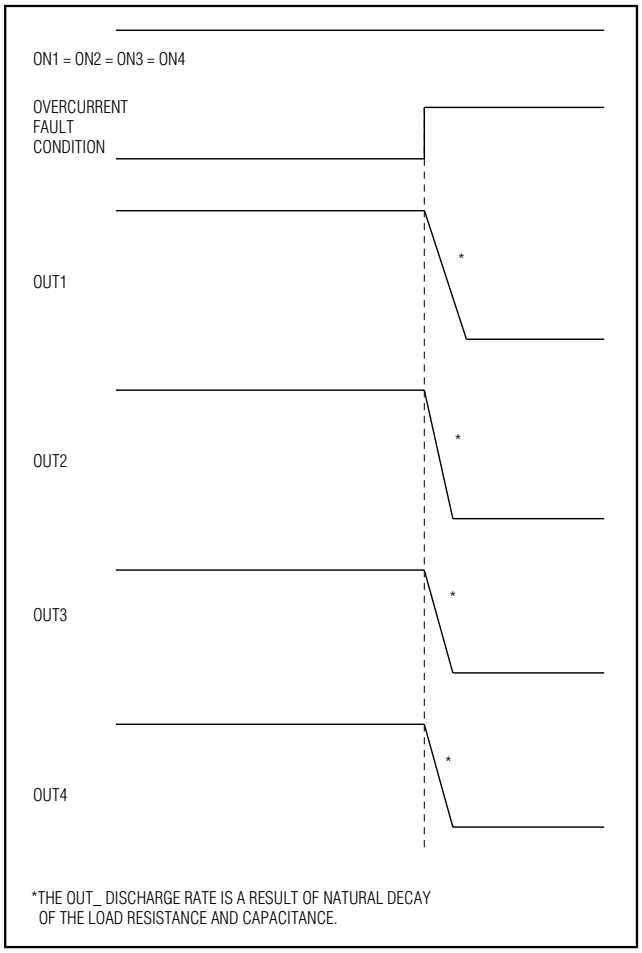


Figure 4. Power-Sequencing Fault Turn-Off

The MAX5927/MAX5929 turn off all channels if any of the above conditions are not met. After a fault-latched shutdown, cycle any of the ON_ inputs to unlatch and restart all channels, depending on the corresponding $V_{ON_}$ state.

Independent Mode

Connect MODE to GND to enter independent mode. While in independent mode, the MAX5927/MAX5929 provide complete independent control for each channel. To turn on a given channel:

- At least one $V_{IN_}$ must exceed V_{UVLO} (2.45V) for the UVLO to startup delay (37.5ms)
- The corresponding $V_{IN_}$ must exceed V_{PWRRDY} (0.95V)
- The corresponding $V_{ON_}$ must exceed $V_{ON,TH}$ (0.875V)

The MAX5927/MAX5929 turn off the corresponding channel if any of the above conditions are not met. During a fault condition on a given channel only, the affected channel is disabled. After a fault-latched shutdown, recycle the corresponding ON_ inputs to unlatch and restart only the corresponding channel.

Startup Period

R_{TIM} sets the duration of the startup period from 0.4ms (R_{TIM} = 4kΩ) to 50ms (R_{TIM} = 500kΩ) (see the *Setting the Startup Period, R_{TIM}* section). The default startup period is fixed at 9ms when TIM is floating. The startup period begins after the turn-on conditions are met as described in the *Mode* section, and the device is not latched or in its autoretry delay (see the *Latched and Autoretry Fault Management* section).

The MAX5927/MAX5929 limit the load current if an overcurrent fault occurs during startup instead of completely turning off the external MOSFETs. The slow comparator is disabled during the startup period and the load current can be limited in two ways:

1) Slowly enhancing the MOSFETs by limiting the MOSFET gate-charging current.
2) Limiting the voltage across the external current-sense resistor.

During the startup period, the gate-drive current is limited to 100µA and decreases with the increase of the gate voltage (see the *Typical Operating Characteristics*). This allows the controller to slowly enhance the MOSFETs. If the fast comparator detects an overcurrent, the MAX5927/MAX5929 regulate the gate voltage to ensure that the voltage across the sense resistor does not exceed $V_{SU,TH}$. This effectively regulates the inrush current during startup.

Figure 6 shows the startup waveforms. STAT_ is asserted immediately after the startup period if no fault condition is present.

VariableSpeed/BiLevel Fault Protection

VariableSpeed/BiLevel fault protection incorporates comparators with different thresholds and response times to monitor the load current (Figure 7). During the startup period, protection is provided by limiting the load current. Protection is provided in normal operation (after the startup period has expired) by discharging the MOSFET gates with a 3mA/50mA pulldown current in response to a fault condition. After a fault, STAT_ is deasserted, the MAX5929L stays latched off and the MAX5929A automatically restart. Use the MAX5927 LATCH input to control whether the STAT_ outputs latch off or Autoretry after a fault condition (see the *Latched and Autoretry Fault Management* section).

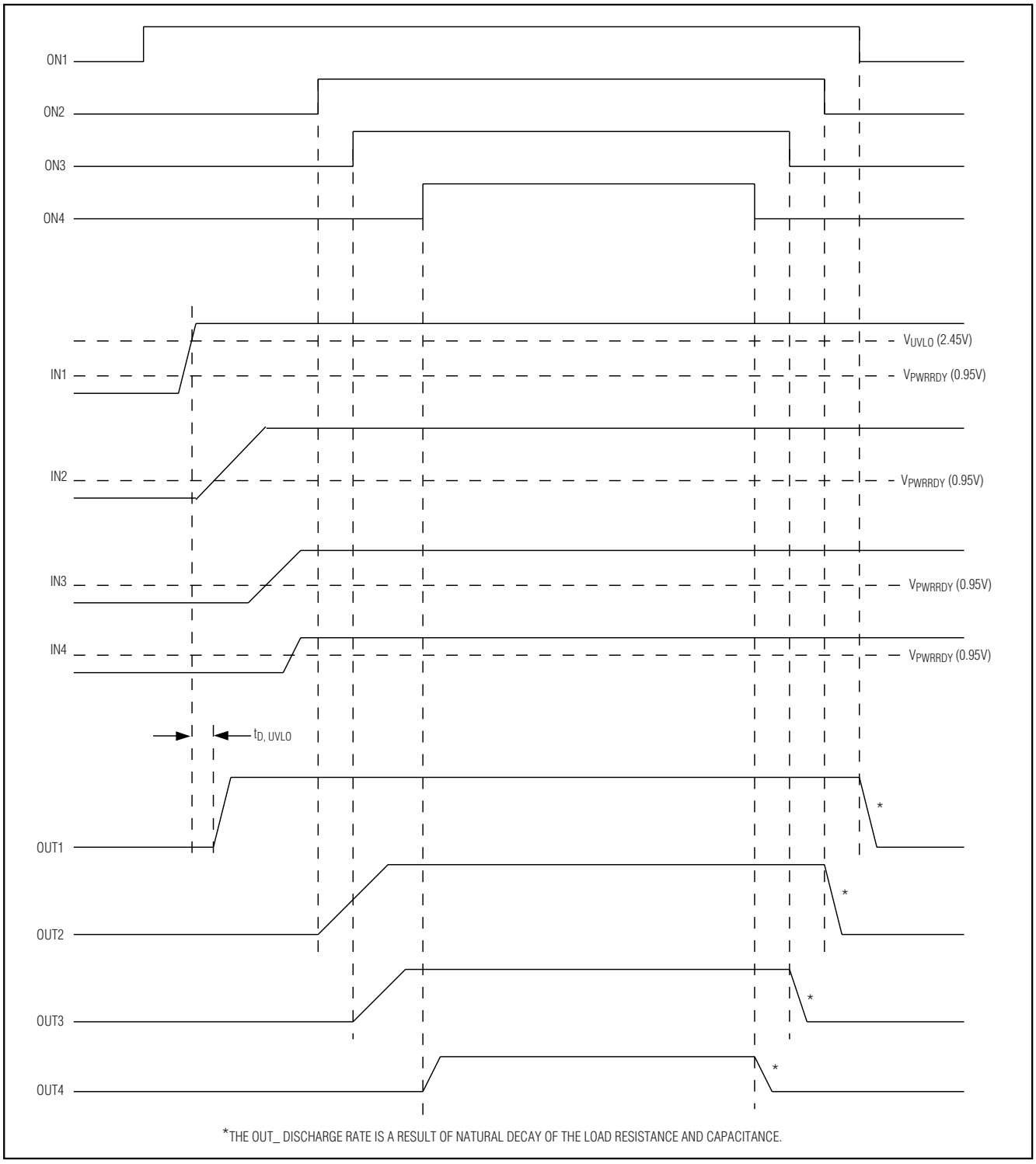


Figure 5. Independent Mode Timing Diagram

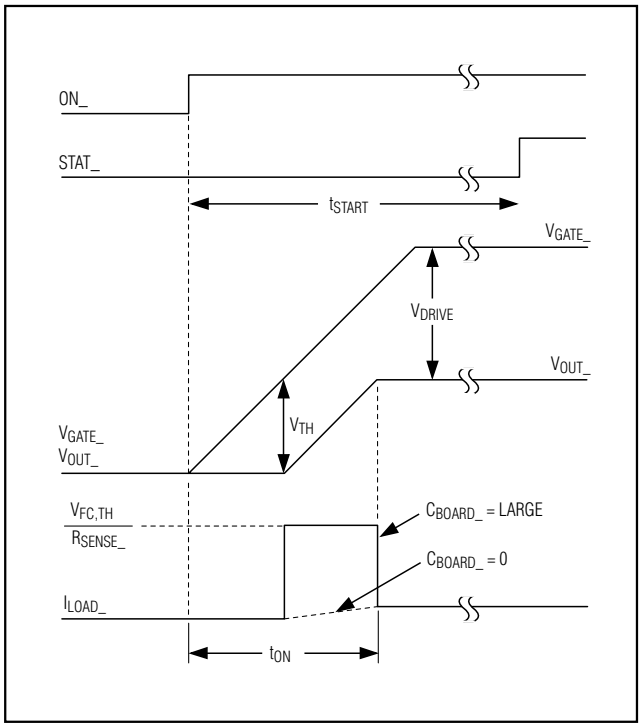


Figure 6. Independent Mode Startup Waveforms

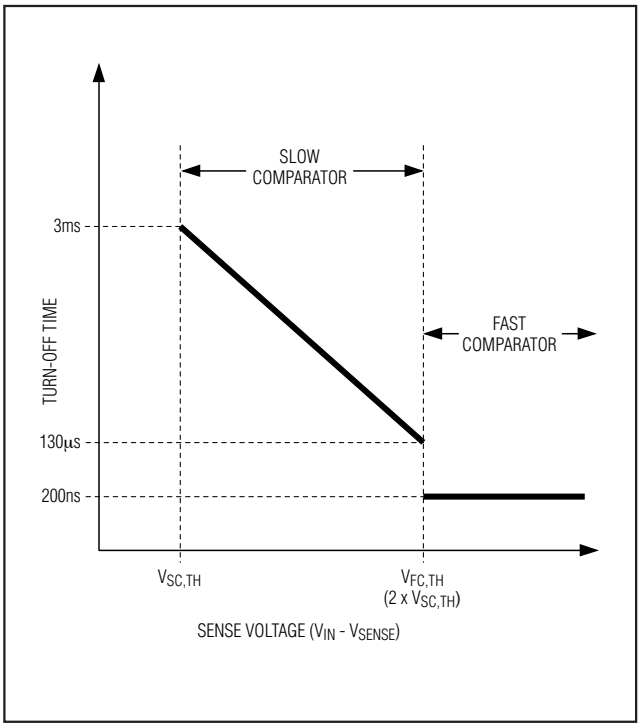


Figure 7. VariableSpeed/BiLevel Response

Slow-Comparator Startup Period

The slow comparator is disabled during the startup period while the external MOSFETs are turning on. Disabling the slow comparator allows the device to ignore the higher-than-normal inrush current charging the board capacitors when a card is first plugged into a live backplane.

Slow-Comparator Normal Operation

After the startup period is complete, the slow comparator is enabled and the device enters normal operation. The comparator threshold voltage ($V_{SC,TH}$) is adjustable from 25mV to 100mV. The slow-comparator response time is 3ms for a 1mV overdrive. The response time decreases to 100µs with a large overdrive. The variable-speed response time allows the MAX5927/MAX5929 to ignore low-amplitude momentary glitches, thus increasing system noise immunity. After an extended overcurrent condition, a fault is generated, STAT_ outputs are deasserted, and the MOSFET gates are discharged with a 3mA pulldown current.

Fast-Comparator Startup Period

During the startup period, the fast comparator regulates the gate voltages to ensure that the voltage across the sense resistor does not exceed the startup fast-comparator threshold voltage ($V_{SU,TH}$), $V_{SU,TH}$ is scaled to two times the slow-comparator threshold ($V_{SC,TH}$).

Fast-Comparator Normal Operation

In normal operation, if the load current reaches the fast-comparator threshold, a fault is generated, STAT_ is deasserted, and the MOSFET gates are discharged with a strong 50mA pulldown current. This happens in the event of a serious current overload or a dead short. The fast-comparator threshold voltage ($V_{FC,TH}$) is scaled to two times the slow-comparator threshold ($V_{SC,TH}$). This comparator has a fast response time of 200ns (Figure 7).

Undervoltage Lockout (UVLO)

The UVLO prevents the MAX5927/MAX5929 from turning on the external MOSFETs until one input voltage exceeds the UVLO threshold (2.45V) for $t_{D,UVLO}$. The MAX5927/MAX5929 use power from the highest input voltage rail for the charge pumps. This allows for more efficient charge-pump operation. The highest $V_{IN_}$ is provided as an output at BIAS. The UVLO protects the external MOSFETs from an insufficient gate-drive volt-

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

Table 2. Selecting Fault Management Mode (MAX5927)

LATCH	FAULT MANAGEMENT
Floating	Fault condition latches MOSFETs off
Low	Autoretry mode

Table 3. Selecting STAT_ Polarity (MAX5927)

POL	STAT_
Low	Asserts low
Floating	Asserts high (open drain)

age. $t_{D,UVLO}$ ensures that the board is fully inserted into the backplane and that the input voltages are stable. The MAX5927/MAX5929 include a UVLO glitch filter, $t_{D,GF}$, to reject all input voltage noise and transients. Bringing all input supplies below the UVLO threshold for longer than $t_{D,GF}$ reinitiates $t_{D,UVLO}$ and the startup period, t_{START}. See Figure 8 for an example of automatic turn-on function.

Latched and Autoretry Fault Management

The MAX5929L always latch the external MOSFETs off when an overcurrent fault is detected, and the MAX5929A are always in autoretry mode. The MAX5927 can be configured to either latch the external MOSFETs off or to autoretry (see Table 2). Toggling ON_ below 0.875V for at least 100µs clears the MAX5929L or MAX5927 (LATCH = FLOAT) fault and reinitiates the startup period. Similarly, the MAX5929A or MAX5927 (LATCH = GND) turn the external MOSFETs off when an overcurrent fault is detected, then automatically restart after the autoretry delay that is internally set to 64 times t_{START}.

Status Outputs (STAT_)

The status (STAT_) outputs are open-drain outputs that assert when hot swap is successful and t_{START} has elapsed. STAT_ deasserts if ON_ is low or if the channel is turned off for any fault condition.

The polarity of the STAT_ outputs is selected using POL for the MAX5927 (see Table 3). Tables 4 and 5 contain the MAX5927/MAX5929 truth tables.

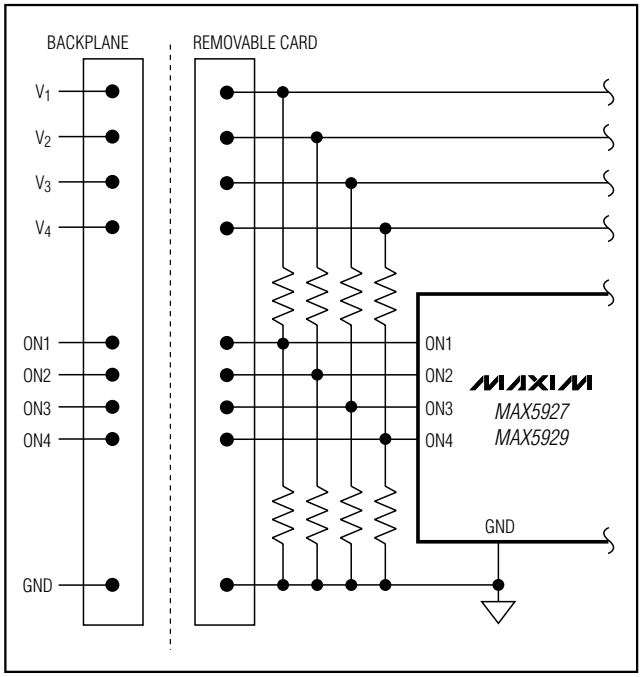


Figure 8. Automatic Turn-On when Input Voltages are Above their Respective Undervoltage Lockout Threshold (Provided $t_{D,UVLO}$ Requirement is Met)

Applications Information

Component Selection

N-Channel MOSFETs

Select the external MOSFETs according to the application's current levels. Table 6 lists recommended components. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ causes output ripple if there is a pulsating load. Determine the device power rating to accommodate a short-circuit condition on the board at startup and when the device is in autoretry mode (see the *MOSFET Thermal Considerations* section).

Using these devices in latched mode allows the use of MOSFETs with lower power ratings. A MOSFET typically withstands single-shot pulses with higher dissipation than the specified package rating. Table 7 lists some recommended MOSFET manufacturers.

Table 4. Status Output Truth Table: Voltage-Tracking and Power-Sequencing Modes

PART	CHANNEL 1 FAULT	CHANNEL 2 FAULT	CHANNEL 3 FAULT	CHANNEL 4 FAULT	STAT1/ GATE1*	STAT2/ GATE2*	STAT3/ GATE3*	STAT4/ GATE4*
MAX5927 (POL = 1), MAX5929_H	Yes	X	X	X	L/OFF	L/OFF	L/OFF	L/OFF
	X	Yes	X	X	L/OFF	L/OFF	L/OFF	L/OFF
	X	X	Yes	X	L/OFF	L/OFF	L/OFF	L/OFF
	X	X	X	Yes	L/OFF	L/OFF	L/OFF	L/OFF
	No	No	No	No	H/ON	H/ON	H/ON	H/ON
MAX5927 (POL = 0), MAX5929_L	Yes	X	X	X	H/OFF	H/OFF	H/OFF	H/OFF
	X	Yes	X	X	H/OFF	H/OFF	H/OFF	H/OFF
	X	X	Yes	X	H/OFF	H/OFF	H/OFF	H/OFF
	X	X	X	Yes	H/OFF	H/OFF	H/OFF	H/OFF
	No	No	No	No	L/ON	L/ON	L/ON	L/ON

**L = Low, H = High.*

Table 5. Status Output Truth Table: Independent Mode

CHANNEL 1 FAULT	CHANNEL 2 FAULT	CHANNEL 3 FAULT	CHANNEL 4 FAULT	STAT1/ GATE1	STAT2/ GATE2	STAT3/ GATE3	STAT4/ GATE4
Yes	Yes	Yes	Yes	Unasserted/OFF	Unasserted/OFF	Unasserted/OFF	Unasserted/OFF
Yes	Yes	Yes	No	Unasserted/OFF	Unasserted/OFF	Unasserted/OFF	Asserted/ON
Yes	Yes	No	Yes	Unasserted/OFF	Unasserted/OFF	Asserted/ON	Unasserted/OFF
Yes	Yes	No	No	Unasserted/OFF	Unasserted/OFF	Asserted/ON	Asserted/ON
Yes	No	Yes	Yes	Unasserted/OFF	Asserted/ON	Unasserted/OFF	Unasserted/OFF
Yes	No	Yes	No	Unasserted/OFF	Asserted/ON	Unasserted/OFF	Asserted/ON
Yes	No	No	Yes	Unasserted/OFF	Asserted/ON	Asserted/ON	Unasserted/OFF
Yes	No	No	No	Unasserted/OFF	Asserted/ON	Asserted/ON	Asserted/ON
No	Yes	Yes	Yes	Asserted/ON	Unasserted/OFF	Unasserted/OFF	Unasserted/OFF
No	Yes	Yes	No	Asserted/ON	Unasserted/OFF	Unasserted/OFF	Asserted/ON
No	Yes	No	Yes	Asserted/ON	Unasserted/OFF	Asserted/ON	Unasserted/OFF
No	Yes	No	No	Asserted/ON	Unasserted/OFF	Asserted/ON	Asserted/ON
No	No	Yes	Yes	Asserted/ON	Asserted/ON	Unasserted/OFF	Unasserted/OFF
No	No	Yes	No	Asserted/ON	Asserted/ON	Unasserted/OFF	Asserted/ON
No	No	No	Yes	Asserted/ON	Asserted/ON	Asserted/ON	Unasserted/OFF
No	No	No	No	Asserted/ON	Asserted/ON	Asserted/ON	Asserted/ON

(Note: STAT_ is asserted when hot swap is successful and t_{ON} has elapsed. STAT_ is unasserted during a fault)

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

Table 6. Recommended N-Channel MOSFETs

PART NUMBER	MANUFACTURER	DESCRIPTION
IRF7413	International Rectifier	11mΩ, 8-pin SO, 30V
IRF7401		22mΩ, 8-pin SO, 20V
IRL3502S		6mΩ, D²PAK, 20V
MMSF3300	Motorola	20mΩ, 8-pin SO, 30V
MMSF5N02H		30mΩ, 8-pin SO, 20V
MTB60N05H		14mΩ, D²PAK, 50V
FDS6670A	Fairchild	10mΩ, 8-pin SO, 30V
ND8426A		13.5mΩ, 8-pin SO, 20V
FDB8030L		4.5mΩ, D²PAK, 30V

Table 7. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistors	Dale-Vishay	402-562-3131	www.vishay.com
	IRC	704-264-8861	www.irctt.com
MOSFETs	International Rectifier	310-233-3331	www.irf.com
	Fairchild	888-522-5372	www.fairchildsemi.com
	Motorola	602-224-3576	www.mot-sps.com/ppd

Sense Resistor

The slow-comparator threshold voltage is adjustable from 25mV to 100mV. Select a sense resistor that causes a drop equal to the slow-comparator threshold voltage at a current level above the maximum normal operating current. Typically, set the overload current at 1.2 to 1.5 times the full load current. The fast-comparator threshold is two times the slow-comparator threshold in normal operating mode. Choose the sense resistor power rating to be greater than or equal to 2 x ($I_{OVERLOAD}$) x $V_{SC,TH}$. Table 7 lists some recommended sense resistor manufacturers.

Slow-Comparator Threshold, R_{LIM} (MAX5927)

The slow-comparator threshold voltage is adjustable from 25mV to 100mV, allowing designers to fine-tune the current-limit threshold for use with standard-value sense resistors. Low slow-comparator thresholds allow for increased efficiency by reducing the power dissipated by the sense resistor. Furthermore, the low 25mV slow-comparator threshold is beneficial when operating with supply rails down to 1V because it allows a small percentage of the overall output voltage to be used for current sensing. The VariableSpeed/BiLevel fault protection feature offers inherent system immunity against load transients and noise. This allows the slow-comparator threshold to be set close to the maximum normal operating level without experiencing nuisance faults. To adjust the slow-comparator threshold, calculate R_{LIM} as follows:

$$R_{LIM} = \frac{V_{TH} - 25mV}{7.5\mu A}$$

where V_{TH} is the desired slow-comparator threshold voltage. Shorting LIM_ to GND sets V_{TH} to 25mV. **Do not leave LIM_ open.**

Setting the Startup Period, R_{TIM}

The startup period (t_{START}) is adjustable from 0.4ms to 50ms. The adjustable startup period feature allows systems to be customized for MOSFET gate capacitance and board capacitance (C_{BOARD}). The startup period is adjusted with a resistor connected from TIM to GND (R_{TIM}). R_{TIM} must be between 4kΩ and 500kΩ. The startup period has a default value of 9ms when TIM is left floating. Calculate R_{TIM} with the following equation:

$$R_{TIM} = \frac{t_{START}}{128 \times 800pF}$$

where t_{START} is the desired startup period.

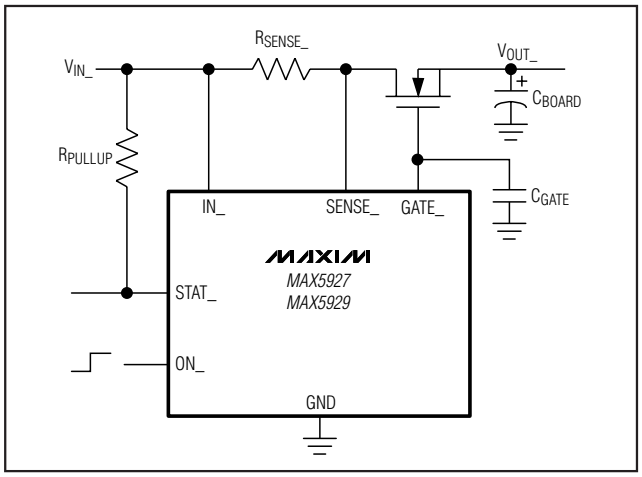


Figure 9. Operating with an External Gate Capacitor

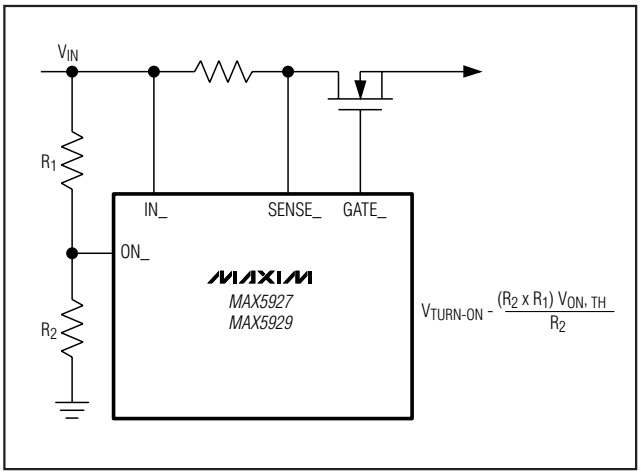


Figure 10. Adjustable Undervoltage Lockout

Startup Sequence

There are two ways of completing the startup sequence. **Case A** describes a startup sequence that slowly turns on the MOSFETs by limiting the gate charge. **Case B** uses the current-limiting feature and turns on the MOSFETs as fast as possible while still preventing a high inrush current. The output voltage ramp-up time (t_{ON}) is determined by the longer of the two timings, case A and case B. Set the startup timer (t_{START}) to be longer than t_{ON} to guarantee enough time for the output voltage to settle.

Case A: Slow Turn-On (Without Current Limit)

There are two ways to turn on the MOSFETs without reaching the fast-comparator current limit:

- If the board capacitance (C_{BOARD}) is small, the inrush current is low.
- If the gate capacitance is high, the MOSFETs turn on slowly.

In both cases, the turn-on time is determined only by the charge required to enhance the MOSFET. The small 100µA gate-charging current effectively limits the output voltage dV/dt. Connecting an external capacitor between GATE and GND extends the turn-on time. The time required to charge/discharge a MOSFET is as follows:

$$t = \frac{C_{GATE} \times \Delta V_{GATE} + Q_{GATE}}{I_{GATE}}$$

where:

C_{GATE} is the external gate to ground capacitance (Figure 9),

ΔV_{GATE} is the change in gate charge,

Q_{GATE} is the MOSFET total gate charge,

I_{GATE} is the gate-charging/discharging current.

In this case, the inrush current depends on the MOSFET gate-to-drain capacitance (C_{rss}) plus any additional capacitance from GATE to GND (C_{GATE}), and on any load current (I_{LOAD}) present during the startup period.

$$I_{INRUSH} = \frac{C_{BOARD}}{C_{rss} + C_{GATE}} \times I_{GATE} + I_{LOAD}$$

Example: Charging and discharging times using the Fairchild FDB7030L MOSFET

If V_{IN1} = 5V then GATE1 charges up to 10.4V (V_{IN1} + V_{DRIVE}), therefore ΔV_{GATE} = 10.4V. The manufacturer's data sheet specifies that the FDB7030L has approximately 60nC of gate charge and C_{rss} = 600pF. The MAX5927/MAX5929 have a 100µA gate-charging current and a 3mA/50mA normal/strong discharging current. C_{BOARD} = 6µF and the load does not draw any current during the startup period. With no gate capacitor, the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 0} \times 100\mu A + 0 = 1A$$

$$I_{CHARGE} = \frac{0 \times 10.4V + 60nC}{100\mu A} = 0.6ms$$

$$t_{DISCHARGE} = \frac{0 \times 10.4V + 60nC}{3mA} = 0.02ms$$

$$t_{DISCHARGE(STRONG)} = \frac{0 \times 10.4V + 60nC}{50mA} = 1.2\mu s$$

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

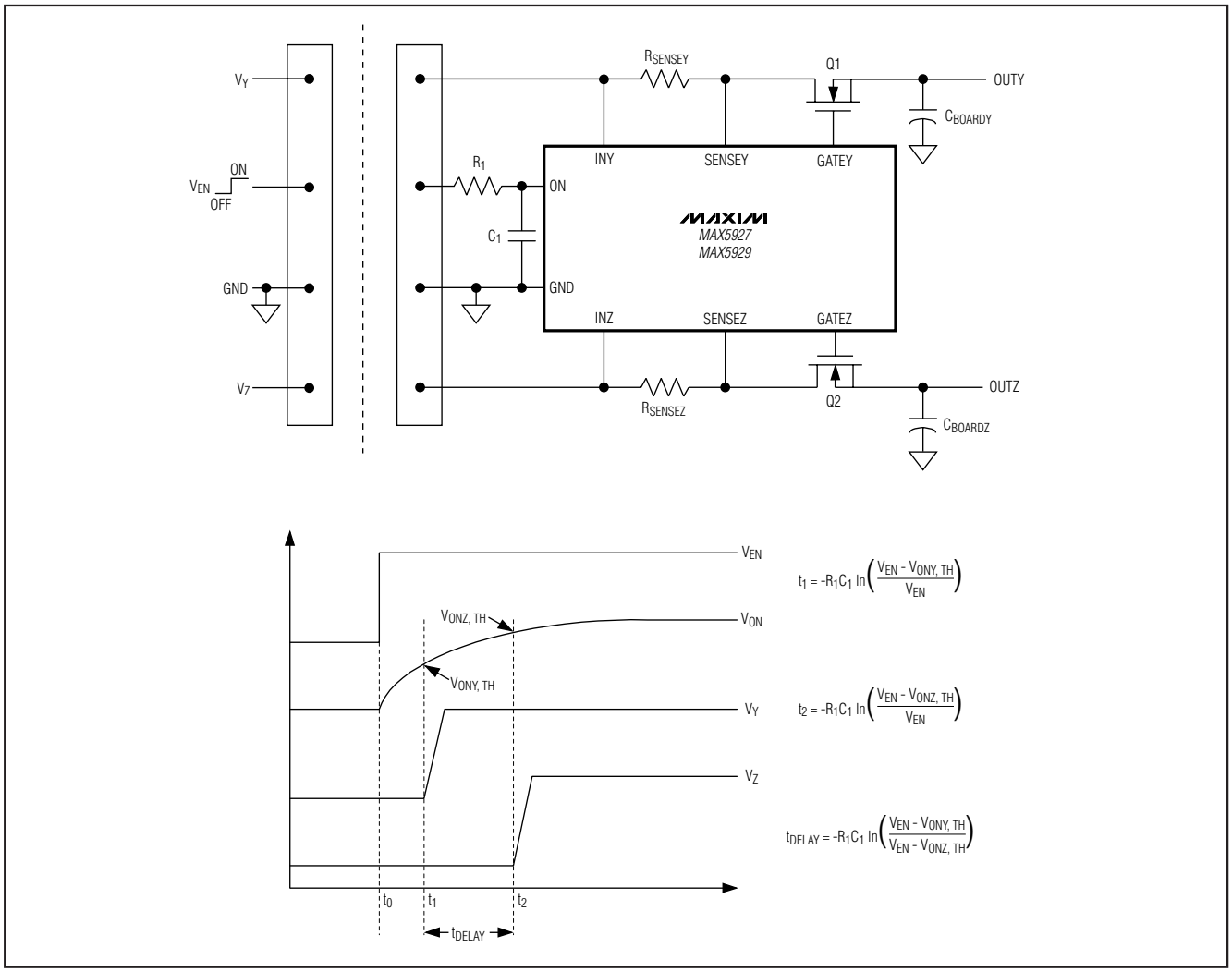


Figure 11. Power Sequencing: Channel Z Turns On t_{DELAY} After Channel Y

With a 22nF gate capacitor, the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 22nF} \times 100\mu A + 0 = 26.5mA$$

$$t_{CHARGE} = \frac{22nF \times 10.4V + 60nC}{100\mu A} = 2.89ms$$

$$t_{DISCHARGE} = \frac{22nF \times 10.4V + 60nC}{3mA} = 0.096ms$$

$$t_{DISCHARGE(STRONG)} = \frac{22nF \times 10.4V + 60nC}{50mA} = 5.8\mu s$$

Case B: Fast Turn-On (With Current Limit)

In applications where the board capacitance (C_{BOARD}) is high, the inrush current causes a voltage drop across R_{SENSE} that exceeds the startup fast-comparator threshold. The fast comparator regulates the voltage across the sense resistor to $V_{FC,TH}$. This effectively regulates the inrush current during startup. In this case, the current charging C_{BOARD} can be considered constant and the turn-on time is:

$$t_{ON} = \frac{C_{BOARD} \times V_{IN} \times R_{SENSE}}{V_{FC,TH}}$$

The maximum inrush current in this case is:

$$I_{INRUSH} = \frac{V_{FC,TH}}{R_{SENSE}}$$

Figure 6 shows the waveforms and timing diagrams for a startup transient with current regulation (see the *Typical Operating Characteristics*). **When operating under this condition, an external gate capacitor is not required.**

ON Comparators

The ON comparators control the on/off function of the MAX5927/MAX5929. ON_ is also used to reset the fault latch (latch mode). Pull $V_{ON_}$ low for 100µs, $t_{UNLATCH}$, to reset the shutdown latch. ON_ also programs the UVLO threshold (see Figure 10). A resistive-divider between $V_{IN_}$, $V_{ON_}$, and GND sets the user programmable turn-on voltage. In power-sequencing mode, an RC circuit can be used at ON_ to set the delay timing (see Figure 11).

Using the MAX5927/MAX5929 on the Backplane

Using the MAX5927/MAX5929 on the backplane allows multiple cards with different input capacitance to be inserted into the same slot even if the card does not have on-board hot-swap protection. The startup period can be triggered if IN_ is connected to ON_ through a trace on the card (Figure 12).

Input Transients

The voltage at IN1, IN2, IN3, or IN4 must be above V_{UVLO} during inrush and fault conditions. When a short-circuit condition occurs on the board, the fast comparator trips cause the external MOSFET gates to be discharged at 50mA according to the mode of operation (see the *Mode* section). The main system power supply must be able to sustain a temporary fault current, without dropping below the UVLO threshold of 2.45V, until the external MOSFET is completely off. If the main system power supply collapses below UVLO, the MAX5927/MAX5929 force the device to restart once the supply has recovered. The MOSFET is turned off in a very short time resulting in a high di/dt. The backplane delivering the power to the external card must have low inductance to minimize voltage transients caused by this high di/dt.

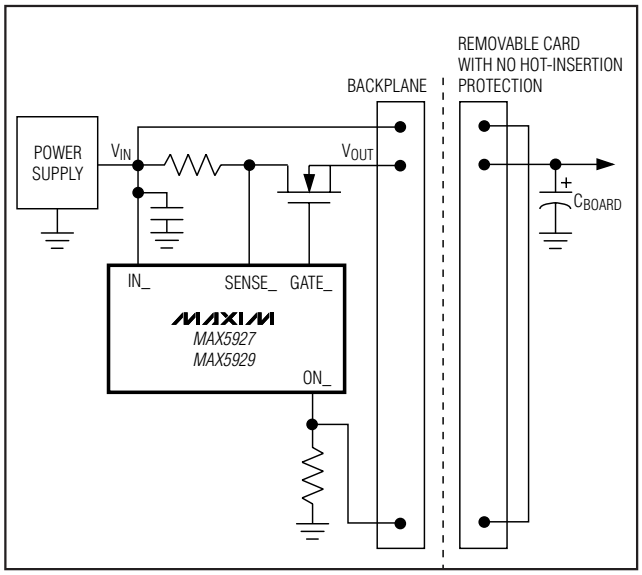


Figure 12. Using the MAX5927/MAX5929 on a Backplane

MOSFET Thermal Considerations

During normal operation, the external MOSFETs dissipate little power. The MOSFET $R_{DS(ON)}$ is low when the MOSFET is fully enhanced. The power dissipated in normal operation is $P_D = I_{LOAD}^2 \times R_{DS(ON)}$. The most power dissipation occurs during the turn-on and turn-off transients when the MOSFETs are in their linear regions. Take into consideration the worst-case scenario of a continuous short-circuit fault, consider these two cases:

1) The single turn-on with the device latched after a fault: MAX5927 (LATCH = high or floating) or MAX5929L.
2) The continuous autoretry after a fault: (MAX5927 (LATCH = low) or MAX5929A.

MOSFET manufacturers typically include the package thermal resistance from junction to ambient ($R_{\theta JA}$) and thermal resistance from junction to case ($R_{\theta JC}$), which determines the startup time and the retry duty cycle ($d = t_{START}/(t_{START} + t_{RETRY})$). Calculate the required transient thermal resistance with the following equation:

$$Z_{\theta JA(MAX)} \le \frac{T_{JMAX} - T_A}{V_{IN} \times I_{START}}$$

where $I_{START} = V_{SU,TH}/R_{SENSE}$.

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

Layout Considerations

To take full tracking advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. Place the MAX5927/MAX5929 close to the card's connector. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections (Figure 13).

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the topside of the board.

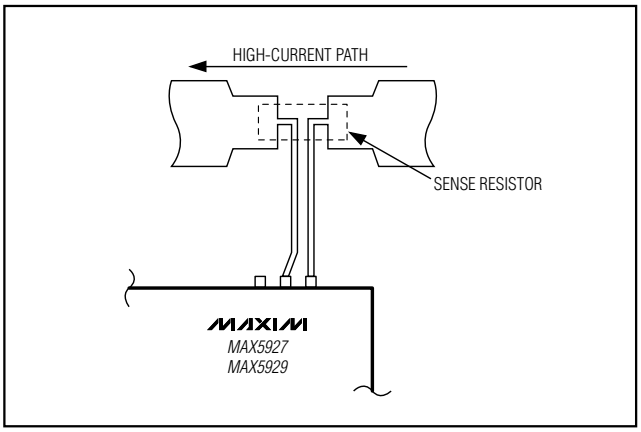
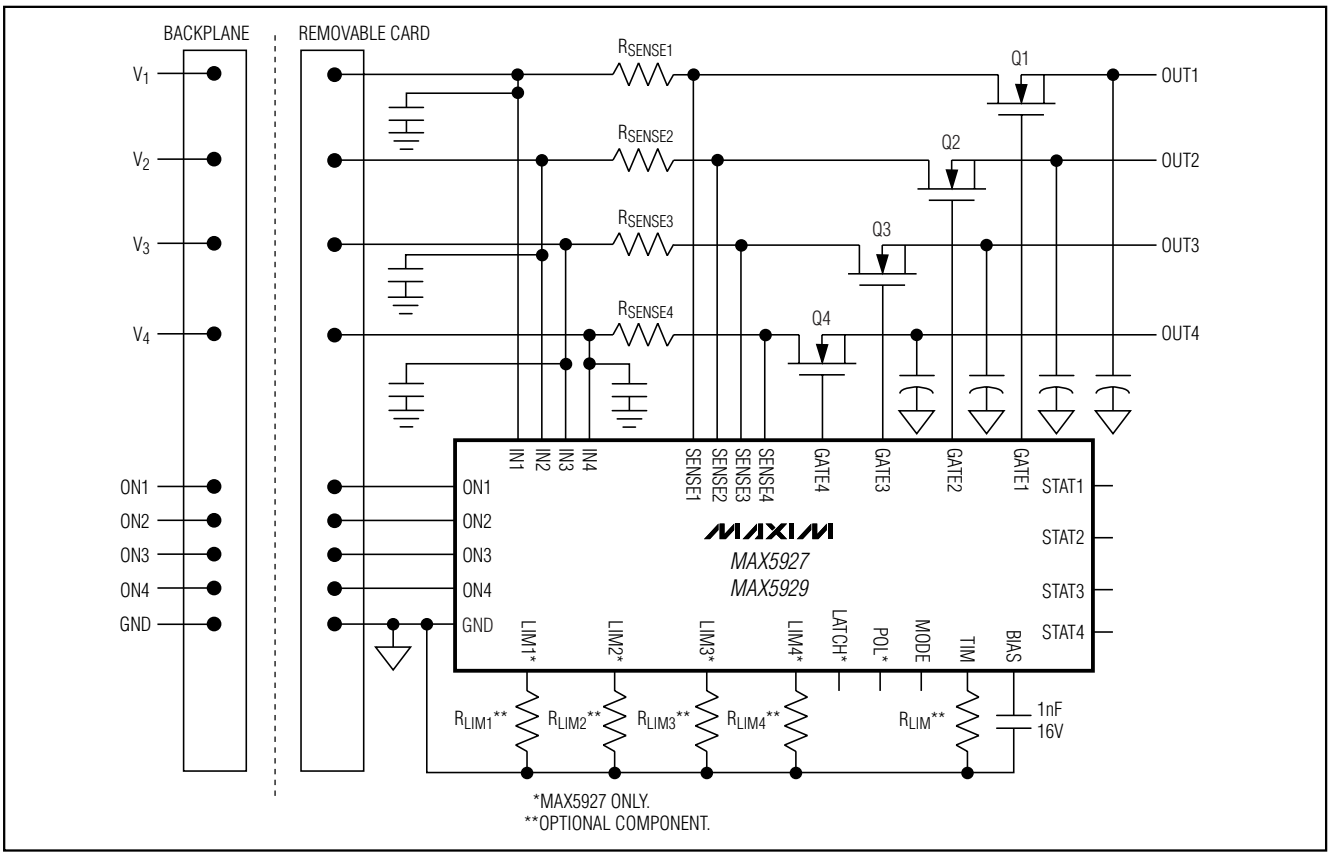


Figure 13. Kelvin Connection for the Current-Sense Resistors

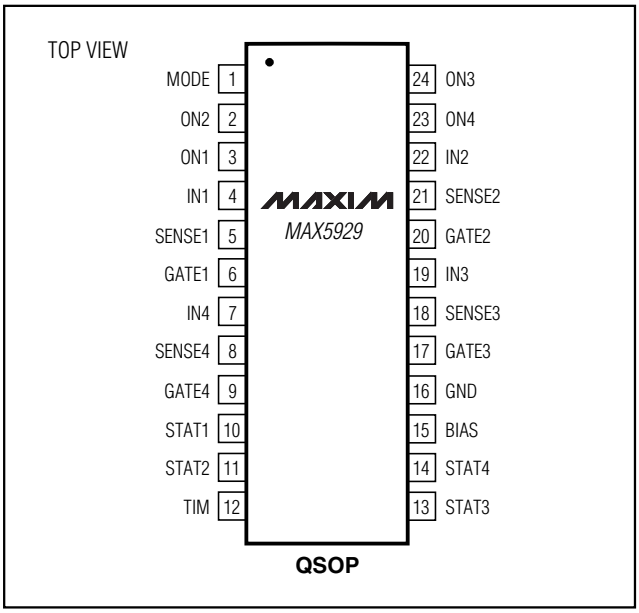
Typical Operating Circuit



Selector Guide

PART	CURRENT LIMIT	FAULT MANAGEMENT	STAT_ POLARITY
MAX5927ETJ	Programmable	Selectable	Selectable
MAX5929LHEEG	Fixed	Latched	Asserted high (open drain)
MAX5929LLEEG	Fixed	Latched	Asserted low
MAX5929AHEEG	Fixed	Autoretry	Asserted high (open drain)
MAX5929ALEEG	Fixed	Autoretry	Asserted low

Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 7704

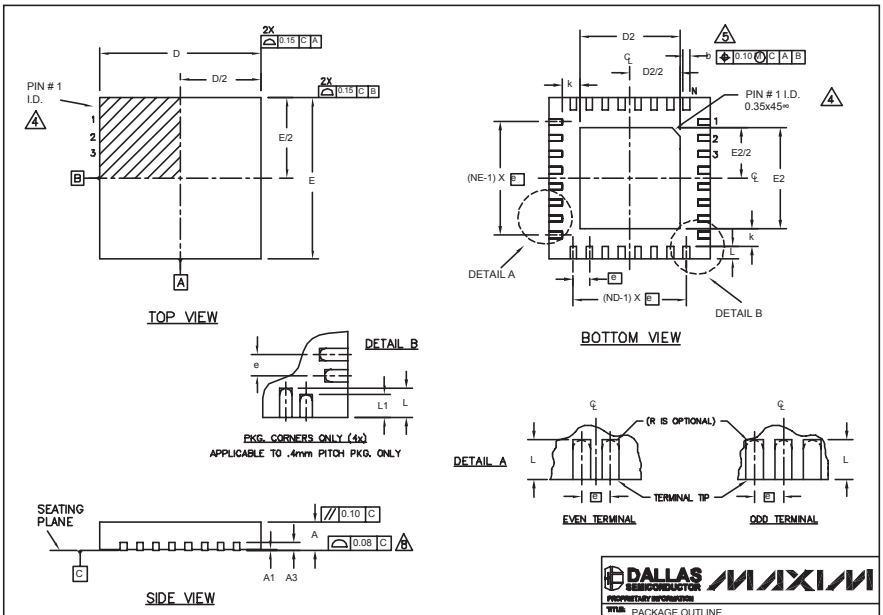
PROCESS: BiCMOS

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
16, 20, 28, 32, 40L, THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	E	1/2

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	-	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	YES
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

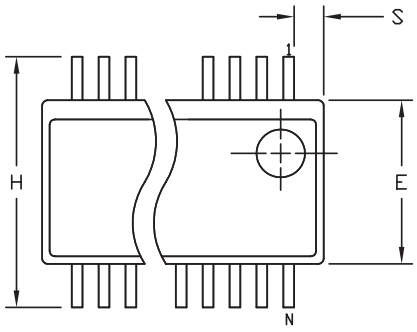
TITLE: PACKAGE OUTLINE
16, 20, 28, 32, 40L, THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	E	2/2

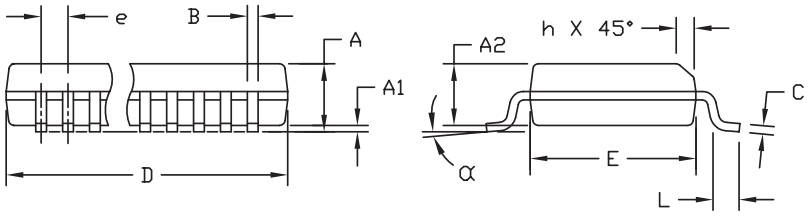
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

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