General Description

The MAX6369–MAX6374 are pin-selectable watchdog timers that supervise microprocessor (µP) activity and signal when a system is operating improperly. During normal operation, the microprocessor should repeatedly toggle the watchdog input (WDI) before the selected watchdog timeout period elapses to demonstrate that the system is processing code properly. If the µP does not provide a valid watchdog input transition before the timeout period expires, the supervisor asserts a watchdog ($\overline{WDO}$) output to signal that the system is not executing the desired instructions within the expected time frame. The watchdog output pulse can be used to reset the µP or interrupt the system to warn of processing errors.

The MAX6369–MAX6374 are flexible watchdog timer supervisors that can increase system reliability through notification of code execution errors. The family offers several pin-selectable watchdog timing options to match a wide range of system timing applications:

- Watchdog startup delay: provides an initial delay before the watchdog timer is started.
- Watchdog timeout period: normal operating watchdog timeout period after the initial startup delay.
- Watchdog output/timing options: open drain (100ms) or push-pull (1ms).

The MAX6369–MAX6374 operate over a +2.5V to +5.5V supply range and are available in miniature 8-pin SOT23 packages.

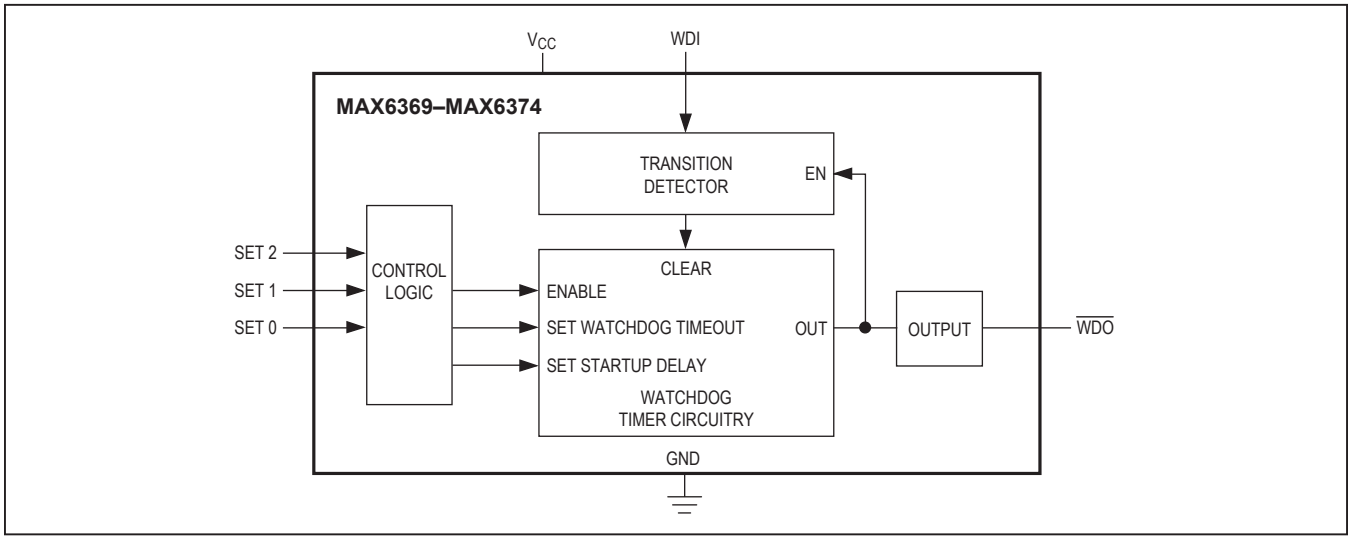
Benefits and Features

- Precision Watchdog Timer for Critical µP Applications
- Pin-Selectable Watchdog Timeout Periods
- Pin-Selectable Watchdog Startup Delay Periods
- Ability to Change Watchdog Timing Characteristics Without Power Cycling
- Open-Drain or Push-Pull Pulsed Active-Low Watchdog Output
- Watchdog Timer Disable Feature
- +2.5V to +5.5V Operating Voltage
- 8µA Low Supply Current
- No External Components Required
- Miniature 8-Pin SOT23 Package
- AEC-Q100 Qualified (MAX6369KA/V+ and MAX6374KA/V+ Only)

Applications

- Embedded Control Systems
- Industrial Controllers
- Critical µP and Microcontroller (µC) Monitoring
- Automotive
- Telecommunications
- Networking

Functional Diagram



Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- WDI ..... -0.3V to +6V
- $\overline{WDO}$ (Open Drain: MAX6369/71/73) ..... -0.3V to +6V
- $\overline{WDO}$ (Push-Pull: MAX6370/72/74 ..... -0.3V to (V_{CC} + 0.3V)
- SET0, SET1, SET2 ..... -0.3V to (V_{CC} + 0.3V)

Maximum Current, Any Pin (input/output) 20mA

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin SOT23 (derate 8.75mW/°C above +70°C) 700mW

Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
V_{CC} Rise or Fall Rate 0.05V/µs
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
Lead(Pb)-free ..... +260°C
Containing Lead (Pb) ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +2.5V to +5.5V, SET_ = V_{CC} or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}			2.5		5.5	V
Supply Current	I_{CC}	No load	T_A = -40°C to +85°C		8	20	µA
			T_A = -40°C to +125°C		10	22	
Input High Voltage	V_{IH}	WDI, SET0, SET1, SET2		0.8 x V_{CC}			V
Input Low Voltage	V_{IL}	WDI, SET0, SET1, SET2	V_{CC} ≥ 3.3V, T_A = -40°C to +85°C			0.8	V
			V_{CC} ≥ 3.3V, T_A = -40°C to +125°C			0.6	
			V_{CC} ≥ 2.5V, T_A = -40°C to +85°C			0.6	
			V_{CC} ≥ 2.5V, T_A = -40°C to +125°C			0.4	
Logic Input Current (Note 2)		V_{WDI} or $V_{SET_}$ = 0V or V_{CC}			0	±10	nA
$\overline{WDO}$ Output Low Voltage	V_{OL}	I_{SINK} = 1.2mA, V_{CC} > 2.7V, watchdog output asserted				0.3	V
		I_{SINK} = 6mA, V_{CC} > 4.5V, watchdog output asserted				0.4	V
$\overline{WDO}$ Leakage Current	I_{LKG}	$V_{\overline{WDO}}$ = 0 to +5.5V, output deasserted, MAX6369/MAX6371/MAX6373				1	µA
$\overline{WDO}$ Output High Voltage	V_{OH}	I_{SOURCE} = 500µA, V_{CC} > 2.7V, watchdog output deasserted		0.8 x V_{CC}			V
		I_{SOURCE} = 800µA, V_{CC} > 4.5V, watchdog output deasserted		V_{CC} - 1.5			

Electrical Characteristics (continued)

(V_{CC} = +2.5V to +5.5V, SET_ = V_{CC} or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX6369/MAX6370						
Startup Delay Period	t_{DELAY}	V_{SET2} = 0V, V_{SET1} = 0V, V_{SET0} = 0V	1		3	ms
		V_{SET2} = 0V, V_{SET1} = 0,V SET0 = V_{CC}	10		30	
		V_{SET2} = 0V, SET1 = V_{CC}, V_{SET0} = 0V	30		90	
		V_{SET2} = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		SET2 = V_{CC}, V_{SET1} = 0V, V_{SET0} = 0V	100		300	ms
		SET2 = V_{CC}, V_{SET1} = 0V, SET0 = V_{CC}	1		3	s
		SET2 = V_{CC}, SET1 = V_{CC}, V_{SET0} = 0V	10		30	
		SET2 = V_{CC}, SET1 = V_{CC}, SET0 = V_{CC}	60		180	
Watchdog Timeout Period	t_{WD}	V_{SET2} = 0V, V_{SET1} = 0V, V_{SET0} = 0V	1		3	ms
		V_{SET2} = 0V, V_{SET1} = 0V, SET0 = V_{CC}	10		30	
		V_{SET2} = 0V, SET1 = V_{CC}, V_{SET0} = 0V	30		90	
		V_{SET2} = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		SET2 = V_{CC}, V_{SET1} = 0V, V_{SET0} = 0V	100		300	ms
		SET2 = V_{CC}, V_{SET1} = 0V, SET0 = V_{CC}	1		3	s
		SET2 = V_{CC}, SET1 = V_{CC}, V_{SET0} = 0V	10		30	
		SET2 = V_{CC}, SET1 = V_{CC}, SET0 = V_{CC}	60		180	
MAX6371/MAX6372						
Startup Delay Period	t_{DELAY}	V_{SET2} = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		All other SET_ conditions	60		180	s
Watchdog Time-Out Period	t_{WD}	V_{SET2} = 0V, V_{SET1} = 0V, V_{SET0} = 0V	1		3	ms
		V_{SET2} = 0V, V_{SET1} = 0V, SET0 = V_{CC}	3		9	
		V_{SET2} = 0V, SET1 = V_{CC}, V_{SET0} = 0V	10		30	
		V_{SET2} = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		SET2 = V_{CC}, V_{SET1} = 0V, V_{SET0} = 0V	100		300	ms
		SET2 = V_{CC}, V_{SET1} = 0V, SET0 = V_{CC}	300		900	
		SET2 = V_{CC}, SET1 = V_{CC}, V_{SET0} = 0V	3		9	s
		SET2 = V_{CC}, SET1 = V_{CC}, SET0 = V_{CC}	60		180	
MAX6373/MAX6374						
Startup Delay Period	t_{DELAY}	V_{SET2} = 0V, V_{SET1} = 0V, V_{SET0} = 0V	3		9	ms
		V_{SET2} = 0V, V_{SET1} = 0V, SET0 = V_{CC}	3		9	s
		V_{SET2} = 0V, SET1 = V_{CC}, V_{SET0} = 0V	60		180	
		SET2 = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		SET2 = V_{CC}, V_{SET1} = 0V, VSET0 = 0V	200		600	µs
		SET2 = V_{CC}, V_{SET1} = 0V, SET0 = V_{CC}	First Edge (Note 3)			
		SET2 = V_{CC}, SET1 = V_{CC}, V_{SET0} = 0V	First Edge (Note 3)			
		SET2 = V_{CC}, SET1 = V_{CC}, SET0 = V_{CC}	60		180	s

Electrical Characteristics (continued)

(V_{CC} = +2.5V to +5.5V, SET_ = V_{CC} or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3V.) (Note 1)

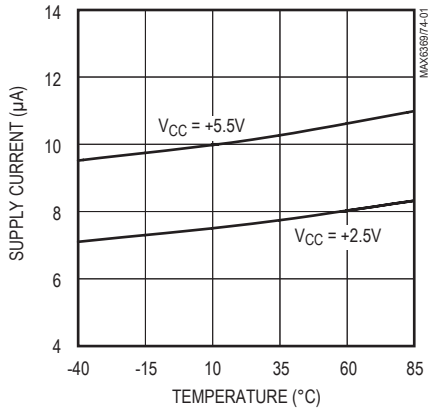
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Watchdog Timeout Period	t_{WD}	V_{SET2} = 0V, V_{SET1} = 0V, V_{SET0} = 0V	3		9	ms
		V_{SET2} = 0V, V_{SET1} = 0V, SET0 = V_{CC}	3		9	s
		V_{SET2} = 0V, SET1 = V_{CC}, V_{SET0} = 0V	1		3	
		V_{SET2} = 0V, SET1 = V_{CC}, SET0 = V_{CC}	Watchdog Disabled			
		SET2 = V_{CC}, V_{SET1} = 0V, V_{SET0} = 0V	30		90	µs
		SET2 = V_{CC}, V_{SET1} = 0V, SET0 = V_{CC}	1		3	s
		SET2 = V_{CC}, SET1 = V_{CC}, V_{SET0} = 0V	10		30	
		SET2 = V_{CC}, SET1 = V_{CC}, SET0 = V_{CC}	10		30	
Watchdog Input Pulse Width (Note 2)	t_{WDI}	After $\overline{WDO}$ deasserted	100			ns
Watchdog Output Pulse Width	$t_{\overline{WDO}}$	MAX6369/MAX6371/MAX6373	100		300	ms
		MAX6370/MAX6372/MAX6374	1		3	ms
Internal Setup Time (Note 4)	t_{SETUP}	After $\overline{WDO}$ deasserted			300	µs

Note 1: Production tested at T_A = +25°C. Guaranteed by design over temperature limits.
Note 2: Guaranteed by design.
Note 3: In this setting the watchdog timer is inactive and startup delay ends when WDI sees its first level transition. See the *Selecting Device Timing* section for more information.
Note 4: After power-up, or a setting change, there is an internal setup time during which WDI is ignored.

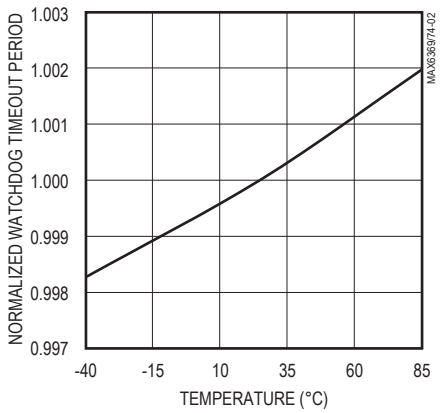
Typical Operating Characteristics

(Circuit of Functional Diagram, T_A = +25°C, unless otherwise noted.)

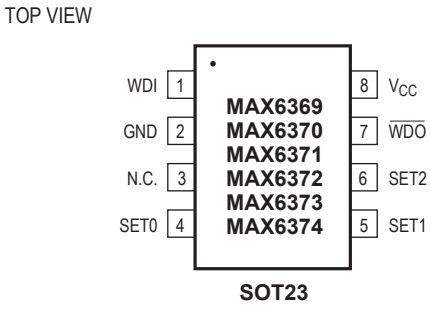
SUPPLY CURRENT vs. TEMPERATURE



WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	WDI	Watchdog Input. If WDI remains either high or low for the duration of the watchdog timeout period (t_{WD}), $\overline{WDO}$ triggers a pulse. The internal watchdog timer clears whenever a $\overline{WDO}$ is asserted or whenever WDI sees a rising or falling edge.
2	GND	Ground
3	N.C.	Not Connected. Do not make any connection to this pin.
4	SET0	Set Zero. Logic input for selecting startup delay and watchdog timeout periods. See Table 1 for timing details.
5	SET1	Set One. Logic input for selecting startup delay and watchdog timeout periods. See Table 1 for timing details.
6	SET2	Set Two. Logic input for selecting startup delay and watchdog timeout periods. See Table 1 for timing details.
7	$\overline{WDO}$	Watchdog Output. Pulses low for the watchdog output pulse width, $t_{\overline{WDO}}$, when the internal watchdog times out. The MAX6369/MAX6371/MAX6373 have open-drain outputs and require a pull-up resistor. The MAX6370/MAX6372/MAX6374 outputs are push-pull.
8	V_{CC}	Supply Voltage (+2.5V to +5.5V)

Detailed Description

The MAX6369–MAX6374 are flexible watchdog circuits for monitoring µP activity. During normal operation, the internal timer is cleared each time the µP toggles the WDI with a valid logic transition (low to high or high to low) within the selected timeout period (t_{WD}). The $\overline{WDO}$ remains high as long as the input is strobed within the selected timeout period. If the input is not strobed before the timeout period expires, the watchdog output is asserted low for the watchdog output pulse width ($t_{\overline{WDO}}$). The device type and the state of the three logic control pins (SET0, SET1, and SET2) determine watchdog timing characteristics. The three basic timing variations for the watchdog startup delay and the normal watchdog timeout period are summarized below (see Table 1 for the timeout characteristics for all devices in the family):

- Watchdog Startup Delay:

  Provides an initial delay before the watchdog timer is started.

  Allows time for the µP system to power up and initialize before assuming responsibility for normal watchdog timer updates.

  Includes several fixed or pin-selectable startup delay options from 200µs to 60s, and an option to wait for the first watchdog input transition before starting the watchdog timer.

Table 1. Minimum Timeout Settings

LOGIC INPUTS			MAX6369/MAX6370	MAX6371/MAX6372	MAX6373/MAX6374	
SET2	SET1	SET0	t_{DELAY}, t_{WD}	t_{DELAY} = 60s, t_{WD}	t_{DELAY}	t_{WD}
0	0	0	1ms	1ms	3ms	3ms
0	0	1	10ms	3ms	3s	3s
0	1	0	30ms	10ms	60s	1s
0	1	1	Disabled	Disabled	Disabled	Disabled
1	0	0	100ms	100ms	200µs	30µs
1	0	1	1s	300ms	First Edge	1s
1	1	0	10s	3s	First Edge	10s
1	1	1	60s	60s	60s	10s

- Watchdog Timeout Period:

  Normal operating watchdog timeout period after the initial startup delay.

  A watchdog output pulse is asserted if a valid watchdog input transition is not received before the timeout period elapses.

  Eight pin-selectable timeout period options for each device, from 30µs to 60s.

  Pin-selectable watchdog timer disable feature.

- Watchdog Output/Timing Options:

  Open drain, active low with 100ms minimum watchdog output pulse (MAX6369/MAX6371/MAX6373).

  Push-pull, active low with 1ms minimum watchdog output pulse (MAX6370/MAX6372/MAX6374).

Each device has a watchdog startup delay that is initiated when the supervisor is first powered or after the user modifies any of the logic control set inputs. The watchdog timer does not begin to count down until the completion of the startup delay period, and no watchdog output pulses are asserted during the startup delay. When the startup delay expires, the watchdog begins counting its normal watchdog timeout period and waiting for WDI transitions. The startup delay allows time for the µP system to power up and fully initialize before assuming responsibility for the normal watchdog timer updates. Startup delay periods vary between the different devices and may be altered by the logic control set pins. To ensure that the system generates no undesired watchdog outputs, the routine watchdog input transitions should begin before the selected minimum startup delay period has expired.

The normal watchdog timeout period countdown is initiated when the startup delay is complete. If a valid logic transition is not recognized at WDI before the watchdog timeout period has expired, the supervisor asserts a watchdog output. Watchdog timeout periods vary between the different devices and may be altered by the logic control set pins. To ensure that the system generates no undesired watchdog outputs, the watchdog input transitions should occur before the selected minimum watchdog timeout period has expired.

The startup delay and the watchdog timeout period are determined by the states of the SET0, SET1, and SET2 pins, and by the particular device within the family. For the MAX6369 and MAX6370, the startup delay is equal to the watchdog timeout period. The startup and watchdog timeout periods are pin selectable from 1ms to 60s (minimum).

For the MAX6371 and MAX6372, the startup delay is fixed at 60s and the watchdog timeout period is pin selectable from 1ms to 60s (minimum).

The MAX6373/MAX6374 provide two timing variations for the startup delay and normal watchdog timeout. Five of the pin-selectable modes provide startup delays from 200µs to 60s minimum, and watchdog timeout delays from 3ms to 10s minimum. Two of the selectable modes

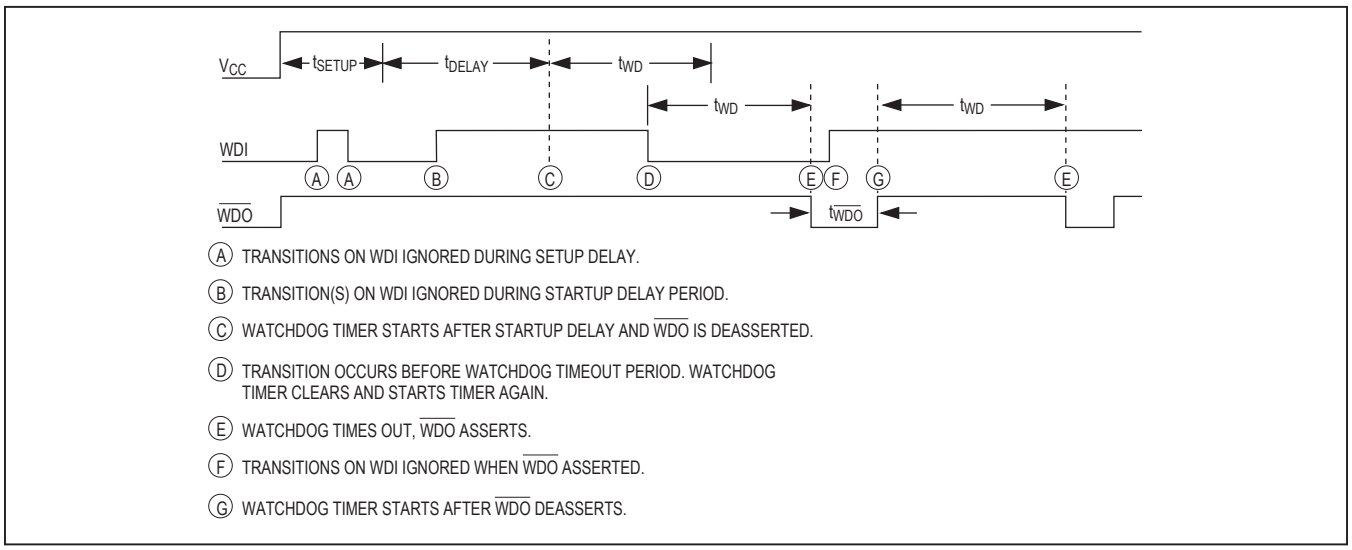


Figure 1. Watchdog Timing

do not initiate the watchdog timer until the device receives its first valid watchdog input transition (there is no fixed period by which the first input must be received). These two extended startup delay modes are useful for applications requiring more than 60s for system initialization.

All the MAX6369–MAX6374 devices may be disabled with the proper logic control pin setting (Table 1).

Applications Information

Input Signal Considerations

Watchdog timing is measured from the last WDI rising or falling edge associated with a pulse of at least 100ns in width. WDI transitions are ignored when $\overline{WDO}$ is asserted, and during the startup delay period (Figure 1). Watchdog input transitions are also ignored for a setup period, t_{SETUP}, of up to 300µs after power-up or a setting change (Figure 2).

Selecting Device Timing

SET2, SET1, and SET0 program the startup delay and watchdog timeout periods (Table 1). Timeout settings can be hard wired, or they can be controlled with logic gates and modified during operation. To ensure smooth transitions, the system should strobe WDI immediately before the timing settings are changed. This minimizes the risk of initializing a setting change too late in the timer countdown period and generating undesired watchdog outputs. After changing the timing settings, two outcomes are possible based on $\overline{WDO}$. If the change is made while $\overline{WDO}$ is asserted, the previous setting is allowed to finish, the characteristics of the new setting are assumed, and the new startup phase is entered after a 300µs setup time (t_{SETUP}) elapses. If the change is made while $\overline{WDO}$ is not asserted, the new setting is initiated immediately, and the new startup phase is entered after the 300µs setup time elapses.

Selecting 011 (SET2 = 0, SET1 = 1, SET0 = 1) disables the watchdog timer function on all devices in the family. Operation can be reenabled without powering down by changing the set inputs to the new desired setting. The device assumes the new selected timing characteristics and enter the startup phase after the 300µs setup time elapses (Figure 2). $\overline{WDO}$ is high when the watchdog timer is disabled.

The MAX6373/MAX6374 offer a first-edge feature. In first-edge mode (settings 101 or 110, Table 1), the internal timer does not control the startup delay period. Instead, startup terminates when WDI sees a transition. If changing to first-edge mode while the device is operating, disable mode must be entered first. It is then safe to select first-edge mode. Entering disable mode first ensures the output is unasserted when selecting first-edge mode and removes the danger of WDI being masked out.

Output

The MAX6369/MAX6371/MAX6373 have an active-low, open-drain output that provides a watchdog output pulse of 100ms. This output structure sinks current when $\overline{WDO}$ is asserted. Connect a pullup resistor from $\overline{WDO}$ to any supply voltage up to +5.5V.

Select a resistor value large enough to register a logic low (see *Electrical Characteristics*), and small enough to register a logic high while supplying all input current and leakage paths connected to the $\overline{WDO}$ line. A 10kΩ pullup is sufficient in most applications. The MAX6370/MAX6372/MAX6374 have push-pull outputs that provide an active-low watchdog output pulse of 1ms. When $\overline{WDO}$ deasserts, timing begins again at the beginning of the watchdog timeout period (Figure 1).

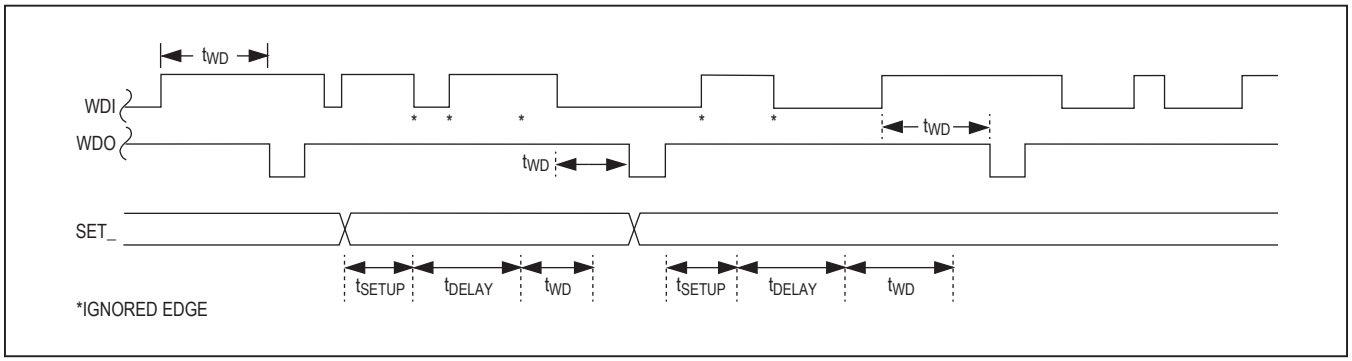


Figure 2. Setting Change Timing

Usage in Noisy Environments

If using the watchdog timer in an electrically noisy environment, a bypass capacitor of 0.1µF should be connected between V_{CC} and GND as close to the device as possible, and no further away than 0.2 inches.

Watchdog Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out. Figure 3 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the end of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing $\overline{WDO}$ to pulse.

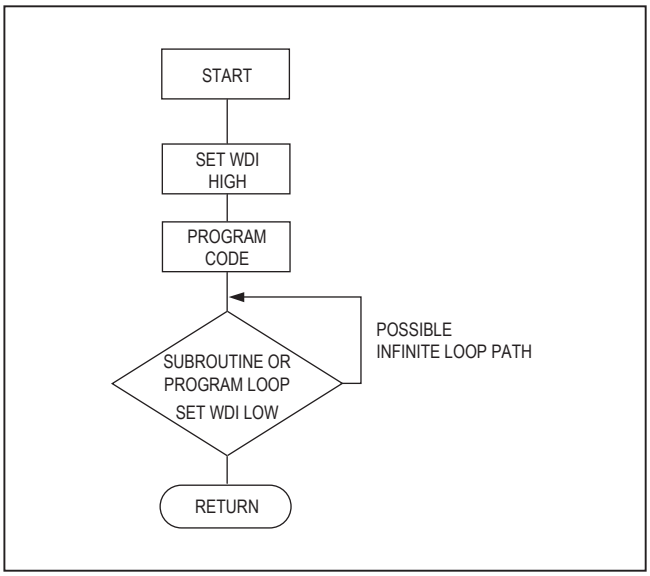


Figure 3. Watchdog Flow Diagram

Selector Guide

PART	OUTPUT	WDO PULSE WIDTH (ms)	MINIMUM STARTUP DELAY	MINIMUM WATCHDOG TIMEOUT
MAX6369	Open Drain	100	Selectable: 1ms to 60s	Selectable: 1ms to 60s
MAX6370	Push-Pull	1	Selectable: 1ms to 60s	Selectable: 1ms to 60s
MAX6371	Open Drain	100	60s	Selectable: 1ms to 60s
MAX6372	Push-Pull	1	60s	Selectable: 1ms to 60s
MAX6373	Open Drain	100	Selectable: 200µs to 60s or first edge	Selectable: 30µs to 10s
MAX6374	Push-Pull	1	Selectable: 200µs to 60s or first edge	Selectable: 30µs to 10s

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX6369KA+T	-40°C to +125°C	8 SOT23	AADC
MAX6369KA-T	-40°C to +125°C	8 SOT23	AADC
MAX6369KA/V+T	-40°C to +125°C	8 SOT23	AEQV
MAX6370KA+T	-40°C to +125°C	8 SOT23	AADD
MAX6371KA+T	-40°C to +125°C	8 SOT23	AADE
MAX6372KA+T	-40°C to +125°C	8 SOT23	AADF
MAX6373KA+T	-40°C to +125°C	8 SOT23	AADG
MAX6373KA-T	-40°C to +125°C	8 SOT23	AADG
MAX6374KA+T	-40°C to +125°C	8 SOT23	AADH
MAX6374KA/V+T	-40°C to +125°C	8 SOT23	AADH

Note: *All devices are available in tape-and-reel only. Required order increment is 2,500 pieces.*

/V denotes an automotive qualified part.

Devices are available in both leaded and lead(Pb)-free packaging.

+Denotes Lead(Pb)-free packages and - denotes leaded packages.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8SN+1, K8SN-1	21-0078	90-0176

Chip Information

TRANSISTOR COUNT: 1500

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/00	Initial release	—
1	7/00	Removed future product asterisk for MAX6370.	1
2	2/03	Corrected limits in *Electrical Characteristics*.	4
3	12/05	Added lead-free information to *Ordering Information*.	1
4	6/10	Revised the *Ordering Information*, *Absolute Maximum Ratings*, *Electrical Characteristics*, and the *Selecting Device Timing* section.	1, 2, 8
5	1/11	Updated the top mark information in the *Ordering Information* section.	1
6	3/15	Deleted minimum value for Internal Setup Time in *Electrical Characteristics* and changed units from ms to µs	4
7	1/16	Added lead-free part numbers and package codes	9, 1
8	7/17	Added *AEC-Q100 Qualified* statement to *Benefits and Features* section	1

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