MAX6397/MAX6398

Overvoltage Protection Switch/Limiter Controllers Operate Up to 72V

General Description

The MAX6397/MAX6398 are small, high-voltage overvoltage protection circuits. These devices disconnect the output load or limit the output voltage during an input overvoltage condition. These devices are ideal for applications that must survive high-voltage transients such as those found in industrial applications.

The MAX6397/MAX6398 monitor the input or output voltages and control an external n-channel MOSFET to isolate or limit the load from overvoltage transient energy. When the monitored input voltage is below the user-adjustable overvoltage threshold, the external n-channel MOSFET is turned on by the GATE output. In this mode, the internal charge pump fully enhances the n-channel MOSFET with a 10V gate-to-source voltage.

When the input voltage exceeds the overvoltage threshold, the protection can disconnect the load from the input by quickly forcing the GATE output low. In some applications, disconnecting the output from the load is not desirable. In these cases, the protection circuit can be configured to act as a voltage limiter where the GATE output sawtooths to limit the voltage to the load.

The MAX6397 also offers an always-on linear regulator that is capable of delivering up to 100mA of output current. This high-voltage linear regulator consumes only 37µA of quiescent current.

The regulator is offered with output options of 5V, 3.3V, 2.5V, or 1.8V. An open-drain, power-good output (POK) asserts when the regulator output falls below 92.5% or 87.5% of its nominal voltage.

The MAX6397/MAX6398 include internal thermal-shutdown protection, disabling the external MOSFET and linear regulator if the chip reaches overtemperature conditions. The devices operate over a wide 5.5V to 72V supply voltage range, are available in small TDFN packages, and are fully specified from -40°C to +125°C.

Applications

- Industrial
- FireWire®
- Notebook Computers
- Wall Cube Power Devices

FireWire is a registered trademark of Apple Computer, Inc.

Features

- 5.5V to 72V Wide Supply Voltage Range
- Overvoltage Protection Controllers Allow User to Size External n-Channel MOSFETs
- Internal Charge-Pump Circuit Ensures MOSFET Gate-to-Source Enhancement for Low $R_{DS(ON)}$ Performance
- Disconnect or Limit Output from Input During Overvoltage Conditions
- Adjustable Overvoltage Threshold
- Thermal-Shutdown Protection
- Always-On, Low-Current (37µA) Linear Regulator Sources Up to 100mA (MAX6397)
- Fully Specified from -40°C to +125°C (T_J)
- Small, Thermally Enhanced 3mm x 3mm TDFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6397_ATA-T*	-40°C to +125°C	8 TDFN-EP**
MAX6398ATT-T*	-40°C to +125°C	6 TDFN-EP**

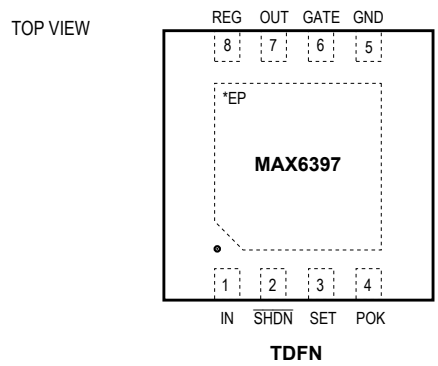
**Replace "-T" with "+T" for lead(Pb)-free/RoHS-compliant packages.*

***EP = Exposed pad.*

The MAX6397 linear regulator is offered in four output voltage options and a choice of a 92.5% or 87.5% POK threshold assertions. See the Selector Guide.

Selector Guide and Typical Operating Circuit appear at end of data sheet.

Pin Configurations



*EXPOSED PAD. CONNECT TO GND.

Pin Configurations continued at end of data sheet.

Absolute Maximum Ratings

(All pins referenced to GND, unless otherwise noted.)
IN, GATE, OUT.....-0.3V to +80V
$\overline{SHDN}$ .....-0.3V to (V_{IN} + 0.3V)
GATE to OUT ..... -0.3 to +20V
SET, REG, POK .....-0.3V to +12V
Maximum Current:
IN, REG 350mA
All Remaining Pins 50mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
Operating Temperature Range (T_A)..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 14V; C_{GATE} = 6000pF, C_{REG} = 4.7µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}			5.5		72	V
Input Supply Current		$\overline{SHDN}$ = high, no load (MAX6397)			118	140	µA
		$\overline{SHDN}$ = high, (MAX6398)			104	130	
		$\overline{SHDN}$ = low, no load (MAX6397)			37	45	
		$\overline{SHDN}$ = low, (MAX6398)			11	20	
IN Undervoltage Lockout		V_{IN} rising, enables GATE		4.66	5	5.50	V
IN Undervoltage-Lockout Hysteresis		V_{IN} falling, disables GATE			175		mV
SET Threshold Voltage	V_{TH}	With respect to GND		1.181	1.215	1.248	V
SET Threshold Hysteresis	V_{HYST}				4		%
SET Input Current	I_{SET}			-50		+50	nA
Startup Response Time	t_{START}	$\overline{SHDN}$ rising (Note 2)			100		µs
GATE Rise Time		GATE rising from GND to V_{OUT} + 8V, C_{GATE} = 6000pF, OUT = GND			1		ms
SET-to-GATE Propagation Delay	t_{OV}	SET rising from V_{TH} - 100mV to V_{TH} + 100mV				0.75	µs
GATE Output High Voltage	V_{OH}	V_{OUT} = V_{IN} = 6V, R_{GATE} to IN = 1MΩ		V_{IN} + 3.8V	V_{IN} + 4.2V	V_{IN} + 4.6V	V
		V_{OUT} = V_{IN}; V_{IN} ≥ 14V, R_{GATE} to IN = 1MΩ		V_{IN} + 8.5V	V_{IN} + 9.2V	V_{IN} + 11.5V	
GATE Output Low Voltage	V_{OL}	GATE sinking 20mA, V_{OUT} = GND				0.38	V
GATE Charge-Pump Current	I_{GATE}	GATE = GND			75		µA
GATE-to-OUT Clamp Voltage	V_{CLMP}			13		18	V
$\overline{SHDN}$ Logic-High Input Voltage	V_{IH}			1.4			
$\overline{SHDN}$ Logic-Low Input Voltage	V_{IL}					0.4	
$\overline{SHDN}$ Input Pulldown Current		$V_{\overline{SHDN}}$ = 2V, $\overline{SHDN}$ is internally pulled down to GND			1		µA
Thermal Shutdown (Note 3)					+150		°C
Thermal-Shutdown Hysteresis					20		°C
REGULATOR (MAX6397)							
Ground Current	I_{GND}	$\overline{SHDN}$ = GND	I_{REG} = 1mA		40	48	µA
			I_{REG} = 100mA		60		

Electrical Characteristics (continued)

(V_{IN} = 14V; C_{GATE} = 6000pF, C_{REG} = 4.7µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

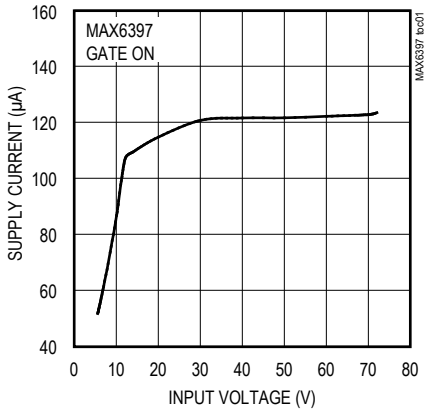
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REG Output Voltage (V_{IN} ≥ V_{REG} + 1.8V)	V_{REG}	MAX6397L/M	I_{REG} = 1mA	4.925	5	5.120	V
			1mA < I_{REG} < 100mA	4.85		5.15	
		MAX6397S/T	I_{REG} = 1mA	3.243	3.3	3.36	
			1mA < I_{REG} < 100mA	3.201		3. 36	
		MAX6397Y/Z	I_{REG} = 1mA	2.246	2.5	2.542	
			1mA < I_{REG} < 100mA	2.41		2.55	
		MAX6397V/W	I_{REG} = 1mA	1.76	1.8	1.837	mV/V
			1mA < I_{REG} < 100mA	1.715		1.837	
Dropout Voltage (Note 4)	ΔV_{DO}	5.5V ≤ V_{IN} ≤ 72V, I_{REG} = 1mA, V_{REG} = 5V				0.12	
		5.5V ≤ V_{IN} ≤ 72V, I_{REG} = 100mA, V_{REG} = 5V				1.2	
Current Limit		V_{IN} = 14V		150		300	mA
Overvoltage-Protection Threshold	V_{OVP}				105		% of V_{REG}
Overvoltage-Protection Sink Current	I_{OVP}	V_{REG} = 1.1 x V_{REG} (Nominal)			15		mA
Line Regulation (Note 5)	ΔV_{REG}/ ΔV_{REG}	6.5V ≤ V_{IN} ≤ 72V, I_{REG} = 10mA, V_{REG} = 5V				0.22	mV/mA
		5.5V ≤ V_{IN} ≤ 72V, I_{REG} = 1mA, V_{REG} = 5V				0.05	
		5.5V ≤ V_{IN} ≤ 72V, I_{REG} = 100mA, V_{REG} = 5V			1.5		
Load Regulation	ΔVREG / ΔIREG	1mA ≤ I_{REG} ≤ 100mA, V_{REG} = 5V				0.8	mV/mA
Power-Supply Rejection Ratio		I_{REG} = 10mA, f = 100Hz, 0.5V_{P-P}			55		dB
Startup Response Time	t_{START}	R_{REG} = 500Ω, V_{REG} = 5V, C_{REG} = 4.7µF			180		µs
POK Assertion Threshold (MAX6397 Only)	V_{POK_TH}	L		4.500	4.67	4.780	V
		M		4.230	4.375	4.500	
		T		2.966	3.053	3.140	
		S		2.805	2.892	2.970	
		Z		2.250	2.304	2.375	
		Y		2.125	2.188	2.250	
		W		1.590	1.653	1.696	
		V		1.524	1.575	1.625	
REG-to-POK Delay		V_{REG} rising or falling			35		µs
POK Leakage Current		V_{POK} = 5V				100	nA
POK Output Low Voltage	V_{OL}	V_{IN} ≥ 1.5V, I_{SINK} = 1.6mA, POK asserted				0.3	V

Note 1: Specifications to T_A = -40°C are guaranteed by design and not production tested.
Note 2: The MAX6397/MAX6398 power up with the external FET in off mode (V_{GATE} = GND). The external FET turns on t_{START} after the device is powered up and all input conditions are valid.
Note 3: For accurate overtemperature-shutdown performance, place the device in close thermal contact with the external MOSFET.
Note 4: Dropout voltage is defined as V_{IN} - V_{REG} when V_{REG} is 2% below the value of V_{REG} for V_{IN} = V_{REG} (nominal) + 2V.
Note 5: Operations beyond the thermal dissipation limit may permanently damage the device.

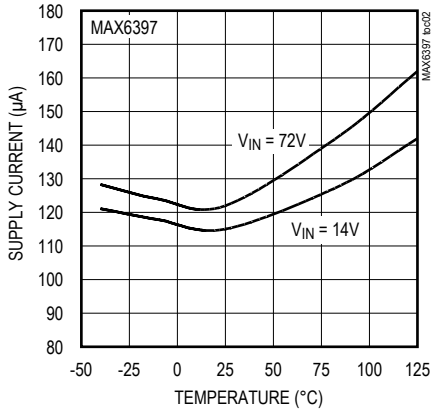
Typical Operating Characteristics

(V_{IN} = 14V, C_{REG} = 4.7µF, I_{REG} = 0, unless otherwise noted.)

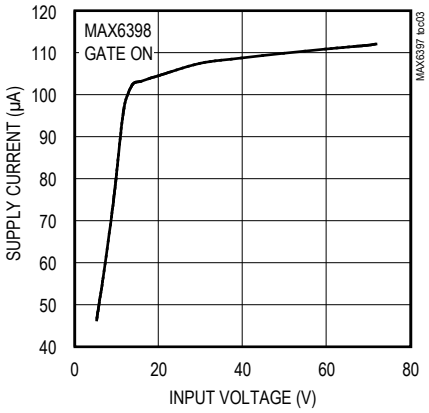
SUPPLY CURRENT vs. INPUT VOLTAGE



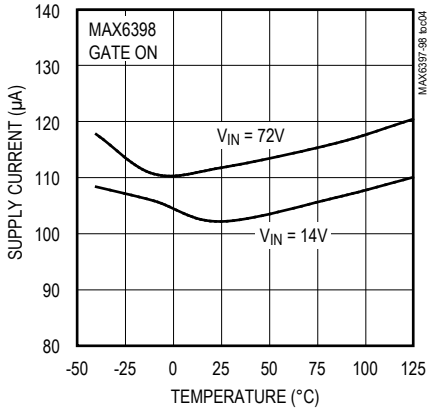
SUPPLY CURRENT vs. TEMPERATURE



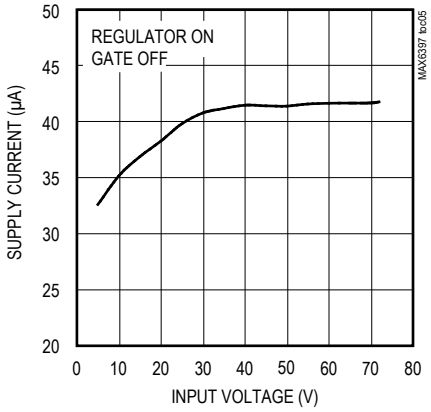
SUPPLY CURRENT vs. INPUT VOLTAGE



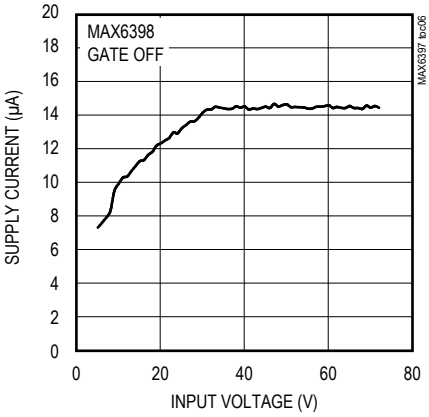
SUPPLY CURRENT vs. TEMPERATURE



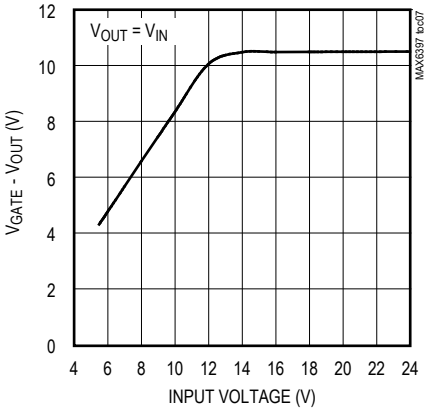
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (MAX6397)



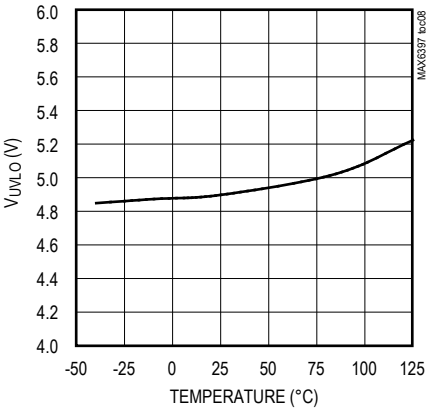
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



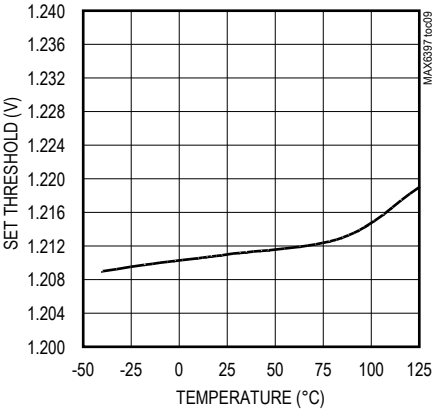
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



UVLO THRESHOLD vs. TEMPERATURE



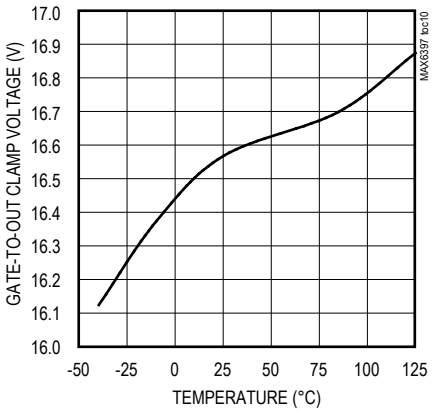
SET THRESHOLD vs. TEMPERATURE



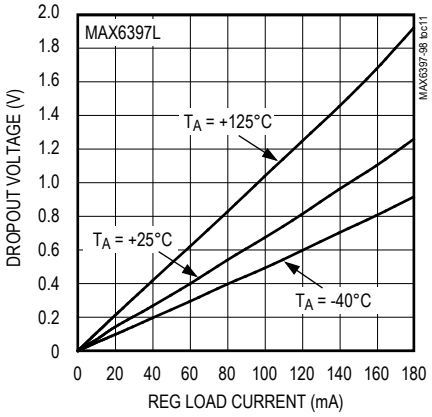
Typical Operating Characteristics (continued)

(V_{IN} = 14V, C_{REG} = 4.7µF, I_{REG} = 0, unless otherwise noted.)

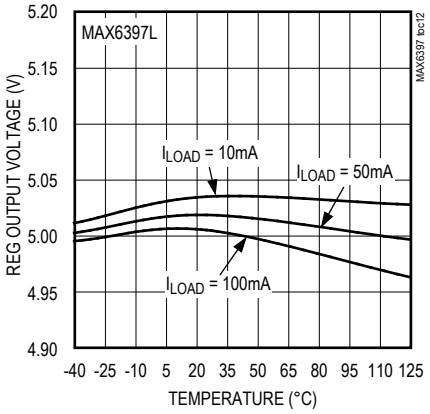
GATE-TO-OUT CLAMP VOLTAGE vs. TEMPERATURE



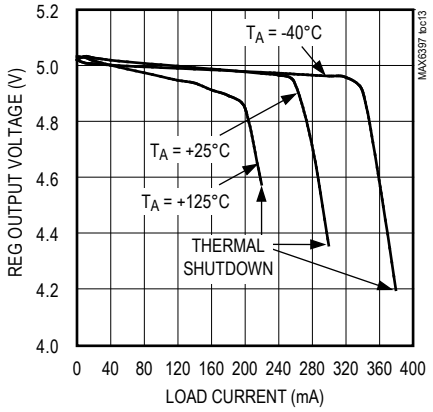
DROPOUT VOLTAGE vs. REG LOAD CURRENT



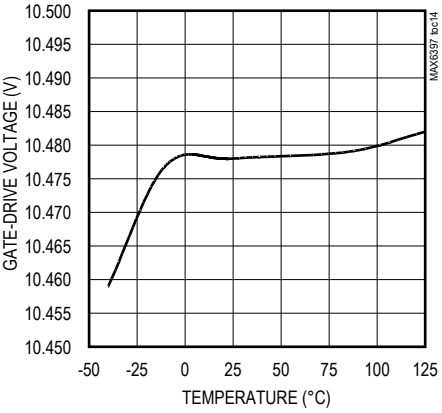
REG OUTPUT VOLTAGE vs. LOAD CURRENT AND TEMPERATURE



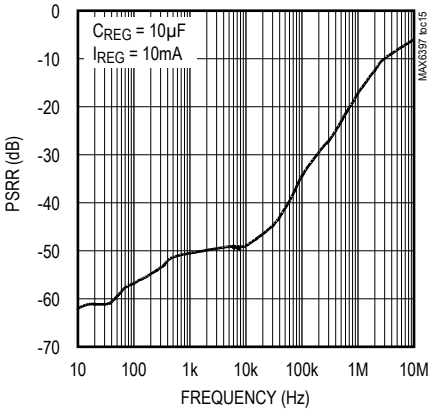
MAXIMUM REG OUTPUT VOLTAGE vs. LOAD CURRENT AND TEMPERATURE



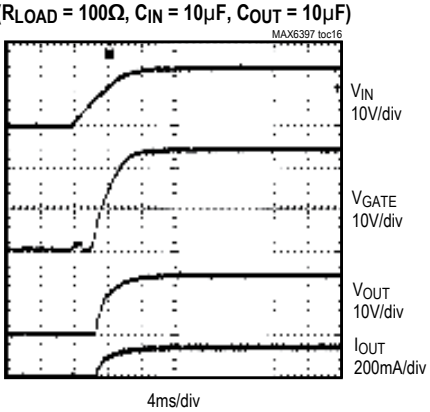
GATE-DRIVE VOLTAGE vs. TEMPERATURE



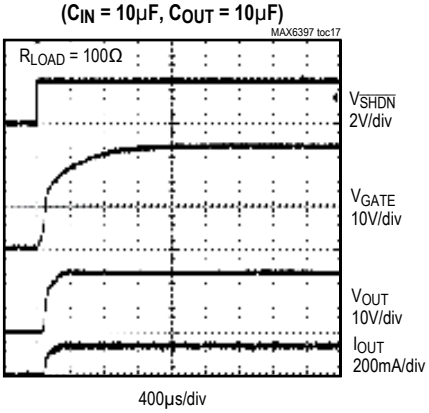
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



STARTUP WAVEFORM (R_{LOAD} = 100Ω, C_{IN} = 10µF, C_{OUT} = 10µF)



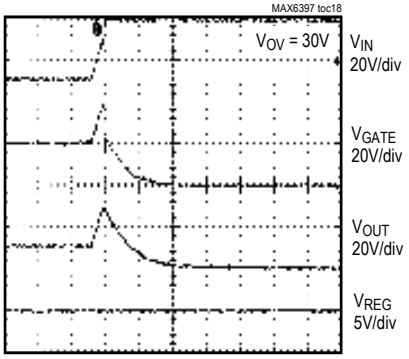
STARTUP WAVEFORM FROM SHUTDOWN (C_{IN} = 10µF, C_{OUT} = 10µF)



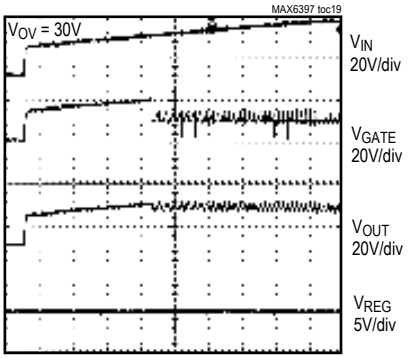
Typical Operating Characteristics (continued)

(V_{IN} = 14V, C_{REG} = 4.7µF, I_{REG} = 0, unless otherwise noted.)

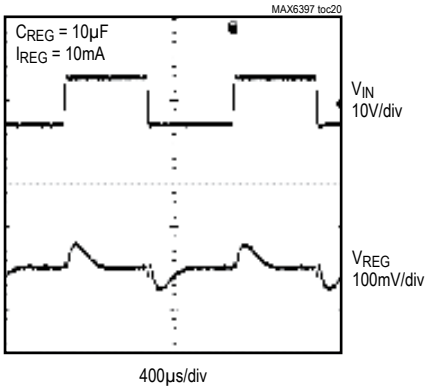
OVERVOLTAGE SWITCH FAULT



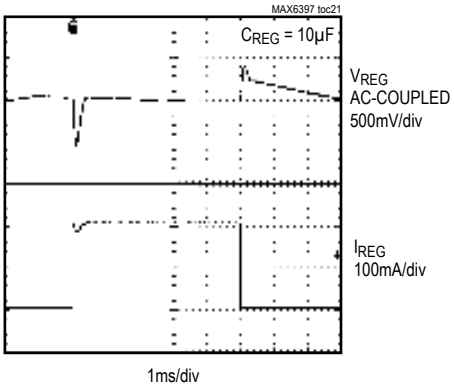
VOLTAGE LIMIT FAULT



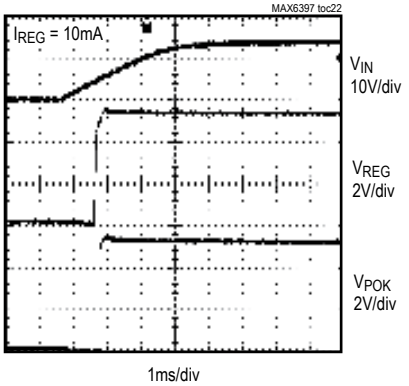
TRANSIENT RESPONSE



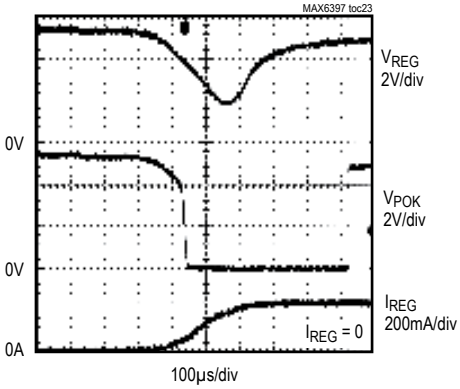
REG LOAD-TRANSIENT RESPONSE



REGULATOR STARTUP WAVEFORM



REGULATOR POK ASSERTION



Pin Description

PIN		NAME	FUNCTION
MAX6397	MAX6398		
1	1	IN	Supply Voltage Input. Bypass with a minimum 10µF capacitor to GND.
2	2	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to force GATE low, turning off the external n-channel MOSFET. REG remains active when in shutdown mode. $\overline{SHDN}$ is internally pulled down to GND with a 1µA source. Connect to IN for normal operation.
3	3	SET	Overvoltage-Threshold-Adjustment Input. Connect SET to an external resistor voltage-divider network to OUT (overvoltage limiter) or IN (overvoltage switch) to adjust the desired overvoltage-limit threshold. Use SET to monitor a system input or output voltage.
4	—	POK	Open-Drain Output. POK remains low until REG exceeds 92.5% or 87.5% of REG nominal output voltage. Connect to an external pullup resistor.
5	4	GND	Ground
6	5	GATE	Gate-Drive Output. Connect GATE to the gate of an external n-channel MOSFET. GATE is a charge pump with a 75µA pullup current to 10V (typ) above IN during normal operation. GATE is quickly shorted to OUT during an overvoltage condition. GATE pulls low when $\overline{SHDN}$ is low.
7	6	OUT	Output-Voltage-Sense Input. Connect to the source of the external n-channel MOSFET.
8	—	REG	Regulator Output. Fixed 5.0V, 3.3V, 2.5V, or 1.8V output. REG sources up to 100mA. Bypass with a minimum 4.7µF capacitor to GND.
—	—	EP	Exposed Pad. Connect to ground plane.

Detailed Description

The MAX6397/MAX6398 are ultra-small, low-current, high-voltage protection circuits for applications that must survive high-voltage transient conditions. These devices monitor the input/output voltages and control an external n-channel MOSFET to isolate the load or to regulate the output voltage from overvoltage-transient energy. The controller allows system designers to size the external MOSFET to their load current and board size.

The MAX6397/MAX6398 drive the MOSFET's gate high when the monitored input voltage is below the adjustable overvoltage threshold. An internal charge-pump circuit provides a 5V to 10V gate-to-source drive (see the *Typical Operating Characteristics*) to ensure low input-to-load voltage drops in normal operating modes. When the input voltage rises above the user-adjusted overvoltage threshold, GATE pulls to OUT, turning off the MOSFET.

The MAX6397/MAX6398 are configurable to operate as overvoltage-protection switches or as closed-looped voltage limiters. In overvoltage-protection switch mode, the input voltage is monitored. When an overvoltage condition occurs at IN, GATE pulls low, disconnecting the load from the power source, and then slowly enhances upon removal of the overvoltage condition. In overvoltage-limit mode, the output voltage is monitored and the MAX6397/MAX6398 regulate the source of the external MOSFET at the adjusted overvoltage threshold, allowing devices within the system to continue operating during an overvoltage condition.

The MAX6397/MAX6398 undervoltage lockout (UVLO) function disables the devices as long as the input remains below the 5V (typ) UVLO turn-on threshold. The MAX6397/MAX6398 have an active-lows $\overline{SHDN}$ input to turn off the external MOSFET, disconnecting the load and reducing power consumption. After power is applied and $\overline{SHDN}$ is driven above its logic-high voltage, there is a 100µs delay before GATE enhancement commences.

The MAX6397 integrates a high input voltage, low-quiescent-current linear regulator, in addition to an overvoltage-protector circuit. The linear regulator remains enabled at all times to power low-current "always-on" applications (independent of the state of the external MOSFET). The regulator is offered with several standard output voltage options (5V, 3.3V, 2.5V, or 1.8V). An open-drain power-good output notifies the system if the regulator

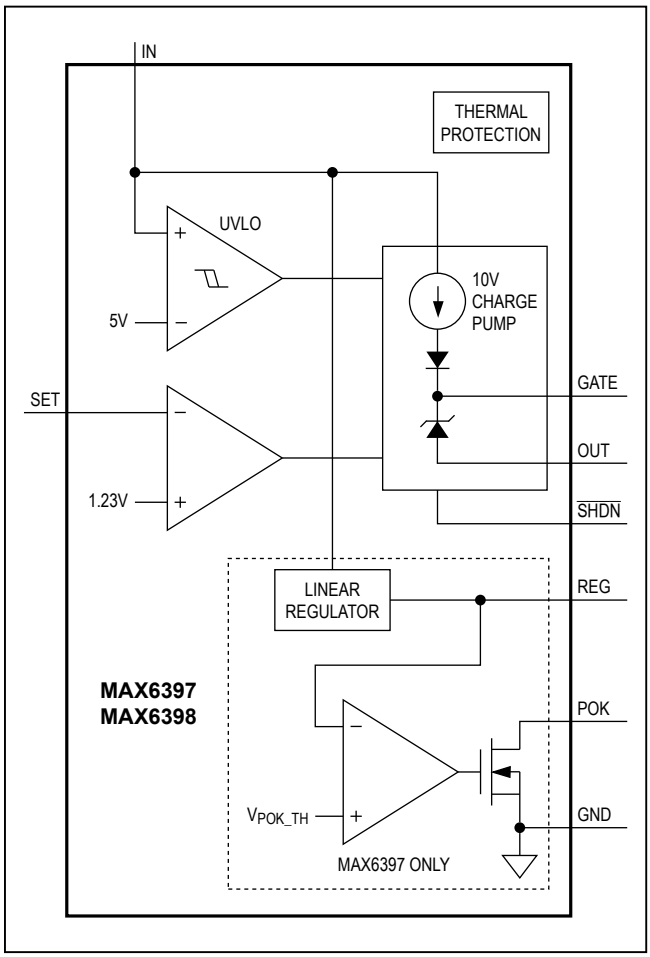


Figure 1. Functional Diagram

output falls to 92.5% or 87.5% of its nominal voltage. The MAX6397's REG output operates independently of the $\overline{SHDN}$ logic input.

The MAX6397/MAX6398 include internal thermal-shutdown protection, disabling the external MOSFET and linear regulator if the chip reaches overtemperature conditions.

Linear Regulator (MAX6397 Only)

The MAX6397 is available with 5.0V, 3.3V, 2.5V, and 1.8V factory-set output voltages. Each regulator sources up to 100mA and includes a current limit of 230mA. The linear regulator operates in an always-on condition regardless of the $\overline{SHDN}$ logic. For fully specified operation, V_{IN} must be greater than 6.5V for the MAX6397L/M (5V regulator output). The actual output current may be limited by the operating condition and package power dissipation.

Power-OK Output

POK is an open-drain output that goes low when REG falls to 92.5% or 87.5% (see the *Selector Guide*) of its nominal output voltage. To obtain a logic-level output, connect a pullup resistor from POK to REG or another system voltage. Use a resistor in the 100kΩ range to minimize current consumption. POK provides a valid logic-output level down to V_{IN} = 1.5V.

GATE Voltage

The MAX6397/MAX6398 use a high-efficiency charge pump to generate the GATE voltage. Upon V_{IN} exceeding the 5V (typ) UVLO threshold, GATE enhances 10V above IN (for V_{IN} ≥14V) with a 75µA pullup current. An overvoltage condition occurs when the voltage at SET pulls above its 1.215V threshold. When the threshold is crossed, GATE falls to OUT within 100ns with a 100mA (typ) pulldown current. The MAX6397/MAX6398 include an internal clamp to OUT that ensures GATE is limited to 18V (max) above OUT to prevent gate-to-source damage to the external FET.

The GATE cycle during overvoltage-limit and overvoltage-switch modes are quite similar but have distinct characteristics. In overvoltage-switch mode (Figure 2a), GATE is enhanced to V_{IN} + 10V while the monitored IN voltage remains below the overvoltage-fault threshold (SET < 1.215V). When an overvoltage fault occurs (SET ≥ 1.215V), GATE is pulled one diode below OUT, turning off the external FET and disconnecting the load from the input. GATE remains low (FET off) as long as V_{IN} is above the overvoltage-fault threshold. As V_{IN} falls back below the overvoltage-fault threshold (-5% hysteresis), GATE is again enhanced to V_{IN} + 10V.

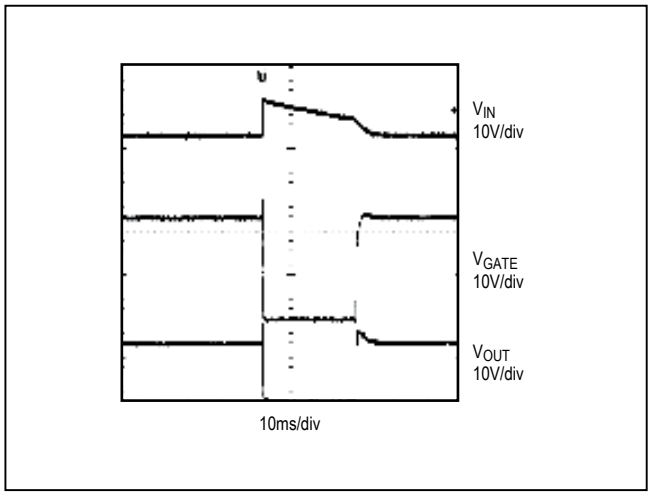


Figure 2a. MAX6397/MAX6398 GATE Waveform During Overvoltage Switch Mode

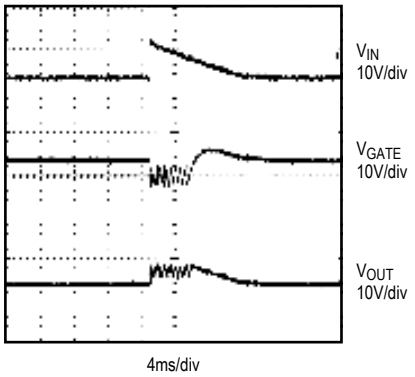


Figure 2b. MAX6397/MAX6398 GATE Waveform During Overvoltage Limit Mode

In overvoltage-limit mode (Figure 2b), GATE is enhanced to V_{IN} + 10V. While the monitored OUT voltage remains below the overvoltage fault threshold (SET < 1.215V). When an overvoltage fault occurs (SET ≥ 1.215V), GATE is pulled low one diode drop below OUT until OUT drops 5% below the overvoltage-fault threshold. GATE is then turned back on until OUT again reaches the overvoltage-fault threshold and GATE is again turned off.

GATE cycles on-off-on-off-on in a sawtooth waveform until OUT remains below the overvoltage-fault threshold and GATE remains constantly on (V_{IN} + 10V). The overvoltage limiter's sawtooth GATE output operates the MOSFET in a switched-linear mode while the input voltage remains above the overvoltage-fault threshold. The sawtooth frequency depends on the load capacitance, load current, and MOSFET turn-on time (GATE charge current and GATE capacitance).

GATE goes high when the following startup conditions are met: V_{IN} is above the UVLO threshold, $\overline{SHDN}$ is high, an overvoltage fault is not present and the device is not in thermal shutdown.

Overvoltage Monitoring

When operating in overvoltage mode, the MAX6397/MAX6398 feedback path (Figure 3) consists of IN, SET's internal comparator, the internal gate charge pump, and the external n-channel MOSFET resulting in a switch-on/off function. When the programmed overvoltage threshold is tripped, the internal fast comparator turns off the external MOSFET, pulling GATE to OUT within t_{OV} and disconnecting the power source from the load. When IN decreases below the adjusted overvoltage threshold, the MAX6397/MAX6398 slowly enhance GATE above OUT, reconnecting the load to the power source.

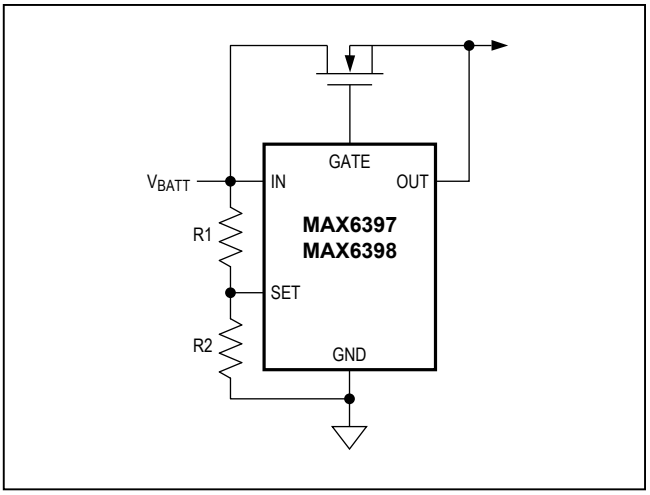


Figure 3. Overvoltage Switch Protection Configuration

Overvoltage Limiter

When operating in overvoltage-limiter mode, the MAX6397/MAX6398 feedback path (Figure 4) consists of OUT, SET's internal comparator, the internal gate charge pump and the external n-channel MOSFET, which results in the external MOSFET operating as a voltage regulator.

During normal operation, GATE is enhanced 10V above OUT. The external MOSFET source voltage is monitored through a resistor-divider between OUT and SET. When OUT rises above the adjusted overvoltage threshold, an internal comparator sinks the charge-pump current, discharging the external GATE, regulating OUT at the set overvoltage threshold. OUT remains active during

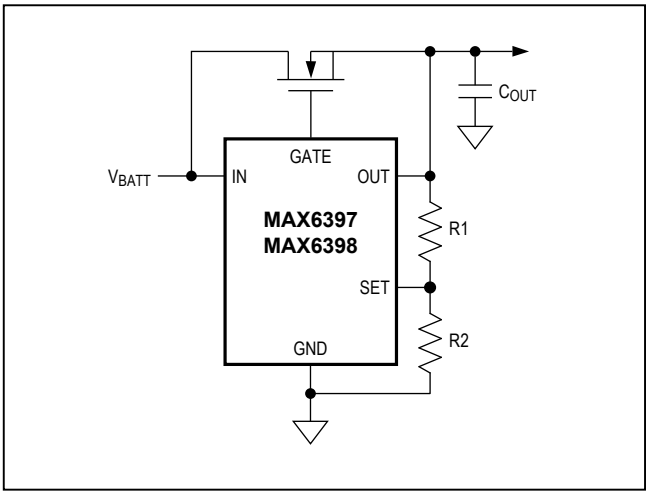


Figure 4. Overvoltage Limiter Protection Switch Configuration

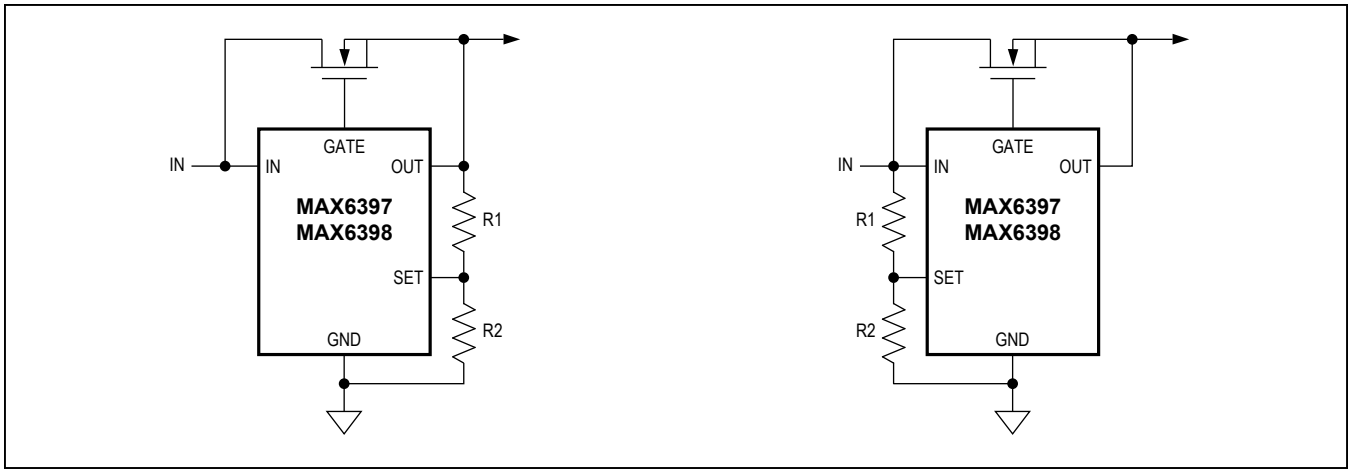


Figure 5. Setting the MAX6397/MAX6398 Overvoltage Threshold

the overvoltage transients and the MOSFET continues to conduct during the overvoltage event, operating in switched-linear mode.

As the transient begins decreasing, OUT fall time will depend on the MOSFET's GATE charge, the internal charge-pump current, the output load, and the tank capacitor at OUT.

For fast-rising transients and very large-sized MOSFETs, add an additional external bypass capacitor from GATE to GND to reduce the effect of the fast-rising voltages at IN. The external capacitor acts as a voltage-divider working against the MOSFETs' drain-to-gate capacitance. For a 6000pF C_{gd}, a 0.1µF capacitor at GATE will reduce the impact of the fast-rising V_{IN} input.

Caution must be exercised when operating the MAX6397/MAX6398 in voltage-limiting mode for long durations. If the V_{IN} is a DC voltage greater than the MOSFET's maximum gate voltage, the FET will dissipate power continuously. To prevent damage to the external MOSFET, proper heatsinking should be implemented.

Applications Information

Setting Overvoltage Thresholds

SET provides an accurate means to set the overvoltage level for the MAX6397/MAX6398. Use a resistor-divider to set the desired overvoltage condition (Figure 5). SET has a rising 1.215V threshold with a 5% falling hysteresis.

Begin by selecting the total end-to-end resistance, R_{TOTAL} = R1 + R2. Choose R_{TOTAL} to yield a total current equivalent to a minimum 100 x I_{SET} (SET's input bias current) at the desired overvoltage threshold.

For example:

With an overvoltage threshold set to 20V:

$$R_{TOTAL} < 20V/(100 \times I_{SET})$$

where I_{SET} is SET's 50nA input bias current.

$$R_{TOTAL} < 4M\Omega$$

Use the following formula to calcue R2:

$$R2 = V_{TH} \times \frac{R_{TOTAL}}{V_{OV}}$$

where V_{TH} is the 1.215V SET rising threshold and V_{OV} is the overvoltage threshold.

R2 = 243kΩ, use a 240kΩ standard resistor.

R_{TOTAL} = R2 + R1, where R1 = 3.76MΩ.

Use a 3.79MΩ standard resistor.

A lower value for total resistance dissipates more power but provides slightly better accuracy.

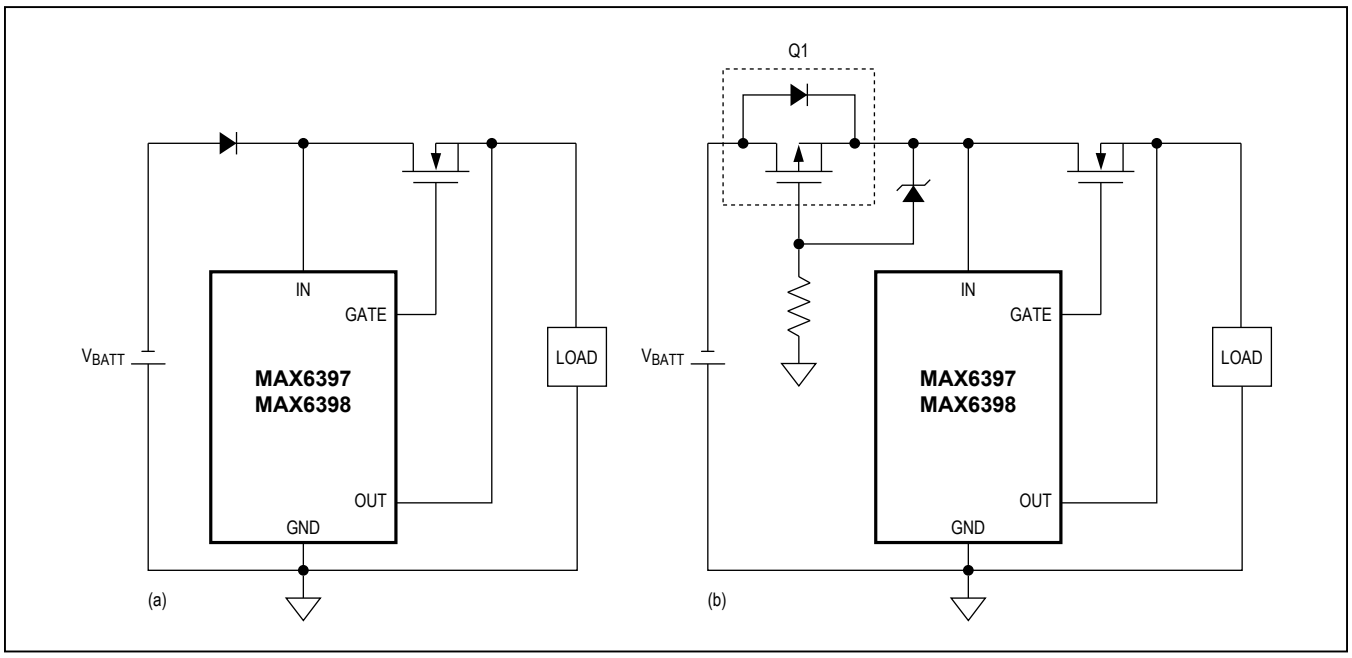


Figure 6. Reverse-Battery Protection Using a Diode or p-Channel MOSFET

Reverse-Battery Protection

Use a diode or p-channel MOSFET to protect the MAX6397/MAX6398 during a reverse-battery insertion (Figures 6a, 6b). Low p-channel MOSFET on-resistance of 30mΩ or less yields a forward-voltage drop of only a few millivolts (versus hundreds of millivolts for a diode, Figure 6a) thus improving efficiency.

Connecting a positive battery voltage to the drain of Q1 (Figure 6b) produces forward bias in its body diode, which clamps the source voltage one diode drop below the drain voltage. When the source voltage exceeds Q1's threshold voltage, Q1 turns on. Once the FET is on, the battery is fully connected to the system and can deliver power to the device and the load.

An incorrectly inserted battery reverse-biases the FET's body diode. The gate remains at the ground potential. The FET remains off and disconnects the reversed battery from the system. The zener diode and resistor combination prevent damage to the p-channel MOSFET during an overvoltage condition.

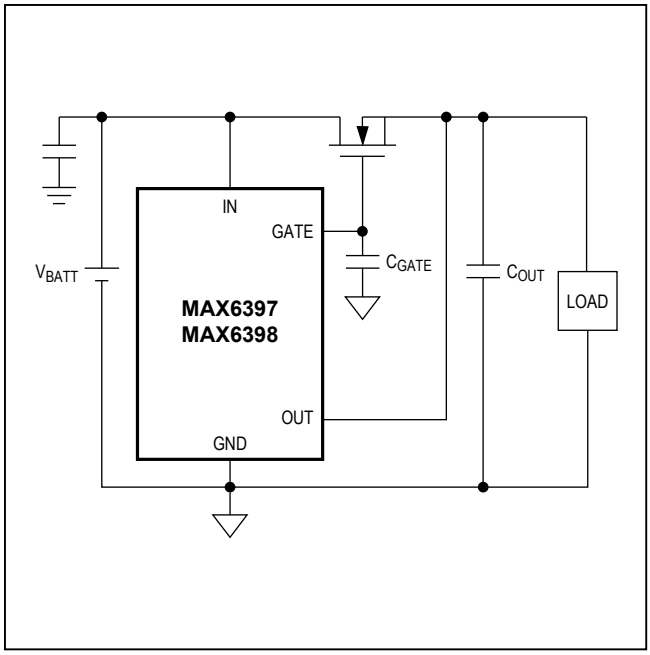


Figure 7. MAX6397/MAX6398 Controlling GATE Inrush Current

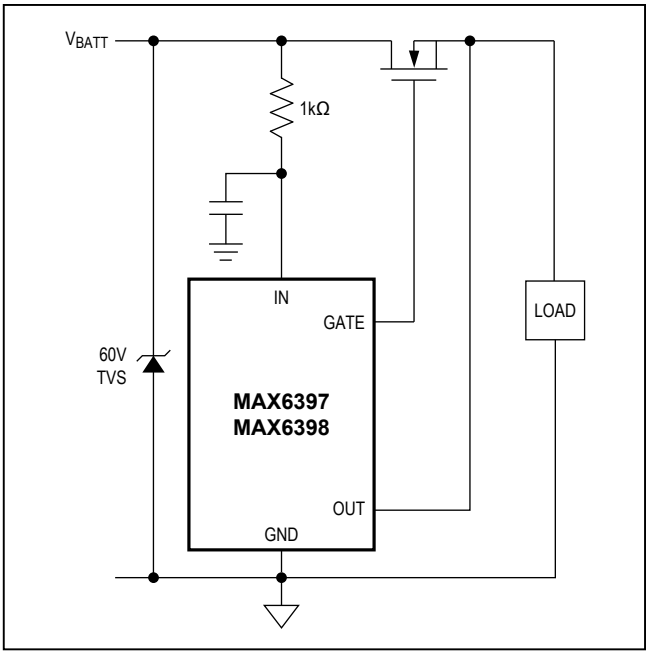


Figure 8. Protecting the MAX6397/MAX6398 Input from High-Voltage Transients

REG Capacitor Selection for Stability

For stable operation over the full temperature range and with load currents up to 100mA, use ceramic capacitor values greater than 4.7µF. Large output capacitors help reduce noise, improve load-transient response, and power-supply rejection at REG. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. At lower temperatures, it may be necessary to increase capacitance.

Under normal conditions, use a 10µF capacitor at IN. Larger input capacitor values and lower ESR provide better supply-noise rejection and line-transient response.

Inrush/Slew-Rate Control

Inrush current control can be implemented by placing a capacitor at GATE (Figure 7) to slowly ramp up the GATE, thus limiting the inrush current and controlling GATE's slew rate during initial turn-on. The inrush current can be approximated using the followng formula:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \times I_{GATE} + I_{LOAD}$$

where I_{GATE} is GATE's 75µA sourcing current, I_{LOAD} is the load current at startup, and C_{OUT} is the output capacitor.

Input Transients Clamping

When the external MOSFET is turned off during an overvoltage occurrence, stray inductance in the power path may cause voltage ringing exceeding the MAX6397/MAX6398 absolute maximum input (IN) supply rating. The following techniques are recommended to reduce the effect of transients:

- Minimize stray inductance in the power path using wide traces, and minimize loop area including the power traces and the return ground path.
- Add a zener diode or transient voltage suppressor (TVS) rated below the IN absolute maximum rating (Figure 8).

Add a resistor in series with IN to limit transient current going into the input for the MAX6398 only.

MOSFET Selection

Select external MOSFETs according to the application current level. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have minimum voltage drop at full load to limit the MOSFET power dissipation. Determine the device power rating to accommodate an overvoltage fault when operating the MAX6397/MAX6398 in overvoltage-limit mode.

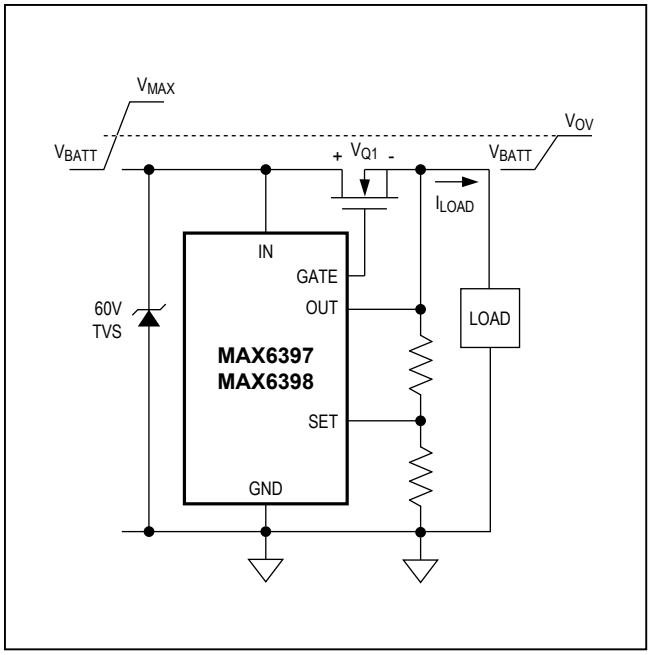


Figure 9. Power Dissipated Across MOSFETs During an Overvoltage Fault (Overvoltage Limiter Mode)

During normal operation, the external MOSFETs dissipate little power. The power dissipated in normal operation is:

$$P_{Q1} = I_{LOAD}2 \times R_{DS(ON)}.$$

The most power dissipation will occur during a prolonged overvoltage event when operating the MAX6397/MAX6398 in voltage limiter mode, resulting in high power dissipated in Q1 (Figure 9) where the power dissipated across Q1 is:

$$P_{Q1} = V_{Q1} \times I_{LOAD}$$

where V_{Q1} is the voltage across the MOSFET's drain and source.

Thermal Shutdown

The thermal-shutdown feature of the MAX6397/MAX6398 shuts off the linear regulator output (REG), and GATE if it exceeds the maximum allowable thermal dissipation. Thermal shutdown also monitors the PCB temperature of the external nFET when the devices sit on the same thermal island. Good thermal contact between the MAX6397/MAX6398 and the external nFET is essential for the thermal-shutdown feature to operate effectively. Place the nFET as close as possible to OUT.

When the junction temperature exceeds T_J = +150°C, the thermal sensor signals the shutdown logic, turning off REG's internal pass transistor and the GATE output, allowing the device to cool. The thermal sensor turns the pass transistor and GATE on again after the IC's junction temperature cools by 20°C. Thermal-overload protection is designed to protect the MAX6397/MAX6398 and the external MOSFET in the event of current-limit fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

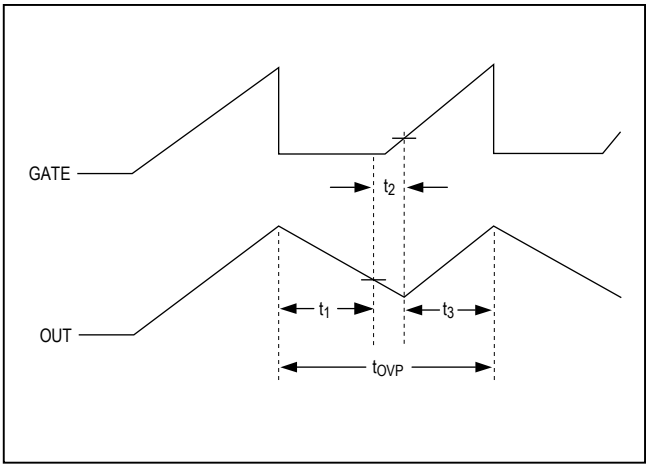


Figure 10. MAX6397/MAX6398 Timing Diagram

Thermal Shutdown

Overvoltage Limiter Mode

When operating the devices in overvoltage-limit mode for a prolonged period of time, a thermal shutdown is possible due to device self-heating. The thermal shutdown is dependent on a number of different factors:

- The device's ambient temperature (T_A)
- The output capacitor (C_{OUT})
- The output load current (I_{OUT})
- The overvoltage-threshold limit (V_{OV})
- The overvoltage-waveform period (t_{OVP})
- The power dissipated across the package (P_{DISS})

When OUT exceeds the adjusted overvoltage threshold, an internal GATE pulldown current is enabled until OUT drops by 5%. The capacitance at OUT is discharged by the internal current sink and the external OUT load current. The discharge time ($\Delta t1$) is approximately:

$$\Delta t1 = C_{OUT} \frac{V_{OV} \times 0.05}{I_{OUT} + I_{GATEPD}}$$

where V_{OV} is the adjusted overvoltage threshold, I_{OUT} is the external load current and I_{GATEPD} is the GATE's internal 100mA (typ) pulldown current.

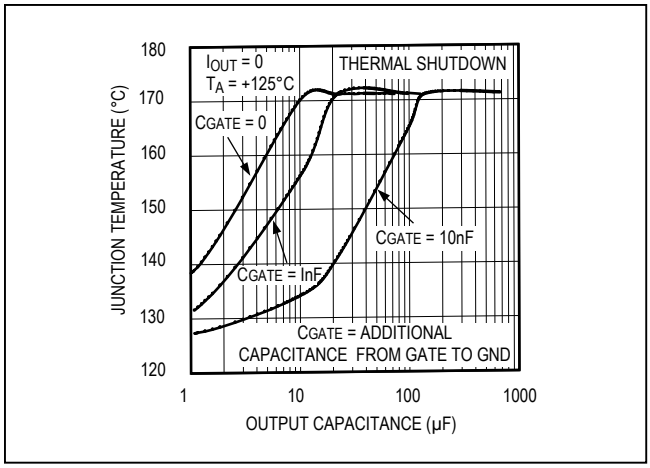


Figure 11. Junction Temperature vs. C_{OUT}

When OUT falls 5% below the overvoltage-threshold point, the internal current sink is disabled and the MAX6397/MAX6398's internal charge pump begins recharging the external GATE voltage. The OUT voltage continues to drop due to the external OUT load current until the MOSFET gate is recharged. The time needed to recharge GATE and re-enhance the external nFET is approximately:

$$\Delta t2 = C_{ISS}\frac{V_{GS(TH)} + V_F}{I_{GATE}}$$

where C_{ISS} is the MOSFET's input capacitance, $V_{GS(TH)}$ is the MOSFET's gate-to-source threshold voltage, V_F is the internal clamp diode forward voltage (V_F = 1.5V typ), and I_{GATE} is the MAX6397/MAX6398 charge-pump current (75µA typ).

During $\Delta t2$, C_{OUT} loses charge through the output load. The voltage across C_{OUT} ($\Delta V2$) decreases until the MOSFET reaches its $V_{GS(TH)}$ threshold and can be approximated using the following formula:

$$\Delta V2 = I_{OUT}\frac{\Delta t2}{C_{OUT}}$$

Once the MOSFET $V_{GS(TH)}$ is obtained, the slope of the output voltage rise is determined by the MOSFET Q_G charge through the internal charge pump, with respect to the drain potential. The time for the OUT voltage to rise again to the overvoltage threshold can be approximated using the following formula:

$$\Delta t3 \cong \frac{Q_{GD}}{V_{GS_QGD}} \times \frac{\Delta V_{OUT}}{I_{GATE}}$$

where ΔV_{OUT} = (V_{OV} x 0.05) + $\Delta V2$.

The total period of the overvoltage waveform can be summed up as follows:

$$t_{OVP} = \Delta t1 + \Delta t2 + \Delta t3$$

The MAX6397/MAX6398 dissipate the most power during an overvoltage event when I_{OUT} = 0 (C_{OUT} is discharged only by the internal current sink). The maximum power dissipation can be approximated using the following equation:

$$P_{DISS} = V_{OV} \times 0.975 \times I_{GATEPD} \times \frac{\Delta t1}{\Delta t_{OVP}}$$

The die temperature (T_J) increase is related to θ_{JC} (8.3°C/W and 8.5°C/W for the MAX6397 and MAX6398, respectively) of the package when mounted correctly with a strong thermal contact to the circuit board. The MAX6397/MAX6398 thermal shutdown is governed by the following equation:

$$T_J = T_A + P_{DISS} \text{ x } (\theta_{JC} + \theta_{CA}) < 170°C$$

(typical thermal-shutdown temperature)

For the MAX6397, the power dissipation of the internal linear regulator must be added to the overvoltage-protection circuit power dissipation to calculate the die temperature. The linear regulator power dissipation is calculated using the following equation:

$$P_{REG} = (V_{IN} - V_{REG})\,(I_{REG})$$

For example, using an IRFR3410 100V n-channel MOSFET, Figure 11 illustrates the junction temperature vs. output capacitor with I_{OUT} = 0, T_A = +125°C, V_{OV} < 16V,V_F = 1.5V, I_{GATE} = 75mA, and I_{GATEPD} = 100mA. Figure 11 shows the relationship between output capacitance versus die temperature for the conditions listed above.

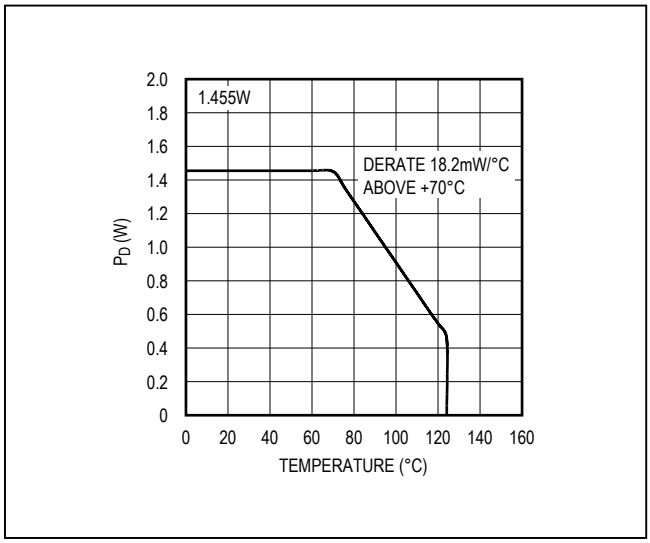


Figure 12. Maximum Power Dissipation vs. Temperature

An additional capacitor can be added to GATE and GND to shift the curves as this increases Δt1. These values are used for illustration only. Customers must verify worst-case conditons for their specific application.

OUTPUT Current Calculation

The MAX6397 high input voltage (+72V max) provides up to 100mA of output current at REG. Package power dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figure 12 depicts the maximum power dissipation curve for the MAX6397. The graph assumes that the exposed metal pad of the MAX6397 package is soldered to 1in2 of PCB copper. Use Figure 10 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation:

$$P_{DISS} = 1.455W \text{ for } T_A \le +70°C$$

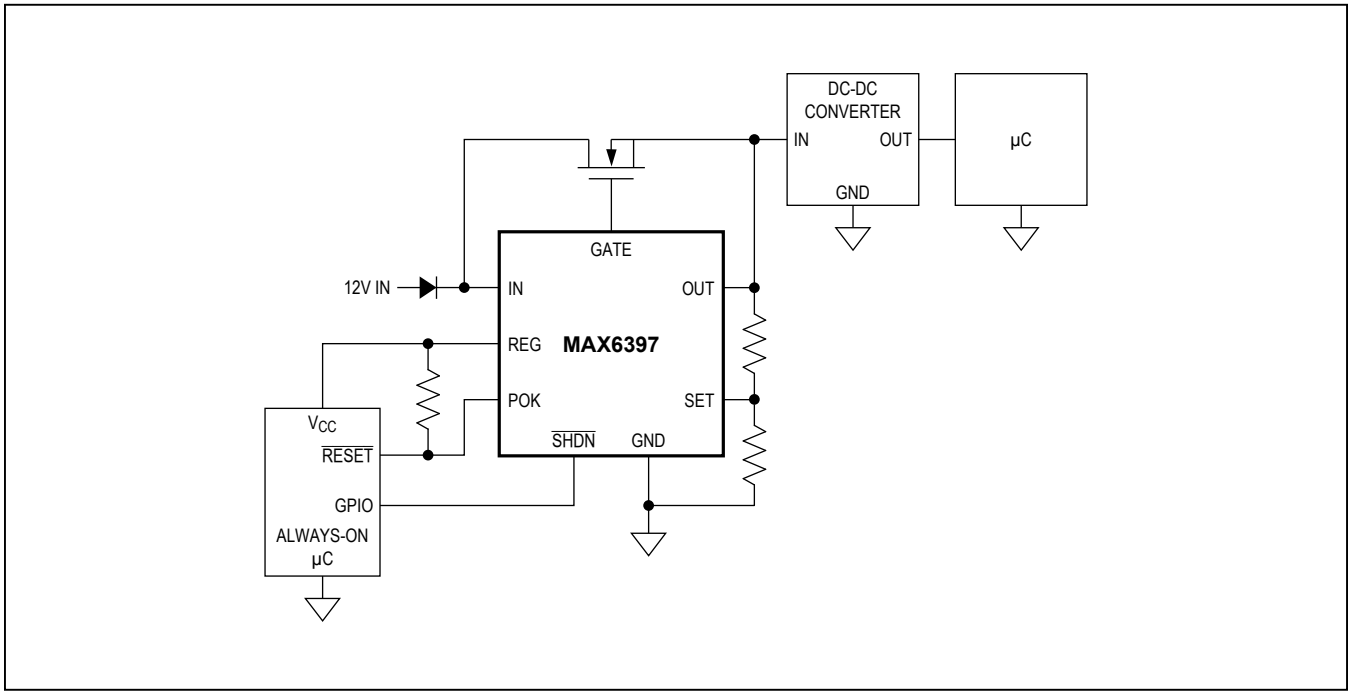
Maximum power dissipation = 1.455 - 0.0182 (T_A - 70°C) for +70°C ≤ T_A ≤ +125°C

where 0.0182 W/°C is the MAX6397 package-thermal derating.

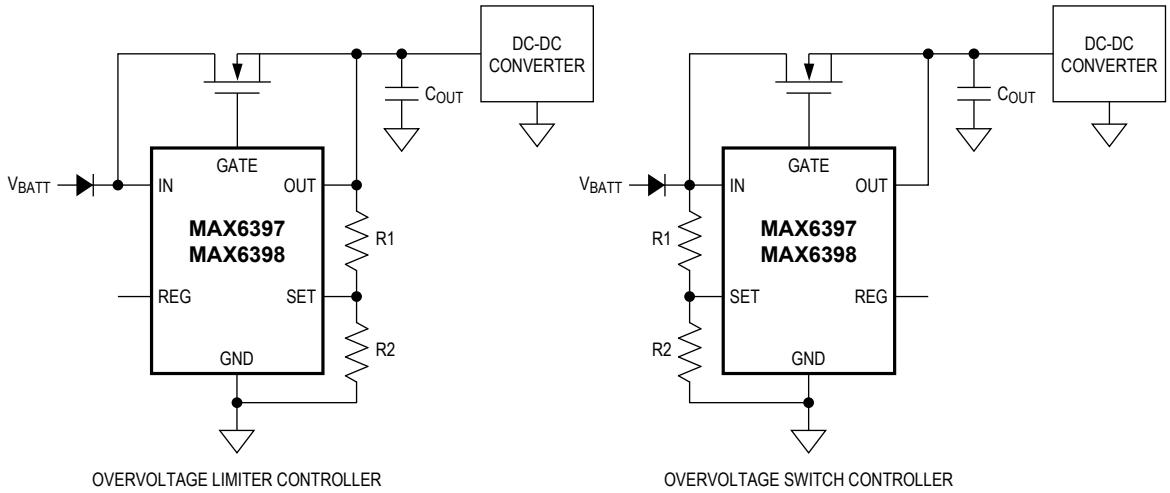
After determining the allowable package dissipation, calculate the maximum output current using the following formula:

$$I_{OUT(MAX)} = \frac{P_{DISS}}{V_{IN} - V_{REG}} \le 100mA$$

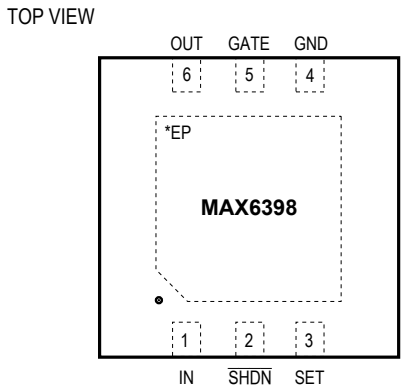
Typical Application Circuit



Typical Operating Circuit



Pin Configurations (continued)



TDFN

*EXPOSED PAD. CONNECT TO GND.

Selector Guide

PART	REG OUTPUT VOLTAGE (V)	POK ASSERTION THRESHOLD (%)	TOP MARK
MAX6397LATA	5.0	92.5	ANN
MAX6397MATA	5.0	87.5	ANO
MAX6397SATA	3.3	87.5	ANQ
MAX6397TATA	3.3	92.5	ANP
MAX6397YATA	2.5	87.5	ANK
MAX6397ZATA	2.5	92.5	ANJ
MAX6397VATA	1.8	87.5	ANM
MAX6397WATA	1.8	92.5	ANL
MAX6398ATT	—	—	AJD

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TDFN	T633+2	21-0137	90-0059
8 TDFN	T833+2	21-0137	90-0058

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/05	Initial release	—
3	1/07	Changed formula and updated Figure 13 caption title	1, 14, 15, 17
4	3/07	Updated *Electrical Characteristics* table.	1, 3, 18
5	1/09	Updated *Electrical Characteristics* table.	3
6	7/14	Deleted automotive references in *General Description*, *Applications*, and *Detailed Description* sections; deleted *Load Dump* section and Figure 5 (renumbering the remaining figures)	1, 7, 10–15

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