# MAX7036

# 300MHz to 450MHz ASK Receiver with Internal IF Filter

## General Description

The MAX7036 low-cost receiver is designed to receive amplitude-shift-keyed (ASK) and on-off-keyed (OOK) data in the 300MHz to 450MHz frequency range. The receiver has an RF input signal range of -109dBm to 0dBm.

The MAX7036 requires few external components and has a power-down pin to put it in a low-current sleep mode, making it ideal for cost- and power-sensitive applications. The low-noise amplifier (LNA), phase-locked loop (PLL), mixer, IF filter, received-signal-strength indicator (RSSI), and baseband sections are all on-chip. The MAX7036 uses a very-low intermediate frequency (VLIF) architecture. The MAX7036 integrates the IF filter on-chip and, therefore, eliminates an external ceramic filter, reducing the bill-of-materials cost. The device also contains an on-chip automatic gain control (AGC) that reduces the LNA gain by 30dB when the input signal power is large. The MAX7036 operates from either a 5V or a 3.3V power supply and draws 5.5mA (typ) of current.

The MAX7036 is available in a 20-pin thin QFN package with an exposed pad and is specified over the AEC-Q100 Level 2 (-40°C to +105°C) temperature range.

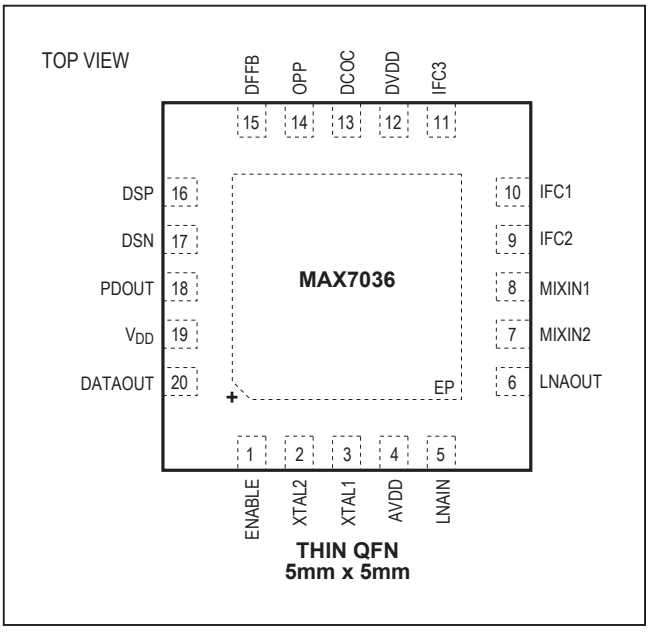
## Applications

- Low-Cost RKE
- Garage Door Openers
- Remote Controls
- Home Automation
- Sensor Networks
- Security Systems

## Benefits and Features

- ASK/OOK Modulation
- < 250µs Enable Turn-On Time
- On-Chip PLL, VCO, Mixer, IF, Baseband
- Low IF (200kHz Nominal)
- 5.5mA DC Current
- 1µA Standby Current
- 3.3V/5V Operation
- Small 20-Pin Thin QFN Package with an Exposed Pad
- AEC-Q100 Qualified

## Pin Configuration




19-4386; Rev 4; 8/21

maxim integrated™

## Absolute Maximum Ratings

$V_{DD}$ to GND.....-0.3V to +6.0V
AVDD to GND.....-0.3V to +4.0V
DVDD to GND.....-0.3V to +4.0V
ENABLE to GND.....-0.3V to ($V_{DD}$ + 0.3V)
LNAIN to GND.....-0.3V to +1.2V
All Other Pins to GND.....-0.3V to ($V_{DVDD}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
20-Pin TQFN (derate 20.8mW/°C above +70°C)...1666.7mW
Junction-to-Case Thermal Resistance ($\theta_{JC}$) (Note 1)
20-Pin TQFN .....2°C/W
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (Note 1)
20-Pin TQFN .....48°C/W
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## 3.3V DC Electrical Characteristics

(*Typical Application Circuit*, 50Ω system impedance, $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.0V to 3.6V, $f_{RF}$ = 300MHz to 450MHz, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.) (100% tested at $T_A$ = +105°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| Supply Current | $I_{IN}$ | $T_A$ < +105°C | $f_{RF}$ = 315MHz | | 5.3 | 6.7 | mA |
| | | | $f_{RF}$ = 433MHz | | 5.8 | 7.3 | |
| | | | Deep-sleep mode, $V_{ENABLE}$ = 0V | | 1 | 2.7 | µA |
| **DIGITAL INPUT (ENABLE)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ | | $V_{DD}$ - 0.4 | | | V |
| Input Low Voltage | $V_{IL}$ | $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ | | | | 0.4 | V |
| Input Current | $I_{ENABLE}$ | 0 ≤ $V_{ENABLE}$ ≤ $V_{DD}$ | | | | 20 | µA |
| **DIGITAL OUTPUT (DATAOUT)** | | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 100µA | | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 100µA | | $V_{DD}$ - 0.4 | | | V |

## 5.0V DC Electrical Characteristics

(*Typical Application Circuit*, 50Ω system impedance, $V_{DD}$ = 4.5V to 5.5V, $f_{RF}$ = 300MHz to 450MHz, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{DD}$ = 5.0V, $T_A$ = +25°C, unless otherwise noted.) (100% tested at $T_A$ = +105°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | $I_{IN}$ | $T_A$ < +105°C | $f_{RF}$ = 315MHz | | 5.4 | 6.8 | mA |
| | | | $f_{RF}$ = 433MHz | | 5.9 | 7.4 | |
| | | | Deep-sleep mode, $V_{ENABLE}$ = 0V | | 1 | 3.4 | µA |
| **DIGITAL INPUT (ENABLE)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{AVDD}$ = $V_{DVDD}$ | | $V_{DD}$ - 0.4 | | | V |
| Input Low Voltage | $V_{IL}$ | $V_{AVDD}$ = $V_{DVDD}$ | | | | 0.4 | V |
| Input Current | $I_{ENABLE}$ | 0 ≤ $V_{ENABLE}$ ≤ $V_{DD}$ | | | | 20 | µA |
| **DIGITAL OUTPUT (DATAOUT)** | | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 100µA | | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 100µA | | $V_{DD}$ - 0.4 | | | V |

## AC Electrical Characteristics

(*Typical Application Circuit*, 50Ω system impedance, $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.0V to 3.6V, $f_{RF}$ = 300MHz to 450MHz, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.3V, $T_A$ = +25°C, $f_{RF}$ = 315MHz, unless otherwise noted.) (100% tested at $T_A$ = +105°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Receiver Input Frequency Range | $f_{RF}$ | | | 300 | | 450 | MHz |
| Maximum Receiver Input Level | $P_{RFIN}$ | | | | 0 | | dBm |
| Sensitivity (Note 2) | | $f_{RF}$ = 315MHz | | | -109 | | dBm |
| | | $f_{RF}$ = 433MHz | | | -107 | | |
| Power-On Time | $t_{ON}$ | Time for valid RSSI output, does not include baseband filter settling | Enable power on ($V_{DD}$ > 3.0V) | | 250 | | µs |
| | | | $V_{DD}$ power on | | 1 | | ms |
| AGC Hysteresis | | | | | 5 | | dB |
| AGC Low Gain-to-High Gain Switching Time | | | | | 13 | | ms |

## AC Electrical Characteristics (continued)

(*Typical Application Circuit*, 50Ω system impedance, $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.0V to 3.6V, $f_{RF}$ = 300MHz to 450MHz, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{AVDD}$ = $V_{DVDD}$ = $V_{DD}$ = 3.3V, $T_A$ = +25°C, $f_{RF}$ = 315MHz, unless otherwise noted.) (100% tested at $T_A$ = +105°C.)

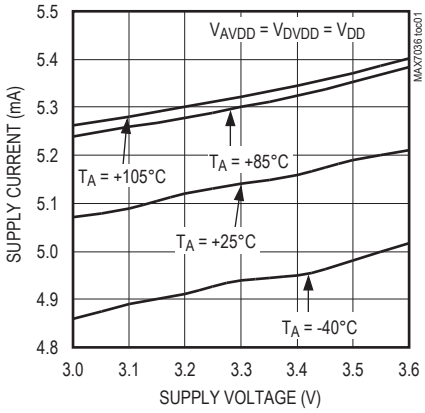
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **LNA/MIXER** | | | | | | | |
| LNA Input Impedance | $Z_{INLNA}$ | Normalized to 50Ω | $f_{RF}$ = 315MHz | | 0.4 - j5.6 | | Ω |
| | | | $f_{RF}$ = 433MHz | | 0.4 - j4.0 | | |
| LO Signal Feedthrough to Antenna | | | | | -75 | | dBm |
| Voltage Gain Reduction | | Low-gain mode, AGC enabled | | | 29 | | dB |
| LNA/Mixer Voltage Gain | | High-gain LNA mode | | | 55 | | dB |
| | | Low-gain LNA mode | | | 26 | | |
| 3dB Cutoff Frequency | $BW_{IF}$ | Set by capacitors on IFC1 and IFC2 (see the *Typical Application Circuit*) | | | 400 | | kHz |
| RSSI Linearity | | | | | ±0.5 | | dB |
| RSSI Dynamic Range | | Includes AGC | | | 80 | | dB |
| RSSI Level | | $P_{RFIN}$ < -120dBm | | | 1.34 | | V |
| | | $P_{RFIN}$ > 0dBm, AGC enabled | | | 2.35 | | |
| Intermediate Frequency | $f_{IF}$ | | | | 200 | | kHz |
| Maximum Data-Filter Bandwidth | $BW_{DF}$ | | | | 50 | | kHz |
| Maximum Data-Slicer Bandwidth | $BW_{DS}$ | | | | 100 | | kHz |
| Maximum Peak Detector Bandwidth | | | | | 50 | | kHz |
| Maximum Data Rate | | Manchester coded | | | 33 | | kbps |
| | | Nonreturn to zero (NRZ) | | | 66 | | |
| Crystal Frequency | $f_{XTAL}$ | | | 9.36 | | 14.06 | MHz |
| Crystal Load Capacitance | $C_{LOAD}$ | | | | 10 | | pF |

**Note 2:** BER = 2 x $10^{-3}$, Manchester coded, data rate = 4kbps. IF bandwidth = 400kHz.

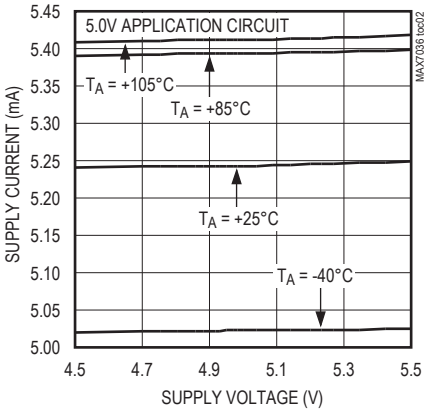
## Typical Operating Characteristics

(*Typical Application Circuit*, $V_{AVDD} = V_{DD} = V_{DVDD} = 3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)

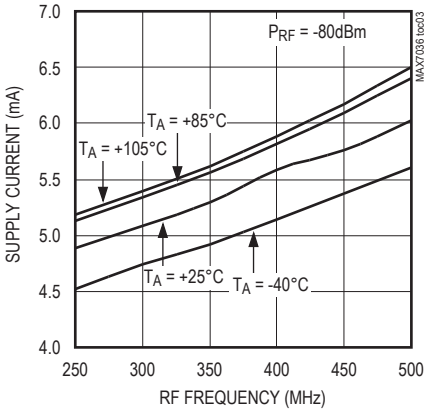
**SUPPLY CURRENT vs. SUPPLY VOLTAGE (3.3V OPERATION)**



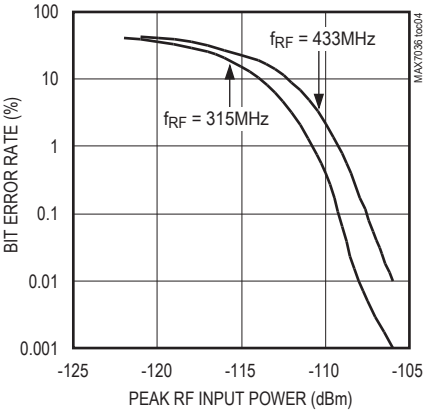

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (5.0V OPERATION)**



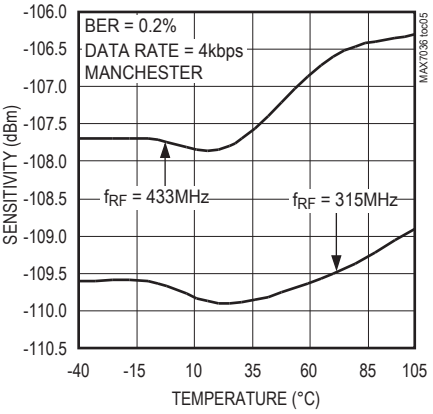

**SUPPLY CURRENT vs. RF FREQUENCY**



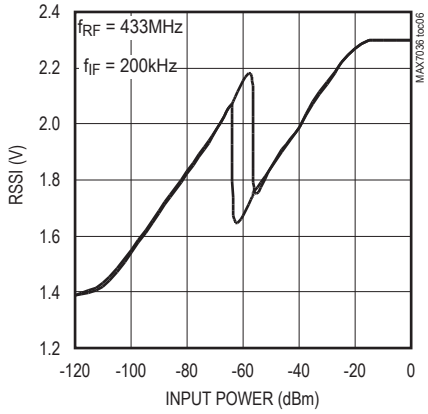

**BIT ERROR RATE vs. PEAK RF INPUT POWER**



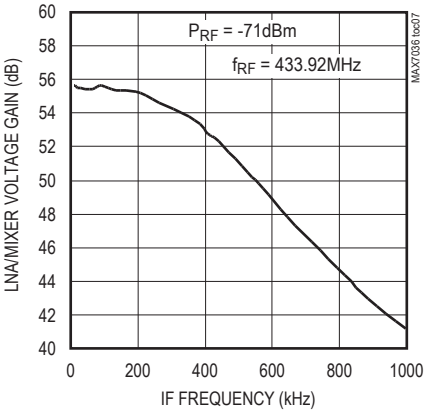

**SENSITIVITY vs. TEMPERATURE**



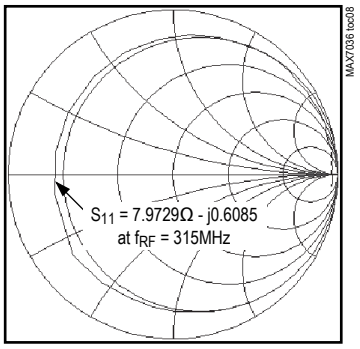

**RSSI vs. INPUT POWER**



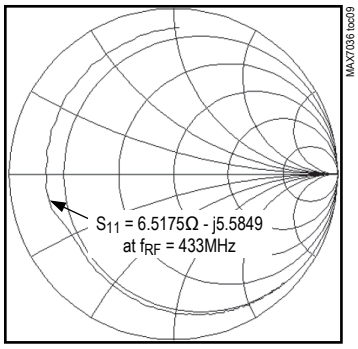

**LNA/MIXER VOLTAGE GAIN vs. IF FREQUENCY**




**$S_{11}$ SMITH CHART PLOT OF RFIN (315MHz CIRCUIT)**



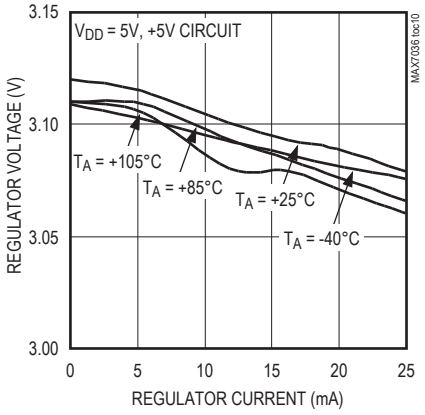

**$S_{11}$ SMITH CHART PLOT OF RFIN (433MHz CIRCUIT)**



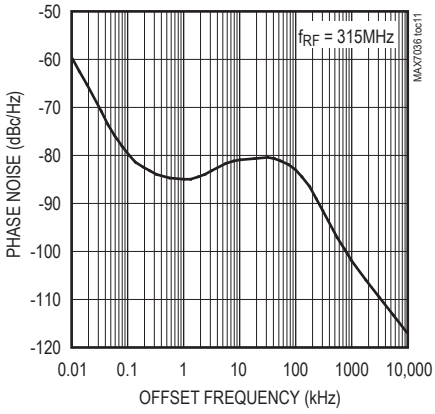
## Typical Operating Characteristics (continued)

(*Typical Application Circuit*, $V_{AVDD} = V_{DD} = V_{DVDD} = 3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)

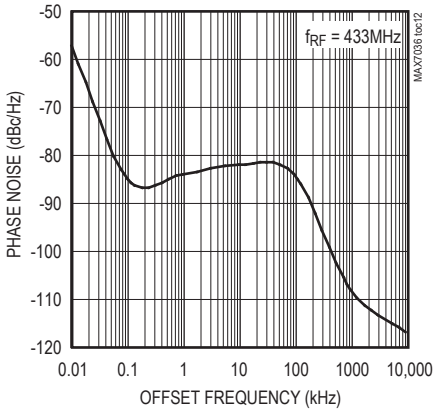
**REGULATOR VOLTAGE vs. REGULATOR CURRENT**




**PHASE NOISE vs. OFFSET FREQUENCY**




**PHASE NOISE vs. OFFSET FREQUENCY**



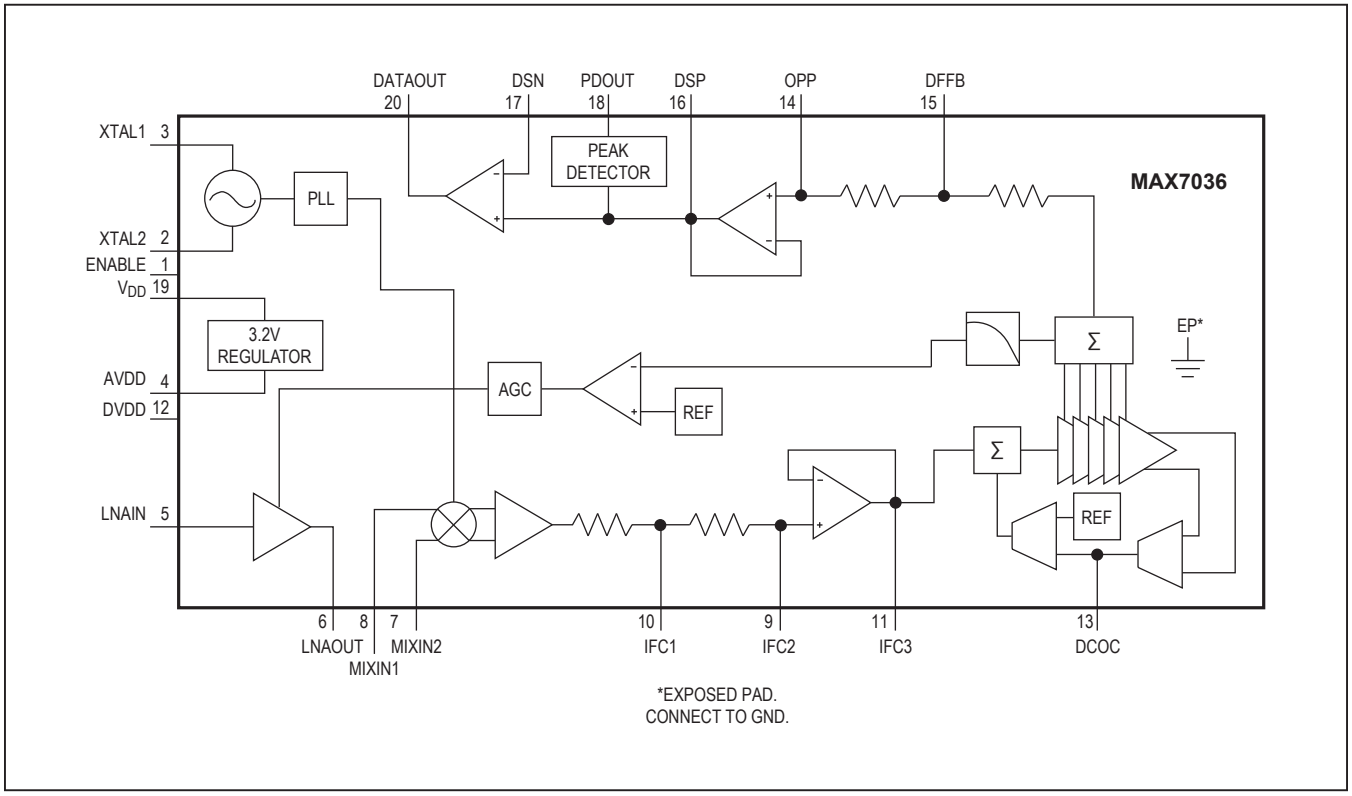

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | ENABLE | Enable Input. Internally pulled down to ground. Set $V_{ENABLE} = V_{DD}$ for normal operation. |
| 2 | XTAL2 | Crystal Input 2. Connect an external crystal from XTAL2 to XTAL1. Bypass to GND if XTAL1 is driven from an AC-coupled external reference (see the *Crystal Oscillator* section). |
| 3 | XTAL1 | Crystal Input 1. Connect an external crystal from XTAL2 to XTAL1. Can also be driven with an AC-coupled external reference oscillator (see the *Crystal Oscillator* section). |
| 4 | AVDD | Positive Analog Supply Voltage. Connect to DVDD. Bypass to GND with a 0.1µF capacitor as close as possible to the device (see the *Typical Application Circuit*). For 5.0V operation, AVDD is internally connected to an on-chip 3.2V LDO regulator. For 3.3V operation, connect AVDD to $V_{DD}$. |
| 5 | LNAIN | Low-Noise Amplifier Input. Must be AC-coupled (see the *Low-Noise Amplifier* section). |
| 6 | LNAOUT | Low-Noise Amplifier Output. Must be connected to AVDD through a parallel LC tank circuit. AC-couple to MIXIN2 (see the *Low-Noise Amplifier* section). |
| 7 | MIXIN2 | 2nd Differential Mixer Input. Connect to the LNAOUT side of the LC tank filter through a 100pF capacitor (see the *Typical Application Circuit*). |
| 8 | MIXIN1 | 1st Differential Mixer Input. Connect to the AVDD side of the LC tank filter through a 100pF capacitor (see the *Typical Application Circuit*). |
| 9 | IFC2 | IF Filter Capacitor Connection 2. This is for the Sallen-Key IF filter. Connect a capacitor from IFC2 to GND. The value of the capacitor is determined by the IF filter bandwidth (see the *Typical Application Circuit*). |
| 10 | IFC1 | IF Filter Capacitor Connection 1. This is for the Sallen-Key IF filter. Connect a capacitor from IFC1 to IFC3. The value of the capacitor is determined by the IF filter bandwidth (see the *Typical Application Circuit*). |
| 11 | IFC3 | IF Filter Capacitor Connection 3. This is for the Sallen-Key IF filter. Connect a capacitor from IFC3 to IFC1. The value of the capacitor is determined by the IF filter bandwidth (see the *Typical Application Circuit*). |
| 12 | DVDD | Positive Digital Supply Voltage Input. Connect to AVDD. Bypass to GND with a 0.01µF capacitor as close as possible to the device (see the *Typical Application Circuit*). |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 13 | DCOC | DC Offset Capacitor Connection. This is for the RSSI amplifier. Connect a 1µF capacitor from this pin to ground (see the *Typical Application Circuit*). |
| 14 | OPP | Noninverting Op-Amp Input. This is for the Sallen-Key data filter. Connect a capacitor from this pin to GND. The value of the capacitor is determined by the data-filter bandwidth. |
| 15 | DFFB | Data-Filter Feedback Input. Input for the feedback of the Sallen-Key data filter. Connect a capacitor from this pin to DSP. The value of the capacitor is determined by the data-filter bandwidth. |
| 16 | DSP | Positive Data-Slicer Input. Connect a capacitor from this pin to DFFB. The value of the capacitor is determined by the data-filter bandwidth. |
| 17 | DSN | Negative Data-Slicer Input |
| 18 | PDOUT | Peak-Detector Output |
| 19 | $V_{DD}$ | Power-Supply Voltage Input. For 5.0V operation, $V_{DD}$ is the input to an on-chip voltage regulator whose 3.2V output drives AVDD. Bypass to ground with a 0.1µF capacitor as close as possible to the device (see the *Typical Application Circuit*). |
| 20 | DATAOUT | Digital Baseband Data Output |
| — | EP | Exposed Pad. Internally connected to ground. Connect to a large ground plane using multiple vias to maximize thermal and electrical performance. |

## Functional Diagram



## Detailed Description

The MAX7036 CMOS RF receiver, and a few external components, provide the complete receiver chain from the antenna to the digital output data. Depending on signal power and component selection, data rates as high as 33kbps Manchester (66kbps NRZ) can be achieved.

The MAX7036 is designed to receive binary ASK/OOK data modulated in the 300MHz to 450MHz frequency range. ASK modulation uses a difference in amplitude of the carrier to represent digital data.

### Voltage Regulator

For operation with a single 3.0V to 3.6V supply voltage, connect AVDD, DVDD, and $V_{DD}$ to the supply voltage. For operation with a single 4.5V to 5.5V supply voltage, connect $V_{DD}$ to the supply voltage. An on-chip voltage regulator drives the AVDD pin to approximately 3.2V. For proper operation, connect DVDD and AVDD together. Bypass $V_{DD}$ and AVDD to GND with 0.1µF capacitors placed as close as possible to the device. Bypass DVDD to GND with a 0.01µF capacitor (see the *Typical Application Circuit*).

### Low-Noise Amplifier

The LNA is an nMOS cascode amplifier. The LNA and mixer have a combined 55dB voltage gain. The gain and noise figures are dependent on both the antenna-matching network at the LNA input and the LC tank network between the LNA output and the mixer inputs.

L2 and C1 comprise the LC tank filter connected to LNAOUT (see the *Typical Application Circuit*). L2 also serves as a bias inductor to LNAOUT. Bypass the power-supply side of L2 to GND with a capacitor that provides a low-impedance path at the RF carrier frequency (e.g., 220pF). Select L2 and C1 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where $L_{TOTAL}$ = L2 + $L_{PARASITICS}$ and $C_{TOTAL}$ = C1 + $C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, LNA output impedance, etc. At high frequencies, these parasitics can have a dramatic effect on the tank filter center frequency and must not be ignored. The total parasitic capacitance is generally 4pF to 6pF. Adjust L2 and C1 accordingly to achieve the desired tank center frequency.

### Automatic Gain Control (AGC)

The AGC circuit monitors the RSSI output. The AGC switches to its low-gain state when the RSSI output reaches 2.2V. The AGC gain reduction is typically 29dB, corresponding to an RSSI voltage drop of 435mV. The LNA resumes high-gain mode when the RSSI level drops back below 1.67V for 13ms for 315MHz and 10ms for 433MHz operation. The AGC has a hysteresis of 5dB. With this AGC function, the MAX7036 can reliably produce an ASK output for RF input levels up to 0dBm, with modulation depth of 30dB.

### Mixer

The mixer cell is a double-balanced mixer that performs a downconversion of the RF input to a typical IF of 200kHz from either a high-side or a low-side injected LO. The mixer output drives the input of the on-chip IF filter.

### Phase-Locked Loop (PLL)

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, asynchronous clock dividers, and crystal-oscillator driver. Besides the crystal, this PLL does not require any external components. The VCO generates the LO. The relationship between the RF, IF, and crystal reference frequencies is given by:

$$f_{XTAL} = \frac{f_{LO}}{32}$$

where $f_{LO} = f_{RF} \pm f_{IF}$

### Received-Signal-Strength Indicator (RSSI)

The RSSI circuit provides a DC output proportional to the logarithm of the input power level. RSSI output voltage has a slope of about 14.5mV/dB (of input power). The RSSI monotonic dynamic range exceeds 80dB. This includes the 30dB of AGC.

## Applications Information

### Crystal Oscillator

The crystal (XTAL) oscillator in the MAX7036 is designed to present a capacitance of approximately 4pF between XTAL1 and XTAL2. In most cases, this corresponds to a 6pF load capacitance applied to the external crystal when typical PCB parasitics are added. The MAX7036 is designed to operate with a typical 10pF load capacitance crystal. **It is very important to use a crystal with a load capacitance equal to the capacitance of the MAX7036 crystal oscillator plus PCB parasitics.** If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating

frequency, introducing an error in the reference frequency. A crystal designed to operate at a higher load capacitance than the value specified for the oscillator is always pulled higher in frequency. Adding capacitance to increase the load capacitance on the crystal increases the start-up time and may prevent oscillation altogether.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right)\times 10^6$$

where:

$f_p$ is the amount the crystal frequency is pulled in ppm.

$C_M$ is the motional capacitance of the crystal.

$C_{CASE}$ is the case capacitance.

$C_{SPEC}$ is the specified load capacitance.

$C_{LOAD}$ is the actual load capacitance.

When the crystal is loaded, as specified (i.e., $C_{LOAD}$ = $C_{SPEC}$), the frequency pulling equals zero.

It is possible to use an external reference oscillator in place of a crystal to drive the VCO. AC-couple the external oscillator to XTAL1 with a 1000pF capacitor. Drive XTAL1 with a signal level of approximately -10dBm. AC-couple XTAL2 to ground with a 1000pF capacitor.

## IF Filter

The IF filter is a 2nd-order Butterworth lowpass filter preceded by a low-frequency DC block. The lowpass filter is implemented as a Sallen-Key filter using an internal op amp and two on-chip 22kΩ resistors. The pole locations are set by the combination of the on-chip resistors and two external capacitors (C9 and C10, Figure 1). The values of these two capacitors for a 3dB cutoff frequency of 400kHz are given below:

$$C9 = \frac{1}{(1.414)(R)(\pi)(f_c)} = \frac{1}{(1.414)(22k\Omega)(3.14)(400kHz)} = 26pF$$

$$C10 = \frac{1}{(2.828)(R)(\pi)(f_c)} = \frac{1}{(2.828)(22k\Omega)(3.14)(400kHz)} = 13pF$$

Because the stray shunt capacitance at each of the pins (IFC1 and IFC2) on a typical PCB is approximately 2pF, choose the value of the external capacitors to be approximately 2pF lower than the desired total capacitance. Therefore, the practical values for C9 and C10 are 22pF and 10pF, respectively.

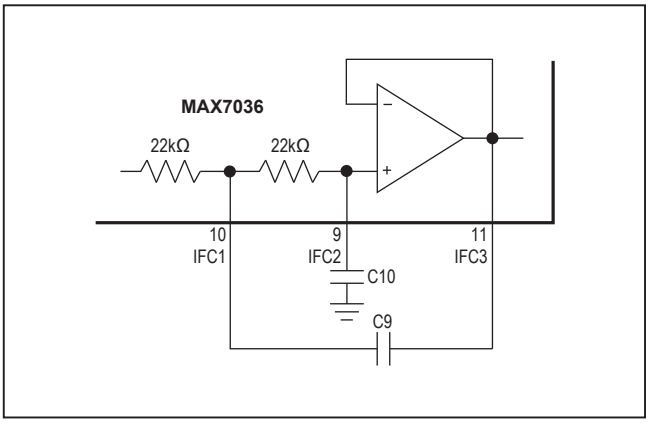



*Figure 1. Sallen-Key Lowpass IF Filter*

## Data Filter

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. Set the corner frequency to approximately 1.5 times the fastest Manchester expected data rate from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 2 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works with the coefficients in Table 1.

$$C5 = \frac{b}{a(100k)(\pi)(f_c)}$$

$$C6 = \frac{a}{4(100k)(\pi)(f_c)}$$

where $f_C$ is the desired corner frequency.

For example, to choose a Butterworth filter response with a corner frequency of 6kHz:

$$C5 = \frac{1.000}{(1.414)(100k\Omega)(3.14)(6kHz)} = 375pF$$

$$C6 = \frac{1.414}{(4)(100k\Omega)(3.14)(6kHz)} = 186pF$$

Choosing standard capacitor values changes C5 to 390pF and C6 to 180pF, as shown in the *Typical Application Circuit*.

## Table 1. Coefficients to Calculate C5 and C6

| FILTER TYPE | a | b |
|---|---|---|
| Butterworth (Q = 0.707) | 1.414 | 1.000 |
| Bessel (Q = 0.577) | 1.3617 | 0.618 |

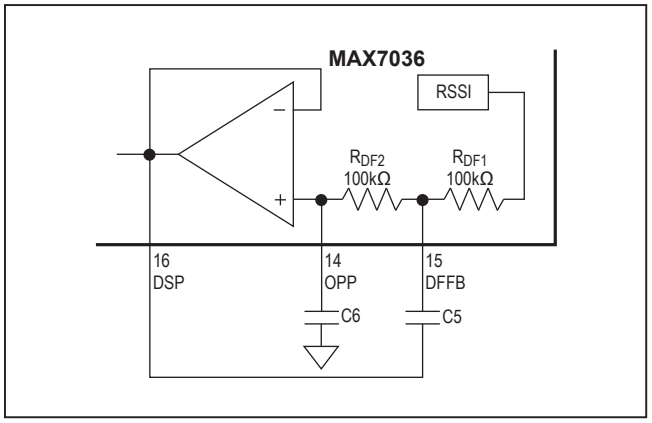



*Figure 2. Sallen-Key Lowpass Data Filter*

### Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. One input is supplied by the data-filter output. Both comparator inputs are accessible off chip to allow for different methods of generating the slicing threshold, which is applied to the second comparator input.

The suggested data-slicer configuration uses a resistor (R1) connected between DSN and DSP with a capacitor (C4) from DSN to GND (Figure 3). This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R1 and C4 affect how fast the threshold tracks to the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

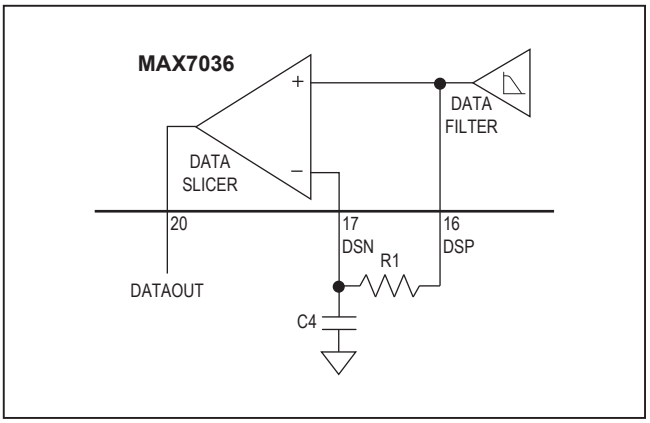



*Figure 3. Generating Data-Slicer Threshold*

Note that a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme (e.g., Manchester coding, which has an equal number of zeros and ones) is used.

### Peak Detector

The peak-detector output (PDOUT), in conjunction with an external RC filter, creates a DC output voltage equal to the peak value of the data signal. The resistor provides a path for the capacitor to discharge, allowing the peak detector to dynamically follow peak changes of the data-filter output voltage. The peak detector can be used for at least two functions. First, it can serve as an RSSI for ASK modulation. Second, it can be used for faster data-slicer response by adding it to the threshold pin (DSN) on the data-slicer comparator (Figure 4). The two capacitors in this circuit should be equal, and the peak detector resistor should be approximately 10 times larger than the resistor

in the RC smoothing circuit between DSP and DSN. This circuit will provide an instantaneous jump of one-half of the DSP increase from “no signal” voltage to peak voltage, which then decays with the same time constant as that of the threshold build-up from the RC smoothing circuit. The DC slicing voltage at DSN is slightly higher (by the ratio of the two resistors in the circuit) than it would be without the speed-up circuit. **Always provide a capacitive path from the PDOUT pin to ground when using the peak-detector output.**

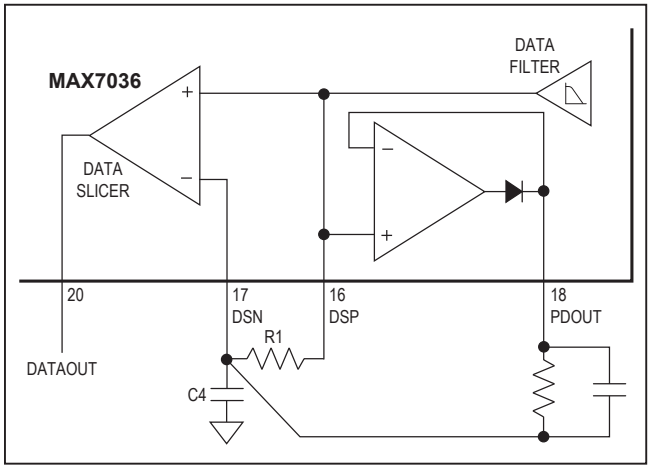



*Figure 4. Using PDOUT for Faster Startup*

## Layout Considerations

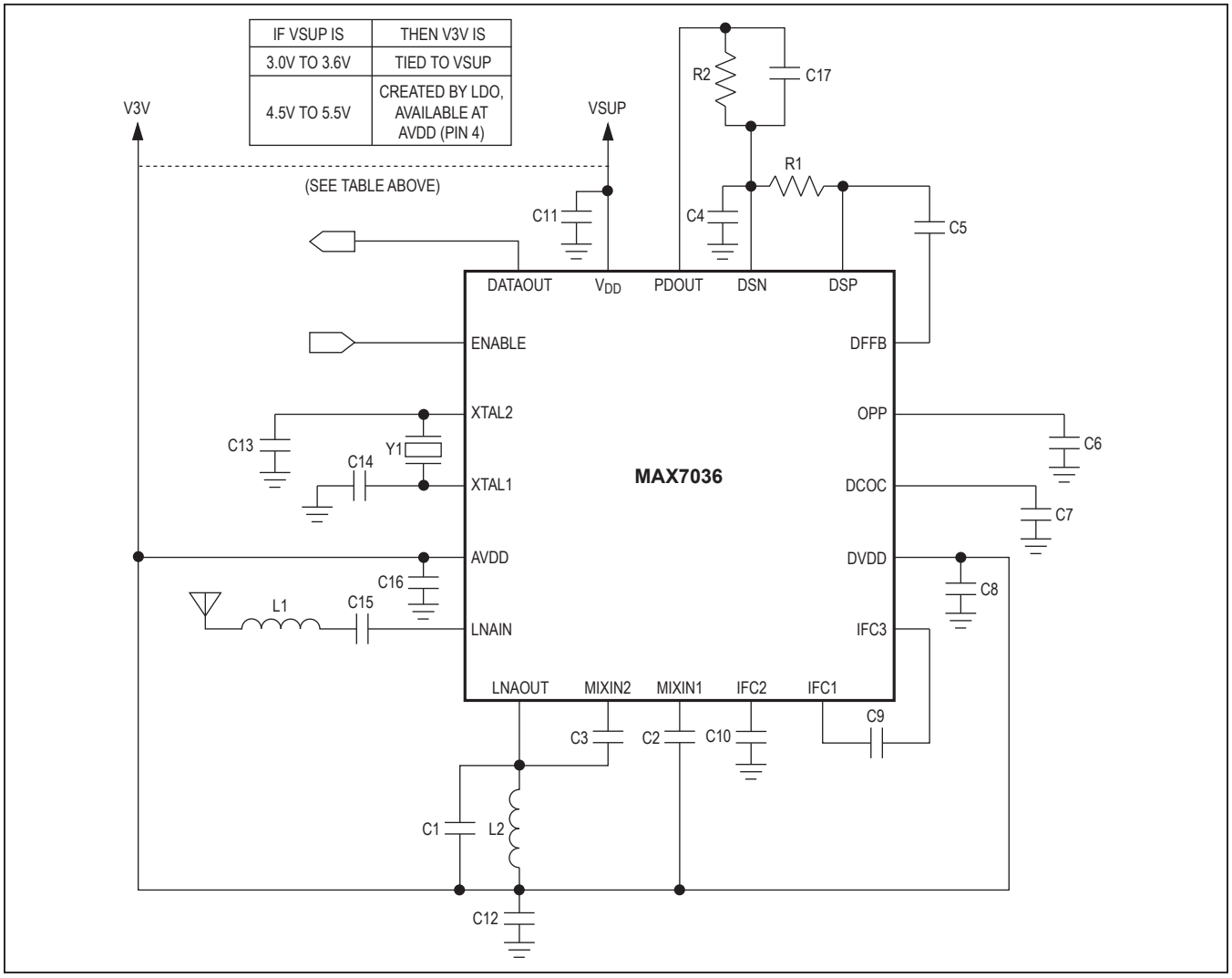
A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are λ/10 or longer act as antennas. Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all power-supply connections.

## Table 2. Component Values

| COMPONENT | $f_{RF}$ = 315MHz | $f_{RF}$ = 433.92MHz |
|---|---|---|
| C1 | 4.7pF | 2.7pF |
| C2 | 100pF | 100pF |
| C3 | 100pF | 100pF |
| C4 | 0.1µF | 0.1µF |
| C5 | 390pF | 390pF |
| C6 | 180pF | 180pF |
| C7 | 1µF | 1µF |
| C8 | 0.01µF | 0.01µF |
| C9 | 22pF | 22pF |
| C10 | 10pF | 10pF |
| C11 | 0.1µF | 0.1µF |
| C12 | 220pF | 220pF |
| C13 | 10pF | 10pF |
| C14 | 10pF | 10pF |
| C15 | 100pF | 100pF |
| C16 | 0.1µF | 0.1µF |
| L1 | 100nH | 47nH |
| L2 | 27nH | 15nH |
| R1 | 22kΩ | 22kΩ |
| Y1 | 9.8375MHz | 13.55375MHz |

## Typical Application Circuit




## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX7036GTP/V+ | -40°C to +105°C | 20 Thin QFN-EP* |
| MAX7036GTP+ | -40°C to +105°C | 20 Thin QFN-EP* |

*/V denotes an automotive qualified part.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 20 Thin QFN-EP | T2055+3 | 21-0140 | 90-0008 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 3/09 | Initial release | — |
| 1 | 8/10 | Updated *Absolute Maximum Ratings*, TOCs 5, 11, and 12, *Pin Description*, *Phase-Locked Loop (PLL)* and *Crystal Oscillator* sections, and *Typical Application Circuit* | 2, 5, 6, 8, 9, 12 |
| 2 | 8/17 | Added AEC-Q100 qualification statement to *Benefits and Features* section | 1 |
| 3 | 1/18 | Updated *Ordering Information* table | 12 |
| 4 | 8/21 | Updated link in *Package Description* section | 12 |

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