MAX7320 I²C Port Expander with Eight Push-Pull Outputs

General Description

The MAX7320 2-wire serial-interfaced peripheral features eight push-pull outputs with selectable power-up logic states.

The +5.5V tolerant $\overline{RST}$ input clears the serial interface, terminating any I²C communication to or from the MAX7320.

The MAX7320 uses two address inputs with four-level logic to allow 16 I²C slave addresses. The slave address also determines the power-up state level for the outputs in groups of four ports.

The MAX7320 supports hot insertion. The serial interface SDA, SCL, AD0, AD2, and $\overline{RST}$ remain high impedance in power-down (V+ = 0V) with up to +6V asserted on them.

The MAX7320 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7320 is available in 16-pin QSOP and 16-pin TQFN packages, and is specified over the automotive temperature range (-40°C to +125°C).

Applications

- Cell Phones/PDAs
- Satellite Radios
- Notebooks
- RAID
- Servers

Benefits and Features

- 400kHz, +5.5V-Tolerant I²C Serial Interface
- +1.71V to +5.5V Operating Voltage
- Eight Push-Pull Output Ports with Selectable Power-Up Logic States
- $\overline{RST}$ Clears the Serial Interface, Terminating Any Serial Transaction to or from the MAX7320
- AD0 and AD2 Inputs Select from 16 Slave Addresses
- Low 0.6µA (typ) Standby Current
- -40°C to +125°C Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX7320AEE+	-40°C to +125°C	16 QSOP	—
MAX7320ATE+	-40°C to +125°C	16 TQFN 3mm x 3mm x 0.8mm	ADB

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configurations, Typical Application Circuit, and Functional Diagram appear at end of data sheet.

Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7319	8	Yes	—	—
MAX7320	—	—	—	8
MAX7321	Up to 8	—	Up to 8	—
MAX7322	4	Yes	—	4
MAX7323	Up to 4	—	Up to 4	4
MAX7328*	Up to 8	—	Up to 8	—
MAX7329**		—		—

**Second source to PCF8574.*
***Second source to PCF8574A.*

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
Supply Voltage V+.....-0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{RST}$.....-0.3V to +6V
O0–07.....0.3V to (V+ + 0.3V)
00–07 Output Current .....±25mA
SDA Input Current..... 10mA
Total V+ Current.....50mA
Total GND Current 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C over +70°C).....667mW
16-Pin Thin QFN (derate 15.6mW/°C over +70°C)....1250mW
Operating Temperature Range.....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		1.71		5.50	V
Power-On Reset Voltage	V_{POR}				1.6	V
Standby Current Voltage (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+		0.6	1.5	µA
Supply Current (Interface Running)	I+	f_{SCL} = 400kHz; other digital inputs at V+		23	55	µA
Input High-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$	V_{IH}	V+ < 1.8V	0.8 x V+			V
		V+ ≥ 1.8V	0.7 x V+			
Input Low-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$	V_{IL}	V+ < 1.8V			0.2 x V+	V
		V+ ≥ 1.8V			0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{RST}$	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, $\overline{RST}$, O0–O7 at V+ or GND	-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{RST}$				10		pF
Output Low Voltage O0–O7	V_{OL}	V+ = +1.71V, I_{SINK} = 1mA		120	240	mV
		V+ = +2.5V, I_{SINK} = 2mA		140	280	
		V+ = +3.3V, I_{SINK} = 3mA		170	310	
		V+ = +5V, I_{SINK} = 5mA		220	380	
Output High Voltage O0–O7	V_{OH}	V+ = +1.71V, I_{SOURCE} = 1mA	V+ - 250	V+ - 130		mV
		V+ = +2.5V, I_{SOURCE} = 2mA	V+ - 350	V+ - 200		
		V+ = +3.3V, I_{SOURCE} = 3mA	V+ - 290	V+ - 150		
		V+ = +5V, I_{SOURCE} = 5mA	V+ - 380	V+ - 230		
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			250	mV

Port And Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	C_L ≤ 100pF			4	µs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

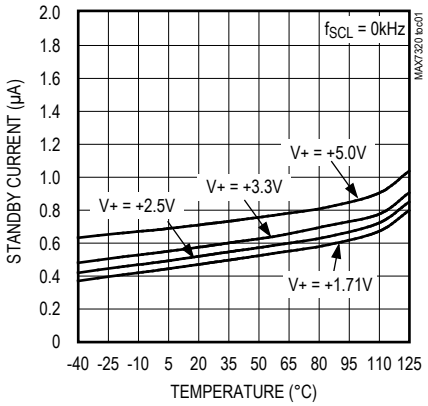
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 3)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Low to Data Out Valid	$t_{VD, DAT}$	SCL low to SDA output valid			3.4	µs
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		$20 + 0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		$20 + 0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Notes 2, 4)		$20 + 0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 2)			400	pF
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	$t_{\overline{RST}}$		1			µs

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V+ and 0.7 x V+, I_{SINK} ≤ 6mA.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

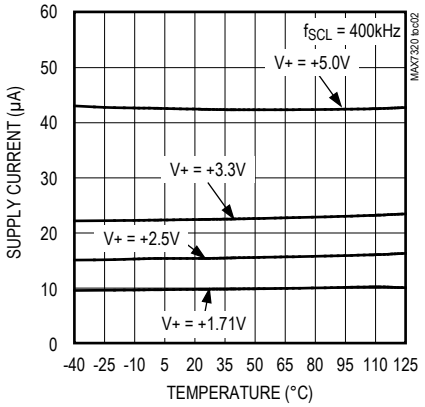
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

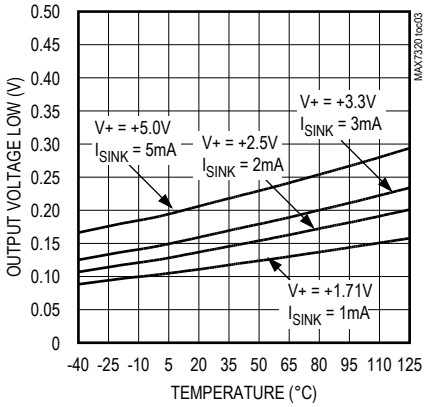
STANDBY CURRENT vs. TEMPERATURE



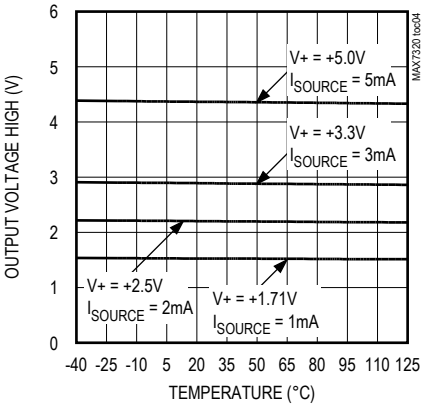
SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE LOW vs. TEMPERATURE



OUTPUT VOLTAGE HIGH vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1, 3	15, 1	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V+, SCL, or SDA to give four logic combinations (see Table 3).
2	16	$\overline{RST}$	Reset Input, Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.
4–7, 9–12	2–5, 7–10	O0–O7	Output Ports. O0 to O7 are push-pull outputs.
8	6	GND	Ground
13	11	N.C.	No Connection. Not internally connected.
14	12	SCL	I²C-Compatible Serial Clock Input
15	13	SDA	I²C-Compatible Serial Data I/O
16	14	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are second sources to the PCF8574 and PCF8574A.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7320 is a general-purpose port expander operating from a +1.71V to +5.5V supply that provides eight push-pull output ports. The MAX7320 is rated to sink a total of 100mA and source a total of 50mA from all eight combined outputs.

The MAX7320 is set to one of 16 I²C slave addresses (0x50 to 0x5F) using address select inputs AD0 and AD2, and is accessed over an I²C serial interface up to 400kHz. Note the MAX7320 offers a different range of I²C slave addresses than the MAX7319, MAX7321, MAX7322, and MAX7323 (these expanders use the address range 0x60 to 0x6F).

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: Eight input ports with programmable latching transition detection interrupt and selectable pullups. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	Output-only versions: Eight push-pull outputs with selectable power-up default states. Push-pull outputs offer faster rise time than open-drain outputs, and require no pullup resistors.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: Eight open-drain I/O ports with latching transition detection interrupt and selectable pullups. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	Four input-only, four output-only versions: Four input ports with programmable latching transition detection interrupt and selectable pullups. Four push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	Four I/O, four output-only versions: Four open-drain I/O ports with latching transition detection interrupt and selectable pullups. Four push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	PCF8574-, PCF8574A-compatible versions: Eight open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports. All ports power up as inputs (or logic-high outputs). Any port can be used as an input by setting the open-drain output to logic-high.
16-PORT EXPANDERS						
MAX7324	101xxxx and 110xxxx	8	Yes	—	8	Software equivalent to a MAX7320 plus a MAX7321.
MAX7325		Up to 8	—	Up to 8	8	Software equivalent to a MAX7320 plus a MAX7319.
MAX7326		4	Yes	—	12	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	Software equivalent to a MAX7320 plus a MAX7323.

Table 2. Read and Write Access to Eight-Port Expander Family

PART	I²C SLAVE ADDRESS	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I²C DATA WRITE	I²C DATA READ
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7-O0 port inputs>
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 port inputs> <0, 0, I5–I2 transition flags, 0, 0>
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 port inputs> <0, 0, P5-P2 transition flags, 0, 0>
MAX7328	0100xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>
MAX7329	0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>

Table 3. MAX7320 Address Map

PIN CONNECTION		DEVICE ADDRESS							OUTPUTS POWER-UP DEFAULT							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O7**	**O6**	**O5**	**O4**	**O3**	**O2**	**O1**	**O0**
SCL	GND	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0
SCL	V+	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1
SCL	SCL	1	0	1	0	0	1	0	1	1	1	1	1	1	1	1
SCL	SDA	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
SDA	GND	1	0	1	0	1	0	0	1	1	1	1	0	0	0	0
SDA	V+	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1
SDA	SCL	1	0	1	0	1	1	0	1	1	1	1	1	1	1	1
SDA	SDA	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
GND	**GND**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
GND	**V+**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
GND	SCL	1	0	1	1	0	1	0	0	0	0	0	1	1	1	1
GND	SDA	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1
V+	**GND**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
V+	**V+**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
V+	SCL	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1
V+	SDA	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

The $\overline{RST}$ input clears the serial interface in case of a hung bus, terminating any serial transaction to or from the MAX7320.

When the MAX7320 is read through the serial interface, the actual logic states at the ports are read back.

Output port power-up logic states are selected by the address select inputs AD0 and AD2. Ports default to logic-high or logic-low on power-up in groups of four (see Table 3).

$\overline{RST}$ Input

The $\overline{RST}$ input voids any I²C transaction involving the MAX7320 and forces the MAX7320 into the I²C STOP condition. A reset does not change the contents of the output register. $\overline{RST}$ is overvoltage tolerant to +5.5V.

Standby Mode

When the serial interface is idle, the MAX7320 automatically enters standby mode, drawing minimal supply current.

Slave Address and Power-Up Default Logic States

Address inputs AD0 and AD2 determine the MAX7320 slave address and set the power-up output logic states. Power-up logic states are set in groups of four (see Table 3). The MAX7320 uses a different range of slave addresses (101xxxx) than the MAX7319, MAX7321, MAX7322, and MAX7323 (110xxxx).

The MAX7320 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7320. The MAX7320 distinguishes whether address inputs AD0 and AD2 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7320 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7320 cannot decode the address inputs AD0 and AD2 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection determines the power-up logic levels of the output ports. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7320. This is guaranteed as part of the I²C specification. Therefore, address inputs AD0 and AD2 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The power-up output state selection logic uses AD0 to select the power-up state for ports O3–O0, and uses AD2 to select the power-up state for ports O7–O4. The rule is that a logic-high, SDA, or SCL connection selects a logic-high power-up state, and a

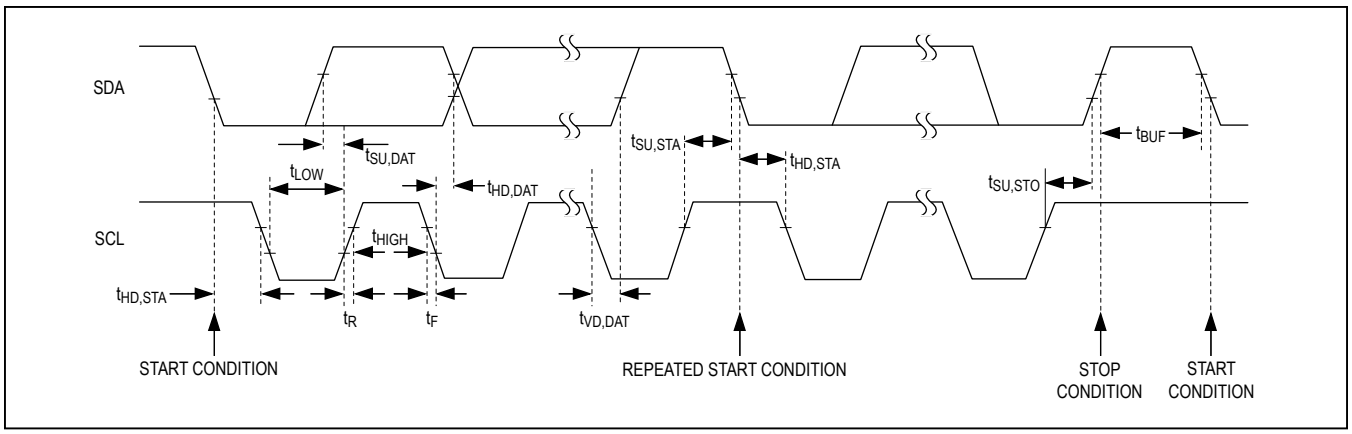


Figure 1. 2-Wire Serial-Interface Timing Details

logic-low selects a logic-low power-up state for each set of four ports (see Table 3). The output power-up logic level configuration is correct for a standard I²C configuration, where SDA or SCL appear to be connected to V+ by the external I²C pullups.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true; for example, in true hot-swap applications in which there is legitimate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7320's supply, and if that pullup supply rises later than the MAX7320's, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD0 and AD2 to GND or V+ (shown in **bold** in Table 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, be aware that unexpected port power-up default states may occur until the first I²C transmission (to any device, not necessarily the MAX7320).

Port Outputs

Write one byte to the MAX7320 to set all output port states simultaneously.

Serial Interface

Serial-Addressing

The MAX7320 operates as a slave that sends and receives data through an I²C interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master initiates all data transfers to and from the MAX7320, and generates the SCL clock that synchronizes the data transfer (Figure 1).

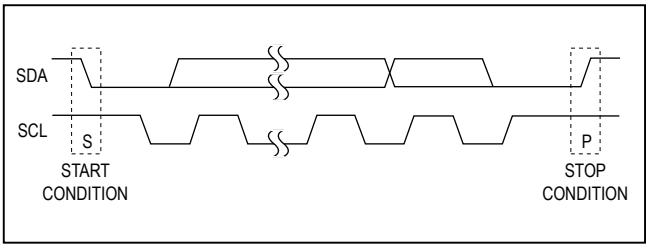


Figure 2. START and STOP Conditions

SDA operates as both an input and an open-drain output. A pullup resistor, 4.7kΩ (typ), is required on SDA. SCL operates only as an input. A pullup resistor, 4.7kΩ (typ), is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7320's 7-bit slave address plus R/$\overline{W}$ bit, one or more data bytes, and finally a STOP condition (Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the ninth clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7320, the device generates the acknowledge bit because the MAX7320 is the recipient. When the MAX7320 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7320 has a 7-bit slave address (Figure 5). The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, and high for a read command.

The 1st (A6), 2nd (A5), and 3rd (A4) bits of the MAX7320 slave address are always 1, 0, and 1. Connect AD0 and AD2 to GND, V+, SDA, or SCL to select the slave address bits A3, A2, A1, and A0. The MAX7320 has 16 possible slave addresses (Table 3), allowing up to 16 MAX7320 devices on an I²C bus.

Note the MAX7320 offers a different range of I²C slave addresses from the MAX7319, MAX7321, MAX7322 and MAX7323, for which 1st (A6), 2nd (A5), and 3rd (A4) bits of the slave address are always 1, 1, and 0.

Accessing the MAX7320

A **single-byte read** from the MAX7320 returns the status of the eight output ports, read back as inputs.

A **2-byte read** repeatedly returns the status of the eight output ports, read back as inputs.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) repeatedly returns the status of the eight output ports, read back as inputs.

A **single-byte write** to the MAX7320 sets the logic state of all eight outputs.

A **multibyte write** to the MAX7320 repeatedly sets the logic state of all eight outputs.

Reading from the MAX7320

A read from the MAX7320 starts with the master transmitting the MAX7320's slave address with the R/$\overline{W}$ bit set high. The MAX7320 acknowledges the slave address, and samples the logic state of the output ports during the acknowledge bit. The master can read one or more bytes from the MAX7320 and then issue a STOP condition (Figure 6). The MAX7320 transmits the current port data, read back from the actual port outputs (not the port output latches) during the acknowledge. If a port is forced to a logic state other than its programmed state, the read back reflects this. If driving a capacitive load, readback port level verification algorithms may need to take the RC rise/fall time into account.

Typically, the master reads one byte from the MAX7320, then issues a STOP condition (Figure 6). However, the master can read 2 or more bytes from the MAX7320, then issue a STOP condition. In this case, the MAX7320 resamples the port outputs during each acknowledge and transmits the new data each time.

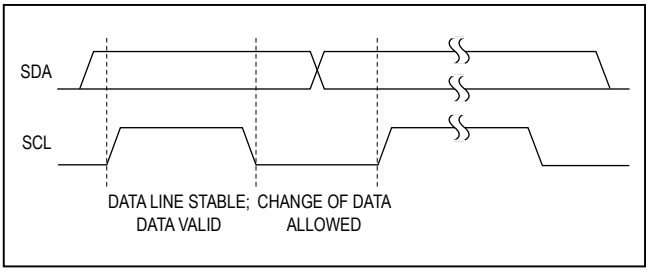


Figure 3. Bit Transfer

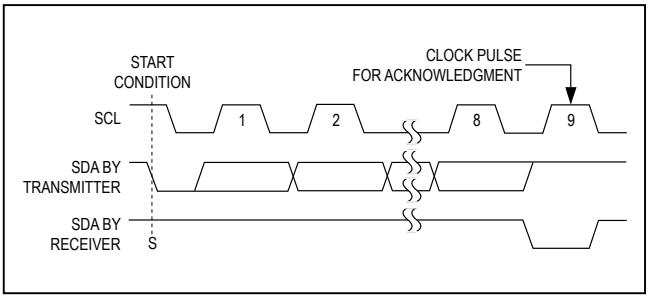


Figure 4. Acknowledge

Writing to the MAX7320

A write to the MAX7320 starts with the master transmitting the MAX7320's slave address with the R/$\overline{W}$ bit set low. The MAX7320 acknowledges the slave address and samples the ports during the acknowledge bit. The master can transmit one or more bytes of data. The MAX7320 acknowledges each subsequent byte of data and updates the output ports until the master issues a STOP condition (Figure 7).

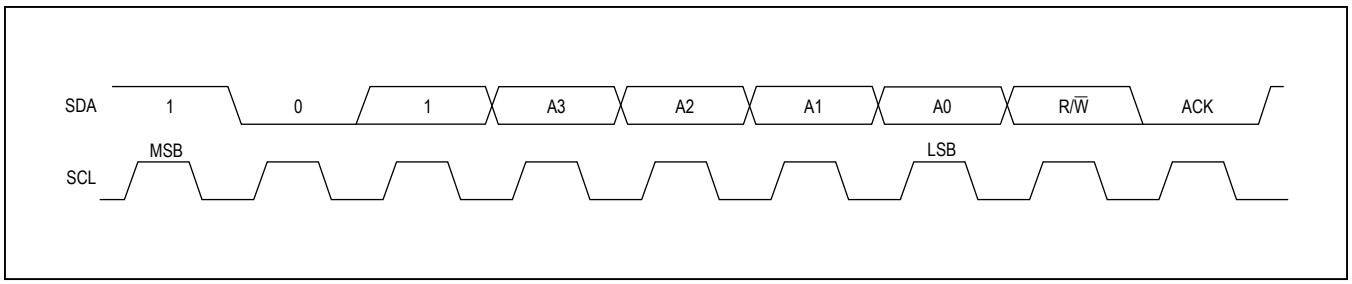


Figure 5. Slave Address

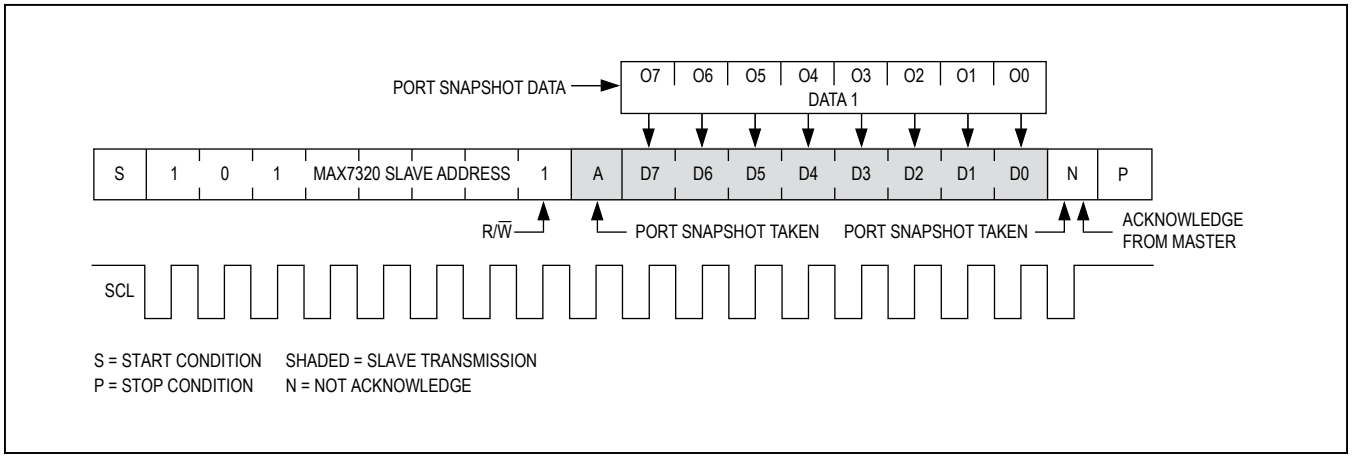


Figure 6. Reading the MAX7320

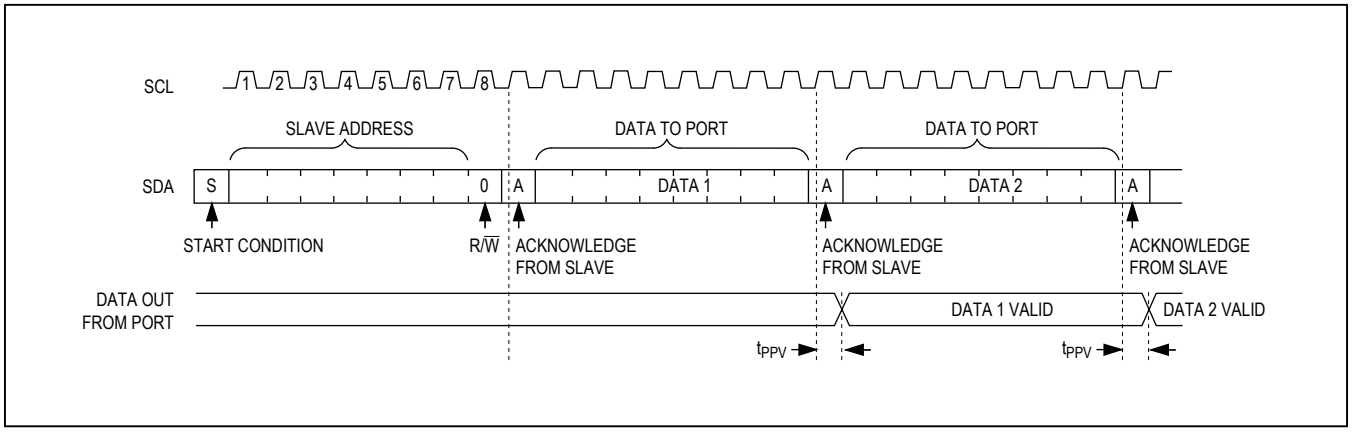
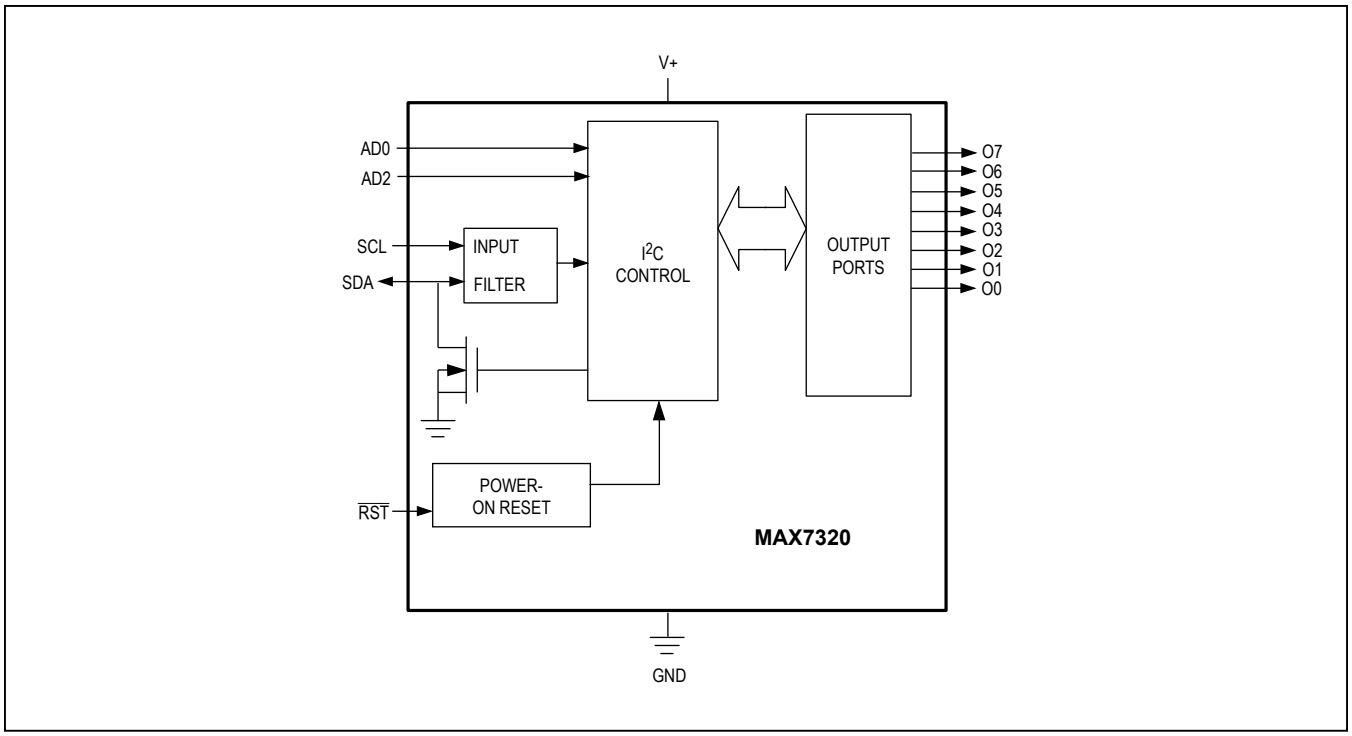


Figure 7. Writing to the MAX7320

Functional Block Diagram



Applications Information

Hot Insertion

SDA, SCL, AD0, AD2, and $\overline{RST}$ are overvoltage protected to +6V independent of V+. This allows the MAX7320 to be operated from a lower supply voltage, such as +3.3V, while the I²C interface is driven from a higher logic level, such as +5V.

Each of the output ports, O0–O7, has a protection diode to V+ and to GND (Figure 8). When a port output is driven to a voltage higher than V+ or lower than GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. When the MAX7320 is powered down (V+ = 0V), each output port appears as a diode connected to GND (Figure 8).

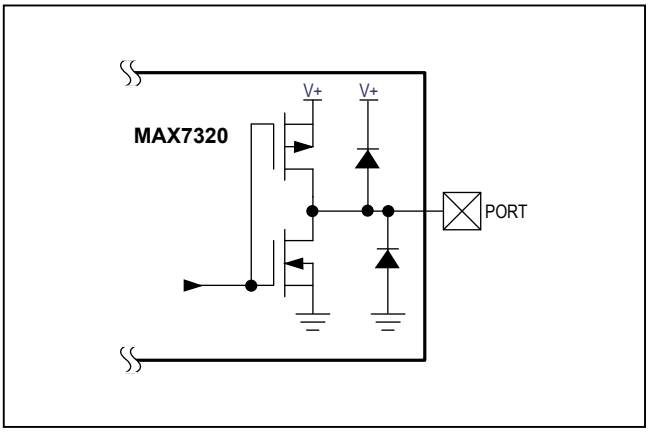


Figure 8. Output Port Structure

Power-Supply Considerations

The MAX7320 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass V+ to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible. For the TQFN version, additionally connect the exposed pad to GND.

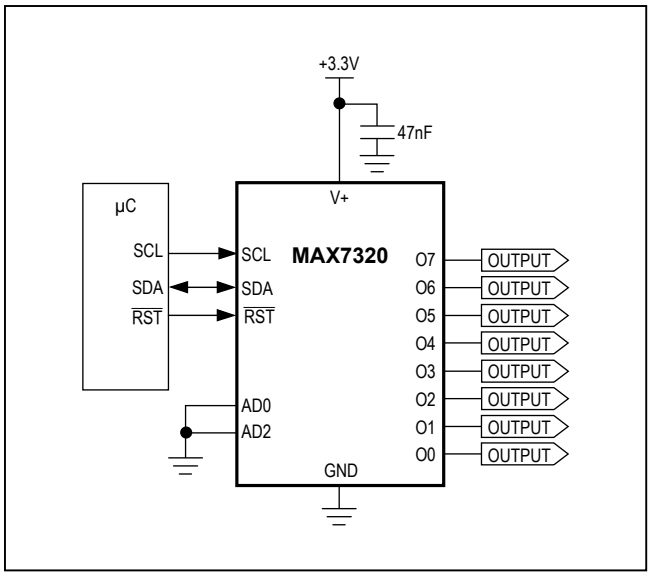
Compatibility with MAX6965, MAX7315, and MAX7316

The MAX7320 is subset pin compatible with the MAX6965, MAX7315, and MAX7316. The pin differences are shown in Table 4. The MAX7320 is not software compatible with MAX6965, MAX7315, or MAX7316. In many cases it is possible to design a PC board to work with all these port expanders, providing design flexibility.

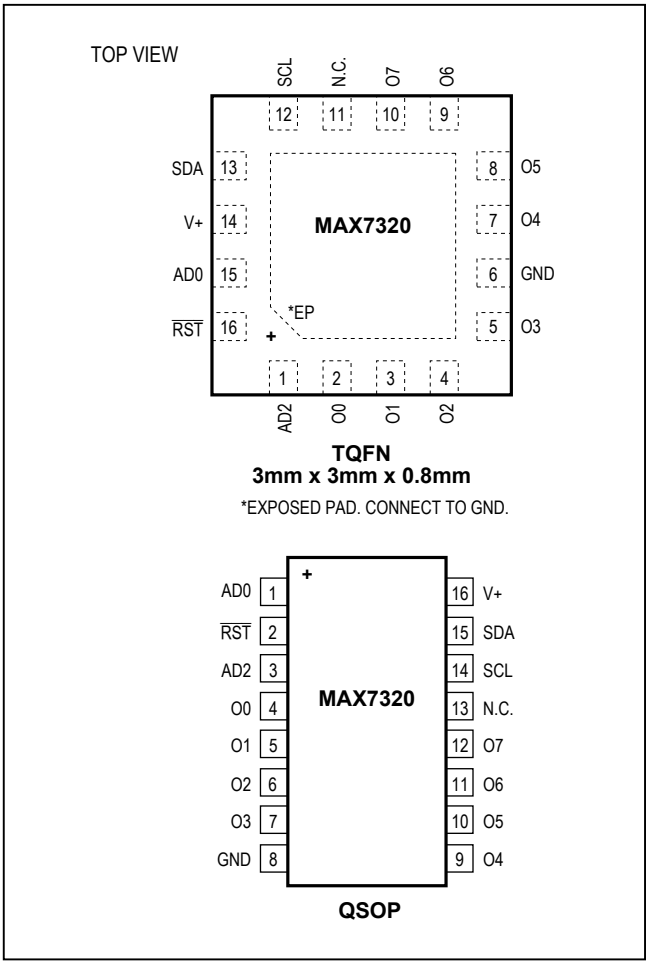
Table 4. MAX7320, MAX6965, MAX7315, and MAX7316 Pin Compatibility

PIN-PACKAGE		PIN FUNCTION		
16 QSOP	16 TQFN	MAX7320	MAX7315	MAX6965 AND MAX7316
1	15	AD0	AD0	BLINK
2	16	$\overline{RST}$	AD1	$\overline{RST}$
3	1	AD2	AD2	AD0

Typical Application Circuit



Pin Configurations



Chip Information

PROCESS: BiCMOS

Connect EP to GND

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167
16 TQFN-EP	T1633+4	21-0136	90-0031

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	—
1	4/15	Removed automotive reference from data sheet	1

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