EVALUATION KIT AVAILABLE

MAX7370

8 x 8 Key-Switch Controller and LED Driver/GPIOs with I²C Interface and High Level of ESD Protection

General Description

The MAX7370 I²C-interfaced peripheral provides microprocessors with management of up to 64 key switches, with optional GPIO and PWM-controlled LED drivers.

The key-switch drivers interface with metallic or resistive switches with on-resistances up to 5kΩ. Key inputs are monitored statically, not dynamically, to ensure low-EMI operation. The IC features autosleep and autowake modes to further minimize the power consumption of the device. The autosleep feature puts the device in a low-power state (1µA typ) after a timeout period. The autowake feature configures the device to return to normal operating mode from sleep upon a keypress.

The key controller debounces and maintains a FIFO buffer of keypress and release events (including auto-repeat, if enabled). An interrupt ($\overline{INT}$) output can be configured to alert keypresses, as they occur, or at the maximum rate.

The same index rows and columns in the device can be used as a direct logic-level translator.

If the device is not used for key-switch control, all keyboard pins can be used as GPIOs. Each GPIO can be programmed to one of the two externally applied logic voltage levels. Four column ports (COL7–COL4) can also be configured as LED drivers that feature constant-current and PWM intensity control. The maximum constant-current level for each open-drain LED port is 20mA. The intensity of the LED on each open-drain port can be individually adjusted through a 256-step PWM control.

The device is offered in a 24-pin (3.5mm x 3.5mm) TQFN package with an exposed pad, and small 25-bump (2.159mm x 2.159mm) wafer-level package (WLP) for cell phones, pocket PCs, and other portable consumer electronic applications.

The device operates over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

Notebooks

PDAs

Handheld Games

Portable Consumer Electronics

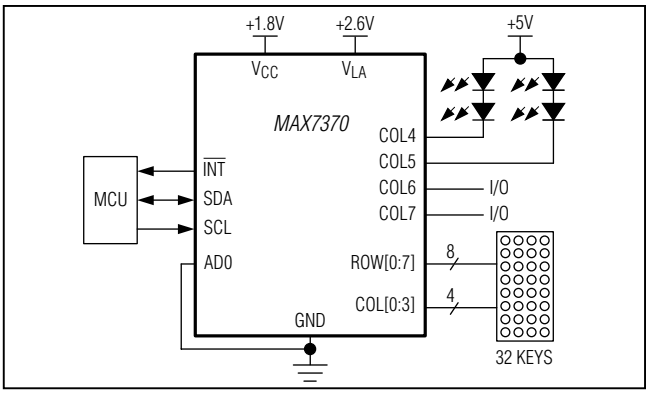
For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX7370.related**.

Features

- **Monitors Up to 64 Keys**
- **Integrated High-ESD Protection**
  - **±8kV IEC 61000-4-2 Contact Discharge**
  - **±15kV IEC 61000-4-2 Air-Gap Discharge**
- **Keyscan Uses Static Matrix Monitoring for Low-EMI Operation**
- **Four LED Driver Pins on COL7–COL4**
- **5V Tolerant, Open-Drain I/O Ports Capable of Constant-Current LED Drive**
- **256-Step PWM Individual LED Intensity-Control Accuracy**
- **Individual LED Blink Rates and Common LED Fade In/Out Rates from 256ms to 4096ms**
- **FIFO Queues Up to 16 Debounced Key Events**
- **User-Configurable Keypress and Release Debounce Time (2ms to 32ms)**
- **Key-Switch Interrupt ($\overline{INT}$) on Each Debounced Event/FIFO Level, or End-of-Definable Time Period**
- **1.62V to 3.6V Operating Supply Voltage**
- **Individually Programmable GPIOs to Two Logic Levels**
- **8-Channel Individual Programmable Level Translators**
- **Provides Optional GPIOs on all ROW_ and COL_ Pins**
- **Supports Hot Insertion**
- **400kbps, 5.5V Tolerant I²C Serial Interface with Selectable Bus Timeout**

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5950; Rev 2; 5/15

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{LA} to GND .....-0.3V to +4V
COL3–COL0, ROW7–ROW0 to GND ..... -0.3V to (V_{CC} + 0.3V)
COL7–COL4 to GND.....-0.3V to +6V
SDA, SCL, AD0, $\overline{INT}$ to GND .....-0.3V to +6V
V_{LA} to V_{CC} .....-0.3V to +2.3V
DC Current on COL7–COL4 to GND 25mA
DC Current on COL3–COL0, ROW7–ROW0 to GND.....7mA
V_{CC}, V_{LA}, GND Current 80mA
DC Current V_{CC}, V_{LA} to COL3–COL0, ROW7–ROW0.....5mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 15.4mW/°C above +70°C) 1229mW
25-Bump WLP (derate 19.2mW/°C above +70°C).....850mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (TQFN) (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

24 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....65.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5.4°C/W

25 WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}		1.62	3.3	3.6	V
Second Logic Supply	V_{LA}		V_{CC}	3.3	3.6	V
Operating Supply Current	I_{CC}	All key switches open, oscillator running		50	65	µA
		N keys pressed		50 + 28 x N		
Sleep-Mode Supply Current	I_{SL}	Not using GPO or LED configuration		1.8	3	µA
POR Threshold	V_{POR}			1.2		V
KEY-SWITCH SPECIFICATIONS						
Key-Switch Source Current	I_{KEY}			28	40	µA
Key-Switch Source Voltage	V_{KEY}			0.45	0.5	V
Key-Switch Resistance	R_{KEY}	(Note 4)			5	kΩ
Startup Time from Sleep	t_{START}			2	2.7	ms
GPIO SPECIFICATIONS						
External Supply Voltage COL7–COL4 (LED Drivers)	V_{LED}				5	V
LED Port-to-Port Sink Current Variation		V_{CC} = 3.3V, V_{OL} = 1V, T_A = +25°C, 10mA output mode		±1.5	±2.4	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
10mA Port Sink Current COL7–COL4	I_{OL}	V_{OL} = 1V	T_A = +25°C	8.6		11.4	mA
			V_{CC} = 3.3V	9.04	10	10.96	
		V_{OL} = 0.5V	V_{CC} = 3.6V, T_A = +25°C		9.5		
20mA Port Sink Current COL7–COL4	I_{OL}	V_{OL} = 1V	T_A = +25°C	18.13		21.52	mA
			V_{CC} = 3.3V	18.47	20	21.34	
		V_{OL} = 0.5V	V_{CC} = 3.6V, T_A = +25°C		19.05		
Input High Voltage COL_, ROW_	V_{IH}	V_S = V_{CC} or V_{LA} depending on reference logic level setting		0.7 x V_S			V
Input Low Voltage COL_, ROW_	V_{IL}					0.3 x V_S	V
Input Leakage Current COL3–COL0, ROW_	$I_{LEAKAGE}$	Input voltage = V_{CC} or V_{GND}		-2		+2	µA
Input Leakage Current COL7–COL4	$I_{LEAKAGE}$	Input voltage = 5V		-1		+1	µA
Input Capacitance COL_, ROW_	C_{IN}				20		pF
Maximum Allowable Load Capacitance for Keyscan Function		N keys pressed simultaneously			500		pF
Output Low Voltage COL_, ROW_	V_{OL}	V_{CC} = 1.62V and I_{SINK} = 2.5mA			50	100	mV
		V_{CC} = 1.62V and I_{SINK} = 5mA			80	250	
Output High Voltage COL3–COL0, ROW_	V_{OH}	V_{CC} = 1.62V and I_{SOURCE} = 2.5mA		V_{CC} - 120	V_{CC} - 40		mV
		V_{CC} = 1.62V and I_{SOURCE} = 5mA		V_{CC} - 250	V_{CC} - 70		
Output Logic-Low Voltage ($\overline{INT}$)	V_{OL}	I_{SINK} = 6mA				0.6	V
PWM Frequency	f_{PWM}	Derived from oscillator clock			500		Hz
SERIAL-INTERFACE SPECIFICATIONS							
Input High Voltage SDA, SCL, AD0	V_{IH}			0.7 x V_{CC}			V
Input Low Voltage SDA, SCL, AD0	V_{IL}					0.3 x V_{CC}	V
Input Leakage Current SDA, SCL, AD0	$I_{LEAKAGE}$	Input voltage = 5.5V or V_{GND}		-1		+1	µA
Output Logic-Low Voltage SDA	V_{OL}	I_{SINK} = 6mA				0.6	V
Input Capacitance SDA, SCL, AD0	C_{IN}	(Notes 4, 5)				10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

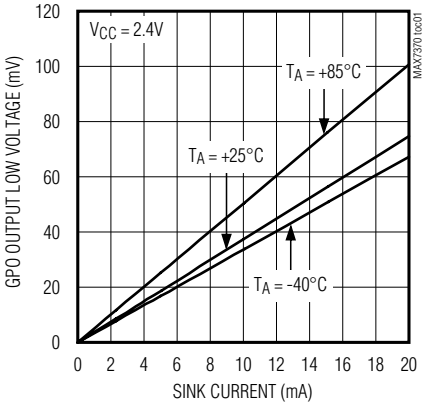
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING SPECIFICATIONS						
SCL Serial-Clock Frequency	f_{SCL}	Bus timeout enabled	0.05		400	kHz
		Bus timeout disabled	0		400	
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 6)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 4, 5)		$20 + 0.1C_B$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 4, 5)		$20 + 0.1C_B$	300	ns
Fall Time of SDA Signal, Transmitting	$t_{F, TX}$	(Notes 4, 7)		$20 + 0.1C_B$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 4, 8)			50	ns
Capacitive Load for Each Bus Line	C_B	(Note 4)			400	pF
Bus Time Out	$t_{TIMEOUT}$		14	19	27	ms
ESD PROTECTION						
ROW7–ROW0, COL7–COL0		IEC 61000-4-2 Air-Gap Discharge		±15		kV
		IEC 61000-4-2 Contact Discharge		±8		
All Other Pins		Human Body Model		±2.5		kV

Note 2: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: All digital inputs at V_{CC} or GND.
Note 4: Guaranteed by design.
Note 5: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 6: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 7: I_{SINK} = 6mA. C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 8: Input filters on the SDA, SCL, and AD0 inputs suppress noise spikes less than 50ns.

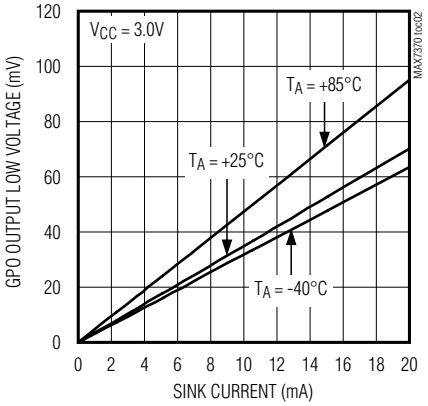
Typical Operating Characteristics

(V_{CC} = 2.5V, V_{LA} = 2.5V, T_A = +25°C, unless otherwise noted.)

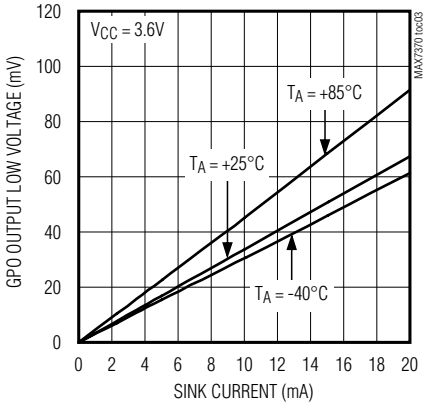
GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (COL7–COL4)



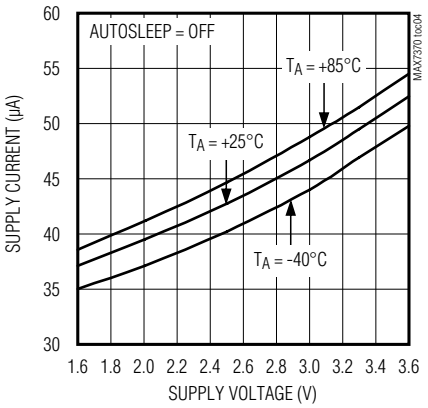
GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (COL7–COL4)



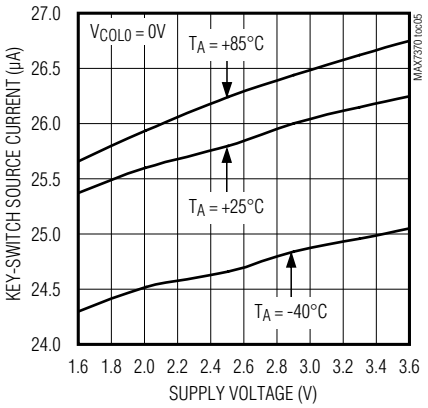
GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (COL7–COL4)



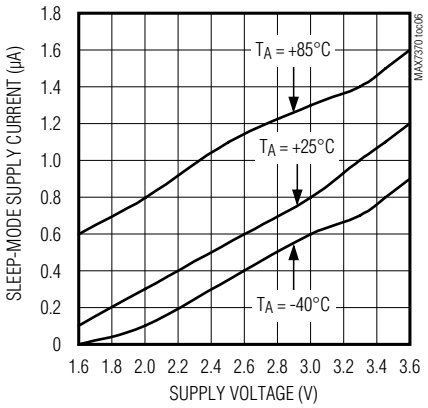
SUPPLY CURRENT vs. SUPPLY VOLTAGE



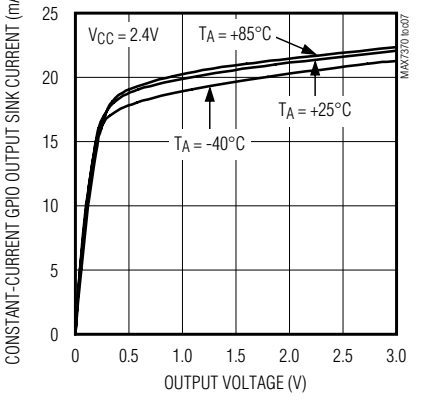
KEY-SWITCH SOURCE CURRENT vs. SUPPLY VOLTAGE



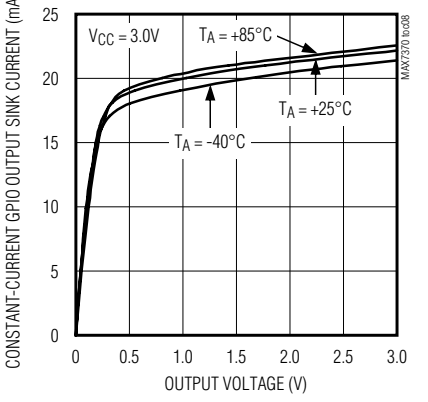
SLEEP-MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



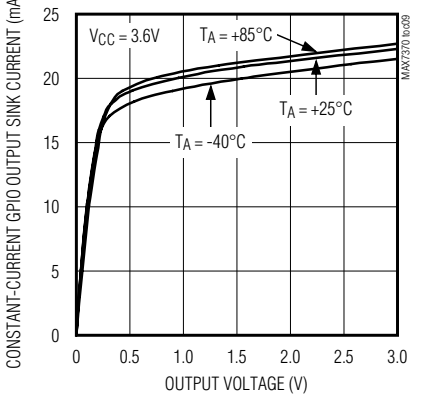
CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (COL7–COL4)



CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (COL7–COL4)

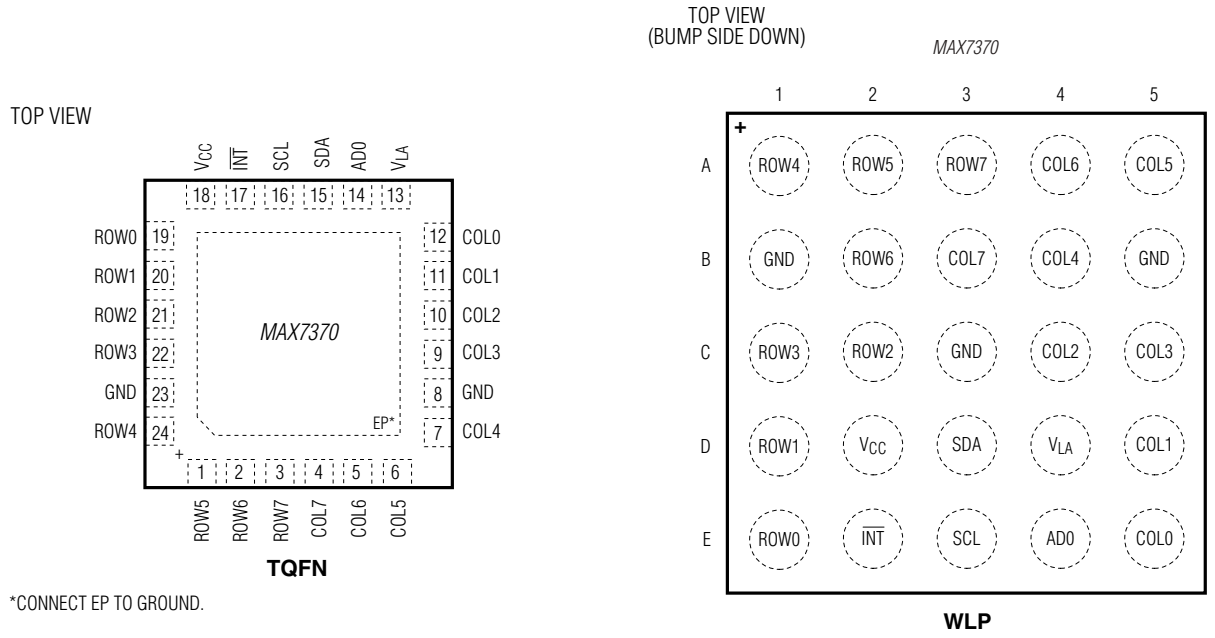


CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (COL7–COL4)



8 x 8 Key-Switch Controller and LED Driver/GPIOs with I²C Interface and High Level of ESD Protection

Pin/Bump Configurations



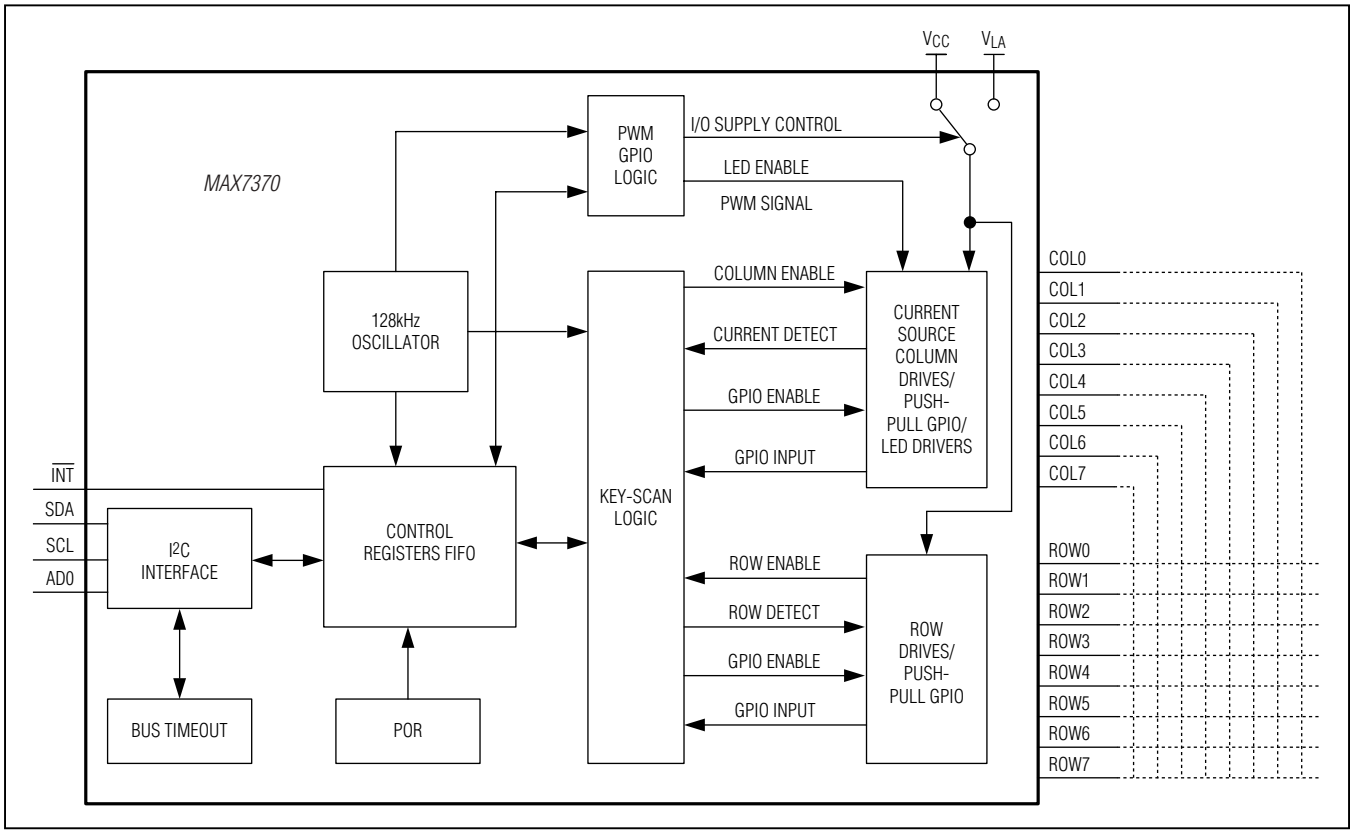
Pin/Bump Description

PIN	BUMP	NAME	FUNCTION
TQFN	WLP		
1	A2	ROW5	Row 5 Input from Key Matrix or GPIO Port
2	B2	ROW6	Row 6 Input from Key Matrix or GPIO Port
3	A3	ROW7	Row 7 Input from Key Matrix or GPIO Port
4	B3	COL7	Column 7 Output from Key Matrix or Open-Drain GPIO Port. COL7 can be configured as a constant-current sink.
5	A4	COL6	Column 6 Output from Key Matrix or Open-Drain GPIO Port. COL6 can be configured as a constant-current sink.
6	A5	COL5	Column 5 Output from Key Matrix or Open-Drain GPIO Port. COL5 can be configured as a constant-current sink.
7	B4	COL4	Column 4 Output from Key Matrix or Open-Drain GPIO Port. COL4 can be configured as a constant-current sink.
8, 23	B1, B5, C3	GND	Ground
9	C5	COL3	Column 3 Output from Key Matrix or GPIO Port
10	C4	COL2	Column 2 Output from Key Matrix or GPIO Port
11	D5	COL1	Column 1 Output from Key Matrix or GPIO Port
12	E5	COL0	Column 0 Output from Key Matrix or GPIO Port

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
13	D4	V_{LA}	Second Logic Level for GPIO Level Shifting (where $V_{CC} \le V_{LA} \le 3.6V$)
14	E4	AD0	Address Input. Selects up to four device slave addresses (Table 3).
15	D3	SDA	I²C-Compatible, Serial-Data I/O
16	E3	SCL	I²C-Compatible, Serial-Clock Input
17	E2	$\overline{INT}$	Active-Low Key-Switch Interrupt Output. $\overline{INT}$ is open-drain and requires a pullup resistor.
18	D2	V_{CC}	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor as close as possible to the device.
19	E1	ROW0	Row 0 Input from Key Matrix or GPIO Port
20	D1	ROW1	Row 1 Input from Key Matrix or GPIO Port
21	C2	ROW2	Row 2 Input from Key Matrix or GPIO Port
22	C1	ROW3	Row 3 Input from Key Matrix or GPIO Port
24	A1	ROW4	Row 4 Input from Key Matrix or GPIO Port
—	—	EP	Exposed Pad (TQFN Only). Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Block Diagram



Detailed Description

The MAX7370 is a microprocessor peripheral low-noise key-switch controller that monitors up to 64 key switches with optional autorepeat, and key events that are presented in a 16-byte FIFO. Key-switch functionality can be traded to provide up to 16 logic inputs. The device also features 12 push-pull GPOs configured for digital I/O and four open-drain GPOs configurable as constant-current outputs for LED applications up to 5V. The device supports a second 1.62V to 3.6V power supply for level translation. The second logic supply voltage (V_{LA}) must be set equal to or higher than V_{CC}.

The device features an automatic sleep mode and automatic wakeup that further reduce supply current consumption. The device can be configured to enter sleep mode after a programmable time following a key event. The FIFO content is maintained and can be read in sleep mode. The device does not enter autosleep when a key is held down. The autowake feature takes the device out of sleep mode following a keypress. Autosleep and autowake are enabled/disabled by programming the configuration register (0x01).

To prevent overloading the microprocessor with too many interrupts, interrupt requests can be triggered after a programmable number of FIFO entries have been exceeded, and/or after a set period of time (0x05). The key-switch status is checked by reading the key-switch FIFO. A 1-byte read access returns both the next key event in the FIFO (if there is one) and the FIFO status.

Up to four of the key-switch outputs function as open-drain GPOs capable of driving additional LEDs when the application requires fewer keys to be scanned. For each key-switch output used as a GPO, the number of monitored key switches reduces by eight.

The device meets ESD requirements for ±8kV contact discharge and 15kV Air-Gap Discharge on all key-switch pins.

Initial Power-Up

On power-up, all control registers are set to power-up values (Table 1) and the device is in sleep mode.

Table 1. Register Address Map and Power-Up Conditions

ADDRESS CODE (hex)	READ/WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x00	Read only	0x3F	Keys FIFO	Read FIFO keyscan data out
0x01	R/$\overline{W}$	0x0B	Configuration	Power-down, key-release enable, autowake, and I²C timeout enable
0x02	R/$\overline{W}$	0xFF	Debounce	Key debounce time setting
0x03	R/$\overline{W}$	0x00	Interrupt	Key-switch interrupt and $\overline{INT}$ frequency setting
0x05	R/$\overline{W}$	0x00	Key repeat	Delay and frequency for key repeat
0x06	R/$\overline{W}$	0x07	Sleep	Idle time to autosleep
0x30	R/$\overline{W}$	0xFF	Key-switch size	Keyscan switch array size
0x31	R/$\overline{W}$	0x00	LED driver enable	LED driver enable register
0x32	R/$\overline{W}$	0xFF	GPI enable	GPI enable for ROW7–ROW0
0x33	R/$\overline{W}$	0xFF	GPI enable	GPI enable for COL7–COL0
0x34	R/$\overline{W}$	0x00	GPIO direction 1	GPIO input/output control register 1 for ROW7–ROW0
0x35	R/$\overline{W}$	0x00	GPIO direction 2	GPIO input/output control register 2 for COL7–COL0
0x36	R/$\overline{W}$	0xFF	GPO output mode 1	GPO open-drain/push-pull output setting for ROW7–ROW0
0x37	R/$\overline{W}$	0x0F	GPO output mode 2	GPO open-drain/push-pull output setting for COL7–COL0

Table 1. Register Address Map and Power-Up Conditions (continued)

ADDRESS CODE (hex)	READ/WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x38	R/$\overline{W}$	0x00	GPIO supply voltage 1	GPIO voltages supplied by V_{CC} or V_{LA} for ROW7–ROW0
0x39	R/$\overline{W}$	0x00	GPIO supply voltage 2	GPIO voltages supplied by V_{CC} or V_{LA} for COL7–COL0
0x3A	R/$\overline{W}$	0xFF	GPIO values 1	Debounced input or output values of ROW7–ROW0
0x3B	R/$\overline{W}$	0xFF	GPIO values 2	Debounced input or output values of COL7–COL0
0x3C	R/$\overline{W}$	0x00	GPIO level-shifter enable	GPIO direct level-shifter pair enable
0x40	R/$\overline{W}$	0x00	GPIO global configuration	GPIO global enable, GPIO reset, LED fade enable
0x42	R/$\overline{W}$	0x00	GPIO debounce	ROW7–ROW0 debounce time setting
0x43	R/$\overline{W}$	0xC0	LED constant-current setting	COL7–COL4 constant-current output setting
0x45	R/$\overline{W}$	0x00	Common PWM	Common PWM duty-cycle setting
0x48	Read only	0x00	I²C timeout flag	I²C timeout since last POR
0x50	R/$\overline{W}$	0x00	COL4 PWM ratio	COL4 individual duty-cycle setting
0x51	R/$\overline{W}$	0x00	COL5 PWM ratio	COL5 individual duty-cycle setting
0x52	R/$\overline{W}$	0x00	COL6 PWM ratio	COL6 individual duty-cycle setting
0x53	R/$\overline{W}$	0x00	COL7 PWM ratio	COL7 individual duty-cycle setting
0x54	R/$\overline{W}$	0x00	COL4 LED configuration	COL4 interrupt, PWM mode control, and blink-period settings
0x55	R/$\overline{W}$	0x00	COL5 LED configuration	COL5 interrupt, PWM mode control, and blink-period settings
0x56	R/$\overline{W}$	0x00	COL6 LED configuration	COL6 interrupt, PWM mode control, and blink-period settings
0x57	R/$\overline{W}$	0x00	COL7 LED configuration	COL7 interrupt, PWM mode control, and blink-period settings
0x58	R/$\overline{W}$	0xFF	Interrupt mask 1	Interrupt mask for ROW7–ROW0
0x59	R/$\overline{W}$	0xFF	Interrupt mask 2	Interrupt mask for COL7–COL0
0x5A	R/$\overline{W}$	0x00	GPI trigger mode 1	GPI edge-triggered detection setting for ROW7–ROW0
0x5B	R/$\overline{W}$	0x00	GPI trigger mode 2	GPI edge-triggered detection setting for COL7–COL0

Keyscan Controller

Key inputs are scanned statically, not dynamically, to ensure low-EMI operation. Since inputs only toggle in response to switch changes, the key matrix can be routed closer to sensitive circuit nodes.

The keyscan controller debounces and maintains a FIFO buffer of keypress and release events (including auto-repeated keypresses, if autorepeat is enabled). Table 2 shows the key-switch order. The user-programmable key-switch debounce time and autosleep timer are derived from the 64kHz clock, which in turn is derived from the 128kHz oscillator. Time delay for autorepeat and key-switch interrupt is based on the key-switch debounce time. There is no limitation for the number of keys pressed simultaneously as long as no ghost keys are generated. If the application requires fewer keys to be scanned, the unused key-switch ports can be configured as GPIOs.

Keys FIFO Register (0x00)

The Keys FIFO register contains the information pertaining to the status of the keys FIFO, as well as the key events that have been debounced. See Table 7. Bits D[5:0] denote which of the 64 keys have been debounced and the keys are numbered as shown in Table 2.

Bit D7 indicates if there is more data in the FIFO, except when D[5:0] indicate key 63 or key 62. When D[5:0] indicate key 63 or key 62, the host should read the FIFO one more time to determine whether there is more data in the FIFO. Use key 62 and key 63 for rarely used keys. D6 indicates if it is a keypress or release event, except when D[5:0] indicate key 63 or key 62.

Reading the keyscan FIFO clears the interrupt ($\overline{INT}$), depending on the setting of bit D5 in the configuration register (0x01).

Configuration Register (0x01)

The Configuration register controls the I²C bus time-out feature, enables key-release detection, enables autowake, and determines how $\overline{INT}$ is deasserted. Write to bit D7 to put the device into sleep mode or operating mode. Autosleep and autowake, when enabled, also change the status of D7. See Table 8.

Debounce Register (0x02)

The Debounce register sets the keypress and key-release time for each debounce cycle. Bits D[3:0] set the debounce time for keypresses, while bits D[7:4] set the debounce time for key releases. Both debounce times are configured in increments of 2ms starting at 2ms and ending at 32ms. See Table 9.

Interrupt Register (0x03)

The Interrupt register contains information related to the settings of the interrupt request function, as well as the status of the $\overline{INT}$ output. If bits D[7:0] are set to 0x00, the $\overline{INT}$ is disabled. There are two types of interrupts, the FIFO-based interrupt and time-based interrupt. Set bits D[4:0] to assert interrupts at the end of the selected number of debounce cycles following a key event. See Table 10. This number ranges from 1–31 debounce cycles. Setting bits D[5:7] set the FIFO-based interrupt when there are 2–14 key events stored in the FIFO. Both interrupts can be configured simultaneously and $\overline{INT}$ asserts depending on which condition is met first. $\overline{INT}$ deasserts depending on the status of bit D5 in the configuration register.

Autorepeat Register (0x05)

The device autorepeat feature notifies the host that at least one key has been pressed for a continuous period. The Autorepeat register enables or disables this feature, sets the time delay after the last key event before the key-repeat code (0x7E) is entered into the FIFO, and sets

Table 2. Key-Switch Mapping

PIN	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7
ROW0	KEY 0	KEY 8	KEY 16	KEY 24	KEY 32	KEY 40	KEY 48	KEY 56
ROW1	KEY 1	KEY 9	KEY 17	KEY 25	KEY 33	KEY 41	KEY 49	KEY 57
ROW2	KEY 2	KEY 10	KEY 18	KEY 26	KEY 34	KEY 42	KEY 50	KEY 58
ROW3	KEY 3	KEY 11	KEY 19	KEY 27	KEY 35	KEY 43	KEY 51	KEY 59
ROW4	KEY 4	KEY 12	KEY 20	KEY 28	KEY 36	KEY 44	KEY 52	KEY 60
ROW5	KEY 5	KEY 13	KEY 21	KEY 29	KEY 37	KEY 45	KEY 53	KEY 61
ROW6	KEY 6	KEY 14	KEY 22	KEY 30	KEY 38	KEY 46	KEY 54	KEY 62
ROW7	KEY 7	KEY 15	KEY 23	KEY 31	KEY 39	KEY 47	KEY 55	KEY 63

the frequency at which the key-repeat code is entered into the FIFO thereafter. The key being pressed is not entered again into the FIFO. Bit D7 specifies whether the autorepeat function is enabled with 0, denoting autorepeat disabled, and 1, denoting autorepeat enabled. Bits D[3:0] specify the autorepeat delay in terms of debounce cycles, ranging from eight debounce cycles to 128 debounce cycles. See Table 11. Bits D[6:4] specify the autorepeat rate or frequency ranging from 4–32 debounce cycles.

Only one autorepeat code is entered into the FIFO, regardless of the number of keys pressed. The autorepeat code continues to be entered in the FIFO at the frequency set by bits D[3:0] until another key event is recorded. Following the key-release event, if any keys are still pressed, the device restarts the autorepeat sequence.

Autosleep Register (0x06)

Autosleep puts the device in sleep mode to draw minimal current. When enabled, the device enters sleep mode if no keys are pressed for the autoshutdown time. See Table 12.

Key-Switch Array Size Register (0x30)

Bits D[7:4] set the row size of the key-switch array, and bits D[3:0] set the column size of the key-switch array. See Table 13. Set the bits to 0 if no key switches are used. The key-switch array should be connected beginning at ROW0 and COL0. If not used as a key-switch matrix pin, then the pin can function as a GPIO port.

Key-Switch Sleep Mode

In sleep mode, the device draws minimal current. Switch-matrix current sources are turned off and pulled up to V_{CC}. When autosleep is enabled, key-switch inactivity for a period longer than the autosleep time puts the part into sleep mode (FIFO data is maintained). Writing a 1 to D7 or a keypress can take the device out of sleep mode. Bit D7 in the configuration register gives the sleep-mode status and can be read any time.

Autowake

Keypresses initiate autowake and the device goes into operating mode. Keypresses that autowake the device are not lost. When a key is pressed while the device is in sleep mode, all analog circuitry, including switch-matrix current sources, turn on in 2ms. The initial key needs to be pressed for 2ms plus the debounce time to be stored in the FIFO. Write a 0 to bit D1 in the configuration register (0x01) to disable autowake.

FIFO Overflow

The FIFO overflow status occurs when the FIFO is full (16 bytes) and additional events occur. If key release is disabled, then the FIFO overflow status occurs when the FIFO is full and not upon additional key events. When the FIFO is overflowed, the first byte read from the FIFO buffer is the overflow byte (0x7F). The order of the original 16 bytes of event data is preserved, but further events could be lost. When the FIFO is full, if the 18th key event is a key release, then the FIFO overflow status is removed.

GPIOs

The device has 16 GPIO ports, four of which have LED control functions. The ports can be used as logic inputs or logic outputs. COL7–COL4 are also configurable as constant-current PWM LED drivers. Each port's logic level is referenced to V_{CC} or V_{LA}. The GPIO ports' inputs can also be debounced. When in PWM mode, the ports are set up to start their PWM cycle in 45° phase increments. This prevents large current spikes on the LED supply voltage when driving multiple LEDs.

LED Driver Enable Register (0x31)

Bits D[3:0] correspond to COL7–COL4 on the device. Set the corresponding bit to 1 for enabling the LED driver circuitry and 0 for normal GPIO function. See Table 14.

GPIO Direction 1 and 2 Registers (0x34, 0x35)

These registers configure the pins as an input or an output port. GPIO Direction 1 register bits D[7:0] correspond with ROW7–ROW0. See Table 15. GPIO Direction 2 register bits D[7:0] correspond with COL7–COL0. See Table 16. Set the corresponding bit to 0 to configure as input and 1 to configure as output.

When the port is initially programmed as an input, there is a delay of one debounce period prior to detecting a transition on the input port. This is to prevent a false interrupt from occurring when changing a port from an output to an input.

GPO Output Mode 1 and 2 Registers (0x36, 0x37)

These registers configure the pin as an open-drain or push-pull output. GPO Output Mode 1 register bits D[7:0] correspond with ROW7–ROW0. See Table 17. GPO Output Mode 2 register bits D[7:0] correspond with COL7–COL0. See Table 18. Set the corresponding bit to 0 to configure the output mode as open-drain and 1 to configure the output mode as push-pull.

GPIO Supply Voltage 1 and 2 Registers (0x38, 0x39)

These registers configure input and output voltages to be referenced to V_{CC} or V_{LA}. GPIO Supply Voltage 1 register bits D[7:0] correspond with ROW7–ROW0. See Table 19. GPIO Supply Voltage 2 register bits D[7:0] correspond with COL7–COL0. See Table 20. Set the bit to 0 for input/output voltages referenced to V_{CC} or set the bit to 1 for the input/output voltage referenced to V_{LA}.

GPIO Values 1 and 2 Registers (0x3A, 0x3B)

The GPIO Values 1 and 2 registers contain the debounced input data for all the GPIOs for ROW7–ROW0 and COL7–COL0, respectively. See Tables 21 and 22. There is one debounce period delay prior to detecting a transition on the input port. This prevents a false interrupt from occurring when changing a port from an output to an input. The GPIO Values 1 and 2 registers report the state of all input ports regardless of any interrupt mask settings.

When writing to the GPIO Values 1 and 2 registers, the corresponding port voltage is set high when written 1 or cleared when written 0. Reading the port when configured as an output always returns the value 0 for the corresponding port regardless of the output value.

GPIO Level-Shifter Enable Register (0x3C)

Enabling bit D_ in this register enables the direct level shifter between GPIO pins COL_ and ROW_. See Table 23. As an example, setting D5 to logic-high enables level shifting between COL5 and ROW5. The direction of the level shifter is controlled by the GPIO Direction 2 register (0x35). When setting the corresponding bit in the GPIO Direction 2 register to 0, COL_ are inputs, and ROW_ are outputs. When setting the bit to 1, ROW_ become inputs and COL_ become outputs.

GPIO Global Configuration Register (0x40)

The GPIO Global Configuration register controls the main settings for the GPIO ports. See Table 24. Bit D5 enables interrupt generation for I²C timeouts. D4 is the main enable/shutdown bit for the GPIOs. Bit D3 functions as a software reset for the GPIO registers (0x31 to 0x5B). Bits D[2:0] set the fade-in/out time for the LED drivers.

GPIO Debounce Configuration Register (0x42)

The GPIO Debounce Configuration Register sets the amount of time a GPIO must be held in order for the device to register a logic transition. See Table 25. The GPIO debounce setting is independent of the key-switch debounce setting. Five bits (D[4:0]) set 32 possible debounce times from 9ms up to 40ms.

LED Constant-Current Setting Register (0x43)

The LED Constant-Current Setting register sets the global constant-current amount. See Table 26. Bit D0 selects the global current values between 10mA and 20mA. This setting only applies to the LED driver-enabled pins, COL7–COL4.

Common PWM Ratio Register (0x45)

The Common PWM Ratio register stores the common constant-current output PWM duty cycle. See Table 27. The values stored in this register translate over to a PWM ratio in the same manner as the individual PWM ratio registers (0x50 to 0x53). Ports can use their own individual PWM value or the common PWM value. Write to this register to change the PWM ratio of several ports at once.

I²C Timeout Flag Register (0x48) (Read Only)

The I²C Timeout Flag register contains a single bit (D0) that indicates if an I²C timeout has occurred. See Table 28. Read this register to clear an I²C timeout-initiated interrupt.

COL4–COL7 Individual PWM Ratio Registers (0x50 to 0x53)

Each LED driver port has an individual PWM ratio register, 0x50 to 0x53. See Table 29. Use values 0x00 to 0xFE in these registers to configure the number of cycles out of 256 the output sinks current (LED is on), from 0 cycles to 254 cycles. Use 0xFF to have an output continuously sink current (always on). For applications requiring multiple ports to have the same intensity, program a particular port's configuration register (0x54 to 0x57) to use the Common PWM Ratio register (0x45). New PWM settings take place at the beginning of a PWM cycle, to allow changes from common intensity to individual intensity with no interruption in the PWM cycle.

COL4–COL7 LED Configuration Registers (0x54 to 0x57)

Registers 0x54 to 0x57 set individual configurations for each port. See Table 30. D5 sets the port's PWM setting to either the common or individual PWM setting. Bits D[4:2] enable and set the port's individual blink period from 0 to 4096ms. Bits D[1:0] set a port's blink duty cycle.

Interrupt Mask 1 and 2 Registers (0x58, 0x59)

The Interrupt Mask 1 and 2 registers control which ports trigger an interrupt for ROW7–ROW0 and COL7–COL0, respectively. See Tables 31 and 32. Set the bit to 0 to enable the interrupt. Set the bit to 1 to mask the interrupt.

If the port that has generated the interrupt is not masked, the interrupt causes the $\overline{INT}$ signal to assert. A read of the GPIO Values 1 and 2 registers (0x3A, 0x3B) is required to deassert the $\overline{INT}$ pin. Note that transitions that occur while the $\overline{INT}$ signal is asserted, but before the read of the GPIO Values 1 and 2 registers, set the appropriate bit of the GPIO Values 1 and 2 registers only, but has no effect on the $\overline{INT}$ pin as it is already asserted. However, transitions that occur when the I²C is active cannot be latched into the GPIO Values 1 and 2 registers until after the read has taken place. If there are transitions that cause the $\overline{INT}$ signal to assert, during the time of an I²C read, they cause the $\overline{INT}$ signal to reassert once the read transaction has taken place. Note that the interrupt configurations only apply when a port is configured as an input.

GPI Trigger Mode 1 and 2 Registers (0x5A, 0x5B)

The GPI Trigger Mode 1 and 2 registers control how ports can trigger an interrupt for ROW7–ROW0 and COL7–COL0, respectively. See Tables 33 and 34. Set the bit to 0 for rising-edge triggering. Set the bit to 1 for rising- and falling-edge triggering.

The inputs are debounced (if enabled) by taking a snapshot of the port state when the transition occurs, and another after the debounce time has elapsed—ensuring that the state of the port is stable prior to triggering the interrupt. After the debounce cycle, an interrupt is generated and the $\overline{INT}$ pin asserted if it is not masked for that particular port. Regardless of whether or not the $\overline{INT}$ signal is masked, the GPIO Values 1 and 2 registers (0x3A, 0x3B) report the state of all input ports.

Sleep Mode

The device is put into sleep mode by clearing bit D7 in the Configuration register, or after power-on reset (POR). In sleep mode, the keyscan controller is disabled and the device draws minimal current. No additional supply current is drawn if no keys are pressed. All switch-matrix current sources are turned off, and row outputs ROW7–ROW0 are low and column outputs COL7–COL0 become high.

The device is taken out of sleep mode and put into operating mode by setting bit D7 in the configuration register. The keyscan controller FIFO buffers are cleared and key monitoring starts. Note that rewriting the configuration register with bit D7 high, when bit D7 was already high, does not clear the FIFOs. The FIFOs are only cleared when the device is changing state from sleep mode to operating mode.

In sleep mode, the internal oscillator is disabled and I²C timeout features are disabled. The GPO or LED ports consume current even in sleep mode. The part does not enter sleep mode if any of the GPIOs or LED drivers are enabled.

LED Fade

Set the fade cycle time in the GPIO Global Configuration register (0x40) to a non-zero value to enable fade in/out. See Table 24. Fade in increases an LED's PWM intensity in 16 even steps, from zero to its stored value. Fade out decreases an LED's PWM intensity in 16 even steps from its current value to zero. Fading occurs automatically in any of the following scenarios:

- Change the common PWM register value from any value to zero to cause all ports using the common PWM register settings to fade out. No ports using individual PWM settings are affected.
- Change the common PWM register value to any value from zero to cause all ports using the common PWM register settings to fade in. No ports using individual PWM settings are affected.
- Take the part out of sleep mode to cause all ports to fade in. Changing an individual PWM intensity during fade in automatically cancels that port's fade and immediately outputs at its newly programmed intensity.

- Put the part into sleep mode to cause all ports to fade out. Changing an individual PWM intensity during fade out automatically cancels that port's fade and immediately turns off.

LED PWM

Each port has an individual PWM ratio register. The value stored in this register configures the number of cycles out of 255 that the output is sinking current (LED is on). Setting a value of 0xFF in an individual intensity register sets the output to continuously sink current (always on). Conversely, setting a value of 0x00 in an individual intensity register sets the output in a high-impedance state (always off).

For applications requiring multiple ports to have the same intensity, the common PWM ratio intensity setting can be used in lieu of the individual intensity setting. To use the common intensity setting, program bit D5 of the corresponding port's configuration register to logic-high. Setting a port to use the common PWM ratio setting copies the value of the common intensity register into the individual intensity register at the beginning of each PWM cycle. This allows an output port to be seamlessly changed from common intensity to individual intensity with no interruption in the PWM cycle.

Outputs are configured to sink a constant current of either 10mA or 20mA during the period of time when the output is on. The setting in the individual GPIO constant-current setting register (0x43) controls the value of the current.

LED Blink

Each LED driver-supported port has its own blink-control settings through registers 0x54 to 0x57. See Table 30. The blink period ranges from 0 (blink disabled) to 4.096s. Settable blink duty cycles range from 6.25% to 50%. All blink periods start at the same PWM cycle for synchronized blinking between multiple ports.

Each port has its own counter to generate blink timing. The blink counter can be programmed to cause the output to gate off and on at a programmable rate. The blink period can be set to 256ms, 512ms, 1.024s, 2.048s, or 4.096s using D[4:2] of the port's individual configuration register. The percentage of time that the LED is on for one blink cycle is set to 50%, 25%, 12.5%, or 6.25% by D[1:0] of the individual configuration register.

Interrupts

Three possible sources generate $\overline{INT}$: key-switch FIFO level/debounce cycle settings, I²C timeout, or GPIOs configured as inputs (registers 0x03, 0x48, 0x5A, and 0x5B). Read the respective data/status registers for each type of interrupt to clear $\overline{INT}$. If multiple sources generate the interrupt, all the related status registers must be read to clear $\overline{INT}$.

Serial Interface

Figure 1 shows the two-wire serial interface timing details.

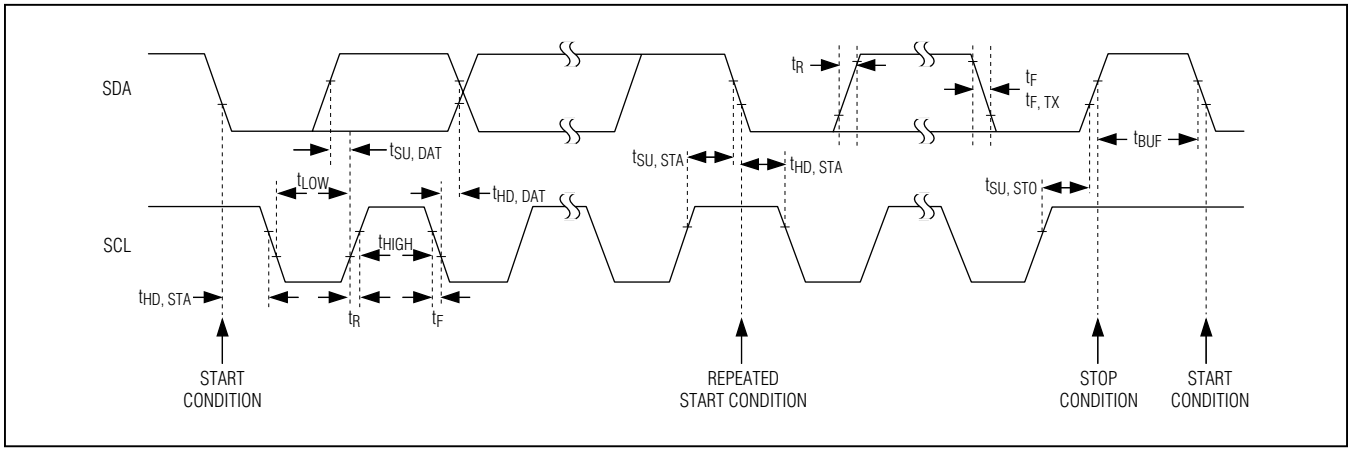


Figure 1. Two-Wire Serial Interface Timing Details

Serial Addressing

The device operates as a slave that sends and receives data through an I²C-compatible two-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer.

The device's SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The device's SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the two-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 2) sent by a master, followed by the device's 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally, a STOP (P) condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 3). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 4), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse; therefore, the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the device, the device generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

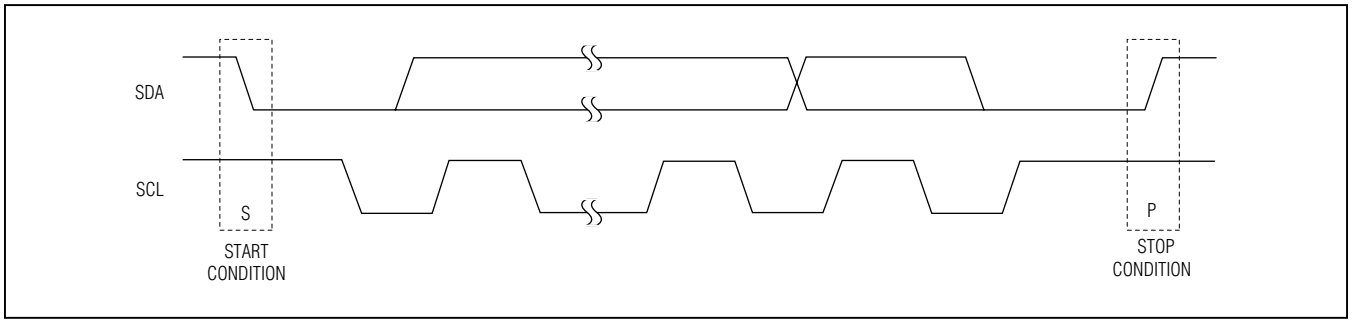


Figure 2. START and STOP Conditions

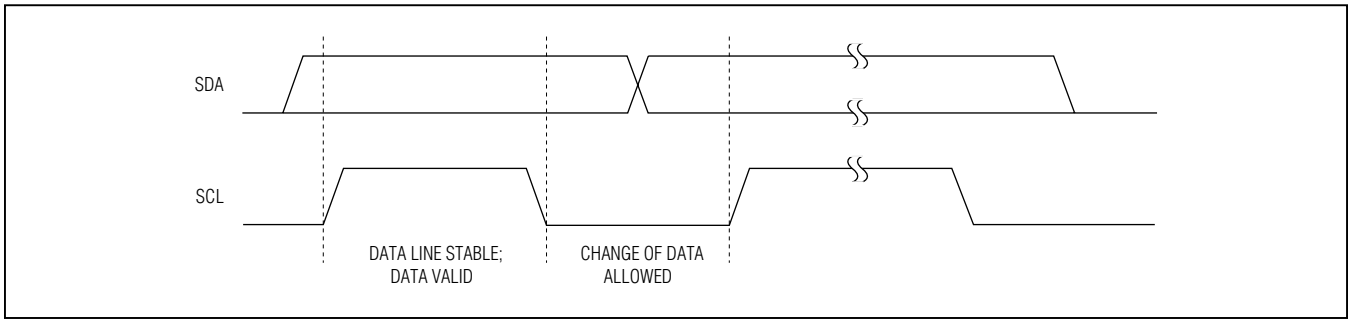


Figure 3. Bit Transfer

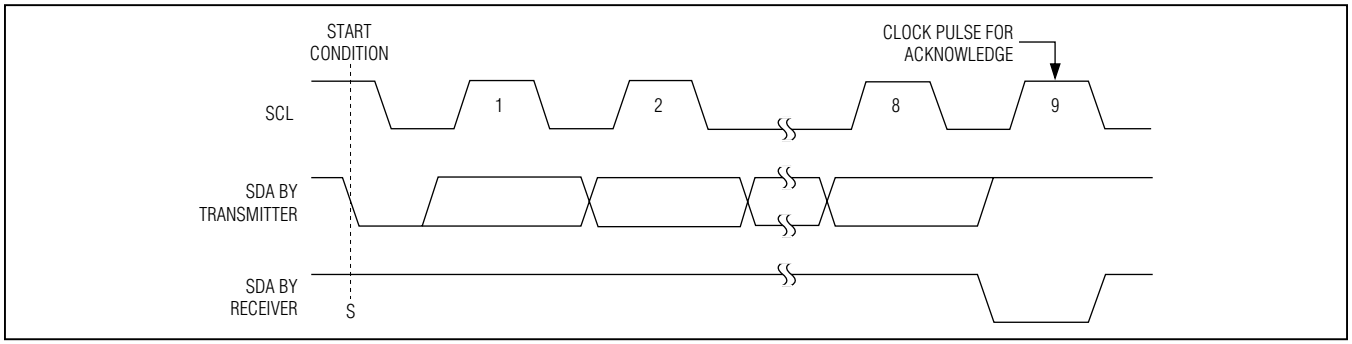


Figure 4. Acknowledge

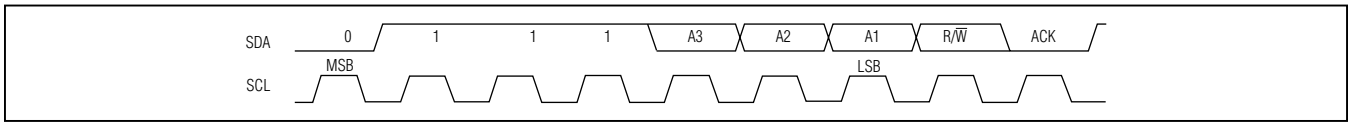


Figure 5. Slave Address

Table 3. Two-Wire Interface Address Map

AD0 PIN	DEVICE ADDRESS							
	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	1	1	0	0	0	R/$\overline{W}$
V_{CC}					0	1		
SDA					1	0		
SCL					1	1		

Slave Addresses

The device has two 7-bit long slave addresses. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

The first 4 bits (MSBs) of the device slave addresses are always 0111. Slave address bits A[3:1] correspond, by the matrix in Table 3, to the states of the device address input pin AD0, and A0 corresponds to the R/$\overline{W}$ bit (Figure 5). The AD0 input can be connected to any of four signals: GND, V_{CC}, SDA, or SCL, giving four possible slave-address pairs, allowing up to four devices to share the same bus. Because SDA and SCL are dynamic signals, care must be taken to ensure that AD0 transitions no sooner than the signals on SDA and SCL.

The device monitors the bus continuously, waiting for a START condition, followed by its slave address. When the device recognizes its slave address, it acknowledges and is then ready for continued communication.

Bus Timeout

The device features a 20ms (min) bus timeout on the two-wire serial interface, largely to prevent the device from holding the SDA I/O low during a read transaction should the SCL lock up for any reason before a serial transaction is completed. Bus timeout operates by causing the device to internally terminate a serial transaction, either read or write, if the time between adjacent edges on SCL exceeds 20ms. After a bus timeout, the device waits for a valid START condition before responding to a consecutive transmission. This feature can be enabled or disabled under user control by writing to the configuration register.

Message Format for Writing the Keyscan Controller

A write to the device comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the command byte. The command byte determines which register of the device is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the device takes no further action (Figure 6) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the device selected by the command byte (Figure 7).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent internal registers of the device, because the command-byte address generally autoincrements (Table 4).

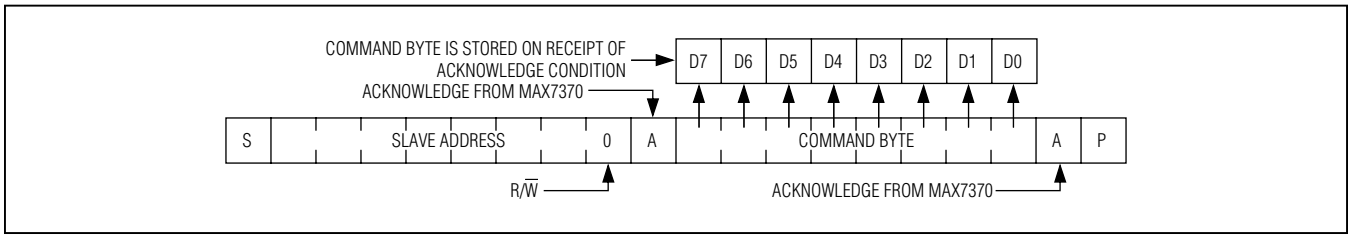


Figure 6. Command Byte Received

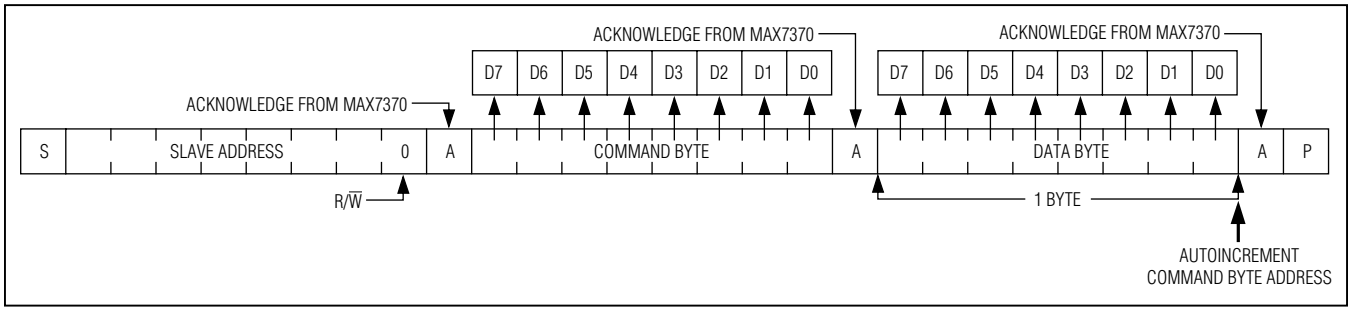


Figure 7. Command and Single Data Byte Received

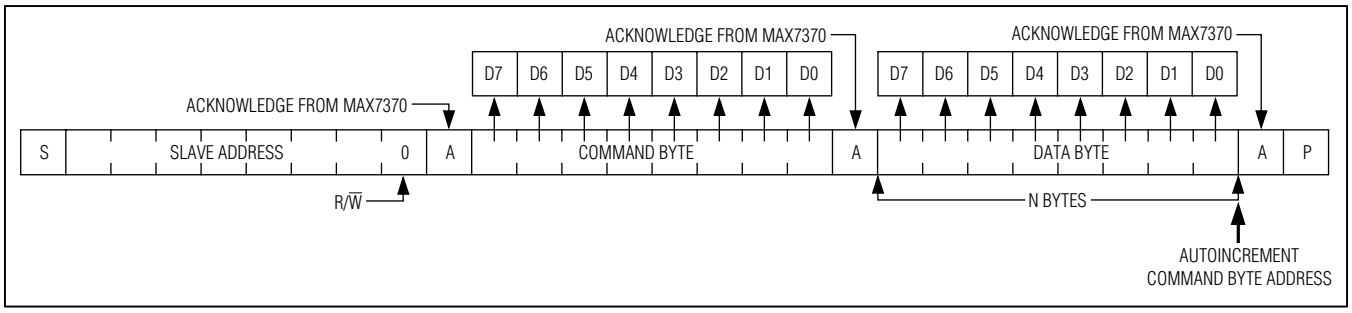


Figure 8. N Data Bytes Received

Message Format for Reading the Keyscan Controller

The device is read using the internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 4). Thus, a read is initiated by first configuring the device's command byte by performing a write (Figure 6). The master can now read N consecutive bytes from the device, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address is generally autoincremented after the write (Figure 8, Table 4).

Table 4. Autoincrement Rules

REGISTER FUNCTION	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS (hex)
Keys FIFO	0x00	0x00
Autosleep	0x06	0x00
All other key switches	0x01 to 0x05	Addr + 0x01
All other GPIOs	0x30 to 0x5B	Addr + 0x01

Operation with Multiple Masters

When the device is operated on a two-wire interface with multiple masters, a master reading the device uses a repeated start between the write that sets the device's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the device's address pointer but before master 1 has read the data. If master 2 subsequently resets the device's address pointer, master 1's read can be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the device to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the device generally increments after each data byte is written or read (Table 4). Autoincrement only functions when doing a multiburst read or write.

Applications Information

Reset from I²C

After a catastrophic event such as ESD discharge or microcontroller reset, use bit D7 of the configuration register (0x01) as a software reset for the key switches. Use bit D4 of the GPIO global configuration register (0x40) as a software reset for the GPIOs.

Ghost-Key Elimination

Ghost keys are a phenomenon inherent with key-switch matrices. When three switches located at the corners of a matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed. This occurs because the potentials at the two sides of the ghost-key switch are identical due to the other three connections—the switch is electrically shorted by the combination of the other three switches (Figure 9). Because the key appears to be pressed electrically, it is impossible to detect which of the four keys is the ghost key.

The device employs a proprietary scheme that detects any three-key combination that generates a fourth ghost key, and does not report the third key that causes a ghost-key event. This means that although ghost keys are never reported, many combinations of three keys are effectively ignored when pressed at the same time. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are not wired in positions that define the vertices of a rectangle (Figure 10). There is no limit on the number of keys that can be pressed simultaneously as long as the keys do not generate ghost-key events and the FIFO is not full.

Low-EMI Operation

The device uses two techniques to minimize EMI radiating from the key-switch wiring. First, the voltage across the switch matrix never exceeds 0.5V if not in sleep mode, independent of supply voltage V_{CC}. This reduces the voltage swing at any node when a switch is pressed to 0.5V (max). Second, the keys are not dynamically scanned, which would cause the key-switch wiring to continuously radiate interference. Instead, the keys are monitored for current draw (only occurs when pressed), and debounce circuitry only operates when one or more keys are actually pressed.

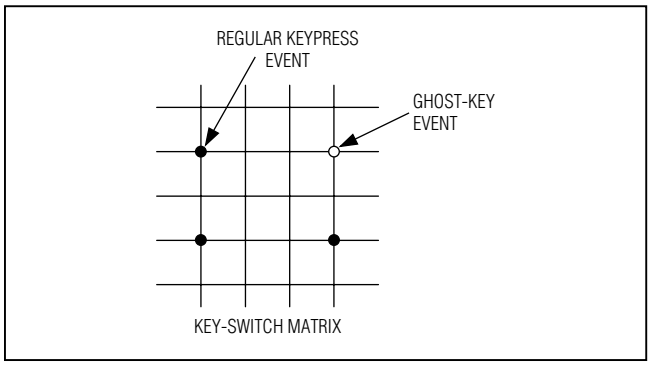


Figure 9. Ghost-Key Phenomenon

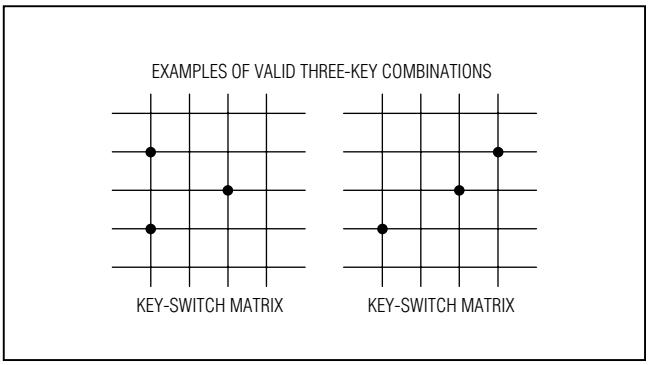


Figure 10. Valid Three-Key Combinations

Switch On-Resistance

The device is designed to be insensitive to resistance, either in the key switches, or the switch routing to and from the appropriate COL_ and ROW_ up to 5kΩ (max). These controllers are therefore compatible with low-cost membrane and conductive carbon switches.

Hot Insertion

The $\overline{INT}$, SCL, and AD0 inputs and SDA remain high impedance with up to 5.5V asserted on them when the device powers down (V_{CC} = 0V). I/O ports remain high impedance with up to 5.5V asserted on them when not powered. Use the device in hot-swap applications.

Staggered PWM

The LED's on-time in each PWM cycle is phase delayed by 45° into four evenly spaced start positions. Optimize phasing, when using fewer than four ports as constant-current outputs, by allocating the ports with the most appropriate start positions. For example, if using two constant-current outputs, choose COL4 and COL6 because their PWM start positions are evenly spaced. In general, choose the ports that spread the current demand from the ports' load supply.

Power-Supply Considerations

The device operates with a 1.62V to 3.6V power-supply voltage. Bypass the power supply (V_{CC}) to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device. Bypass the logic power supply (V_{LA}) to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device.

ESD Protection

All the device pins meet the ±2.5kV Human Body Model ESD tolerances. Key-switch inputs and GPIOs meet IEC 61000-4-2 ESD protection. The IEC test stresses consist of 10 consecutive ESD discharges per polarity at the maximum specified level and below (per IEC 61000-4-2). Test criteria include:

- The powered device does not latch up during the ESD discharge event.
- The device subsequently passes the final test used for prescreening.

Tables 5 and 6 are taken from the IEC 61000-4-2: Edition 1.1 1999-05: *Electromagnetic compatibility (EMC) Testing and measurement techniques—Electrostatic discharge immunity test*.

Table 5. ESD Test Levels

1A—CONTACT DISCHARGE		1B—AIR DISCHARGE	
LEVEL	**TEST VOLTAGE (kV)**	**LEVEL**	**TEST VOLTAGE (kV)**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X	Special	X	Special

X = Open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment might be needed.

Table 6. ESD Waveform Parameters

LEVEL	INDICATED VOLTAGE (kV)	FIRST PEAK OF CURRENT DISCHARGE ±10% (A)	RISE TIME (t_r) WITH DISCHARGE SWITCH (ns)	CURRENT (±30%) AT 30ns (A)	CURRENT (±30%) AT 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 7. Keys FIFO Register Format (0x00)

SPECIAL FUNCTION	KEYS FIFO REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
The key number indicated by D[5:0] is a key event. D7 is always for a keypress of key 62 and key 63. When D7 is 0, the key read is the last data in the FIFO. When D7 is 1, there is more data in the FIFO. When D6 is 1, key data read from the FIFO is a key release. When D6 is 0, key data read from the FIFO is a keypress.	FIFO not-empty flag	Key-release flag	Key number/key event					
FIFO is empty.	0	0	1	1	1	1	1	1
FIFO is overflow. Continue to read data in the FIFO.	0	1	1	1	1	1	1	1
Key 63 is pressed. Read one more time to determine whether there is more data in the FIFO.	1	0	1	1	1	1	1	1
Key 63 is released. Read one more time to determine whether there is more data in the FIFO.	1	1	1	1	1	1	1	1
Key repeat. Indicates the last data in the FIFO.	0	0	1	1	1	1	1	0
Key repeat. Indicates more data in the FIFO.	0	1	1	1	1	1	1	0
Key 62 is pressed. Read one more time to determine whether there is more data in the FIFO.	1	0	1	1	1	1	1	0
Key 62 is released. Read one more time to determine whether there is more data in the FIFO.	1	1	1	1	1	1	1	0

Table 8. Configuration Register (0x01)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION		DEFAULT VALUE
D7	Sleep	X (when 0x40 D4 = 1)	Key-switch operating mode. Key switches always remain active when constant-current PWM is enabled (bit 4 of register 0x40 is high), regardless of autosleep, autowake, or an I²C write to this bit.		0
		0 (when 0x40 D4 = 0)	Key-switch sleep mode. The entire chip is shut down.	When constant-current PWM is disabled (bit 4 of register 0x40 is low), I²C write, autosleep, and autowake all can change this bit. This bit can be read back by I²C any time for current status.	
		1 (when 0x40 D4 = 0)	Key-switch operating mode.		
D6	Reserved	0	—		0
D5	Interrupt	0	$\overline{INT}$ cleared when the FIFO is empty.		0
		1	$\overline{INT}$ cleared after host read. In this mode, I²C should read the FIFO until interrupt condition is removed or further $\overline{INT}$ could be lost.		
D4	Reserved	0	—		0
D3	Key-release enable	0	Disable key releases.		1
		1	Enable key releases.		
D2	Reserved	0	—		0
D1	Autowake enable	0	Disable keypress wakeup.		1
		1	Enable keypress wakeup.		
D0	Timeout disable	0	I²C timeout enabled.		1
		1	I²C timeout disabled.		

X = Don't care.

Table 9. Key-Switch Debounce Register (0x02)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
DEBOUNCE TIME	**RELEASE DEBOUNCE TIME**				**PRESS DEBOUNCE TIME**			
2ms	X				0	0	0	0
4ms					0	0	0	1
6ms					0	0	1	0
⋮								
28ms	X				1	1	0	1
30ms					1	1	1	0
32ms					1	1	1	1
2ms	0	0	0	0	X			
4ms	0	0	0	1				
6ms	0	0	1	0				
⋮								
28ms	1	1	0	1	X			
30ms	1	1	1	0				
32ms	1	1	1	1				
Power-on default (32ms)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

X = Don't care.

Table 10. Key-Switch Interrupt Register (0x03)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	FIFO-BASED $\overline{INT}$			**TIME-BASED $\overline{INT}$**				
Power-up default setting All $\overline{INT}$ disabled	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Time-based $\overline{INT}$ disabled	X			0	0	0	0	0
$\overline{INT}$ asserts every debounce cycle				0	0	0	0	1
$\overline{INT}$ asserts every 2 debounce cycles				0	0	0	1	0
⋮								
$\overline{INT}$ asserts every 29 debounce cycles	X			1	1	1	0	1
$\overline{INT}$ asserts every 30 debounce cycles				1	1	1	1	0
$\overline{INT}$ asserts every 31 debounce cycles				1	1	1	1	1
FIFO-based $\overline{INT}$ disabled	0	0	0	X				
$\overline{INT}$ asserts when the FIFO has 2 key events	0	0	1					
$\overline{INT}$ asserts when the FIFO has 4 key events	0	1	0					
⋮								
$\overline{INT}$ asserts when the FIFO has 10 key events	1	0	1	X				
$\overline{INT}$ asserts when the FIFO has 12 key events	1	1	0					
$\overline{INT}$ asserts when the FIFO has 14 key events	1	1	1					
Both time-based and FIFO-based interrupts active	Not all zero			Not all zero				

X = Don't care.

Table 11. Key-Switch Autorepeat Register (0x05)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	ENABLE	AUTOREPEAT RATE			AUTOREPEAT DELAY			
Autorepeat is disabled	0	X	X	X	X	X	X	X
Autorepeat is enabled	1	Autorepeat rate			Autorepeat delay			
Autorepeat delay is 8 debounce cycles	1	X			0	0	0	0
Autorepeat delay is 16 debounce cycles	1				0	0	0	1
Autorepeat delay is 24 debounce cycles	1				0	0	1	0
⋮								
Autorepeat delay is 112 debounce cycles	1	X			1	1	0	1
Autorepeat delay is 120 debounce cycles	1				1	1	1	0
Autorepeat delay is 128 debounce cycles	1				1	1	1	1
Autorepeat frequency is 4 debounce cycles	1	0	0	0	X			
Autorepeat frequency is 8 debounce cycles	1	0	0	1				
Autorepeat frequency is 12 debounce cycles	1	0	1	0				
⋮								
Autorepeat frequency is 24 debounce cycles	1	1	0	1	X			
Autorepeat frequency is 28 debounce cycles	1	1	1	0				
Autorepeat frequency is 32 debounce cycles	1	1	1	1				
Power-on default setting	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

X = Don't care.

Table 12. Autosleep Register (0x06)

REGISTER DESCRIPTION AUTOSLEEP (ms)	REGISTER DATA							
	RESERVED				AUTOSHUTDOWN TIME			
	D7	D6	D5	D4	D3	D2	D1	D0
Autosleep disabled	0	0	0	0	0	0	0	0
8192	0	0	0	0	0	0	0	1
4096	0	0	0	0	0	0	1	0
2048	0	0	0	0	0	0	1	1
1024	0	0	0	0	0	1	0	0
512	0	0	0	0	0	1	0	1
256	0	0	0	0	0	1	1	0
256	0	0	0	0	0	1	1	1
Power-up default settings	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

Table 13. Key-Switch Array Size Register (0x30)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	ROWS				COLUMNS			
No rows are key switches	0	0	0	0	X			
ROW0 is a key switch	0	0	0	1				
ROW0 to ROW1 are key switches	0	0	1	0				
ROW0 to ROW2 are key switches	0	0	1	1				
ROW0 to ROW3 are key switches	0	1	0	0				
ROW0 to ROW4 are key switches	0	1	0	1				
ROW0 to ROW5 are key switches	0	1	1	0				
ROW0 to ROW6 are key switches	0	1	1	1				
ROW0 to ROW7 are key switches	1	X	X	X				
No columns are key switches	X				0	0	0	0
COL0 is a key switch					0	0	0	1
COL0 to COL1 are key switches					0	0	1	0
COL0 to COL2 are key switches					0	0	1	1
COL0 to COL3 are key switches					0	1	0	0
COL0 to COL4 are key switches					0	1	0	1
COL0 to COL5 are key switches					0	1	1	0
COL0 to COL6 are key switches					0	1	1	1
COL0 to COL7 are key switches					1	X	X	X
Power-up default setting	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

X = Don't care.

Table 14. LED Driver Enable Register (0x31)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:4]	Reserved	0000	—	0000
D3	COL7	0	GPIO function	0
		1	LED driver enable	
D2	COL6	0	GPIO function	0
		1	LED driver enable	
D1	COL5	0	GPIO function	0
		1	LED driver enable	
D0	COL4	0	GPIO function	0
		1	LED driver enable	

Table 15. GPIO Direction 1 Register (0x34)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	Set as input pin	0
		1	Set as output pin	
D6	ROW6	0	Set as input pin	0
		1	Set as output pin	
D5	ROW5	0	Set as input pin	0
		1	Set as output pin	
D4	ROW4	0	Set as input pin	0
		1	Set as output pin	
D3	ROW3	0	Set as input pin	0
		1	Set as output pin	
D2	ROW2	0	Set as input pin	0
		1	Set as output pin	
D1	ROW1	0	Set as input pin	0
		1	Set as output pin	
D0	ROW0	0	Set as input pin	0
		1	Set as output pin	

Table 16. GPIO Direction 2 Register (0x35)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Set as input pin	0
		1	Set as output pin	
D6	COL6	0	Set as input pin	0
		1	Set as output pin	
D5	COL5	0	Set as input pin	0
		1	Set as output pin	
D4	COL4	0	Set as input pin	0
		1	Set as output pin	
D3	COL3	0	Set as input pin	0
		1	Set as output pin	
D2	COL2	0	Set as input pin	0
		1	Set as output pin	
D1	COL1	0	Set as input pin	0
		1	Set as output pin	
D0	COL0	0	Set as input pin	0
		1	Set as output pin	

Table 17. GPO Output Mode 1 Register (0x36)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D6	ROW6	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D5	ROW5	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D4	ROW4	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D3	ROW3	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D2	ROW2	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D1	ROW1	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D0	ROW0	0	Port is an open-drain output	1
		1	Port is a push-pull output	

Table 18. GPO Output Mode 2 Register (0x37)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Port is an open-drain output	0
D6	COL6	0	Port is an open-drain output	0
D5	COL5	0	Port is an open-drain output	0
D4	COL4	0	Port is an open-drain output	0
D3	COL3	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D2	COL2	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D1	COL1	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D0	COL0	0	Port is an open-drain output	1
		1	Port is a push-pull output	

Note: *When programmed as GPO, COL7–COL4 are always open drain and bits D[7:4] are not writable.*

Table 19. GPIO Supply Voltage 1 Register (0x38)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	ROW7 supplied by V_{CC}	0
		1	ROW7 supplied by V_{LA}	
D6	ROW6	0	ROW6 supplied by V_{CC}	0
		1	ROW6 supplied by V_{LA}	
D5	ROW5	0	ROW5 supplied by V_{CC}	0
		1	ROW5 supplied by V_{LA}	
D4	ROW4	0	ROW4 supplied by V_{CC}	0
		1	ROW4 supplied by V_{LA}	
D3	ROW3	0	ROW3 supplied by V_{CC}	0
		1	ROW3 supplied by V_{LA}	
D2	ROW2	0	ROW2 supplied by V_{CC}	0
		1	ROW2 supplied by V_{LA}	
D1	ROW1	0	ROW1 supplied by V_{CC}	0
		1	ROW1 supplied by V_{LA}	
D0	ROW0	0	ROW0 supplied by V_{CC}	0
		1	ROW0 supplied by V_{LA}	

Table 20. GPIO Supply Voltage 2 Register (0x39)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	COL7 supplied by V_{CC}	0
		1	COL7 supplied by V_{LA}	
D6	COL6	0	COL6 supplied by V_{CC}	0
		1	COL6 supplied by V_{LA}	
D5	COL5	0	COL5 supplied by V_{CC}	0
		1	COL5 supplied by V_{LA}	
D4	COL4	0	COL4 supplied by V_{CC}	0
		1	COL4 supplied by V_{LA}	
D3	COL3	0	COL3 supplied by V_{CC}	0
		1	COL3 supplied by V_{LA}	
D2	COL2	0	COL2 supplied by V_{CC}	0
		1	COL2 supplied by V_{LA}	
D1	COL1	0	COL1 supplied by V_{CC}	0
		1	COL1 supplied by V_{LA}	
D0	COL0	0	COL0 supplied by V_{CC}	0
		1	COL0 supplied by V_{LA}	

Table 21. GPIO Values 1 Register (0x3A)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	Clear ROW7 low	1
		1	Set ROW7 high	
D6	ROW6	0	Clear ROW6 low	1
		1	Set ROW6 high	
D5	ROW5	0	Clear ROW5 low	1
		1	Set ROW5 high	
D4	ROW4	0	Clear ROW4 low	1
		1	Set ROW4 high	
D3	ROW3	0	Clear ROW3 low	1
		1	Set ROW3 high	
D2	ROW2	0	Clear ROW2 low	1
		1	Set ROW2 high	
D1	ROW1	0	Clear ROW1 low	1
		1	Set ROW1 high	
D0	ROW0	0	Clear ROW0 low	1
		1	Set ROW0 high	

Table 22. GPIO Values 2 Register (0x3B)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Clear COL7 low	1
		1	Set COL7 high*	
D6	COL6	0	Clear COL6 low	1
		1	Set COL6 high*	
D5	COL5	0	Clear COL5 low	1
		1	Set COL5 high*	
D4	COL4	0	Clear COL4 low	1
		1	Set COL4 high*	
D3	COL3	0	Clear COL3 low	1
		1	Set COL3 high	
D2	COL2	0	Clear COL2 low	1
		1	Set COL2 high	
D1	COL1	0	Clear COL1 low	1
		1	Set COL1 high	
D0	COL0	0	Clear COL0 low	1
		1	Set COL0 high	

**Open-drain output, pullup resistor required.*

Table 23. GPIO Level-Shifter Enable Register (0x3C)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Level shifting disabled	0
		1	Level shift between COL7 and ROW7 enabled; direction controlled by GPIO direction 2 register (0x35)	
D6	COL6	0	Level shifting disabled	0
			Level shift between COL6 and ROW6 enabled; direction controlled by GPIO direction 2 register (0x35)	
D5	COL5	0	Level shifting disabled	0
		1	Level shift between COL5 and ROW5 enabled; direction controlled by GPIO direction 2 register (0x35)	
D4	COL4	0	Level shifting disabled	0
		1	Level shift between COL4 and ROW4 enabled; direction controlled by GPIO direction 2 register (0x35)	
D3	COL3	0	Level shifting disabled	0
		1	Level shift between COL3 and ROW3 enabled; direction controlled by GPIO direction 2 register (0x35)	
D2	COL2	0	Level shifting disabled	0
		1	Level shift between COL2 and ROW2 enabled; direction controlled by GPIO direction 2 register (0x35)	
D1	COL1	0	Level shifting disabled	0
		1	Level shift between COL1 and ROW1 enabled; direction controlled by GPIO direction 2 register (0x35)	
D0	COL0	0	Level shifting disabled	0
		1	Level shift between COL0 and ROW0 enabled; direction controlled by GPIO direction 2 register (0x35)	

Table 24. GPIO Global Configuration Register (0x40)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Reserved	0	—	00
D5	I²C timeout interrupt enable	0	Disabled	0
		1	$\overline{INT}$ is asserted when I²C bus times out. $\overline{INT}$ is deasserted when a read is performed on the I²C timeout flag register (0x48).	
D4	GPIO enable	0	PWM, constant-current circuits, and GPIs are shut down. GPO values depend on their setting. Register 0x31 to 0x5B values are stored and cannot be changed. The entire part is shut down if the key switches are in sleep mode (D7 of register 0x01).	0
		1	Normal GPIO operation. PWM, constant-current circuits, and GPIOs are enabled regardless of key-switch sleep-mode state (see Table 8).	
D3	GPIO reset	0	Normal operation	0
		1	Return all GPIO registers (registers 0x31 to 0x5B) to their POR value. This bit is momentary and resets itself to 0 after the write cycle.	
D[2:0]	Fade-in/out time	000	No fading	000
		XXX	PWM intensity ramps up (down) between the common PWM value and 0% duty cycle in 16 steps over the following time period: D[2:0] = 001 = 256ms D[2:0] = 010 = 512ms D[2:0] = 011 = 1024ms D[2:0] = 100 = 2048ms D[2:0] = 101 = 4096ms D[2:0] = 110/111 = Undefined	

Table 25. GPIO Debounce Configuration Register (0x42)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED			DEBOUNCE TIME				
Power-up default setting Debounce time is 9ms	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Debounce time is 10ms	0	0	0	0	0	0	0	1
Debounce time is 11ms	0	0	0	0	0	0	1	0
Debounce time is 12ms	0	0	0	0	0	0	1	1
⋮								
Debounce time is 37ms	0	0	0	1	1	1	0	0
Debounce time is 38ms	0	0	0	1	1	1	0	1
Debounce time is 39ms	0	0	0	1	1	1	1	0
Debounce time is 40ms	0	0	0	1	1	1	1	1

Table 26. LED Constant-Current Setting Register (0x43)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Reserved	11	Set always as 11	11
D[5:1]	Reserved	00000	—	00000
D0	Constant-current setting	0	Constant current is 20mA	0
		1	Constant current is 10mA	

Table 27. Common PWM Register (0x45)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	COMMON PWM							
Power-up default setting Common PWM ratio is 0/256	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Common PWM ratio is 1/256	0	0	0	0	0	0	0	1
Common PWM ratio is 2/256	0	0	0	0	0	0	1	0
Common PWM ratio is 3/256	0	0	0	0	0	0	1	1
⋮								
Common PWM ratio is 252/256	1	1	1	1	1	1	0	0
Common PWM ratio is 253/256	1	1	1	1	1	1	0	1
Common PWM ratio is 254/256	1	1	1	1	1	1	1	0
Common PWM ratio is **256/256** (100% duty cycle)	1	1	1	1	1	1	1	1

Table 28. I²C Timeout Flag Register (0x48) (Read Only)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:1]	Reserved	0000000	—	0000000
D0	I²C timeout flag	0	No I²C timeout has occurred since last read or POR.	0
		1	I²C timeout has occurred since last read or POR. This bit is reset to zero when a read is performed on this register. I²C timeouts must be enabled for this function to work (see Table 8).	

Table 29. COL4–COL7 Individual PWM Ratio Registers (0x50 to 0x53)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	PORT PWM							
Power-up default setting PORT PWM ratio is 0/256	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
PORT PWM ratio is 1/256	0	0	0	0	0	0	0	1
PORT PWM ratio is 2/256	0	0	0	0	0	0	1	0
PORT PWM ratio is 3/256	0	0	0	0	0	0	1	1
	⋮							
PORT PWM ratio is 252/256	1	1	1	1	1	1	0	0
PORT PWM ratio is 253/256	1	1	1	1	1	1	0	1
PORT PWM ratio is 254/256	1	1	1	1	1	1	1	0
PORT PWM ratio is **256/256** (100% duty cycle)	1	1	1	1	1	1	1	1

Table 30. COL4–COL7 LED Configuration Registers (0x54 to 0x57)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Don't care	00	—	00
D5	Common PWM	0	Port uses individual PWM intensity register to set the PWM ratio	0
		1	Port uses common PWM intensity register to set the PWM ratio	
D[4:2]	Blink period	000	Port does not blink	000
		001	Port blink period is 256ms	
		010	Port blink period is 512ms	
		011	Port blink period is 1024ms	
		100	Port blink period is 2048ms	
		101	Port blink period is 4096ms	
		110/111	Undefined	
D[1:0]	Blink-on time	00	LED is on for 50% of the blink period	00
		01	LED is on for 25% of the blink period	
		10	LED is on for 12.5% of the blink period	
		11	LED is on for 6.25% of the blink period	

Table 31. Interrupt Mask 1 Register (0x58)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	Interrupt is not masked	1
		1	Interrupt is masked	
D6	ROW6	0	Interrupt is not masked	1
		1	Interrupt is masked	
D5	ROW5	0	Interrupt is not masked	1
		1	Interrupt is masked	
D4	ROW4	0	Interrupt is not masked	1
		1	Interrupt is masked	
D3	ROW3	0	Interrupt is not masked	1
		1	Interrupt is masked	
D2	ROW2	0	Interrupt is not masked	1
		1	Interrupt is masked	
D1	ROW1	0	Interrupt is not masked	1
		1	Interrupt is masked	
D0	ROW0	0	Interrupt is not masked	1
		1	Interrupt is masked	

Table 32. Interrupt Mask 2 Register (0x59)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Interrupt is not masked	1
		1	Interrupt is masked	
D6	COL6	0	Interrupt is not masked	1
		1	Interrupt is masked	
D5	COL5	0	Interrupt is not masked	1
		1	Interrupt is masked	
D4	COL4	0	Interrupt is not masked	1
		1	Interrupt is masked	
D3	COL3	0	Interrupt is not masked	1
		1	Interrupt is masked	
D2	COL2	0	Interrupt is not masked	1
		1	Interrupt is masked	
D1	COL1	0	Interrupt is not masked	1
		1	Interrupt is masked	
D0	COL0	0	Interrupt is not masked	1
		1	Interrupt is masked	

Table 33. GPI Trigger Mode 1 Register (0x5A)

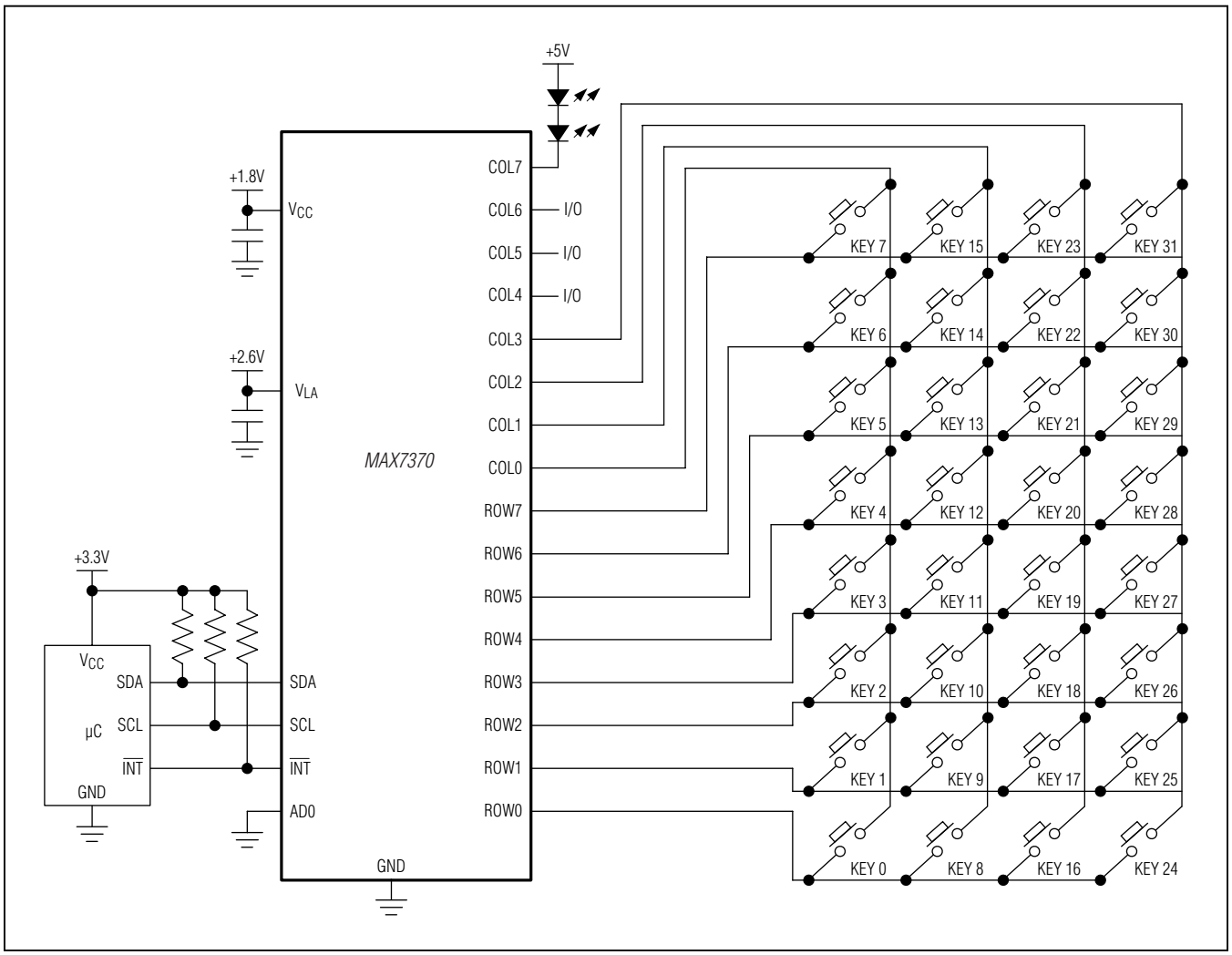
REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	ROW7	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D6	ROW6	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D5	ROW5	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D4	ROW4	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D3	ROW3	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D2	ROW2	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D1	ROW1	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D0	ROW0	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	

Table 34. GPI Trigger Mode 2 Register (0x5B)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	COL7	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D6	COL6	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D5	COL5	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D4	COL4	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D3	COL3	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D2	COL2	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D1	COL1	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D0	COL0	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	

8 x 8 Key-Switch Controller and LED Driver/GPIOs with I²C Interface and High Level of ESD Protection

Typical Application Circuit



8 x 8 Key-Switch Controller and LED Driver/GPIOs with I²C Interface and High Level of ESD Protection

Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape-carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*, available at **www.maximintegrated.com**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T243A3+1	21-0188	90-0122
25 WLP	W252F2+1	21-0453	Refer to Application Note 1891

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7370ETG+	-40°C to +85°C	24 TQFN-EP*
MAX7370EWA+**	-40°C to +85°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed. pad.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	3/12	Updated ESD protection specifications	1, 4, 8, 19
2	5/15	Updated Table 1	8

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

© 2015 Maxim Integrated Maxim Integrated and the Maxim Integrated logo are trademarks of Maxim Integrated Products, Inc.