19-0516; Rev 1; 9/08

EVALUATION KIT AVAILABLE

Dual 300mA Pin-Programmable LDO Linear Regulators

General Description

The MAX8633–MAX8636 offer low-dropout (LDO) voltage and ultra-low-power regulation in a subminiaturized 2mm x 2mm µDFN package. The devices operate from a 2.7V to 5.5V supply and deliver up to 300mA from each output, with a typical dropout voltage of 90mV at 100mA load current. Each device is designed with internal p-channel MOSFET pass transistors to ensure a low-quiescent supply current of 54µA (typical, both LDOs on). Other features include low-noise operation (MAX8634/MAX8636), output current limiting, and thermal shutdown.

The MAX8633 features an open-drain, active-low $\overline{\text{RESET}}$ output to monitor OUT2, eliminating external components and adjustments. The MAX8633 asserts a $\overline{\text{RESET}}$ signal (120ms minimum timeout) when VOUT2 drops below 87% of the nominal output voltage. The MAX8634/MAX8636 feature a noise bypass input to the internal reference for low output noise ($45\mu V_{RMS}$ typ). The MAX8634/MAX8635 provide independent $\overline{\text{SHDN}}$ inputs for disabling the regulators, while the MAX8633/MAX8636 provide a single $\overline{\text{SHDN}}$ input for disabling both regulators.

The MAX8633/MAX8635/MAX8636 have two logic inputs that select one of nine preset output-voltage combinations, eliminating external 1% resistors, as well as inventory burden. The MAX8634 has one logic input to select three output-voltage options.

The MAX8633–MAX8636 are available in an 8-pin, 2mm x 2mm µDFN package for minimizing footprint, and an 8-pin, 3mm x 3mm TDFN package for higher power dissipation. The devices are specified over the extended temperature range (-40°C to +85°C). All packages are lead free.

Applications

Cellular and Cordless Phones

PDAs and Digital Cameras

Small LCD Displays

Notebook Computers

Wireless LAN Cards

Handheld Instruments

Pin Configurations and Selector Guide appear at end of data sheet.

Features

- **Pin-Programmable Output Voltages**
- **300mA Output Current**
- **Low 90mV Dropout at 100mA Load**
- **Open-Drain, Active-Low $\overline{\text{RESET}}$ (MAX8633)**
- **Low 45µV$_{RMS}$ Output Noise (MAX8634/MAX8636)**
- **Low 54µA Quiescent Supply Current**
- **Low < 1µA Maximum Shutdown Current**
- **Output Current Limit**
- **Thermal Shutdown**

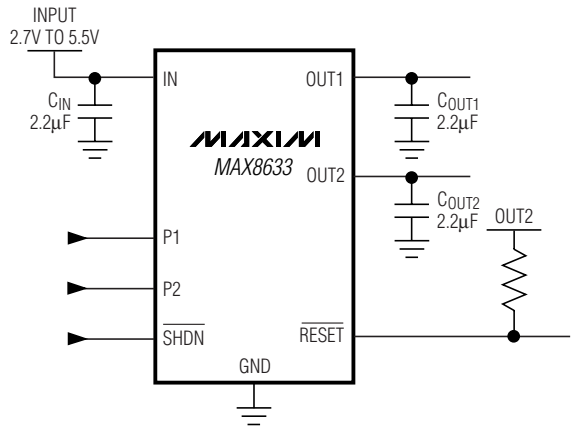
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX8633ELA+	-40°C to +85°C	8 µDFN 2mm x 2mm	AAH
MAX8633ETA+	-40°C to +85°C	8 TDFN 3mm x 3mm	AOQ
MAX8634ELA+	-40°C to +85°C	8 µDFN 2mm x 2mm	AAI

+Denotes a lead-free/RoHS-compliant package.

Ordering Information continued at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual 300mA Pin-Programmable LDO Linear Regulators

ABSOLUTE MAXIMUM RATINGS

(All voltages refer to GND, unless otherwise noted.)
IN .....-0.3V to +6.0V
$\overline{SHDN}$, $\overline{SHDN1}$, $\overline{SHDN2}$, $\overline{RESET}$,
P, P1, P2, BP, OUT1, OUT2 .....-0.3V to (V_{IN} + 0.3V)
Continuous Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin µDFN 2mm x 2mm
(derate 4.8mW/°C above +70°C).....380mW
8-Pin TDFN 3mm x 3mm
(derate 23.8mW/°C above +70°C).....1904mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.7V, $\overline{SHDN}$ = $\overline{SHDN1}$ = $\overline{SHDN2}$ = IN, P = P1 = P2 = GND, C_{IN} = 2.2µF, C_{OUT1} = 2.2µF, C_{OUT2} = 2.2µF, C_{BP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}			2.7		5.5	V
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising; hysteresis = 95mV (typ)		2.15	2.25	2.35	V
Ground Current	I_Q	$I_{OUT_}$ = 0mA			54	75	µA
		$I_{OUT_}$ = 100mA			60		
		$I_{OUT_}$ = 10mA, dropout (Note 2)			60		
Shutdown Supply Current	I_{OFF}	$\overline{SHDN_}$ = GND	T_A = +25°C		0.005	1	µA
			T_A = +85°C		0.01		
OUT1, OUT2							
Output Voltage Accuracy (for Any Output Voltage)		$I_{OUT_}$ = 70mA; T_A = +25°C		-0.7		+0.7	%
		$I_{OUT_}$ = 70mA		-1		+1	
		$I_{OUT_}$ = 0.1mA to 300mA; V_{IN} = ($V_{OUT_}$ + 0.5V) to 5.5V		-1.8		+1.7	
Current Limit	I_{LIM}	OUT_ = 0V		400	500	600	mA
Drop-Out Voltage	V_{IN} - V_{OUT}	$V_{OUT_}$ = 2.8V (MAX8633); $V_{OUT_}$ = 2.85V (MAX8634/MAX8635/MAX8636); $I_{OUT_}$ = 100mA (Note 2)			90	200	mV
Output Noise		f = 10Hz to 100kHz; $I_{OUT_}$ = 10mA	MAX8633 MAX8635		450		$µV_{RMS}$
			MAX8634 MAX8636		45		
Output AC Power-Supply Rejection Ratio	PSRR	$I_{OUT_}$ = 30mA	f < 1kHz		60		dB
			f < 10kHz		55		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, $\overline{SHDN}$ = $\overline{SHDN1}$ = $\overline{SHDN2}$ = IN, P = P1 = P2 = GND, C_{IN} = 2.2µF, C_{OUT1} = 2.2µF, C_{OUT2} = 2.2µF, C_{BP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SHUTDOWN INPUTS ($\overline{SHDN}$, $\overline{SHDN1}$, AND $\overline{SHDN2}$)							
Input Voltage High	V_{IH}	V_{IN} = 2.7V to 5.5V		1.5			V
Input Voltage Low	V_{IL}	V_{IN} = 2.7V to 5.5V				0.5	V
Input Bias Current	$I_{\overline{SHDN}_}$	V_{IN} = 2.7V to 5.5V; $V_{\overline{SHDN}_}$ = GND or IN	T_A = +25°C		0.1	1000	nA
			T_A = +85°C		1		
Turn-On Delay		From $\overline{SHDN}$ = high to 87% of $V_{OUT_}$; $I_{OUT_}$ = 70mA			90		µs
TRI-LEVEL INPUTS (P, P1, P2)							
Termination Resistance to IN or GND for Setting High, Open, and Low States		IN = 2.7 to 5.5V	For high or low state			1	kΩ
			For open state	100			
Input Load Capacitance for Open State		Design guide only				50	pF
$\overline{RESET}$							
$\overline{RESET}$ High Threshold		Percent of nominal OUT2; OUT2 rising		84	87	90	%
$\overline{RESET}$ Threshold Hysteresis		Percent of nominal OUT2; OUT2 falling			4.5		%
$\overline{RESET}$ Output Voltage Low		$I_{\overline{RESET}}$ = 20µA; V_{IN} = 1.0V			10	100	mV
		$I_{\overline{RESET}}$ = 500µA; V_{IN} = 3.7V			5	100	
$\overline{RESET}$ Output High Leakage Current	I_{LEAK}	$V_{\overline{RESET}}$ = V_{IN} = 5.5V	T_A = +25°C		0.1	300	nA
			T_A = +85°C		1		
$\overline{RESET}$ Delay	t_{RP}	From OUT2 rising to $\overline{RESET}$ rising		120	150	180	ms
THERMAL PROTECTION							
Thermal-Shutdown Threshold	T_{SHDN}				+165		°C
Thermal-Shutdown Hysteresis	ΔT_{SHDN}				15		°C

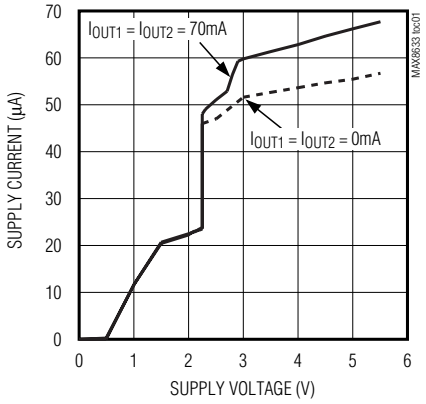
Note 1: All units are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: The dropout voltage is defined as V_{IN} - $V_{OUT_}$ when $V_{OUT_}$ drops by 100mV from $V_{OUT_}$ when measured at V_{IN} = +3.7V.
Note 3: Connect P_ to IN or GND through a resistor less than 1kΩ.

Dual 300mA Pin-Programmable LDO Linear Regulators

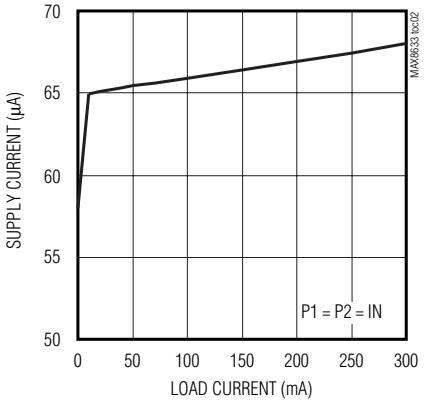
Typical Operating Characteristics

(V_{IN} = 3.8V, P = P1 = P2 = GND, $I_{OUT1, 2}$ = 70mA, C_{OUT1} = 2.2µF, C_{OUT2} = 2.2µF, C_{BP} = 0.01µF, C_{IN} = 2.2µF, and T_A = +25°C, unless otherwise noted.)

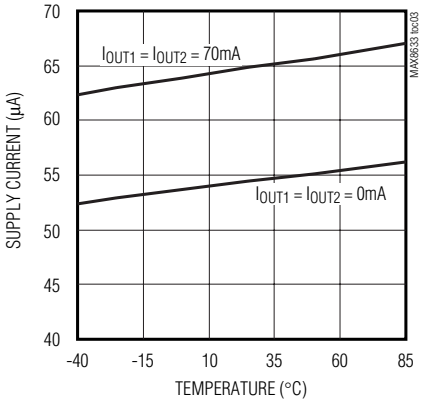
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX8633ELA+)



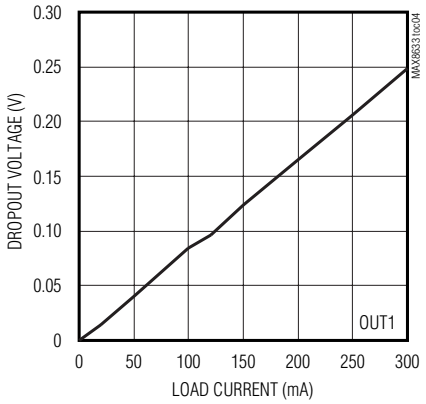
SUPPLY CURRENT vs. LOAD CURRENT (MAX8635ELA+)



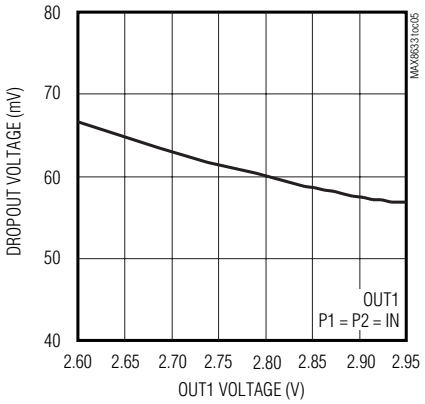
SUPPLY CURRENT vs. TEMPERATURE (MAX8633ELA+)



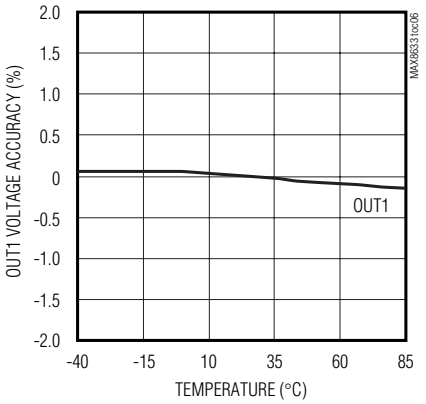
DROPOUT VOLTAGE vs. LOAD CURRENT (MAX8633ELA+)



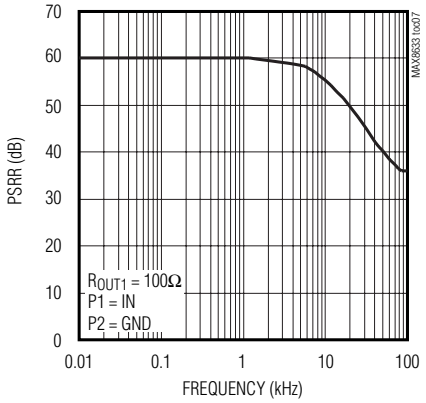
DROPOUT VOLTAGE vs. OUT1 VOLTAGE (MAX8633ELA+)



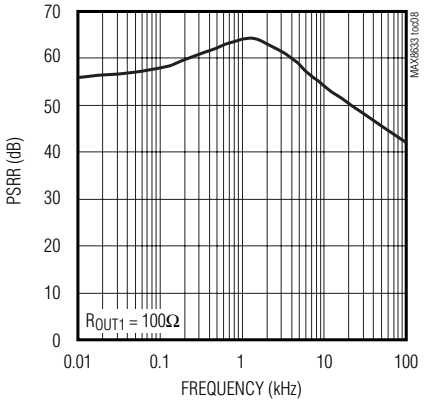
OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE (MAX8633ELA+)



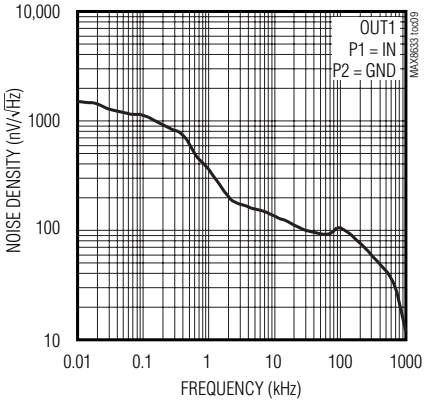
PSRR vs. FREQUENCY (MAX8636ELA+)



CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY (MAX8636ELA+)



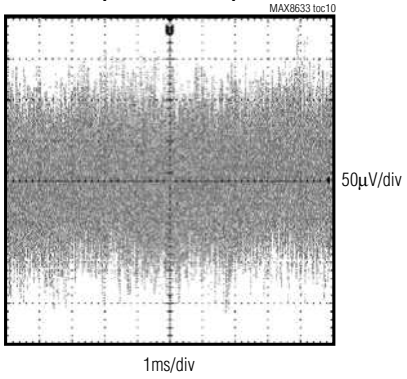
OUTPUT SPECTRAL NOISE DENSITY vs. FREQUENCY (MAX8636ELA+)



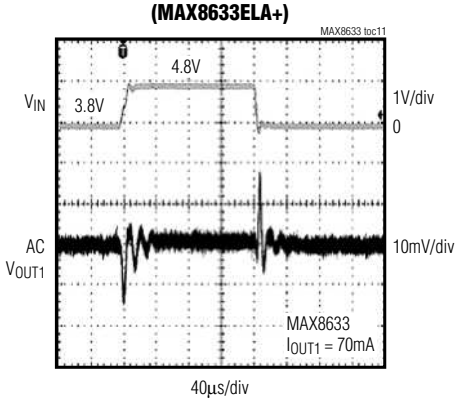
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, P = P1 = P2 = GND, $I_{OUT1, 2}$ = 70mA, C_{OUT1} = 2.2µF, C_{OUT2} = 2.2µF, C_{BP} = 0.01µF, C_{IN} = 2.2µF, and T_A = +25°C, unless otherwise noted.)

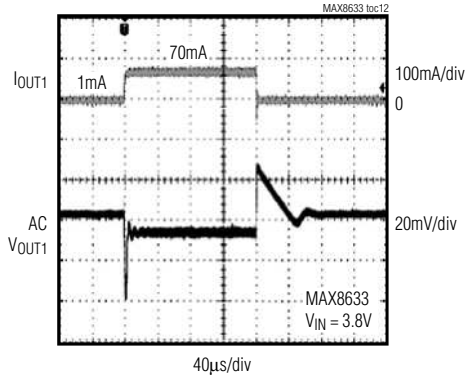
OUTPUT NOISE DC TO 100kHz (MAX8636ELA+)



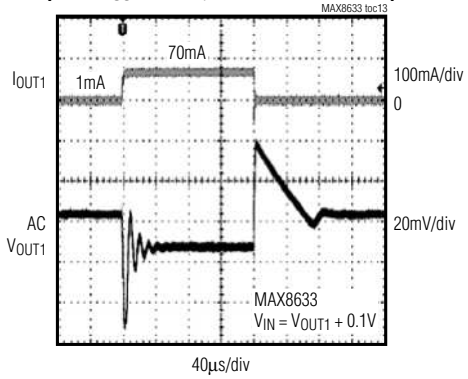
LINE TRANSIENT RESPONSE (MAX8633ELA+)



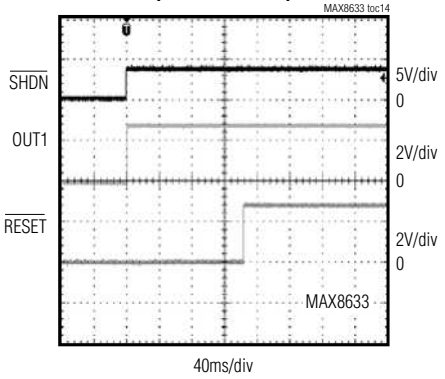
LOAD TRANSIENT (MAX8633ELA+ OUT1 ILOAD = 1mA TO 70mA)



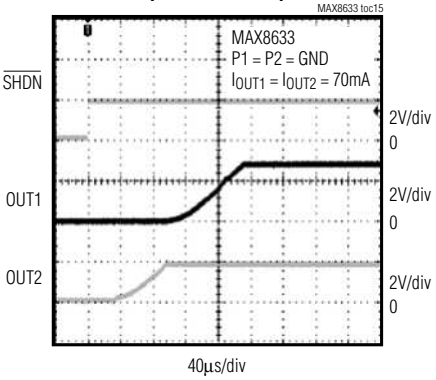
LOAD TRANSIENT NEAR DROPOUT (V_{IN} = V_{OUT} + 0.1V, MAX8633ELA+ OUT1)



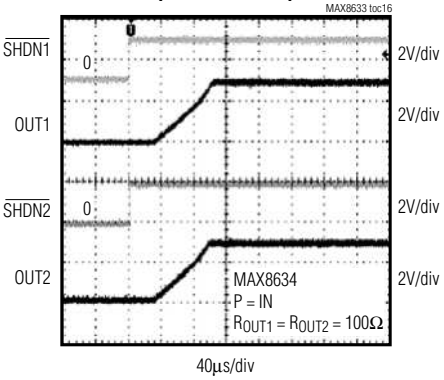
RESET TIMING (MAX8633ELA+)



OUT1 AND OUT2 TURN-ON SEQUENCE (MAX8633ELA+)



EXITING SHUTDOWN (MAX8634ELA+)



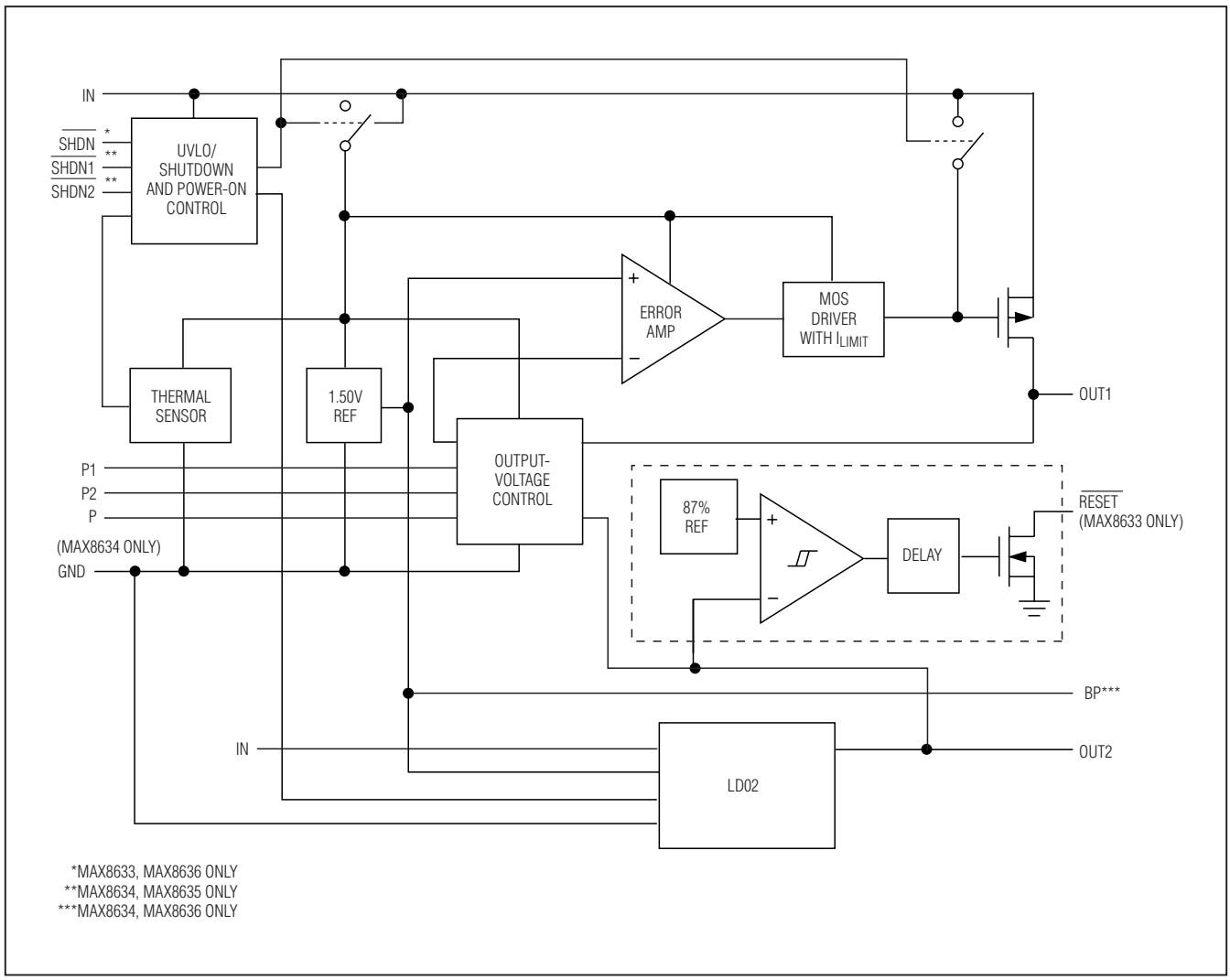
Dual 300mA Pin-Programmable LDO Linear Regulators

Pin Description

PIN				NAME	FUNCTION
MAX8633	MAX8634	MAX8635	MAX8636		
1	1	1	1	IN	Regulator Input. Supply voltage from 2.7V to 5.5V. Bypass IN with a ceramic capacitor of at least 2.2µF to GND (see the *Capacitor Selection and Regulator Stability* section).
2	—	—	2	$\overline{SHDN}$	Shutdown Input, Active Low. Drive $\overline{SHDN}$ logic low to shut down both regulators. Connect $\overline{SHDN}$ to IN or drive logic high for normal operation (see the *Power-On Sequence (MAX8633/Max8636 Only)* section).
—	2	2	—	$\overline{SHDN1}$	LDO1 Shutdown Input, Active Low. Drive $\overline{SHDN1}$ logic low to shut down OUT1. Connect $\overline{SHDN1}$ to IN or drive logic high for normal operation.
—	3	5	—	$\overline{SHDN2}$	LDO2 Shutdown Input, Active Low. Drive $\overline{SHDN2}$ logic low to shut down OUT2. Connect $\overline{SHDN2}$ to IN or drive logic high for normal operation.
3	—	3	3	P2	Programming Input 2. The state of P1 and P2 selects one of nine output-voltage options (see Tables 1, 3).
4	—	4	4	P1	Programming Input 1. The state of P1 and P2 selects one of nine output-voltage options (see Tables 1, 3).
—	4	——	—	P	Programming Input. The state of P selects one of three output-voltage options for the MAX8634 (see Table 2).
5	—	—	—	$\overline{RESET}$	Reset Output, Active Low, Open Drain. $\overline{RESET}$ goes high impedance 120ms (min) after V_{OUT2} rises above 87% of the nominal output voltage. $\overline{RESET}$ is forced logic low when V_{OUT2} is below 82.5% of the nominal output voltage. Connect $\overline{RESET}$ to OUT1, OUT2, or another voltage of V_{IN} or lower with a pullup resistor.
—	5	—	5	BP	Reference Noise Bypass. Bypass BP to GND with a 0.01µF ceramic capacitor to reduce output noise.
6	6	6	6	GND	Ground
7	7	7	7	OUT2	Regulator 2 Output. Guaranteed 300mA output current (see the *Calculating Maximum Output Power* section). Bypass OUT2 with a ceramic capacitor of at least 2.2µF to GND (see the *Capacitor Selection and Regulator Stability* section).
8	8	8	8	OUT1	Regulator 1 Output. Guaranteed 300mA output current (see the *Calculating Maximum Output Power* section). Bypass OUT1 with a ceramic capacitor of at least 2.2µF to GND (see the *Capacitor Selection and Regulator Stability* section).
EP*	EP*	EP*	EP*	EP	Exposed Paddle. Solder the exposed paddle to a large pad or circuit-board ground plane to increase thermal dissipation.

**TDFN package only.*

Functional Diagram



Dual 300mA Pin-Programmable LDO Linear Regulators

Detailed Description

The MAX8633–MAX8636 are low-power, low-quiescent current, low-dropout linear regulators designed primarily for battery-powered applications. Pin-programmable inputs allow easy configuration of OUT1 and OUT2 voltages without external 1% resistors. The devices can supply up to 300mA from each output, provided they do not exceed the maximum package power dissipation.

The MAX8633–MAX8636 regulate OUT1 and OUT2 by using simple control loops incorporating internal 1.50V reference, error amplifiers, p-channel pass transistors, and internal feedback voltage-dividers. Reset circuitry ensures controlled startup and provides undervoltage lockout. The MAX8633–MAX8636 determine output voltages at OUT1 and OUT2 based on the state of P1 and P2 (P for MAX8634) at power-on.

$\overline{\text{RESET}}$ (MAX8633)

The MAX8633 features an integrated reset circuit. $\overline{\text{RESET}}$ is logic-low on power-up and goes high impedance 150ms after OUT2 reaches 87% of its nominal regulation voltage. During power-down or undervoltage conditions, $\overline{\text{RESET}}$ is driven low when OUT2 falls below 82.5% of its nominal regulation voltage.

Output Programming Inputs (P1, P2, P)

Output voltages for OUT1 and OUT2 are determined at power-up by the state of P1 and P2. Programming inputs P1 and P2 eliminate external 1% feedback resistors while providing nine preset output-voltage options (see Table 1 for the MAX8633; see Table 3 for the MAX8635/MAX8636).

The MAX8634 provides three preset output-voltage options with one programming input (see Table 2). The MAX8633–MAX8636 configure output voltages at OUT1 and OUT2 based on the state of P1 and P2 (P for MAX8634) at power-on. Subsequent changes to P, or P1 and P2 do not change the output voltages unless the supply power is cycled, or all $\overline{\text{SHDN}}$ inputs are simultaneously driven low to shut down the device.

Power-On Sequence (MAX8633/MAX8636 Only)

The MAX8633/MAX8636 provide a single shutdown input ($\overline{\text{SHDN}}$) to disable OUT1 and OUT2. During power-on, inrush current is limited by a built-in startup sequence. At power-on, OUT1 is disabled until OUT2 reaches 87% of its regulation voltage, then OUT1 is enabled.

If $\overline{\text{SHDN}}$ is connected to IN and the input voltage drops below the undervoltage-lockout (UVLO) threshold, both LDOs are disabled. The LDOs will not power on again until both of the following conditions are satisfied:

1) The input voltage is raised above the UVLO threshold 2.25V (typ).
2) OUT2 is discharged below 1.2V (typ).

Internal p-Channel Pass Transistor

The MAX8633–MAX8636 feature 0.9Ω p-channel MOSFET pass transistors; p-channel MOSFETs provide several advantages over similar designs using pnp pass transistors, resulting in higher efficiency and longer battery life. MOSFET pass transistors do not require base drive current of pnps, reducing quiescent current

Table 1. Output-Voltage Programming (MAX8633)

P1	P2	OUT1 (V)	(OUT2) (V)
Open	Open	2.80	1.50
Open	GND	2.90	1.50
Open	IN	3.00	1.50
GND	Open	3.00	1.60
GND	GND	2.80	1.80
GND	IN	2.60	1.85
IN	Open	2.90	1.85
IN	GND	2.80	2.60
IN	IN	3.00	2.80

Table 2. Output-Voltage Programming (MAX8634)

P	OUT1 (V)	OUT2 (V)
Open	2.85	2.85
GND	3.00	2.85
IN	2.60	2.60

Table 3. Output-Voltage Programming (MAX8635/MAX8636)

P1	P2	OUT1 (V)	OUT2 (V)
Open	Open	2.80	1.50
Open	GND	2.90	1.50
Open	IN	3.00	1.50
GND	Open	2.60	1.80
GND	GND	2.80	1.80
GND	IN	3.00	2.50
IN	Open	3.00	2.80
IN	GND	2.85	2.85
IN	IN	3.00	3.00

considerably. Under heavy loads, pnp base-drive current becomes large, further reducing efficiency; pnp-based regulators also require considerable current in dropout when the pass transistor saturates. The MAX8633–MAX8636 do not suffer from these problems. With both outputs active, the devices consume only 54µA of quiescent current at no load, and 60µA with 100mA load current for each output (see *Typical Operating Characteristics*). A pnp-based regulator has a high dropout voltage that is independent of the load. The dropout voltage of a p-channel MOSFET is proportional to load current providing for low-dropout voltage at heavy loads and extremely low dropout at lighter loads.

Current Limit

The MAX8633–MAX8636 provide independent current limiting for OUT1 and OUT2. Output current is limited to 500mA (typ) and 400mA (min) for each regulator.

Shutdown ($\overline{SHDN1}$, $\overline{SHDN2}$, $\overline{SHDN}$)

The MAX8634/MAX8635 have independent shutdown control inputs ($\overline{SHDN1}$ and $\overline{SHDN2}$) and the MAX8633/MAX8636 have one shutdown control input ($\overline{SHDN}$) for both outputs. Drive $\overline{SHDN1}$ low to shut down OUT1. Drive $\overline{SHND2}$ low to shut down OUT2. Drive both $\overline{SHDN1}$ and $\overline{SHDN2}$ low to shut down the entire device, reducing supply current to 1µA max. For the MAX8634, drive $\overline{SHDN}$ low to shut down the entire device. Connect $\overline{SHDN1}$, $\overline{SHDN2}$, or $\overline{SHDN}$ to a logic-high or IN to permanently enable the corresponding LDO(s).

Thermal-Overload Protection

Thermal-shutdown circuitry protects the MAX8633–MAX8636 from damage due to excessive junction temperature. The shutdown circuit disables OUT1 and OUT2 when the junction temperature (T_J) exceeds +165°C. Both regulators are reenabled when T_J falls by 15°C.

Low-Noise Operation (MAX8634/MAX8636)

An external 0.01µF bypass capacitor at BP in conjunction with an internal resistor creates a lowpass filter. The MAX8634/MAX8636 exhibit less than 45µV_{RMS} of output voltage noise with C_{BP} = 0.01µF and C_{OUT} = 2.2µF. These values are shown in the Output Noise Spectral Density graph in the *Typical Operating Characteristics* section. If output noise is not critical, omit the BP capacitor to reduce total solution size and cost.

Applications Information

Capacitor Selection and Regulator Stability

Use a ceramic input capacitor of at least 2.2µF and a ceramic output capacitor of at least 2.2µF for each output to ensure stable operation over the entire temperature range. Output capacitors can be reduced to 1µF for load currents less than 150mA. The MAX8633–MAX8636 are optimized for ceramic capacitors and require low equivalent-series resistance (ESR) to achieve the stated specifications for low-output noise and power-supply rejection. To ensure proper operation over the specified temperature range, dielectrics such as X7R or X5R are recommended. If Z5U or Y5V dielectrics are used, it may be necessary to increase the value of the output capacitors to ensure stability at temperatures below -10°C. Tantalum capacitors are not recommended due to their higher ESR.

For loads up to 300mA, or for improved load-transient response, 2.2µF or larger output capacitors can be used.

PSRR and Operation from Sources Other than Batteries

The MAX8633–MAX8636 deliver low-dropout voltages and low-quiescent currents in battery-powered systems. When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors and through passive filtering techniques. Power-supply rejection is 60dB at frequencies below 1kHz (see the Power-Supply Rejection Ratio vs. Frequency in the *Typical Operating Characteristics*).

P1 and P2 (P for MAX8634) External Termination

The pin-programmable inputs (P1 and P2 for MAX8633/MAX8635/MAX8636, P for MAX8634) should be connected to IN, GND, or left open. If P_ inputs are left open, ensure the external capacitance is less than 50pF. If P_ inputs are set high or low, ensure the resistance to IN or GND is less than 1kΩ. The MAX8633–MAX8636 configure output voltages at OUT1 and OUT2 based on the state of P1 and P2 (P for MAX8634) at power-on. Subsequent changes to P, or P1 and P2 do not change the output voltages unless the supply power is cycled, or all $\overline{SHDN}$ inputs are simultaneously driven low to shut down the device.

Load-Transient Considerations

The MAX8633–MAX8636 load-transient response graphs (see *Typical Operating Characteristics*) show two components of the output response: a DC step in the output voltage due to the change in load current, and the transient response. Increase the value and decrease the ESR of the output capacitor to attenuate transient spikes.

Dual 300mA Pin-Programmable LDO Linear Regulators

Input-Output Voltage (Dropout Voltage)

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX8633–MAX8636 use a p-channel MOSFET pass transistor, dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see *Typical Operating Characteristics*).

Calculating Maximum Output Power

The maximum output power of the MAX8633–MAX8636 is limited by the maximum power dissipation of the package. By calculating the power dissipation of the device as a function of the input voltage, output voltages, and output currents, the worst-case power dissipation can be obtained. The worst-case power dissipation should not exceed the package's maximum power rating:

where:

$$P_D = \left(V_{IN(MAX)} - V_{OUT1}\right) \times I_{OUT1} + \left(V_{IN(MAX)} - V_{OUT2}\right) \times I_{OUT2}$$

$V_{IN(MAX)}$ = Maximum input voltage

V_{OUT1} = Output voltage of OUT1

V_{OUT2} = Output voltage of OUT2

I_{OUT1} = Maximum output current of OUT1

I_{OUT2} = Maximum output current of OUT2

P_D must be less than P_{DMAX}, the maximum power dissipation of the package. If P_D is greater than P_{DMAX}, consider using the 8-pin TDFN package.

P_{DMAX} = 380mW for the 8-pin µDFN. Derate by 4.8mW/°C above +70°C.

P_{DMAX} = 1904mW for the 8-pin TDFN. Derate by 23.8mW/°C above +70°C.

PC Board Layout Guidelines

Follow these guidelines for good PC board layout:

- Keep the input and output traces short and wide if possible, especially at the ground terminals.
- Use thick copper PC boards to enhance thermal performance. Connect the exposed paddle of the TDFN package to the ground plane or a large copper pad.
- Place output, input, and bypass capacitors as close as possible to the IC.
- Ensure the noise bypass capacitor and associated PC board traces are routed away from noise sources to ensure low-output voltage noise.

An evaluation kit (MAX8633EVKIT) is available for a layout example to speed designs.

Selector Guide

PART	OUTPUT VOLTAGE OPTIONS	$\overline{SHDN}$ INPUTS	LOW NOISE	$\overline{RESET}$
MAX8633	9	1	—	YES
MAX8634	3	2	YES	—
MAX8635	9	2	—	—
MAX8636	9	1	YES	—

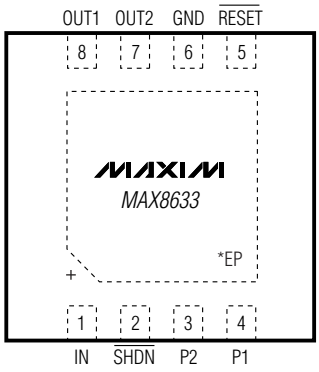
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX8634ETA+	-40°C to +85°C	8 TDFN 3mm x 3mm	AOR
MAX8635ELA+	-40°C to +85°C	8 µDFN 2mm x 2mm	AAJ
MAX8635ETA+	-40°C to +85°C	8 TDFN 3mm x 3mm	AOS
MAX8636ELA+	-40°C to +85°C	8 µDFN 2mm x 2mm	AAK
MAX8636ETA+	-40°C to +85°C	8 TDFN 3mm x 3mm	AOT

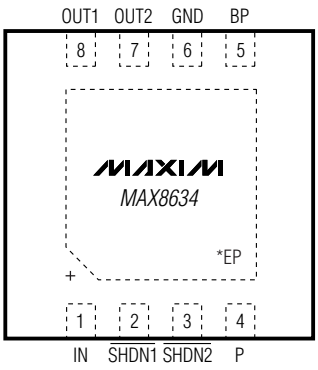
+Denotes a lead-free/RoHS-compliant package.

Pin Configurations

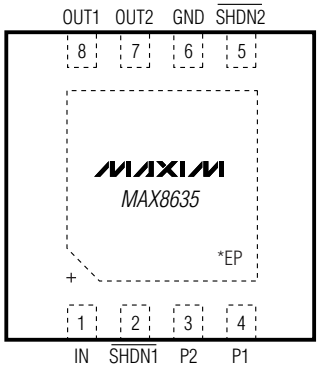
TOP VIEW



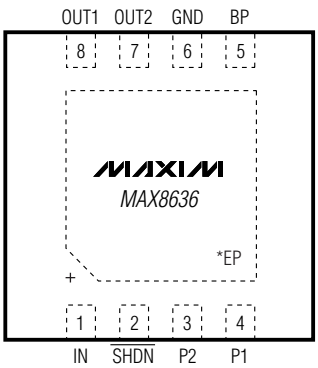
2mm x 2mm µDFN
3mm x 3mm TDFN



2mm x 2mm µDFN
3mm x 3mm TDFN



2mm x 2mm µDFN
3mm x 3mm TDFN



2mm x 2mm µDFN
3mm x 3mm TDFN

*EP = EXPOSED PADDLE. CONNECT EXPOSED PADDLE TO GND (TDFN ONLY).

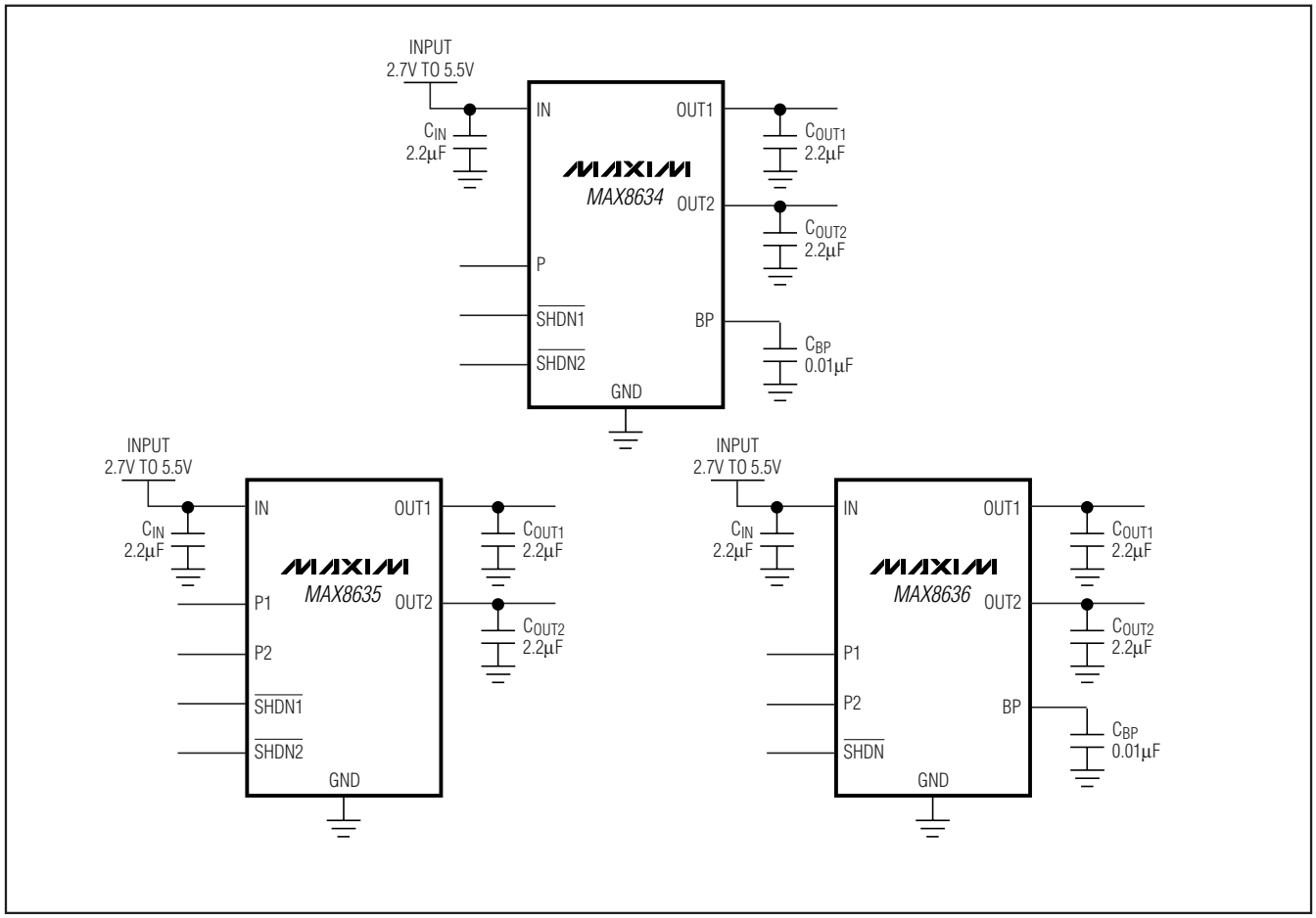
Chip Information

PROCESS: BiCMOS

CONNECT EXPOSED PADDLE TO GND.

Dual 300mA Pin-Programmable LDO Linear Regulators

Typical Operating Circuits (continued)



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TDFN	T833-2	**21-0137**
8 µDFN	L822-1	**21-0164**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/06	Initial release	—
1	9/08	Added LDO $\overline{\text{SHDN}}$ restart conditions	8

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