19-3319; Rev 2; 9/05

EVALUATION KIT AVAILABLE

Dynamically Adjustable 6-Bit VID Step-Down Controller

General Description

The MAX8720 step-down controller is intended for core CPU DC-DC converters in notebook computers. It features a dynamically adjustable output, ultra-fast transient response, high DC accuracy, and the high efficiency needed for leading-edge CPU core power supplies. Maxim's proprietary Quick-PWM™ quick-response, constant-on-time, PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The output voltage can be dynamically adjusted through the 6-bit digital-to-analog converter (DAC) over a 0.275V to 1.850V range in 25mV steps. The MAX8720 has independent four-level logic inputs for setting the suspend voltage (S0-S1). Precision slew-rate control provides "just-in-time" arrival at the new DAC setting, minimizing surge currents to and from the battery. The internal DAC of the MAX8720 is synchronized to the slew-rate clock for improved operation under aggressive power management of newer chipsets and operating systems that can make incomplete mode transitions. Remote feedback and ground-sense inputs allow easy compensation for IR drops in PC board traces.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX8720 is available in a 28-pin QSOP or 36-pin 6mm x 6mm thin QFN package.

Applications

CPU Core Supply Converters

GPU Core Supply Converters

Notebook and Subnotebook Computers

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Pin Configurations appear at end of data sheet.

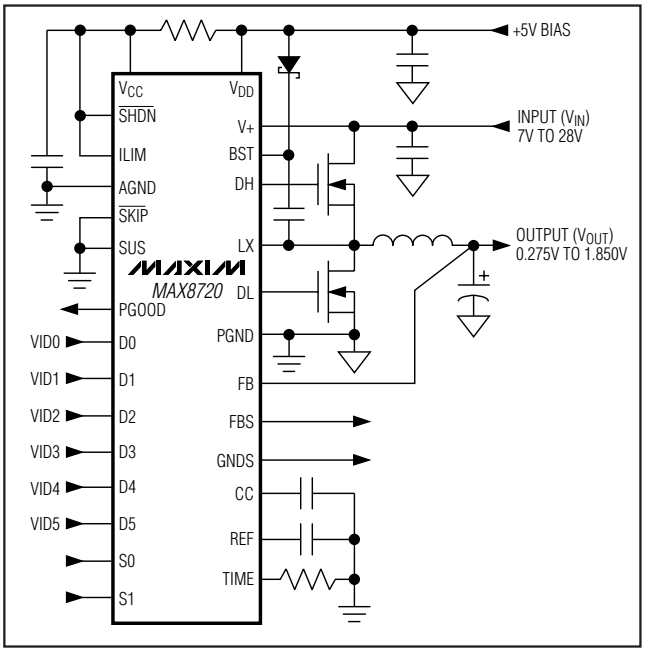
Features

- **Quick-PWM Architecture**
- **±1% V_{OUT} Accuracy Over Line and Load**
- **6-Bit On-Board DAC with Input Muxes**
- **Precision-Adjustable V_{OUT} Slew Control**
- **0.275V to 1.850V Output Adjust Range**
- **Remote Feedback and Ground Sense**
- **Supports Voltage-Positioned Applications**
- **2V to 28V Battery Input Range**
- **200kHz/300kHz/550kHz/1000kHz Switching Frequency**
- **Over/Undervoltage Protection**
- **Drives Large Synchronous-Rectifier FETs**
- **800µA (typ) I_{CC} Supply Current**
- **10µA (typ) Shutdown Supply Current**
- **2V ±0.75% Reference Output**
- **PGOOD Blanking During Transition**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8720EEI	-40°C to +85°C	28 QSOP
MAX8720ETX	-40°C to +85°C	36 Thin QFN 6mm x 6mm

Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to AGND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
AGND to PGND .....-0.3V to +0.3V
V+ to PGND .....-0.3V to +30V
$\overline{SHDN}$ to AGND .....-0.3V to +16V
D0–D5, PGOOD, SUS, $\overline{SKIP}$ to AGND .....-0.3V to +6V
FB, FBS, GNDS to AGND .....-0.3V to (V_{CC} + 0.3V)
CC, ILIM, REF, TIME to AGND .....-0.3V to (V_{CC} + 0.3V)
S0, S1, TON to AGND .....-0.3V to (V_{CC} + 0.3V)
BST to PGND .....-0.3V to +36V
LX to BST .....-6V to +0.3V
DH to LX .....-0.3V to (BST + 0.3V)
DL to PGND .....-0.3V to (V_{DD} + 0.3V)
REF Short Circuit to AGND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C) 860mW
36-Pin TQFN (derate 26.3mW/°C above +70°C) 2105mW
Operating Temperature
Extended Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: For the MAX8720EEI, AGND and PGND refer to a single pin designated GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{DD} = V_{CC} = +5V, V_{OUT} = 1.25V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 0.9V to 1.85V	-1		+1	%
			DAC codes from 0.45V to 0.875V	-10		+10	mV
			DAC codes from 0.275V to 0.425V	-18		+18	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
Remote-Sense Voltage Error		FB to FBS or AGND to GNDS = 0 to 25mV			3		mV
FBS Input Bias Current		FB, FBS		-0.2		+0.2	µA
GNDS Input Bias Current		GNDS		-1		+1	µA
FB Input Resistance				115	180	265	kΩ
TIME Frequency Accuracy		150kHz, R_{TIME} = 120kΩ		-8		+8	%
		818kHz, R_{TIME} = 22kΩ		-12		+12	
		38kHz, R_{TIME} = 470kΩ		-12		+12	
On-Time (Note 2)	t_{ON}	V+ = 5V, FB = 1.25V, TON = GND (1000kHz)		230	260	290	ns
		V+ = 12V, FB = 1.25V	TON = REF (550kHz)	165	190	215	
			TON = open (300kHz)	320	355	390	
			TON = V_{CC} (200kHz)	465	515	565	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{DD} = V_{CC} = +5V, V_{OUT} = 1.25V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Off-Time (Note 2)	$t_{OFF(MIN)}$	TON = V_{CC}, open, or REF (200kHz, 300kHz, or 550kHz)			400	500	ns
		TON = GND (1000kHz)			300	375	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above their regulation points			700	1200	µA
Quiescent Supply Current (V_{DD})	I_{DD}	FB forced above their regulation points			<1	5	µA
Quiescent Battery Supply Current (V+)	I_+				25	40	µA
Shutdown Supply Current (V_{CC})	I_{CC}	$\overline{SHDN}$ = GND			10	25	µA
Shutdown Supply Current (V_{DD})	I_{DD}	$\overline{SHDN}$ = GND			<1	5	µA
Shutdown Battery Supply Current (V+)	I_+	$\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0V or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	T_A = +25°C to +85°C	1.985	2.00	2.015	V
			T_A = 0°C to +85°C	1.98	2.00	2.02	
Reference Load Regulation	ΔV_{REF}	I_{REF} = 0 to 50µA				0.01	V
REF Sink Current		REF in regulation		10			µA
FAULT DETECTION							
V_{CC} Undervoltage-Lockout Threshold		Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
Output Overvoltage Trip Threshold				2.20	2.25	2.30	V
Output Overvoltage Fault-Propagation Delay	t_{OVP}	FB forced 2% above regulation			10		µs
Output Undervoltage-Protection Trip Threshold		With respect to unloaded output voltage		65	70	75	%
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FB forced 2% below trip threshold			10		µs
PGOOD Transition Blanking Time		After X = Y, clock speed set by R_{TIME}			8		clk
PGOOD Lower Trip Threshold		Measured at FB with respect to unloaded output voltage, hysteresis = 1%		-17	-15	-13	%
PGOOD Upper Trip Threshold		Measured at FB with respect to unloaded output voltage, hysteresis = 1%		+13	+15	+17	%
PGOOD Propagation Delay	t_{PGOOD}	Falling edge, 50mV overdrive			10		µs
PGOOD Output Low Voltage		I_{SINK} = 4mA				0.4	V
PGOOD Leakage Current	I_{PGOOD}	High state, PGOOD forced to 5.5V				1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 10°C			+150		°C
CURRENT LIMIT							
ILIM Adjustment Range				0.5		V_{REF}	V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{DD} = V_{CC} = +5V, V_{OUT} = 1.25V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Limit Threshold (Fixed)	V_{LIMIT}	V_{PGND} - V_{LX}, ILIM = V_{CC}	T_A = +25°C to +85°C	90	100	110	mV
			T_A = 0°C to +85°C	85		115	
Current-Limit Threshold (Adjustable)	V_{LIMIT}	V_{PGND} - V_{LX}	V_{ILIM} = 2.00V	165	200	230	mV
			V_{ILIM} = 0.50V	35	50	65	
Current-Limit Threshold (Negative)	V_{NEG}	V_{LX} - V_{PGND}, $\overline{SKIP}$ = ILIM = V_{CC},		-140	-117	-90	mV
		V_{LX} - V_{PGND}, $\overline{SKIP}$ = V_{CC}, adjustable mode, percent of current limit			-117		%
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{PGND} - V_{LX}, $\overline{SKIP}$ = GND			4		mV
Current-Limit Default Switchover Threshold				3	V_{CC} - 1	V_{CC} - 0.4	V
ILIM Leakage Current						0.1	µA
GATE DRIVERS							
DH Gate-Driver On-Resistance (Note 3)	R_{DH}	BST-LX forced to 5V	QSOP package		1.0	3.5	Ω
			TQFN package		1.0	4.5	
DL Gate-Driver On-Resistance (Note 3)	R_{DL}	DL, high state	QSOP package		1.0	3.5	Ω
			TQFN package		1.0	4.0	
		DL, low state			0.4	1.0	
DH Gate-Driver Source/Sink Current	I_{DH}	DH forced to 2.5V, BST-LX forced to 5V			2		A
DL Gate-Driver Source Current	I_{DL} (SOURCE)	DL forced to 2.5V			1.6		A
DL Gate-Driver Sink Current	I_{DL} (SINK)	DL forced to 2.5V			4		A
Dead Time	t_{DEAD}	DL rising			35		ns
		DH rising			26		
INPUTS AND OUTPUTS							
$\overline{SHDN}$ Input Level	$V_{\overline{SHDN}}$	Logic high		2.4			V
		Logic low				0.4	
		No-fault mode		12		15	
Logic Input High Voltage	V_{IH}	D0–D5, $\overline{SKIP}$, SUS		2.4			V
Logic Input Low Voltage	V_{IL}	D0–D5, $\overline{SKIP}$, SUS				0.8	V
Logic Input Current		D0–D5, $\overline{SKIP}$, SUS		-1		+1	µA
Four-Level Input Logic		TON, S0, S1	High	V_{CC} - 0.2			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			GND			0.5	
Input Leakage Current		$\overline{SHDN}$, TON, S0, S1 forced to V_{CC} or GND		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ =15V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{DD} = V_{CC} = +5V, V_{OUT} = 1.25V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery Voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 0.9V to 1.85V	-1		+1	%
			DAC codes from 0.45V to 0.875V	-15		+15	mV
			DAC codes from 0.275V to 0.425V	-18		+18	
FB Input Resistance				115		265	kΩ
TIME Frequency Accuracy		150kHz, R_{TIME} = 120kΩ		-8		+8	%
		818kHz, R_{TIME} = 22kΩ		-12		+12	
		38kHz, R_{TIME} = 470kΩ		-12		+12	
On-Time (Note 2)	t_{ON}	V+ = 5V, FB = 1.25V, TON = GND (1000kHz)		230		290	ns
		V+ = 12V, FB = 1.25V	TON = REF (550kHz)	165		215	
			TON = open (300kHz)	320		390	
			TON = V_{CC} (200kHz)	465		565	
Minimum Off-Time (Note 2)	$t_{OFF(MIN)}$	TON = V_{CC}, open, or REF (200kHz, 300kHz, or 550kHz)				500	ns
		TON = GND (1000kHz)				375	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above their regulation points				1300	µA
Quiescent Supply Current (V_{DD})	I_{DD}	FB forced above their regulation points				5	µA
Quiescent Battery Supply Current (V+)	I_+					40	µA
Shutdown Supply Current (V_{CC})	I_{CC}	$\overline{SHDN}$ = GND				25	µA
Shutdown Supply Current (V_{DD})	I_{DD}	$\overline{SHDN}$ = GND				5	µA
Shutdown Battery Supply Current (V+)	I_+	$\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0V or 5V				5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no REF load		1.98		2.02	V
FAULT DETECTION							
V_{CC} Undervoltage-Lockout Threshold		Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V

Dynamically Adjustable 6-Bit VID Step-Down Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ =15V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{DD} = V_{CC} = +5V, V_{OUT} = 1.25V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Overvoltage Trip Threshold				2.20		2.30	V
Output Undervoltage-Protection Trip Threshold		With respect to unloaded output voltage		65		75	%
PGOOD Lower Trip Threshold		Measured at FB with respect to unloaded output voltage, hysteresis = 1%		-17.5		-12.5	%
PGOOD Upper Trip Threshold		Measured at FB with respect to unloaded output voltage, hysteresis = 1%		+12.5		+17.5	%
CURRENT LIMIT							
ILIM Adjustment Range				0.5		V_{REF}	V
Current-Limit Threshold (Fixed)	V_{LIMIT}	V_{PGND} - V_{LX}, ILIM = V_{CC}		80		115	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	V_{PGND} - V_{LX}	V_{ILIM} = 2.00V	160		240	mV
			V_{ILIM} = 0.50V	33		65	
Current-Limit Threshold (Negative)	V_{NEG}	V_{LX} - V_{PGND}, $\overline{SKIP}$ = ILIM = V_{CC}		-140		-85	mV
GATE DRIVERS							
DH Gate-Driver On-Resistance (Note 3)	R_{DH}	BST-LX forced to 5V	QSOP package			3.5	Ω
			TQFN package			4.5	
DL Gate-Driver On-Resistance (Note 3)	R_{DL}	DL, high state	QSOP package			3.5	Ω
			TQFN package			4.0	
		DL, low state				1.0	
INPUTS AND OUTPUTS							
$\overline{SHDN}$ Input Level	$V_{\overline{SHDN}}$	Logic high		2.4			V
		Logic low				0.4	
		No-fault mode		12		15	
Logic Input High Voltage	V_{IH}	D0–D5, $\overline{SKIP}$, SUS		2.4			V
Logic Input Low Voltage	V_{IL}	D0–D5, $\overline{SKIP}$, SUS				0.8	V
Four-Level Input Logic		TON, S0, S1	High	V_{CC} - 0.2			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			GND			0.5	

Note 2: On-time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

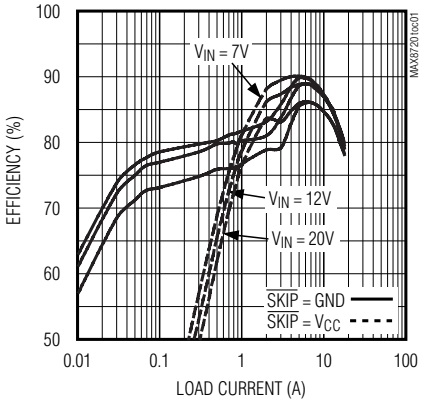
Note 3: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the thin QFN package. The QSOP and thin QFN package contain the same die, and the thin QFN package imposes no additional resistance in the circuit.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

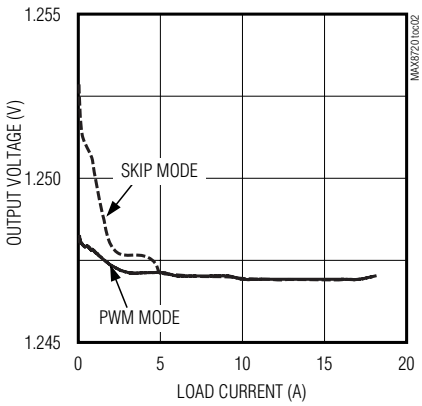
Typical Operating Characteristics

(MAX8720 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, TON = open, T_A = +25°C, unless otherwise noted.)

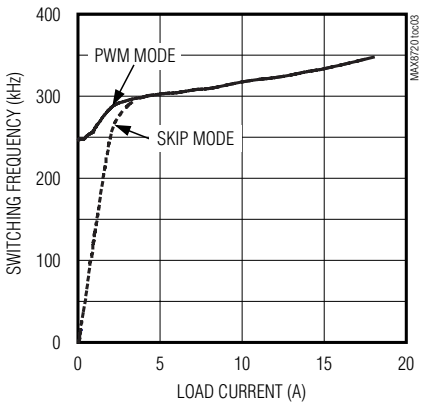
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.25V)



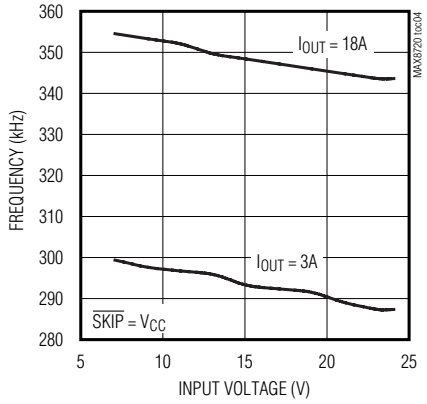
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.25V)



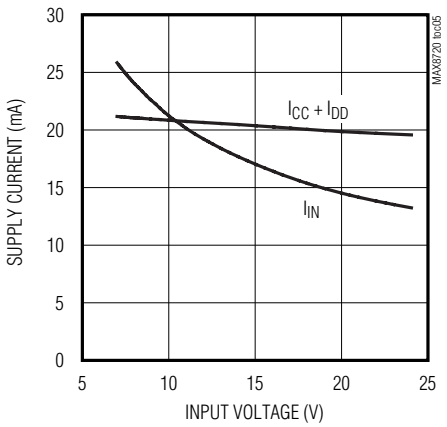
SWITCHING FREQUENCY vs. LOAD CURRENT



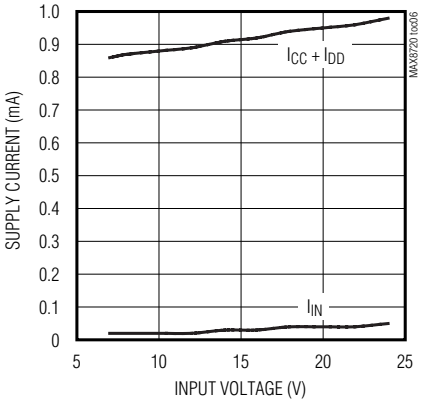
SWITCHING FREQUENCY vs. INPUT VOLTAGE



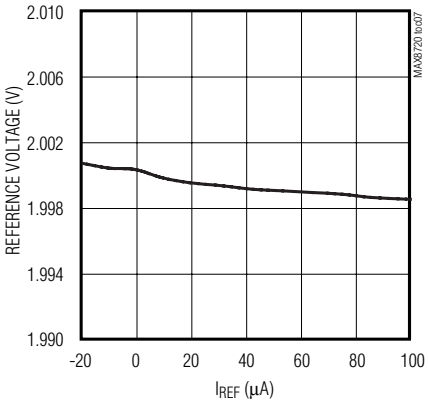
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PWM MODE)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



REFERENCE LOAD REGULATION

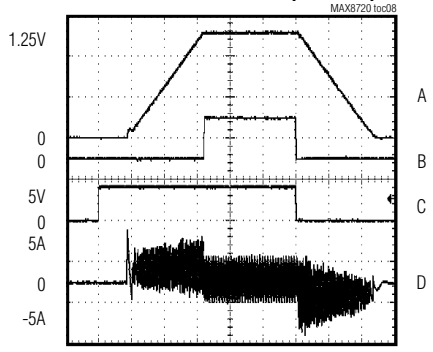


Dynamically Adjustable 6-Bit VID Step-Down Controller

Typical Operating Characteristics (continued)

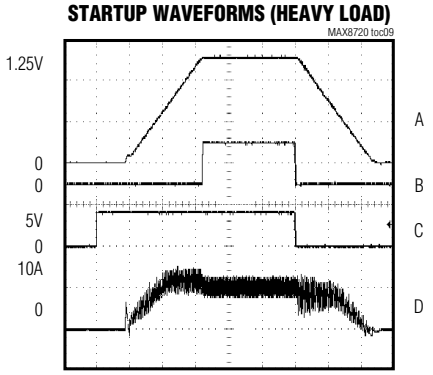
(MAX8720 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, TON = open, T_A = +25°C, unless otherwise noted.)

STARTUP WAVEFORMS (NO LOAD)



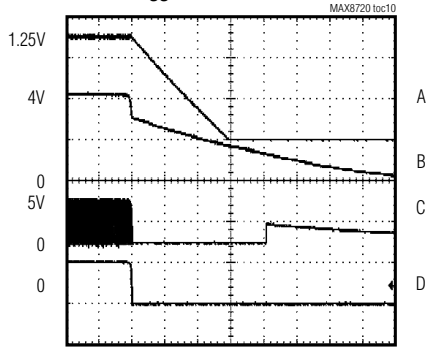
I_{OUT} = NO LOAD
A = V_{OUT}, 500mV/div C = $\overline{SHDN}$, 5V/div
B = PGOOD, 5V/div D = INDUCTOR CURRENT, 5A/div

STARTUP WAVEFORMS (HEAVY LOAD)



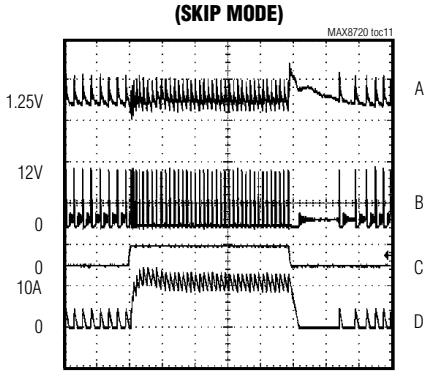
I_{OUT} = 10A
A = V_{OUT}, 500mV/div C = $\overline{SHDN}$, 5V/div
B = PGOOD, 5V/div D = INDUCTOR CURRENT, 10A/div

V_{CC} UVLO WAVEFORM



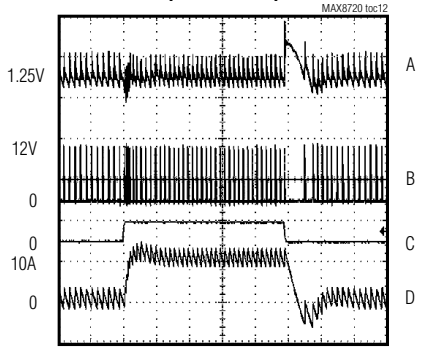
I_{OUT} = 1A
A = V_{OUT}, 500mV/div C = DL, 5V/div
B = V_{CC}, 2V/div D = PGOOD, 5V/div

LOAD TRANSIENT (SKIP MODE)



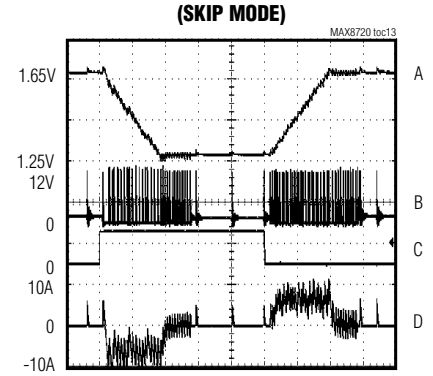
$\overline{SKIP}$ = GND, I_{OUT} = 1A TO 11A TO 1A
A = V_{OUT}, 50mV/div C = CONTROL, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

LOAD TRANSIENT (PWM MODE)



$\overline{SKIP}$ = V_{CC}, I_{OUT} = 1A TO 11A TO 1A
A = V_{OUT}, 50mV/div C = CONTROL, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

DYNAMIC OUTPUT VOLTAGE TRANSITION (SKIP MODE)

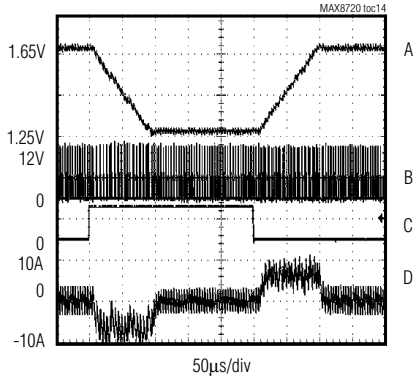


$\overline{SKIP}$ = GND, I_{OUT} = 0.2A
A = V_{OUT}, 200mV/div C = D4, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

Typical Operating Characteristics (continued)

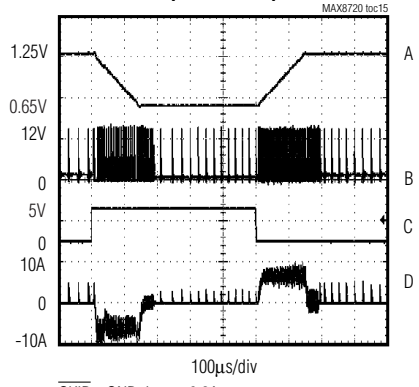
(MAX8720 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, TON = open, T_A = +25°C, unless otherwise noted.)

DYNAMIC OUTPUT VOLTAGE TRANSITION (PWM MODE)



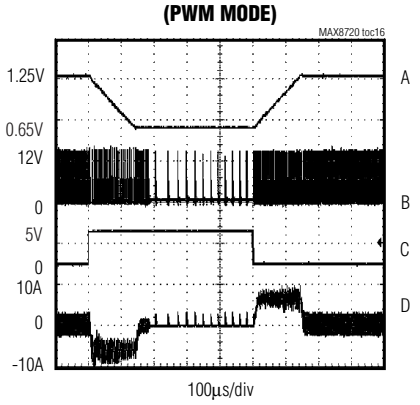
$\overline{SKIP}$ = V_{CC}, I_{OUT} = 0.2A
A = V_{OUT}, 200mV/div C = D4, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

SUSPEND TRANSITION (SKIP MODE)



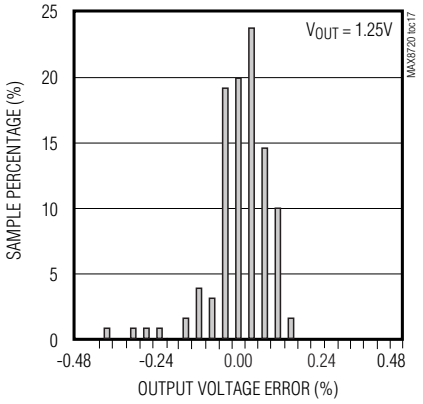
$\overline{SKIP}$ = GND, I_{OUT} = 0.2A
A = V_{OUT}, 500mV/div C = D4, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

SUSPEND TRANSITION (PWM MODE)

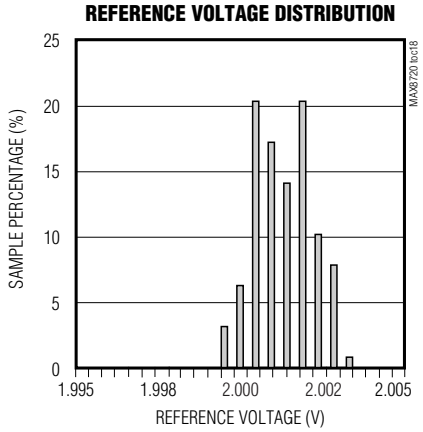


$\overline{SKIP}$ = V_{CC}, I_{OUT} = 0.2A
A = V_{OUT}, 500mV/div C = D4, 5V/div
B = LX, 10V/div D = INDUCTOR CURRENT, 10A/div

OUTPUT VOLTAGE DISTRIBUTION



REFERENCE VOLTAGE DISTRIBUTION



Dynamically Adjustable 6-Bit VID Step-Down Controller

Pin Description

PIN		NAME	FUNCTION
28 QSOP	36 THIN QFN		
1	33	V+	Battery Voltage-Sense Connection. Connect V+ to input power source. V+ is used only for PWM one-shot timing. DH on-time is inversely proportional to input voltage over a 2V to 28V range.
2	34	$\overline{SHDN}$	Shutdown Control Input. Connect $\overline{SHDN}$ to V_{CC} for normal operation. Connect $\overline{SHDN}$ to GND to put the controller into its shutdown state. Forcing $\overline{SHDN}$ to 12V to 15V disables both the overvoltage-protection and undervoltage-protection circuits and clears the fault latch. Do not connect $\overline{SHDN}$ to >15V.
3	35	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 470kΩ to 22kΩ resistor sets the clock from 38kHz to 818kHz, f_{SLEW} = 150kHz x 120kΩ / R_{TIME}. To reduce inrush current, f_{SLEW} = 150kHz x 120kΩ / 4 x R_{TIME} during power-up and power-down transient.
4	1	FB	Fast Feedback Input. Connect FB to the junction of the external inductor and output-capacitor node (Figure 1).
5	2	FBS	Feedback Remote-Sense Input. For nonvoltage-positioned circuits, connect FBS to V_{OUT} directly at the load. FBS internally connects to the integrator that fine tunes the DC output voltage. For voltage-positioned circuits, connect FBS directly to FB near the IC to disable the FBS remote-sense integrator amplifier. To disable all three integrator amplifiers, connect FBS to V_{CC}.
6	3	CC	Integrator Capacitor Connection. Connect a 47pF to 1000pF (47pF typ) capacitor from CC to AGND to set the integration time constant. CC can be left open if FBS is connected to V_{CC}.
7, 8	4, 5	S0, S1	Suspend-Mode Voltage-Select Input. S0 and S1 are four-level digital inputs that select the suspend-mode VID code for the suspend-mode multiplexer inputs. If SUS is high, the suspend-mode VID code is delivered to the DAC.
9	7	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 10Ω resistor. Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
10	8	TON	On-Time Selection Control Input. This is a four-level input that sets the K-factor to determine DH on-time. Connect TON to the following pins for the indicated operation: GND = 1000kHz REF = 550kHz Open = 300kHz V_{CC} = 200kHz
11	9	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.22µF or greater ceramic capacitor. The reference can source up to 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error.
12	10	ILIM	Current-Limit Adjustment. The PGND–LX current-limit threshold defaults to 100mV if ILIM is connected to V_{CC}. In adjustable mode, the current-limit threshold voltage is 1/10th the voltage seen at ILIM over a 0.5V to 3.0V range. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V. Connect ILIM to REF for a fixed 200mV threshold.

Pin Description (continued)

PIN		NAME	FUNCTION
28 QSOP	36 THIN QFN		
13	11	GNDS	Ground Remote-Sense Input. For nonvoltage-positioned circuits, connect GNDS to ground directly at the load. GNDS internally connects to the integrator that fine tunes the output voltage. The output voltage rises by an amount of GNDS - AGND. For voltage-positioned circuits, increase the output voltage by biasing GNDS with a resistor-divider from REF to AGND.
14	12	PGOOD	Open-Drain Power-Good Output. PGOOD is normally high when the output is in regulation. If V_{FB} is not within a ±15% window of the DAC setting, PGOOD is asserted low. During DAC code transitions, PGOOD is forced high for an additional 8 clocks after the slew-rate controller finishes the transition. PGOOD is low during shutdown. PGOOD upper threshold is blanked whenever the MAX8720 is in pulse-skipping mode ($\overline{SKIP}$ = GND or SUS = high).
15	—	GND	Analog and Power Ground. Also connects to the current-limit comparator.
16	16, 17	DL	Low-Side Gate-Driver Output. DL swings from PGND to V_{DD}.
17	19	V_{DD}	Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to power ground with a 1µF or greater ceramic capacitor.
18	20	SUS	Suspend-Mode Control Input. When SUS is high, the suspend-mode VID code, as programmed by S0 and S1, is delivered to the DAC. Connect SUS to GND if the suspend-mode multiplexer is not used. PGOOD upper threshold is blanked when SUS is high.
19	21	D0	DAC Code Inputs. D0 is the LSB and D5 is the MSB for the 6-bit DAC.
20	22	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect $\overline{SKIP}$ to V_{CC} for low-noise, forced-PWM mode, or connect $\overline{SKIP}$ to GND to enable pulse-skipping operation. PGOOD upper threshold is blanked when $\overline{SKIP}$ = GND.
21	23	D5	DAC Code Inputs. D0 is the LSB and D5 is the MSB for the 6-bit DAC.
22	24	D4	
23	25	D3	
24	26	D2	
25	27	D1	
26	29	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode as shown in Figure 1. An optional resistor in series with BST allows the DH pullup current to be adjusted.
27	31	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. It also connects to the current-limit comparator and the skip-mode zero-crossing comparator.
28	32	DH	High-Side Gate-Driver Output. DH swings from LX to BST.
—	13	AGND	Analog Ground. Connect the backside pad to AGND.
—	14,15	PGND	Power Ground. Also connects to the current-limit comparator.
—	6, 18, 28, 30, 36	N.C.	Not internally connected.

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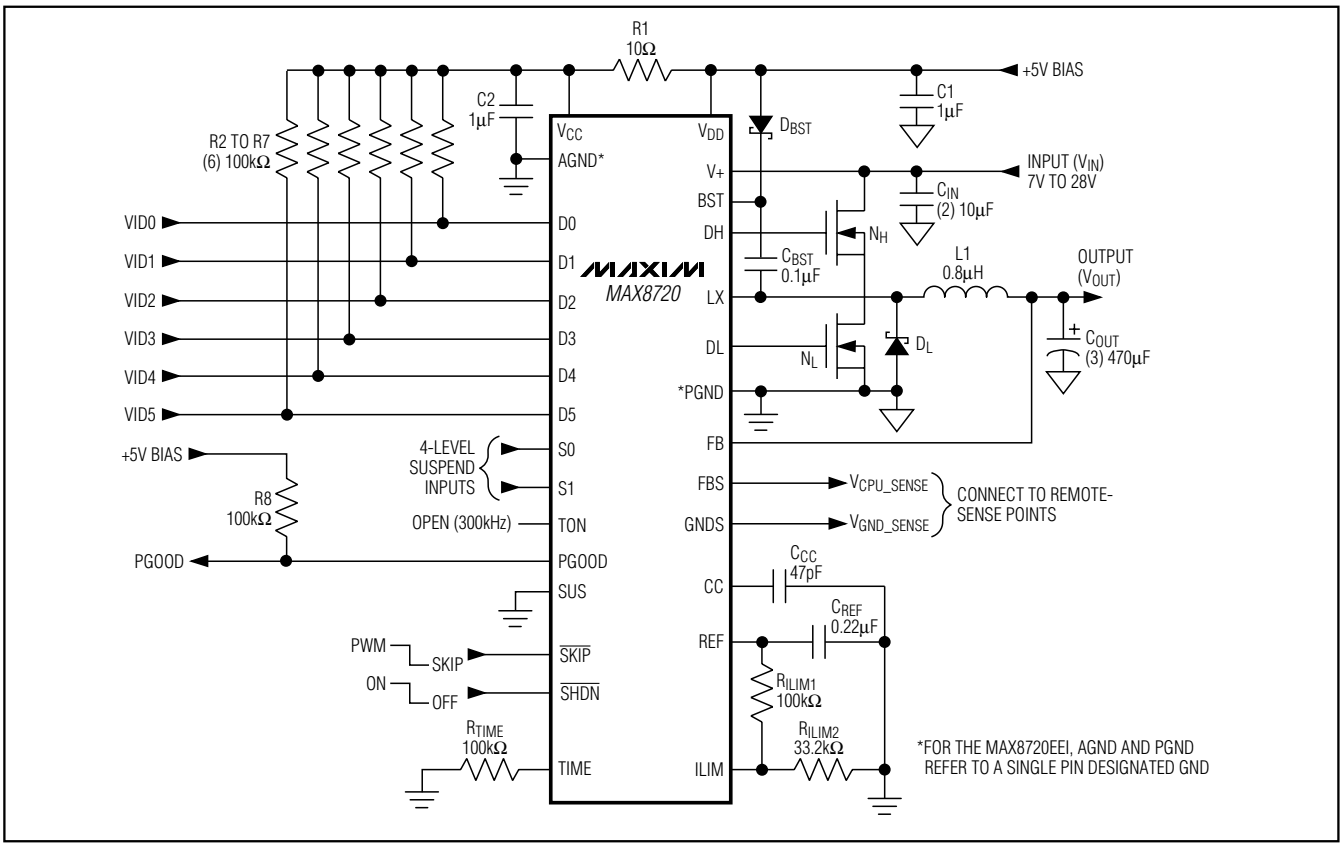


Figure 1. MAX8720 Standard Application Circuit

Detailed Description

The MAX8720 is a constant-on-time, quick-PWM controller with 6-bit VID inputs to dynamically set the output voltage from 0.275V to 1.85V. The MAX8720 standard application circuit (Figure 1) generates a low-voltage 1.25V/15A output typical of low-power CPU and GPU core supplies in a notebook computer. The input supply range is 7V to 24V. See Table 1 for component selections and Table 2 for component manufacturers.

5V Bias Supply (V_{CC} and V_{DD})

The MAX8720 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient, 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 4mA \text{ to } 40mA \text{ (typ)}$$

where I_{CC} is 800µA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V+ and V_{DD} can be connected together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Reference (REF)

The 2V reference is accurate to ±0.75% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF or greater ceramic capacitor. The reference sources up to 100µA and sinks 10µA to support external loads. Loading the reference reduces the output voltages slightly, because of the reference load regulation error.

Table 1. Component Selection for Standard Applications

COMPONENT	15A/300kHz
Input Voltage	V_{IN} = 7V to 24V
Output Voltage	V_{OUT} = 1.25V
C_{IN} Input Capacitor	(2) 10µF, 25V TDK C3225X7R1E106M AVX 12103D106M Taiyo Yuden TMK325BJ106MM
C_{OUT} Output Capacitor	(3) 470µF, 2.5V, 9mΩ low-ESR polymer capacitor Sanyo 2R5TPE470M9
N_H High-Side MOSFET	Siliconix SI7390DP
N_L Low-Side MOSFET	Siliconix SI7356DP
D_L Schottky Rectifier	3A, 30V, 0.45V_f Nihon EC31QS03L
L1 Inductor	0.8µH, 20A, 4.9mΩ Sumida CDEP104-0R8MC-50

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode type with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avx.com
Central Semiconductor	www.centralsemi.com
Coiltronics	www.coiltronics.com
Fairchild Semiconductor	www.fairchildsemi.com
Kemet	www.kemet.com
Nihon	www.niec.co.jp
Panasonic	www.panasonic.com/industrial
Sanyo	www.secc.co.jp
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Table 3. K-Factor

TON SETTING	TON FREQUENCY (kHz)	K-FACTOR (µs)
V_{CC}	200	5 ±10
Open	300	3.3 ±10
REF	550	1.8 ±12.5
GND	1000	1.0 ±12.5

$$\text{On-Time} = K (V_{OUT} + 0.075V) / V_{IN}$$

where K is set by the TON pin-strap connection and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch (Table 3).

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* table (±10% at 200kHz and 300kHz, and ±12% at 550kHz and 1000kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range. For example, the 1000kHz setting typically runs approximately 10% slower with inputs much greater than +5V due to the very short on-times required.

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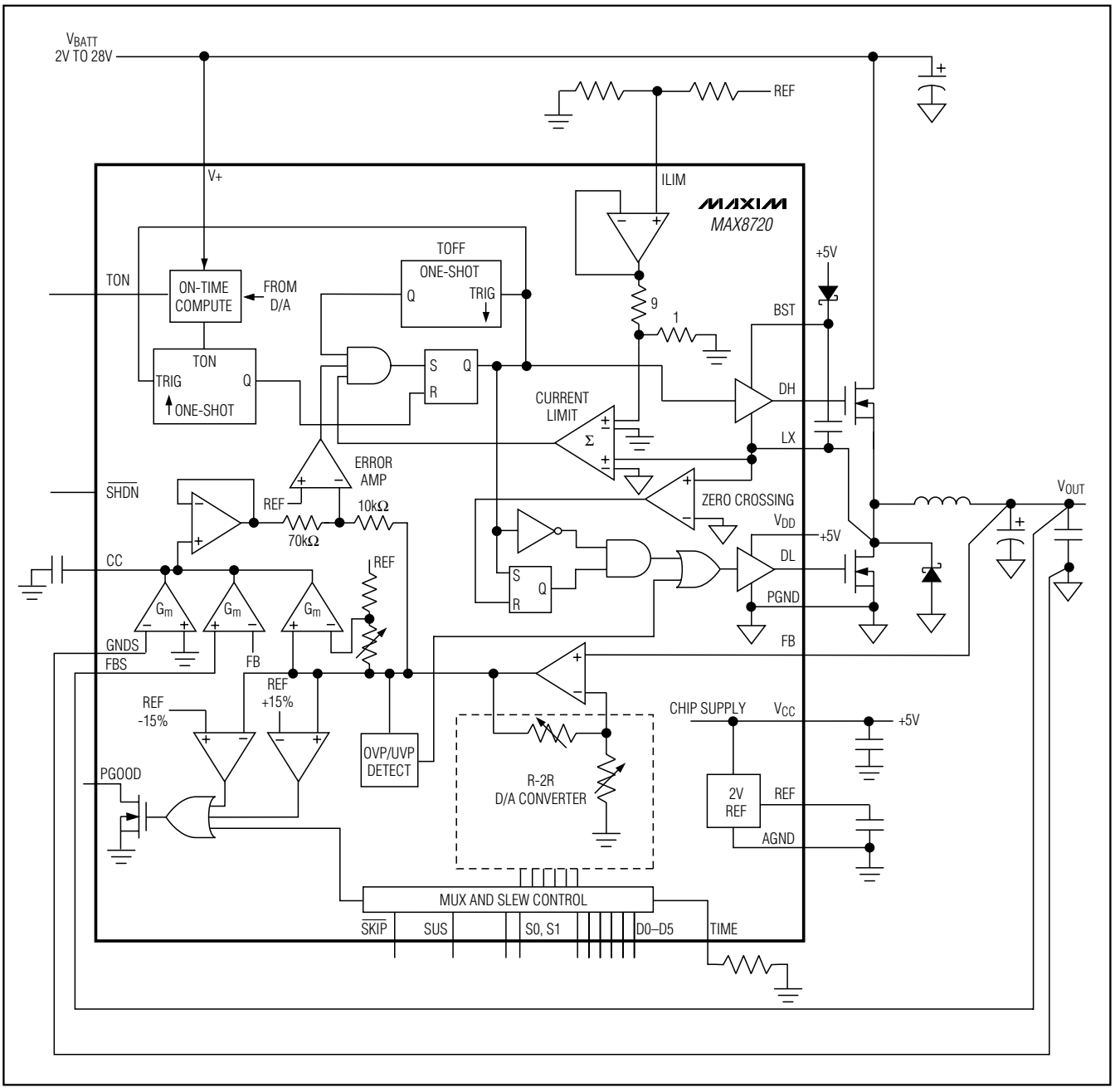


Figure 2. MAX8720 Block Diagram

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output-capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode ($\overline{SKIP}$ = high) and during

dynamic output-voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT} + V_{DIS}}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time calculated by the MAX8720.

Integrator Amplifiers and Output-Voltage Offsets

Three integrator amplifiers provide a fine adjustment to the output regulation point. One amplifier integrates the difference between GNDS and AGND, and a second integrates the difference between FBS and FB. The third amplifier integrates the difference between REF and the DAC output. These three transconductance amplifiers' outputs are directly summed inside the chip, so the integration time constant can be set easily with one capacitor. The G_m of each amplifier is 160µS (typ).

The integrator block has the ability to lower the output voltage by 2% and raise it by 6%. For each amplifier, the differential input voltage range is at least ±70mV total, including DC offset and AC ripple. The integrator corrects for approximately 90% of the total error, due to finite gain.

The FBS amplifier corrects for DC voltage drops in PC board traces and connectors in the output bus path between the DC-DC converter and the load. The GNDS amplifier performs a similar DC correction task for the output ground bus. The third integrator amplifier corrects the small offset of the error amplifier and provides an averaging function that forces V_{OUT} to be regulated at the average value of the output ripple waveform.

Integrators have both beneficial and detrimental characteristics. Although they correct for drops due to DC bus resistance and tighten the DC output-voltage tolerance limits by averaging the peak-to-peak output ripple, they can interfere with achieving the fastest possible load-transient response. The fastest transient response is achieved when all three integrators are disabled.

This can work very well if the MAX8720 circuit is placed very close to the CPU. All three integrators can be disabled by connecting FBS to V_{CC}. When the integrators are disabled, CC can be left unconnected, which eliminates a component but leaves GNDS connected to any convenient ground. When the inductor is in continuous conduction, the output voltage has a DC regulation higher than the trip level by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light loaded), the output voltage has a DC regulation higher than the trip level by approximately 1.5% due to slope compensation.

There is often a connector, or at least many milliohms of PC board trace resistance, between the DC-DC converter and the CPU. In these cases, the best strategy is to place most of the bulk bypass capacitors close to the CPU, with just one capacitor on the other side of the connector near the MAX8720 to control ripple if the CPU card is unplugged. In this situation, the remote-sense lines (GNDS and FBS) and integrators provide a real benefit.

Forced-PWM Mode ($\overline{SKIP}$ = High)

The low-noise forced-PWM mode ($\overline{SKIP}$ = high) disables the zero-crossing comparator, allowing the inductor current to reverse at light loads. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 40mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is required during downward output-voltage transitions. The MAX8720 uses PWM mode during all transitions, but only while the slew-rate controller is active. Due to voltage positioning, when a transition uses high negative inductor current, the output voltage does not settle to its final intended value until well after the slew-rate controller terminates. Because of this it is possible, at very high negative slew currents, for the output to end up high enough to cause PGOOD to go low.

Thus, it is necessary to use forced-PWM mode during all negative transitions. Most applications should use PWM mode exclusively, although there is some benefit to using skip mode while in the low-power suspend state.

Automatic Pulse-Skipping Switchover ($\overline{SKIP}$ = GND)

In skip mode ($\overline{SKIP}$ = GND), an inherent automatic switchover to PFM takes place at light loads (Figure 3). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the

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threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to half the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). For a 7V to 24V battery range, this threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} = \frac{KV_{OUT}(V_{IN} - V_{OUT})}{2LV_{IN}}$$

where K is the on-time scale factor (Table 2). For example, in the standard application circuit this becomes:

$$I_{LOAD(SKIP)} = \frac{3.3\mu s \times 1.25V(12V - 1.25V)}{2 \times 0.8\mu H \times 12V} = 2.31A$$

The crossover point occurs at a lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input-voltage levels.

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and battery voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. When combined with the undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. The current-limit threshold voltage adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 100mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by LX and PGND. Place the IC close to the low-side MOSFET with short, direct traces, making a Kelvin-sense connection to the source and drain terminals.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX8720 interprets the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1in from the MAX8720).

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.4Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. Applications with high input voltages and long, inductive DL traces may require additional gate-to-source capacitance to ensure fast-rising LX edges do not pull up the low-side MOSFET's gate voltage, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the minimum threshold voltage:

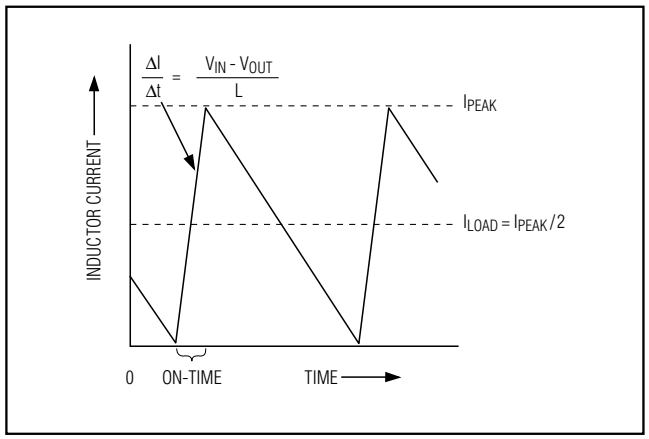


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

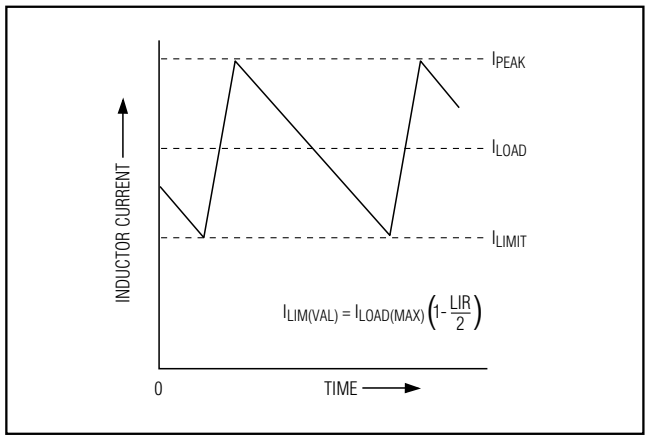


Figure 4. Valley Current-Limit Threshold

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Typically, adding 4700pF between DL and power ground (C_{NL} in Figure 5), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents may be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFETs' turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 5). Slowing down the high-side MOSFETs also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

V_{CC} POR and UVLO

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the PWM for operation. V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching, forces PGOOD low, and forces the DL gate driver low. When V_{CC} rises above 4.2V, the DAC inputs are sampled and the output voltage begins to slew to the DAC setting.

If V_{CC} drops low enough to trip the UVLO comparator, it is assumed that there is not enough supply voltage to make valid decisions. The MAX8720 immediately forces both DH and DL low. The output discharges to 0V at a rate dependent on the load and the total output capacitance. This prevents negative output voltages, eliminating the need for a Schottky diode to GND at the output.

For automatic startup, the battery voltage should be present before V_{CC}. If the MAX8720 attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The $\overline{SHDN}$ pin can be toggled to reset the fault latch.

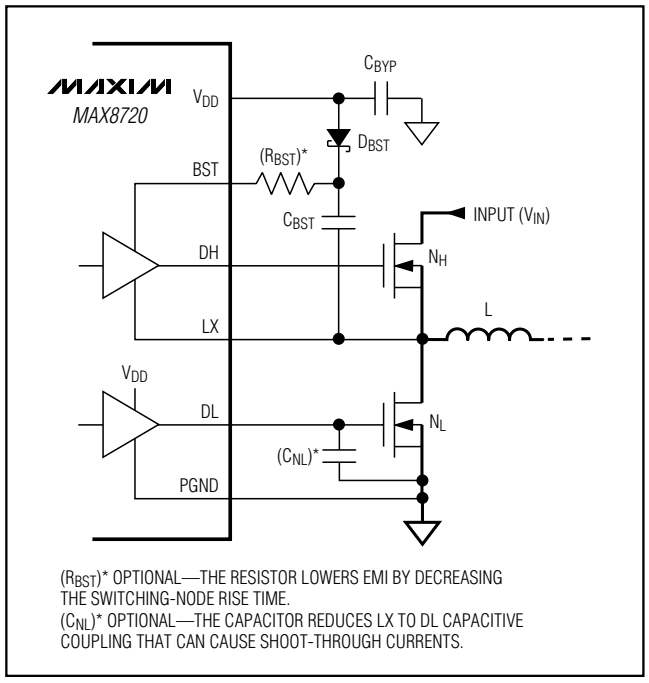


Figure 5. Reducing the Switching-Node Rise Time

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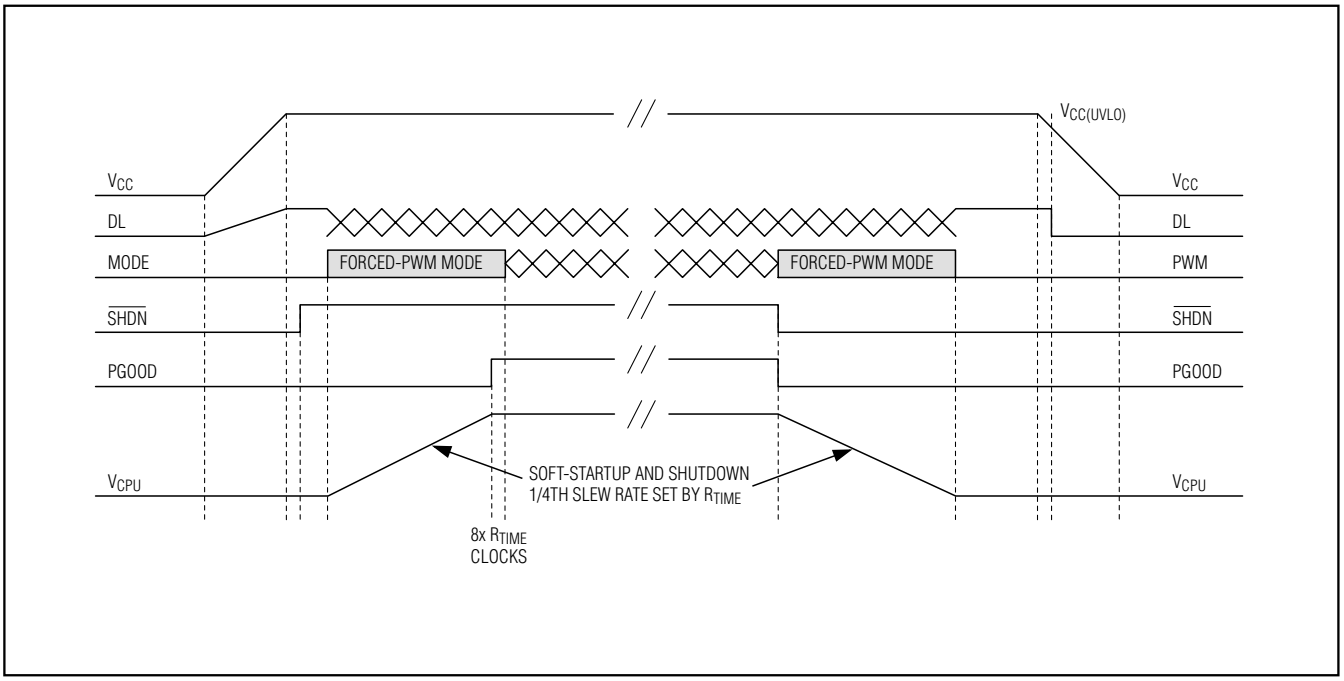


Figure 6. Soft-Startup and Soft-Shutdown

Soft-Startup and Soft-Shutdown ($\overline{SHDN}$)

When $\overline{SHDN}$ goes low, the MAX8720 enters low-power shutdown mode. PGOOD goes low immediately. The output voltage ramps down to 0V in 25mV steps at 1/4th the clock rate set by R_{TIME}. The slow rampdown of the output voltage results in smaller negative inductor currents, eliminating negative voltages on the output. When the DAC reaches the 0V setting, DL goes high, DH goes low, the reference is turned off, and the supply current drops to approximately 10µA.

When $\overline{SHDN}$ goes high, the reference powers up, and after the reference UVLO is passed, the DAC target is evaluated and switching begins. The slew-rate controller ramps up from 0V in 25mV steps at 1/4th the clock rate set by R_{TIME} to the currently selected code value (based on SUS). Full output current is available immediately. PGOOD goes high after the slew-rate controller has terminated and the output voltage is in regulation.

Nominal Output Voltage Setting

The MAX8720 uses a multiplexer that selects from two different inputs (Figure 7)—the VID DAC inputs or the suspend-mode S0, S1 inputs. On startup, the MAX8720 slews the target voltage from ground to either the decoded D0–D5 (SUS = low) voltage or the S0, S1 voltage (SUS = high).

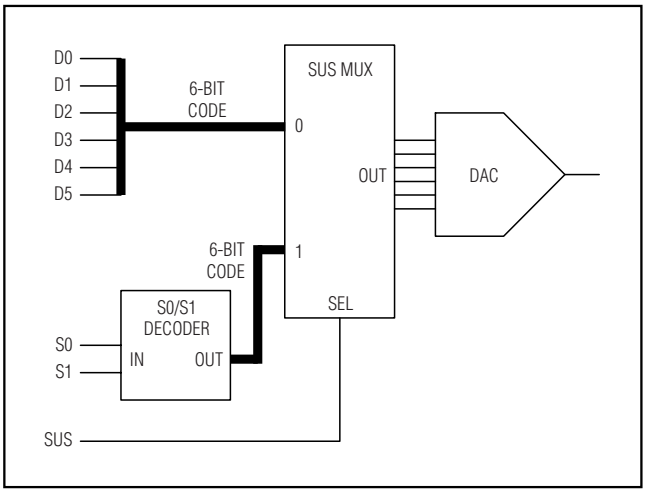


Figure 7. Internal Multiplexers Functional Diagram

DAC Inputs (D0–D5)

The digital-to-analog converter (DAC) programs the output voltage. It typically receives a preset digital code from the CPU pins, which are either hardwired to GND or left open-circuit. They can also be driven by digital logic, general-purpose I/O, or an external mux. Do not leave D0–D5 floating—use 1MΩ or less pullup resistors if the inputs may float. D0–D5 can be changed while the

Table 4. Output Voltage vs. DAC Codes

D5	D4	D3	D2	D1	D0	V_{OUT}	D5	D4	D3	D2	D1	D0	V_{OUT}
0	0	0	0	0	0	1.850	1	0	0	0	0	0	1.050
0	0	0	0	0	1	1.825	1	0	0	0	0	1	1.025
0	0	0	0	1	0	1.800	1	0	0	0	1	0	1.000
0	0	0	0	1	1	1.775	1	0	0	0	1	1	0.975
0	0	0	1	0	0	1.750	1	0	0	1	0	0	0.950
0	0	0	1	0	1	1.725	1	0	0	1	0	1	0.925
0	0	0	1	1	0	1.700	1	0	0	1	1	0	0.900
0	0	0	1	1	1	1.675	1	0	0	1	1	1	0.875
0	0	1	0	0	0	1.650	1	0	1	0	0	0	0.850
0	0	1	0	0	1	1.625	1	0	1	0	0	1	0.825
0	0	1	0	1	0	1.600	1	0	1	0	1	0	0.800
0	0	1	0	1	1	1.575	1	0	1	0	1	1	0.775
0	0	1	1	0	0	1.550	1	0	1	1	0	0	0.750
0	0	1	1	0	1	1.525	1	0	1	1	0	1	0.725
0	0	1	1	1	0	1.500	1	0	1	1	1	0	0.700
0	0	1	1	1	1	1.475	1	0	1	1	1	1	0.675
0	1	0	0	0	0	1.450	1	1	0	0	0	0	0.650
0	1	0	0	0	1	1.425	1	1	0	0	0	1	0.625
0	1	0	0	1	0	1.400	1	1	0	0	1	0	0.600
0	1	0	0	1	1	1.375	1	1	0	0	1	1	0.575
0	1	0	1	0	0	1.350	1	1	0	1	0	0	0.550
0	1	0	1	0	1	1.325	1	1	0	1	0	1	0.525
0	1	0	1	1	0	1.300	1	1	0	1	1	0	0.500
0	1	0	1	1	1	1.275	1	1	0	1	1	1	0.475
0	1	1	0	0	0	1.250	1	1	1	0	0	0	0.450
0	1	1	0	0	1	1.225	1	1	1	0	0	1	0.425
0	1	1	0	1	0	1.200	1	1	1	0	1	0	0.400
0	1	1	0	1	1	1.175	1	1	1	0	1	1	0.375
0	1	1	1	0	0	1.150	1	1	1	1	0	0	0.350
0	1	1	1	0	1	1.125	1	1	1	1	0	1	0.325
0	1	1	1	1	0	1.100	1	1	1	1	1	0	0.300
0	1	1	1	1	1	1.075	1	1	1	1	1	1	0.275

SMPS is active, initiating a transition to a new output voltage level. If this mode of DAC control is used, connect SUS low. Change D0–D5 together, avoiding greater than 50ns skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level, followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are shown in Table 4.

Suspend Mode (S0, S1, SUS)

When the CPU enters low-power suspend mode, the processor sets the regulator to a lower output voltage to reduce power consumption. The MAX8720 includes a suspend-mode input (S0, S1) and a digital SUS control input. The suspend voltage is programmed using the 4-level S0, S1 inputs (Table 5). The suspend voltage adjustment range is from 0.275V to 0.650V.

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Table 5. Suspend-Mode DAC Codes

S1	S0	V_{OUT}		S1	S0	V_{OUT}
GND	GND	0.650		OPEN	GND	0.450
GND	REF	0.625		OPEN	REF	0.425
GND	OPEN	0.600		OPEN	OPEN	0.400
GND	V_{CC}	0.575		OPEN	V_{CC}	0.375
REF	GND	0.550		V_{CC}	GND	0.350
REF	REF	0.525		V_{CC}	REF	0.325
REF	OPEN	0.500		V_{CC}	OPEN	0.300
REF	V_{CC}	0.475		V_{CC}	V_{CC}	0.275

When the CPU suspends operation (SUS = high), the controller overrides the 6-bit VID DAC code set by D0–D5, and slews the output voltage to the target voltage set by the S0, S1 inputs. During the transition, the MAX8720 blanks both PGOOD thresholds (PGOOD forced high impedance) until the slew-rate controller reaches the suspend-mode voltage, plus 8 extra R_{TIME} clocks. After this blanking time expires, the MAX8720 automatically switches to a pulse-skipping control scheme regardless of $\overline{SKIP}$.

Output-Voltage-Transition Timing

The MAX8720 is designed to perform output-voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output-voltage level with the lowest possible peak currents for a given output capacitance. This makes the IC ideal for CPUs and GPUs that operate at different voltages.

At the beginning of an output-voltage transition (VID change or SUS level change), the MAX8720 enters forced-PWM mode and blanks the PGOOD output (forced high impedance). PGOOD remains blanked during the transition and is re-enabled when the slew-rate controller has set the internal DAC to the final value and 8 additional slew-rate clock periods have passed. The slew-rate clock frequency (set by resistor R_{TIME}) must be set fast enough to ensure that the longest required transition is completed within the allowed transition time.

The output-voltage transition is performed in 25mV steps, preceded by a delay and followed by one additional clock period. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX8720's slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX8720 automatically controls the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM. The transition time is given by:

$$t_{TRANS} = \frac{|V_{OLD} - V_{NEW}|}{25mV \times f_{SLEW}} + t_{DELAY}$$

where f_{SLEW} = 150kHz x 120kΩ / R_{TIME}, V_{OLD} is the original DAC setting, V_{NEW} is the new DAC setting, and t_{DELAY} ranges from zero to a maximum of 2 / f_{SLEW}. See Time Frequency Accuracy in the *Electrical Characteristics* table for f_{SLEW} accuracy. The practical range of R_{TIME} is 22kΩ to 470kΩ, corresponding to 1.22µs to 26µs per 25mV step. Although the DAC takes discrete 25mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output-voltage transition is:

$$I_{L(AVE)} = C_{OUT} \times 25mV \times f_{SLEW}$$

Suspend Transition (Forced-PWM Operation Selected)

When the MAX8720 enters suspend mode while configured for forced-PWM operation ($\overline{SKIP}$ pulled high), the controller ramps the output voltage down to the S0, S1 programmed voltage at the slew rate determined by R_{TIME}. The controller blanks PGOOD (forced high impedance) until the transition is completed plus 8 extra R_{TIME} clocks—the internal target voltage equals the selected S0, S1 DAC voltage. After this blanking time expires, the controller enters pulse-skipping operation.

When exiting suspend mode (SUS pulled low), the MAX8720 immediately enters forced-PWM mode and ramps the output up at the slew rate set by R_{TIME}. The controller blanks PGOOD (forced high impedance) until the transition is completed plus 8 extra R_{TIME} clocks—the internal target voltage equals the selected D0–D5 DAC voltage.

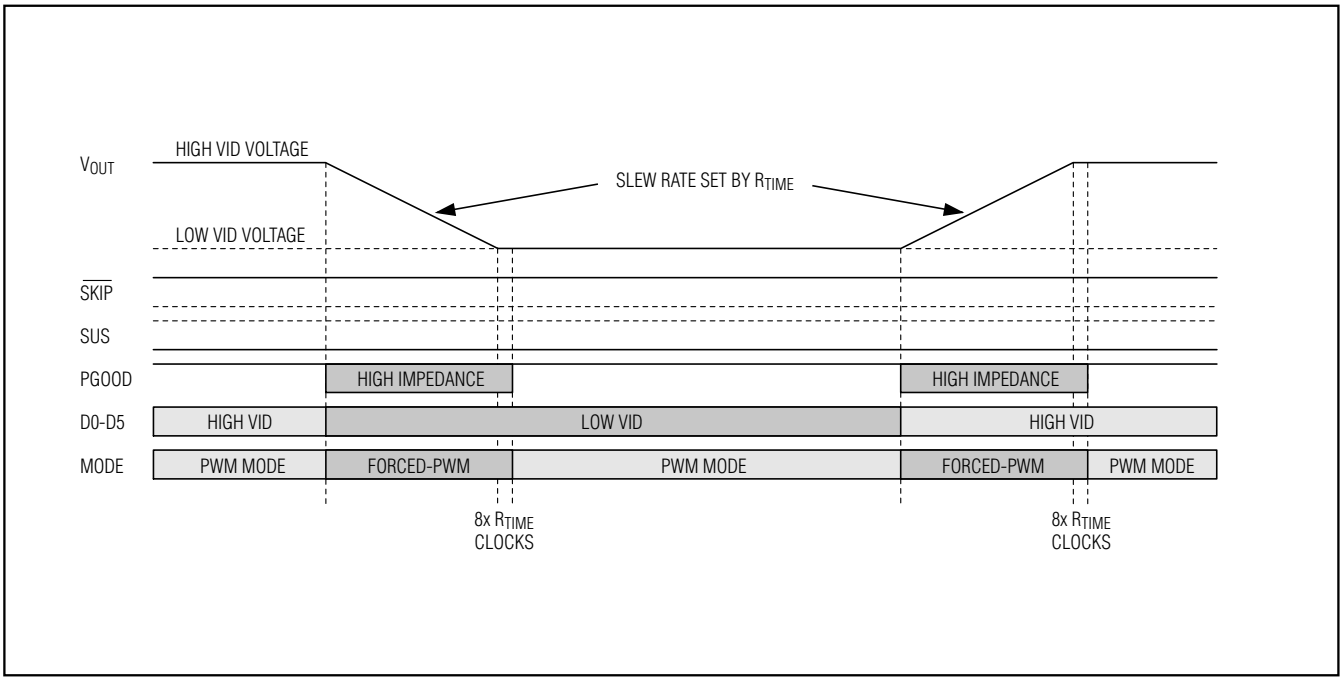


Figure 8. VID Transition in Forced-PWM Mode ($\overline{SKIP}$ = High)

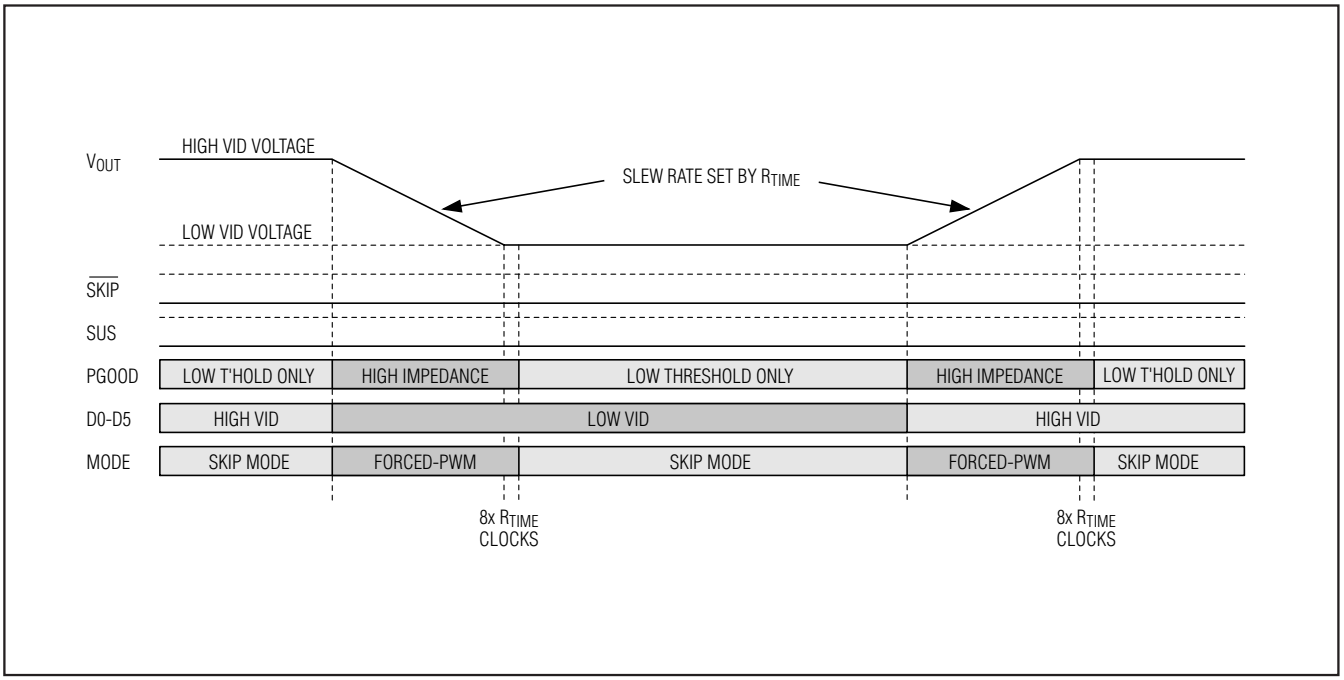


Figure 9. VID Transition in Pulse-Skipping Mode ($\overline{SKIP}$ = GND)

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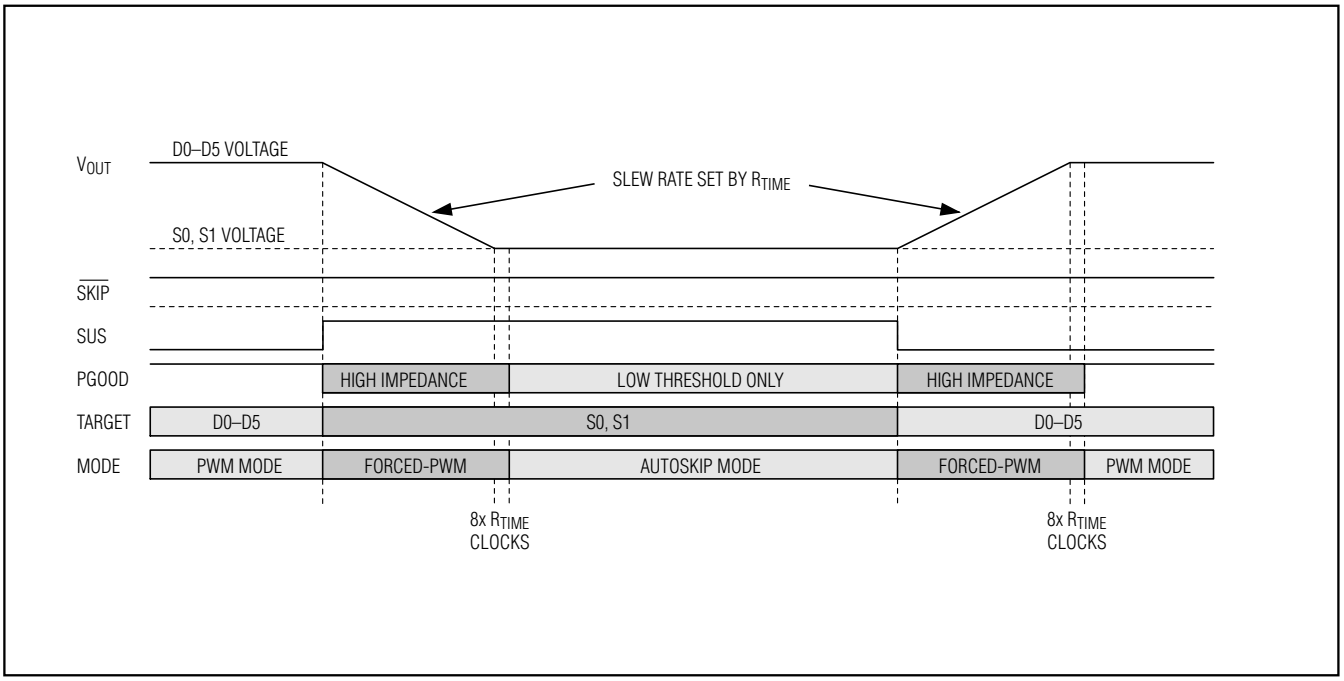


Figure 10. Suspend Transition in Forced-PWM Mode ($\overline{SKIP}$ = High)

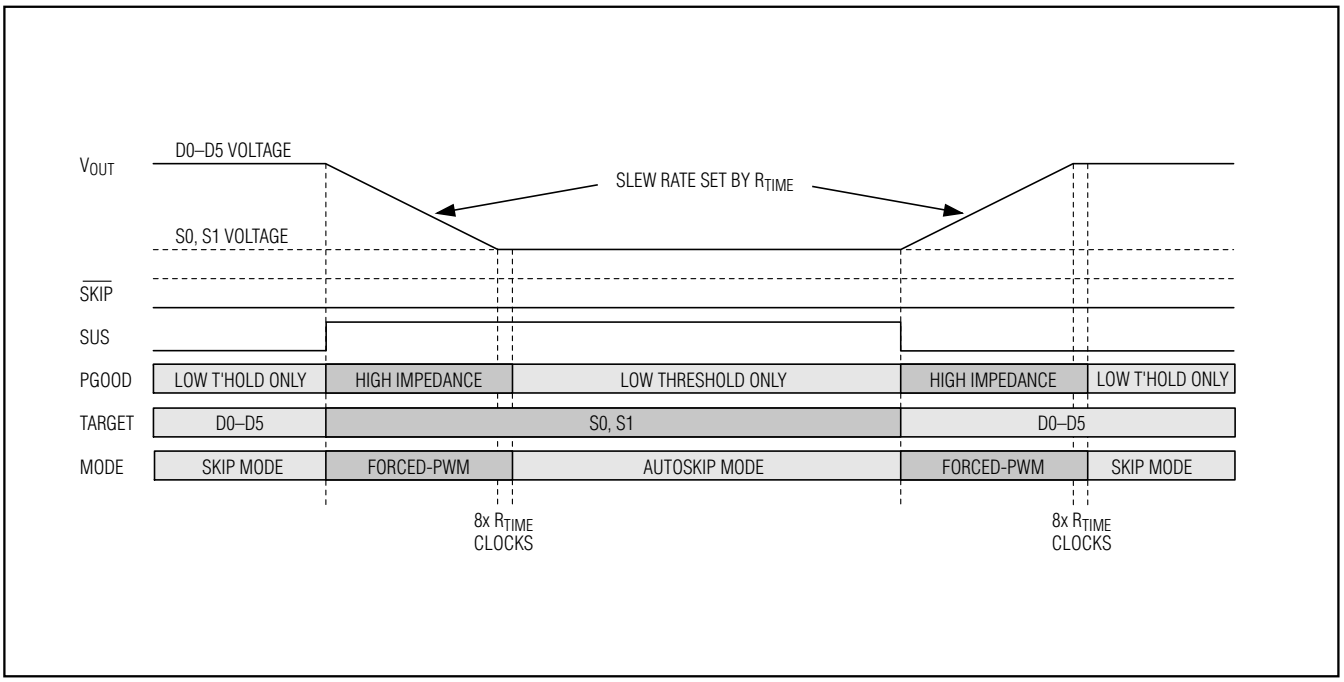


Figure 11. Suspend Transition in Pulse-Skipping Mode ($\overline{SKIP}$ = GND)

Suspend Transition (Pulse-Skipping Operation Selected)

If the MAX8720 is configured for pulse-skipping operation ($\overline{SKIP}$ = GND) when SUS goes high, the MAX8720 immediately enters forced-PWM mode, ramping the output voltage down to the S0, S1 programmed voltage at the slew rate determined by R_{TIME}. The controller blanks PGOOD (forced high impedance) until the transition is completed plus 8 extra R_{TIME} clocks—the internal target voltage equals the selected S0, S1 DAC voltage. After this blanking time expires, the controller enters pulse-skipping operation.

When exiting suspend mode (SUS pulled low), the MAX8720 immediately enters forced-PWM mode and ramps the output up at the slew rate set by R_{TIME}. The controller blanks PGOOD (forced high impedance) until the transition is completed plus 8 extra R_{TIME} clocks—the internal target voltage equals the selected D0–D5 DAC voltage. After this blanking time expires, the controller returns to pulse-skipping operation.

Output Overvoltage Protection

The overvoltage-protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The output voltage is continuously monitored for overvoltage. If the output is more than 2.25V, OVP is triggered and the circuit shuts down. The DL low-side gate-driver output is then latched high until $\overline{SHDN}$ is toggled or V_{CC} power is cycled below 1V. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. DL is also kept high continuously in shutdown when V_{CC} is above the UVLO threshold.

Output Undervoltage Shutdown

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX8720 output voltage is under 70% of the nominal value, the PWM is latched off and won't restart until V_{CC} power is cycled or $\overline{SHDN}$ is toggled. To allow startup, UVP is ignored until the internal DAC reaches the final target plus 8 extra R_{TIME} clocks.

UVP can be defeated through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The over/undervoltage-protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to disable the OVP, UVP, and thermal-shutdown features, and clear the fault latch if it has been set. The no-fault test mode is entered by forcing 12V to 15V on $\overline{SHDN}$.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output-capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency, and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

  The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor

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value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}\ f_{SW}\ I_{LOAD(MAX)}\ LIR}$$

For example: $I_{LOAD(MAX)}$ = 15A, V_{IN} = 12V, V_{OUT} = 1.25V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.3

$$L = \frac{1.25V \times (12V - 1.25V)}{12V \times 300kHz \times 15A \times 0.3} = 0.83\mu H$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output-voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur.

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})\left(K\frac{V_{OUT}}{V_{IN}} + t_{OFF(MIN)}\right)}{2C_{OUT}\ V_{OUT}\left[K\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 3.

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}\ V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The peak inductor current occurs at $I_{LOAD(MAX)}$ plus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)}\left(1 - \frac{LIR}{2}\right)$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of N_L. For the 100mV default setting, the minimum current-limit threshold is 90mV.

Connect ILIM to V_{CC} for a default 100mV current-limit threshold. For an adjustable threshold, connect a resistor-divider from REF to GND, with ILIM connected to the center tap. The external adjustment range of 0.5V to 2.0V corresponds to a current-limit threshold of 50mV to 200mV. When adjusting the current limit, use 1% tolerance resistors and a 10µA divider current to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors (see the *Output-Capacitor Stability Requirements* section), the filter capacitor's ESR dominates the output voltage ripple. Thus, the output capacitor's size depends on the maximum ESR required to meet the output-voltage-ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = R_{ESR}\ I_{LOAD(MAX)}\ LIR$$

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too

low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le V_{STEP} / I_{LOAD(MAX)}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that may affect the overall stability (see the *Output-Capacitor Stability Considerations* section).

Output-Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

$$\text{where } f_{ESR} = \frac{1}{2\pi\ R_{ESR}\ C_{OUT}}$$

A voltage-positioned circuit has the ESR zero frequency lowered due to the external resistor in series with the output-capacitor ESR, guaranteeing stability. For a voltage-positioned circuit, the minimum ESR requirement of the output capacitor is reduced by the voltage-positioning resistor value.

The boundary condition of instability is given by the following equation:

$$R_{ESR} \times C_{OUT} \ge 1 / (2 \times f_{SW})$$

For good phase margin, it is recommended to increase the equivalent RC time constant by a factor of two. The standard application circuit (Figure 1) operating at 300kHz with C_{OUT} = 1410µF and R_{ESR} = 3mΩ easily meets this requirement.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double pulsing is more of a nuisance than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{OUT(MAX)}}{V_{IN}} \sqrt{V_{OUT}(V_{IN} - V_{OUT})}$$

For most applications, nontantalum chemistries (ceramic or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a switch or a connector in series with the battery. If the MAX8720 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are

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significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., SO-8, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX8720 DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power MOSFET Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\,(N_H\ RESISTIVE) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 \times R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\,(N_H\ SWITCHING) = \frac{(V_{IN(MAX)})^2\, C_{RSS}\, f_{SW}\, I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (2A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC-adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\,(N_L\ RESISTIVE) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2\ R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{I_{LOAD(MAX)}\ LIR}{2}\right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3rd of the load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume the IRF7821 n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single IRF7821 has a maximum gate charge of 14nC (V_{GS} = 5V). Using the above equation, the required boost capacitance is:

$$C_{BST} = \frac{1 \times 14nC}{200mV} = 0.07\mu F$$

Select the closest standard value. This example requires a 0.1µF ceramic capacitor.

Applications Information

Dropout Performance

The output-voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot (375ns max at 1000kHz). For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient-response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP} / \Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current is less able to increase during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this may be adjusted up or down to allow tradeoffs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{DIS}}{\left(1 - \frac{t_{OFF(MIN)} \times h}{K}\right)} + V_{CHG} - V_{DIS}$$

where V_{DIS} and V_{CHG} are the parasitic voltage drops in the discharge and charge paths, respectively (see the *On-Time One-Shot (TON)* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT} = 1.6V

f_{SW} = 550kHz

K = 1.8µs, worst-case K = 1.58µs

$t_{OFF(MIN)}$ = 500ns

$V_{DIS} = V_{CHG}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = (1.6V + 0.1V) / (1 - 0.5\mu s \times 1.5 / 1.58\mu s) + 0.1V - 0.1V = 3.2V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = (1.6V + 0.1V) / (1 - 0.5\mu s \times 1.0 / 1.58\mu s) + 0.1V - 0.1V = 2.5V$$

Therefore, V_{IN} must be greater than 2.5V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance is 3.2V.

One-Stage (Battery Input) vs. Two-Stage (5V Input) Applications

The MAX8720 can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. The transient response of the single stage is better due to the ability to ramp up the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has worse transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Dynamically Adjustable 6-Bit VID Step-Down Controller

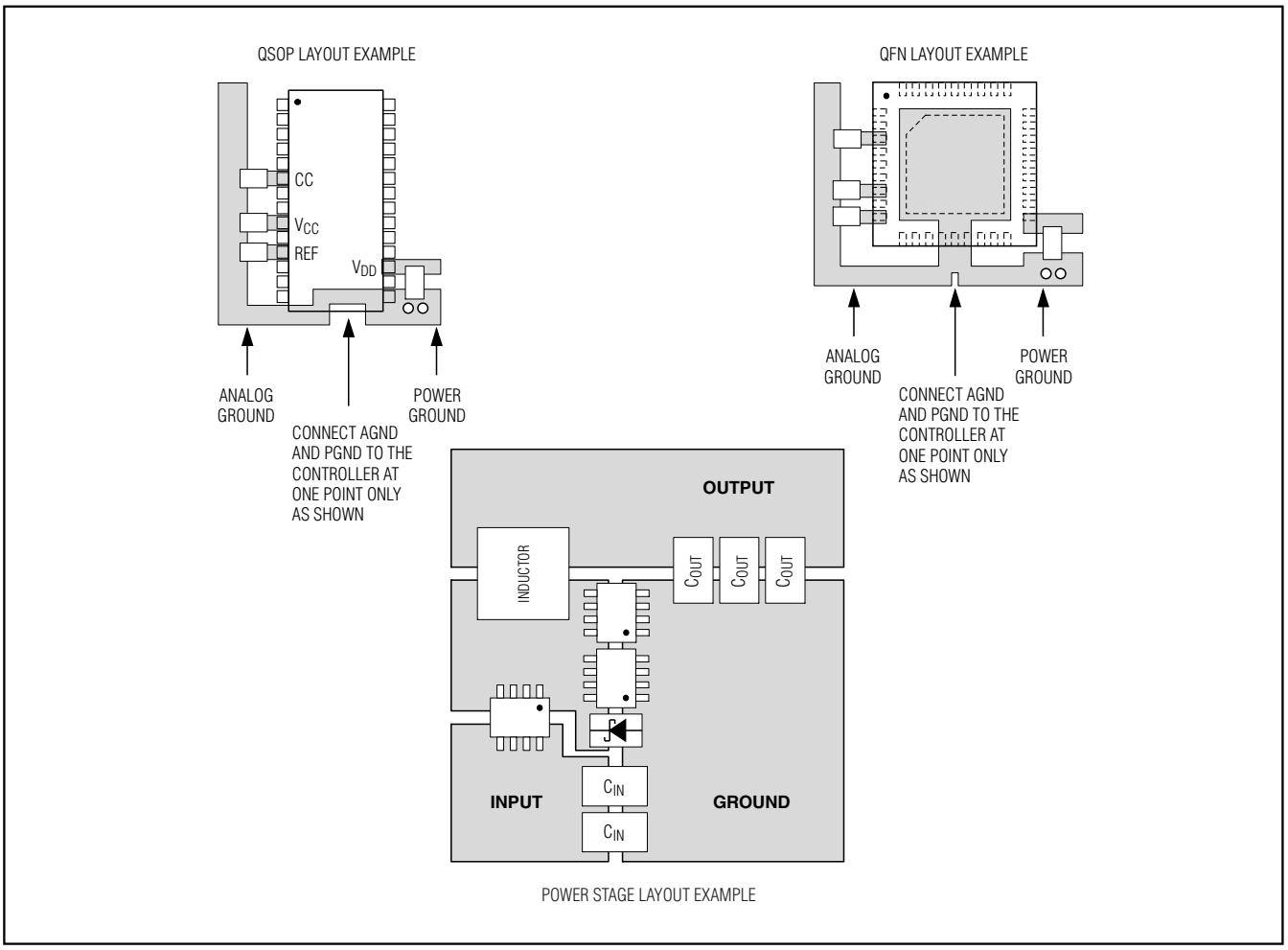


Figure 12. PC Board Layout Example

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 12). If possible, mount all of the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (NL source, C_{IN}, C_{OUT}, and DL anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite NL and NH to keep LX, GND, DH, and the DL gate-drive lines short and wide. The DL and DH_ gate traces must be short and wide (50 to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive deadtime sensing.
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figures 1 and 12. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

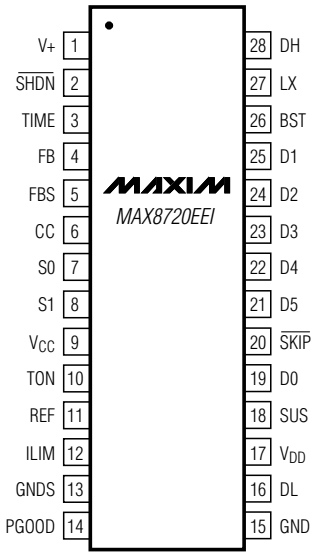
Chip Information

TRANSISTOR COUNT: 7190

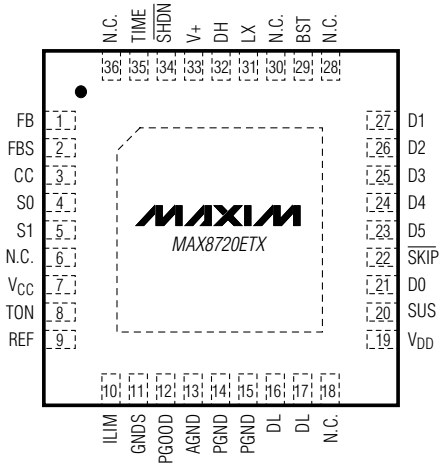
PROCESS: BiCMOS

Pin Configurations

TOP VIEW



QSOP



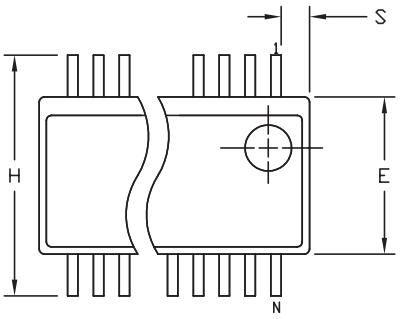
THIN QFN
6mm x 6mm

Dynamically Adjustable 6-Bit VID Step-Down Controller

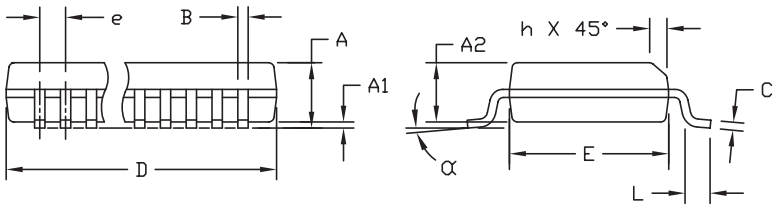
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

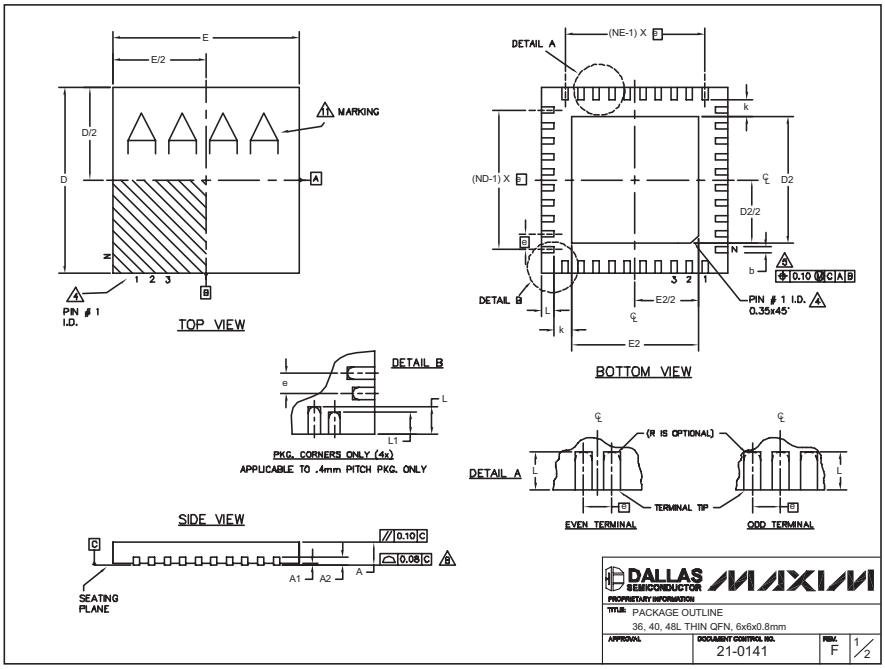
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. F
2/2

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