19-0756; Rev 0; 1/07

EVALUATION KIT AVAILABLE

SMBus Level 2 Battery Charger with Remote Sense

General Description

The MAX8731A is an SMBus™ programmable multi-chemistry battery charger. The MAX8731A uses a minimal command set to easily program the charge voltage, charge current, and adapter current limit.

The MAX8731A charges one to four Li+ series cells and delivers up to 8A charge current. The MAX8731A drives n-channel MOSFETs for improved efficiency and reduced cost. Low-offset current-sense amplifiers provide high accuracy with 10mΩ sense resistors.

The MAX8731A current-sense amplifiers provide high accuracy (3% at 3.5A) and also provide fast cycle-by-cycle current-mode control to protect against battery short circuit and system load transients.

The charger employs dual remote sense, which reduces charge time by measuring the feedback voltage directly at the battery, improving accuracy of initial transition into constant-voltage mode. The MAX8731A provides 0.5% battery voltage accuracy directly at the battery terminal.

The MAX8731A provides a digital output that indicates the presence of the AC adapter, as well as an analog output that indicates the adapter current within 4% accuracy.

The MAX8731A is available in a small 5mm x 5mm, 28-pin, thin (0.8mm) QFN package. An evaluation kit is available to reduce design time. The MAX8731A is available in a lead-free package.

SMBus is a trademark of Intel Corp.

Applications

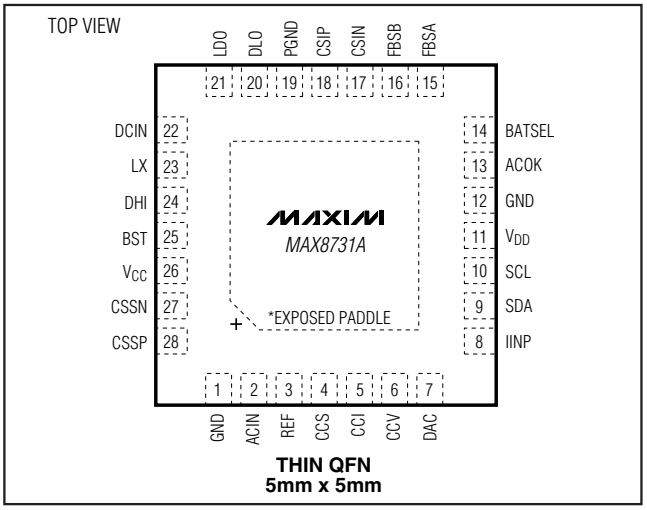
Notebook Computers

Tablet PCs

Medical Devices

Portable Equipment with Rechargeable Batteries

Pin Configuration



THIN QFN 5mm x 5mm

Features

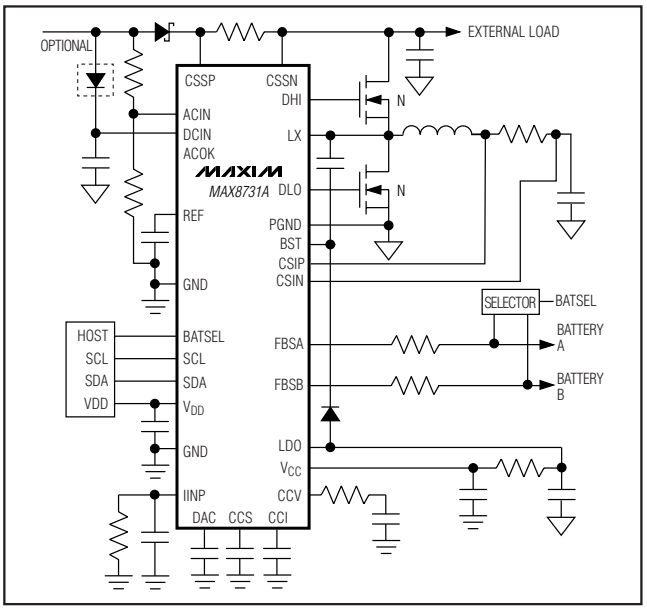
- ♦ **0.5% Battery Voltage Accuracy**
- ♦ **3% Input Current-Limit Accuracy**
- ♦ **3% Charge-Current Accuracy**
- ♦ **SMBus 2-Wire Serial Interface**
- ♦ **Cycle-by-Cycle Current Limit**
  - **Battery Short-Circuit Protection**
  - **Fast Response for Pulse Charging**
  - **Fast System-Load-Transient Response**
- ♦ **Dual-Remote-Sense Inputs**
- ♦ **Monitor Outputs for**
  - **Adapter Current (4% Accuracy)**
  - **AC Adapter Detection**
- ♦ **11-Bit Battery Voltage Setting**
- ♦ **6-Bit Charge-Current/Input-Current Setting**
- ♦ **8A (max) Battery Charger Current**
- ♦ **11A (max) Input Current**
- ♦ **+8V to +26V Input Voltage Range**
- ♦ **Charges Li+, NiMH, and NiCd Battery Chemistries**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8731AETI+	-40°C to +85°C	28 Thin QFN (5mm x 5mm)	T2855-6

+Indicates a lead-free package.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

SMBus Level 2 Battery Charger with Remote Sense

ABSOLUTE MAXIMUM RATINGS

DCIN, CSSN, CSIN, FBSA, FBSB to GND .....-0.3V to +28V
CSSP to CSSN, CSIP to CSIN, PGND to GND .....-0.3V to +0.3V
BST to GND .....-0.3V to +32V
BST to LX .....-0.3V to +6V
DHI to LX .....-0.3V to +(V_{BST} + 0.3)V
DLO to PGND .....-0.3V to +(LDO + 0.3)V
LX to GND .....-6V to +28V
CCI, CCS, CCV, DAC, REF,
IINP to GND .....-0.3V to (V_{CC} + 0.3)V
V_{DD}, SCL, SDA, BATSEL, ACIN, ACOK, V_{CC} to GND,
LDO to PGND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN
(derate 20.8mW/°C above +70°C) .....1666.7 mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF, V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
Battery Full-Charge Voltage and Accuracy	ChargingVoltage() = 0x41A0	16.716	16.8	16.884	V
		-0.5		+0.5	%
	ChargingVoltage() = 0x3130	12.491	12.592	12.693	V
		-0.8		+0.8	%
	ChargingVoltage() = 0x20D0	8.333	8.4	8.467	V
		-0.8		+0.8	%
	ChargingVoltage() = 0x1060	4.150	4.192	4.234	V
		-1.0		+1.0	%
Battery Undervoltage-Lockout Trip Point for Trickle Charge			2.5		V
CHARGE-CURRENT REGULATION					
CSIP-to-CSIN Full-Scale Current-Sense Voltage		78.22	80.64	83.06	mV
Charge Current and Accuracy	RS2, Figure 1 = 10mΩ; ChargingCurrent() = 0x1f80	7.822	8.064	8.306	A
		-3		+3	%
	RS2, Figure 1 = 10mΩ; ChargingCurrent() = 0x0f80	3.809	3.968	4.126	A
		-4		+4	%
	RS2, Figure 1 = 10mΩ; ChargingCurrent() = 0x0080 (128mA)	64		400	mA
Charge-Current Gain Error	Based on ChargeCurrent() = 128mA and 8.064A	-2		+2	%
FBSA/FBSB/CSIP/CSIN Input Voltage Range		0		19	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF, V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Battery Quiescent Current	Adapter present, not charging, I_{CSIP} + I_{CSIN} + I_{LX} + $I_{FBS_}$, $V_{FBS_}$ = V_{LX} = V_{CSIN} = V_{CSIP} = 19V				2	5	µA
	Adapter absent, I_{CSIP} + I_{CSIN} + I_{LX} + I_{FBSA} + I_{FBSB} + I_{CSSP} + I_{CSSN}, $V_{FBS_}$ = V_{LX} = V_{CSIN} = V_{CSIP} = 19V, V_{DCIN} = 0V					+1	
Adapter Quiescent Current	I_{DCIN} + I_{CSSP} + I_{CSSN}	$V_{Adapter}$ = 26V, $V_{Battery}$ = 16.8V, not charging			200	500	µA
		$V_{Adapter}$ = 19V, $V_{Battery}$ = 16.8V	Charging		0.4	1	mA
			Not charging		200	500	µA
		$V_{Adapter}$ = 8V, $V_{Battery}$ = 4V	Charging		0.4	1	mA
			Not charging		200	500	µA
INPUT-CURRENT REGULATION							
CSSP-to-CSSN Full-Scale Current-Sense Voltage	$V_{FBS_}$ = 19V			106.7	110	113.3	mV
Input Current Accuracy	RS1, Figure 1 = 10mΩ, InputCurrent() = 11004mA or 3584mA			-3		+3	%
	RS1, Figure 1 = 10mΩ, InputCurrent() = 2048mA			-5		+5	
POR Input Current	RS1, Figure 1 = 10mΩ				256		mA
Input Current-Limit Gain Error	Based on InputCurrent() = 1024mA and 11004mA			-2		+2	%
Input Current-Limit Offset				-1		+1	mV
CSSP/CSSN Input Voltage Range				8		26	V
IINP Transconductance	$V_{CSSP - CSSN}$ = 110mV			2.85	3.0	3.15	mA/V
IINP Offset	Based on $V_{CSSP - CSSN}$ = 110mV and 20mV			-1.5		+1.5	mV
IINP Accuracy	$V_{CSSP - CSSN}$ = 110mV			-5		+5	%
	$V_{CSSP - CSSN}$ = 55mV or 35mV			-4		+4	
	$V_{CSSP - CSSN}$ = 20mV			-10		+10	
IINP Output Voltage Range				0		3.5	V
SUPPLY AND LINEAR REGULATOR							
DCIN, Input Voltage Range				8.0		26.0	V
DCIN Undervoltage-Lockout Trip Point	DCIN falling			7	7.4		V
	DCIN rising				7.5	7.85	
Power-Fail Threshold	V_{CSSP} - V_{CSIN} falling			9	15	21	mV
	V_{CSSP} - V_{CSIN} rising			160	210	271	

SMBus Level 2 Battery Charger with Remote Sense

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF, V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LDO Output Voltage	8.0V < V_{DCIN} < 28V, no load	5.25	5.4	5.55	V
LDO Load Regulation	0 < I_{LDO} < 30mA		34	100	mV
LDO Undervoltage-Lockout Threshold	V_{DCIN} = 8.0V, V_{LDO} falling	3.20	4.00	5.15	V
V_{DD} Range		2.7		5.5	V
V_{DD} UVLO Rising			2.5	2.7	V
V_{DD} UVLO Hysteresis			100		mV
V_{DD} Quiescent Current	DCIN < 6V, V_{DD} = 5.5V, SCL = SDA = 5.5V		16	27	µA
REFERENCE					
REF Output Voltage	0 < I_{REF} < 500µA	4.071	4.096	4.120	V
REF Undervoltage-Lockout Trip Point	REF falling		3.1	3.9	V
ACOK					
ACOK Sink Current	V_{ACOK} = 0.4V, ACIN = 1.5V	1			mA
ACOK Leakage Current	V_{ACOK} = 5.5V, ACIN = 2.5V			1	µA
ACIN					
ACIN Threshold		2.007	2.048	2.089	V
ACIN Threshold Hysteresis		10	20	30	mV
ACIN Input Bias Current		-1		+1	µA
REMOTE-SENSE INPUTS					
FBS_ Range	V_{CSIN} - V_{FBS}	0		200	mV
FBS_ Gain	ΔV_{CSIN} / $\Delta(V_{CSIN}$ - $V_{FBS_})$	0.95	1.00	1.05	V/V
CSIN-FBS_ Clamp Voltage		225	250	275	mV
FBS_ Bias Current	Charger switching, FBS_ selected			14	µA
FBS_ Bias Current	Charger not switching or FBS_ not selected	-2		+2	µA
SWITCHING REGULATOR					
Off-Time	V_{CSIN} = 16.0V, V_{CSSP} = 19V	360	400	440	ns
	V_{CSIN} = 16.0V, V_{CSSP} = 17V	260	300	360	
BST Supply Current	DHI high		500	800	µA
LX Input Bias Current	V_{DCIN} = 28V, V_{CSIN} = V_{LX} = 20V, DHI low			2	µA
Maximum Discontinuous-Mode Peak Current (I_{MIN})			0.5		A
DHI On-Resistance Low	I_{DHI} = -10mA		1	3	Ω
DHI On-Resistance High	I_{DHI} = 10mA		3	5	Ω
DLO On-Resistance High	I_{DLO} = 10mA		3	5	Ω
DLO On-Resistance Low	I_{DLO} = -10mA		1	3	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF, V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS					
GMV Amplifier Transconductance	ChargingVoltage() = 16.8V, $V_{FBS_}$ = 16.8V	0.0625	0.125	0.2500	mA/V
GMI Amplifier Transconductance	ChargingCurrent() = 3968mA, V_{CSIP} - V_{CSIN} = 39.68mV	0.5	1.0	2.0	mA/V
GMS Amplifier Transconductance	InputCurrent() = 3968mA, V_{CSSP} - V_{CSSN} = 79.36mV	0.5	1.0	2.0	mA/V
CCI/CCS/CCV Clamp Voltage	0.25V < $V_{CCI/S/V}$ < 2.0V	120	250	600	mV
LOGIC LEVELS					
SDA/SCL Input-Low_Voltage	V_{DD} = 2.7V to 5.5V			0.8	V
SDA/SCL Input-High_Voltage	V_{DD} = 2.7V to 5.5V	2.1			V
SDA/SCL Input Bias Current	V_{DD} = 2.7V to 5.5V	-1		+1	µA
BATSEL Input-Low_Voltage				0.8	V
BATSEL Input-High_Voltage		2.1			V
BATSEL Input Bias Current		-1		+1	µA
SDA, Output Sink Current	$V_{(SDA)}$ = 0.4V	6			mA

SMBus TIMING SPECIFICATIONS (V_{DD} = 2.7V to 5.5V) (see Figures 4 and 5)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Frequency	f_{SMB}		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Timeout	$t_{TIMEOUT}$	(Note 1)	25		35	ms
SCL Low Period	T_{LOW}		4.7			µs
SCL High Period	T_{HIGH}		4			µs
Maximum Charging Period Without a ChargeVoltage() or ChargeCurrent() Command			140	175	210	s

SMBus Level 2 Battery Charger with Remote Sense

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION							
Battery Full-Charge Voltage and Accuracy	ChargingVoltage() = 0x41A0			16.632		16.968	V
				-1		+1	%
	ChargingVoltage() = 0x3130			12.466		12.717	V
				-1		+1	%
	ChargingVoltage() = 0x20D0			8.316		8.484	V
				-1		+1	%
	ChargingVoltage() = 0x1060			4.129		4.255	V
				-1.5		+1.5	%
CHARGE-CURRENT REGULATION							
CSIP-to-CSIN Full-Scale Current-Sense Voltage				78.22		83.05	mV
Charge Current and Accuracy	RS2, Figure 1 = 10mΩ; ChargingCurrent()= 0x1f80			7.822		8.305	A
				-3		+3	%
	RS2, Figure 1 = 10mΩ; ChargingCurrent() = 0x0f80			3.809		4.126	A
				-4		+4	%
	RS2, Figure 1 =10mΩ; ChargingCurrent() = 0x0080			30		400	mA
Charge-Current Gain Error	Based on ChargeCurrent() = 128mA and 8.064A			-2		+2	%
FBSA/FBSB/CSIP/CSIN Input-Voltage Range				0		19	V
Battery Quiescent Current	Adapter present, not charging, I_{CSIP} + I_{CSIN} + I_{LX} + I_{FBS}, $V_{FBS_}$ = V_{LX} = V_{CSIN} = V_{CSIP} = 19V					5	µA
	Adapter absent, I_{CSIP} + I_{CSIN} + I_{LX} + I_{FBSA} + I_{FBSB} + I_{CSSP} + I_{CSSN}, $V_{FBS_}$= V_{LX} = V_{CSIN} = V_{CSIP} = 19V, V_{DCIN} = 0V					1	
Adapter Quiescent Current	I_{DCIN} + I_{CSSP} + I_{CSSN}	$V_{Adapter}$ = 26V, $V_{Battery}$ = 16.8V, not charging				500	µA
		$V_{Adapter}$ = 19V, $V_{Battery}$ = 16.8V	Charging			1	mA
			Not charging			500	µA
		$V_{Adapter}$ = 8V, $V_{Battery}$ = 4V	Charging			1	mA
			Not charging			500	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT-CURRENT REGULATION					
CSSP-to-CSSN Full-Scale Current-Sense Voltage	$V_{FBS_}$ = 19V	103.3		116.6	mV
Input Current Accuracy	RS1, Figure 1 = 10mΩ; InputCurrent() = 11004mA or 3584mA	-6		+6	%
	RS1, Figure 1 = 10mΩ; InputCurrent() = 2048mA	-5		+5	
Input Current-Limit Gain Error	Based on InputCurrent() = 1024mA and 11004mA	-5		+5	%
Input Current-Limit Offset	Based on InputCurrent() = 1024mA and 11004mA	-1		+1	mV
CSSP/CSSN Input Voltage Range		8		26	V
IINP Transconductance	$V_{CSSP - CSSN}$ = 110mV	2.7		3.3	mA/V
IINP Offset	Based on $V_{CSSP - CSSN}$ = 110mV and 20mV	-1.5		+1.5	mV
IINP Accuracy	$V_{CSSP - CSSN}$ = 110mV	-5		+5	%
	$V_{CSSP - CSSN}$ = 55mV or 35mV	-4		+4	
	$V_{CSSP - CSSN}$ = 20mV	-10		+10	
IINP Output Voltage Range		0		3.5	V
SUPPLY AND LINEAR REGULATOR					
DCIN, Input Voltage Range		8.0		26.0	V
DCIN Undervoltage-Lockout Trip Point	DCIN falling	7			—
	DCIN rising			7.85	
POWER_FAIL Threshold	V_{CSSP} - V_{CSIN} falling	9		21	mV
	V_{CSSP} - V_{CSIN} rising	160		271	
LDO Output Voltage	8.0V < V_{DCIN} < 28V, no load	5.25		5.55	V
LDO Load Regulation	0 < I_{LDO} < 30mA			100	mV
LDO Undervoltage-Lockout Threshold	V_{DCIN} = 8.0V, V_{LDO} falling	3.20		5.15	V
V_{DD} Range		2.7		5.5	V
V_{DD} UVLO Rising				2.7	V
V_{DD} Quiescent Current	DCIN < 6V, V_{DD} = 5.5V, SCL = SDA = 5.5V			27	µA
REFERENCE					
REF Output Voltage	0 < I_{REF} < 500µA	4.053		4.139	V
REF Undervoltage-Lockout Trip Point	REF falling			3.9	V
ACOK					
ACOK Sink Current	V_{ACOK} = 0.4V, ACIN = 1.5V	1			mA

SMBus Level 2 Battery Charger with Remote Sense

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ACIN					
ACIN Threshold		2.007		2.089	V
ACIN Threshold Hysteresis		10		30	mV
REMOTE-SENSE INPUTS					
FBS_ Range	V_{CSIN} - V_{FBS}	0		200	mV
FBS_ Gain	ΔV_{CSIN} / $\Delta(V_{CSIN}$ - $V_{FBS_})$	0.9		1.1	V/V
CSIN-FBS_ Clamp Voltage		220		280	mV
FBS_ Bias Current	Charger switching, FBS_ selected			14	µA
SWITCHING REGULATOR					
Off-Time	V_{CSIN} = 16.0V, V_{CSSP} = 19V	360		440	ns
	V_{CSIN} = 16.0V, V_{CSSP} = 17V	260		350	
BST Supply Current	DHI high			800	µA
DHI On-Resistance Low	I_{DHI} = -10mA			3	Ω
DHI On-Resistance High	I_{DHI} = 10mA			5	Ω
DLO On-Resistance High	I_{DLO} = 10mA			5	Ω
DLO On-Resistance Low	I_{DLO} = -10mA			3	Ω
ERROR AMPLIFIERS					
GMV Amplifier Transconductance	ChargingVoltage() = 16.8V, $V_{FBS_}$ = 16.8V	0.0625		0.2500	mA/V
GMI Amplifier Transconductance	ChargingCurrent() = 3968mA, V_{CSIP} - V_{CSIN} = 39.68mV	0.5		2.0	mA/V
GMS Amplifier Transconductance	InputCurrent() = 3968mA, V_{CSSP} - V_{CSSN} = 79.36mV	0.5		2.0	mA/V
CCI/CCS/CCV Clamp Voltage	0.25V < $V_{CCI/S/V}$ < 2.0V	150		600	mV
LOGIC LEVELS					
SDA/SCL Input Low Voltage	V_{DD} = 2.7V to 5.5V			0.8	V
SDA/SCL Input High Voltage	V_{DD} = 2.7V to 5.5V	2.3			V
BATSEL Input Low Voltage				0.8	V
BATSEL Input High Voltage		2.3			V
SDA, Output Sink Current	$V_{(SDA)}$ = 0.4V	6			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{LX} = V_{CSSP} = V_{CSSN} = 19V, V_{BST} - V_{LX} = 4.5V, V_{FBSA} = V_{FBSB} = V_{CSIP} = V_{CSIN} = 16.8V, BATSEL = GND = PGND = 0, C_{LDO} = 1µF, V_{CC} = LDO, C_{REF} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V, ACIN = 2.5V; pins CCI, CCV, and CCS are compensated per Figure 1; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

SMB TIMING SPECIFICATION (V_{DD} = 2.7V to 5.5V) (see Figures 4 and 5)						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
SMBus Frequency	f_{SMB}		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
START Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
START Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Timeout	$t_{TIMEOUT}$	(Note 1)	25		35	ms
SCL Low Period	T_{LOW}		4.7			µs
SCL High Period	T_{HIGH}		4			µs
Maximum Charging Period Without a ChargeVoltage() or ChargeCurrent() Command			140		210	s

Note 1: Devices participating in a transfer time out when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).

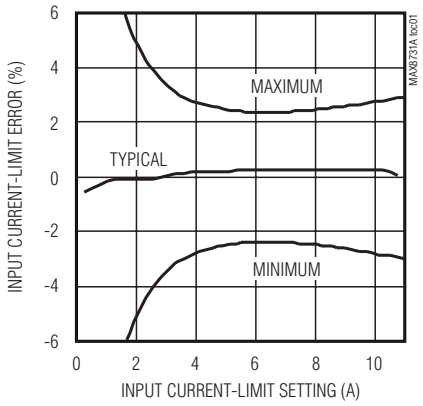
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

SMBus Level 2 Battery Charger with Remote Sense

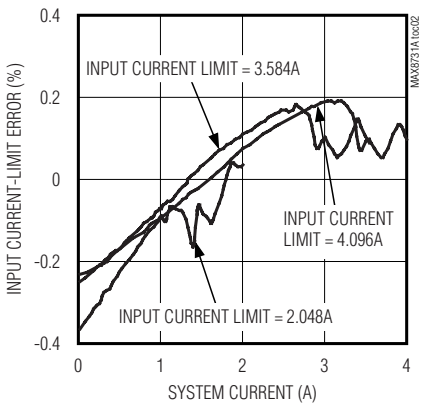
Typical Operating Characteristics

(Circuit of Figure 1, adapter = 19.5V, ChargeVoltage() = 16.8V, ChargeCurrent() = 3.854A, InputCurrent() = 3.584A, T_A = +25°C, unless otherwise noted.)

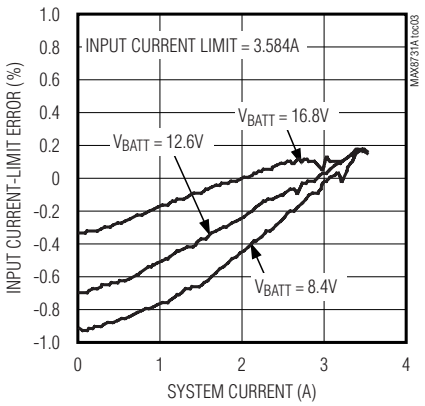
INPUT CURRENT-LIMIT ERROR vs. INPUT CURRENT-LIMIT SETTING



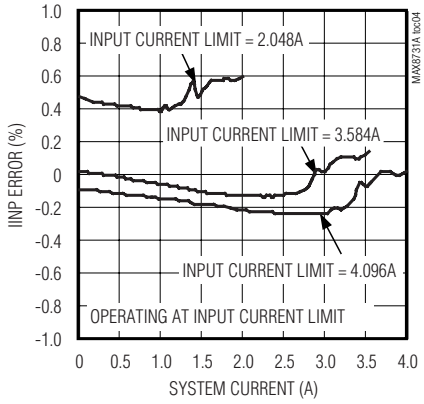
INPUT CURRENT-LIMIT ERROR vs. SYSTEM CURRENT



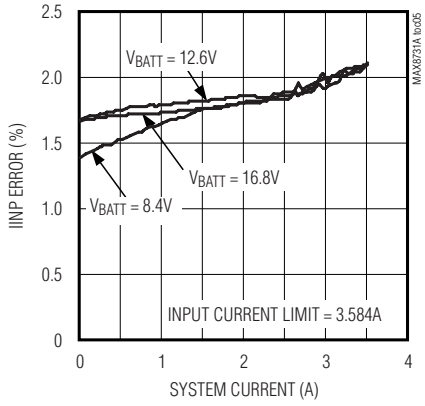
INPUT CURRENT-LIMIT ERROR vs. SYSTEM CURRENT



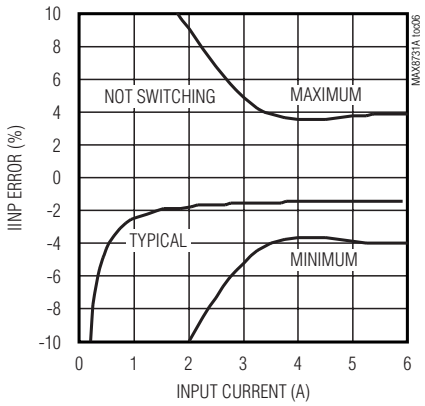
IINP ERROR vs. SYSTEM CURRENT



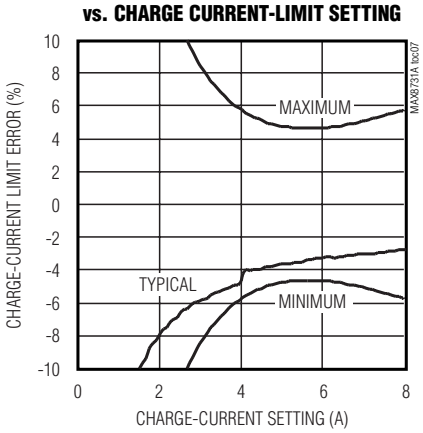
IINP ERROR vs. SYSTEM CURRENT



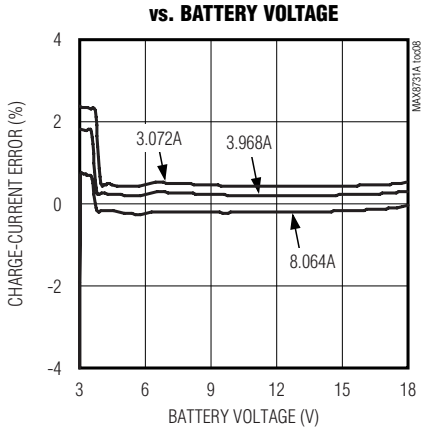
IINP ERROR vs. INPUT CURRENT



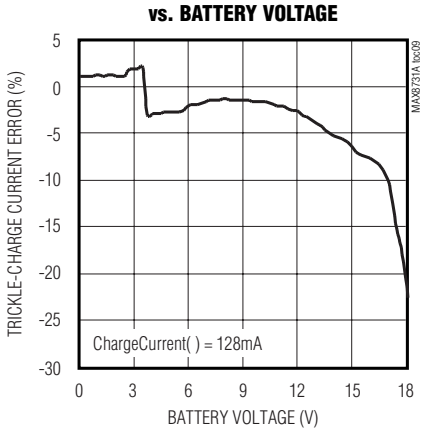
CHARGE-CURRENT ERROR vs. CHARGE CURRENT-LIMIT SETTING



CHARGE-CURRENT ERROR vs. BATTERY VOLTAGE



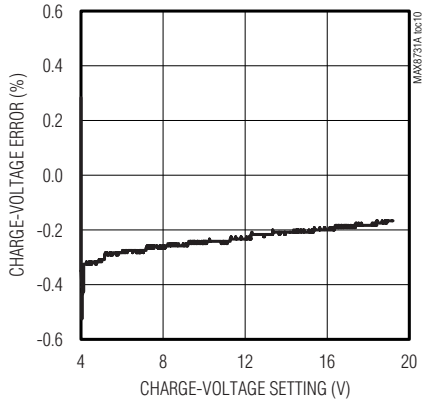
TRICKLE-CHARGE CURRENT ERROR vs. BATTERY VOLTAGE



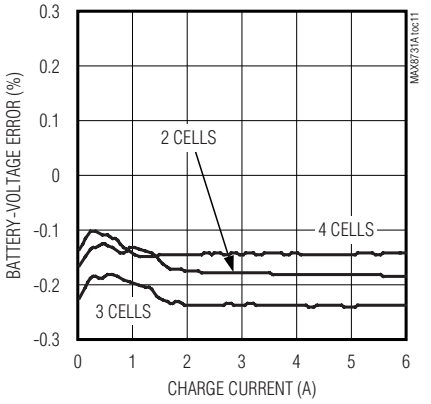
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19.5V, ChargeVoltage() = 16.8V, ChargeCurrent() = 3.854A, InputCurrent() = 3.584A, T_A = +25°C, unless otherwise noted.)

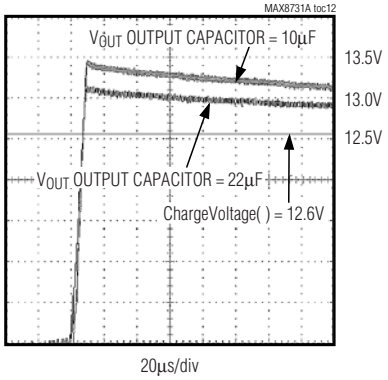
CHARGE-VOLTAGE ERROR vs. CHARGE-VOLTAGE SETTING



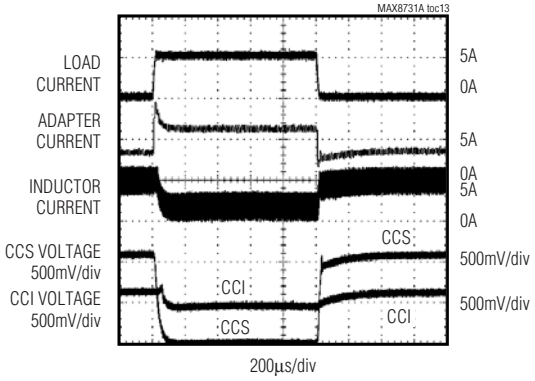
BATTERY-VOLTAGE ERROR vs. CHARGE CURRENT



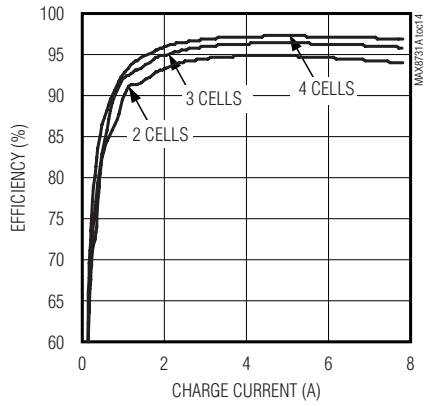
BATTERY REMOVAL



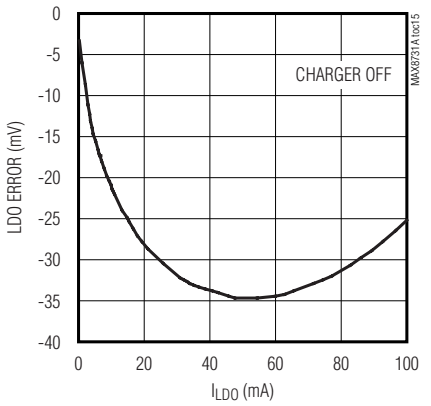
SYSTEM LOAD TRANSIENT



EFFICIENCY vs. CHARGE CURRENT



LDO LOAD REGULATION

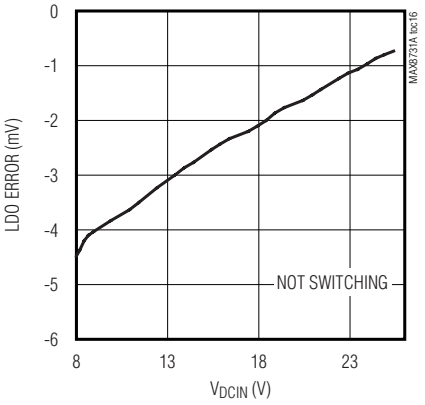


SMBus Level 2 Battery Charger with Remote Sense

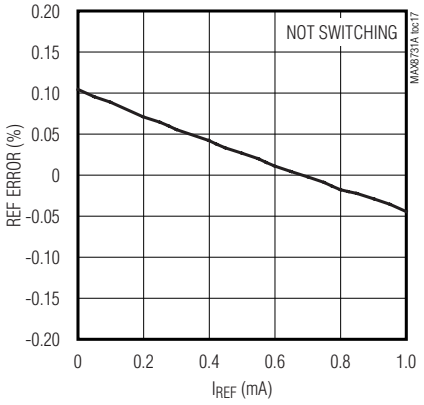
Typical Operating Characteristics (continued)

(Circuit of Figure 1, adapter = 19.5V, ChargeVoltage() = 16.8V, ChargeCurrent() = 3.854A, InputCurrent() = 3.584A, T_A = +25°C, unless otherwise noted.)

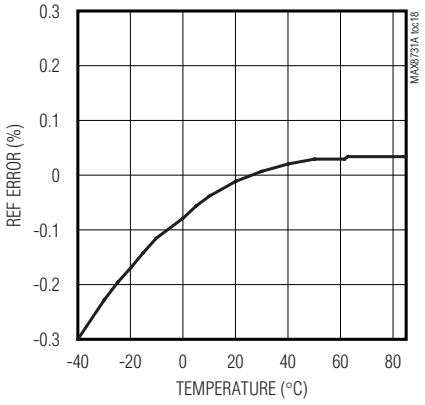
LDO LINE REGULATION



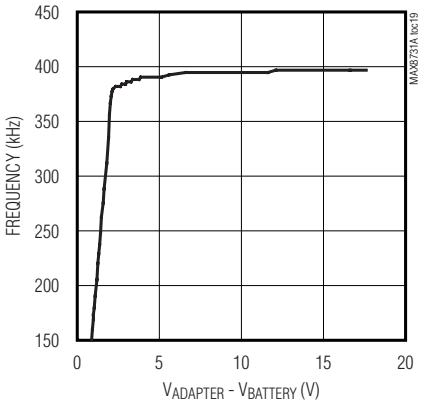
REF LOAD REGULATION



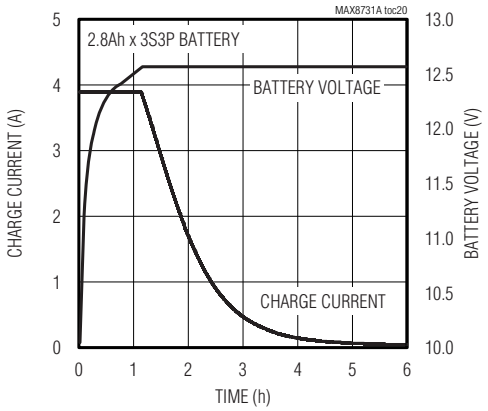
REF ERROR vs. TEMPERATURE



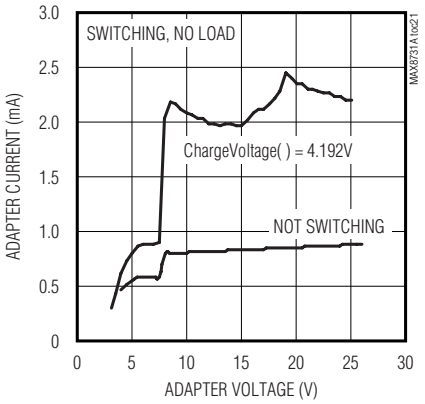
SWITCHING FREQUENCY



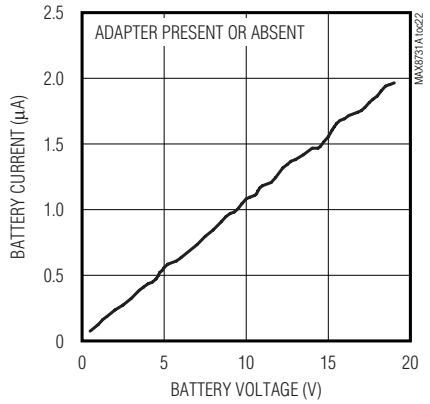
BATTERY-CHARGE CURVE



ADAPTER CURRENT vs. ADAPTER VOLTAGE



BATTERY-LEAKAGE CURRENT vs. BATTERY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 12	GND	Analog Ground. Connect directly to the paddle.
2	ACIN	AC Adapter Detect Input. ACIN is the input to an uncommitted comparator.
3	REF	4.096V Voltage Reference. Bypass REF with a 1µF capacitor to GND.
4	CCS	Input Current Regulation Loop-Compensation Point. Connect 0.01µF from CCS to GND.
5	CCI	Output Current Regulation Loop-Compensation Point. Connect 0.01µF from CCI to GND.
6	CCV	Voltage Regulation Loop-Compensation Point. Connect 10kΩ in series with 0.01µF to GND.
7	DAC	DAC Voltage Output. Bypass with 0.1µF from DAC to GND.
8	IINP	Input Current Monitor Output. IINP sources the current proportional to the current sensed across CSSP and CSSN. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
9	SDA	SMBus Data I/O. Open-drain output. Connect an external pullup resistor according to SMBus specifications.
10	SCL	SMBus Clock Input. Connect an external pullup resistor according to SMBus specifications.
11	V_{DD}	Logic Circuitry Supply-Voltage Input. Bypass with a 0.1µF capacitor to GND.
13	ACOK	AC Detect Output. This open-drain output is high impedance when ACIN is greater than REF/2. The ACOK output remains low when the MAX8731A is powered down. Connect a 10kΩ pullup resistor from V_{CC} to ACOK.
14	BATSEL	Battery Voltage Select Input. Drive BATSEL high to select battery B, or drive BATSEL low to select battery A. Any change of BATSEL immediately stops charging. Charging begins again in approximately 10ms.
15	FBSA	Remote-Sense Input for the Output Voltage of Battery A. Connect a 100Ω resistor from FBSA to the battery connector, and a 10nF capacitor from FBSA to PGND.
16	FBSB	Remote-Sense Input for the Output Voltage of Battery B. Connect a 100Ω resistor from FBSB to the battery connector, and a 10nF capacitor from FBSB to PGND.
17	CSIN	Charge Current-Sense Negative Input
18	CSIP	Charge Current-Sense Positive Input. Connect a 10mΩ current-sense resistor between CSIP and CSIN.
19	PGND	Power Ground
20	DLO	Low-Side Power MOSFET Driver Output. Connect to low-side n-channel MOSFET. DLO drives between LDO and PGND.
21	LDO	Linear-Regulator Output. LDO is the output of the 5.4V linear regulator supplied from DCIN. LDO also directly supplies the DLO driver and the BST charge pump. Bypass with a 1µF ceramic capacitor from LDO to PGND.
22	DCIN	Charger Bias Supply Input. Bypass DCIN with a 0.1µF capacitor to PGND.
23	LX	High-Side Power MOSFET Driver Source Connection. Connect to the source of the high-side n-channel MOSFET.
24	DHI	High-Side Power MOSFET Driver Output. Connect to the high-side n-channel MOSFET gate.
25	BST	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BST to LX.
26	V_{CC}	Device Power-Supply Input. Connect to LDO through an RC filter as shown in Figure 1.
27	CSSN	Input Current-Sense Negative Input
28	CSSP	Input Current-Sense Positive Input. Connect a 10mΩ current-sense resistor between CSSP and CSSN.
—	BP	Backside Paddle. Connect the backside paddle to analog ground.

SMBus Level 2 Battery Charger with Remote Sense

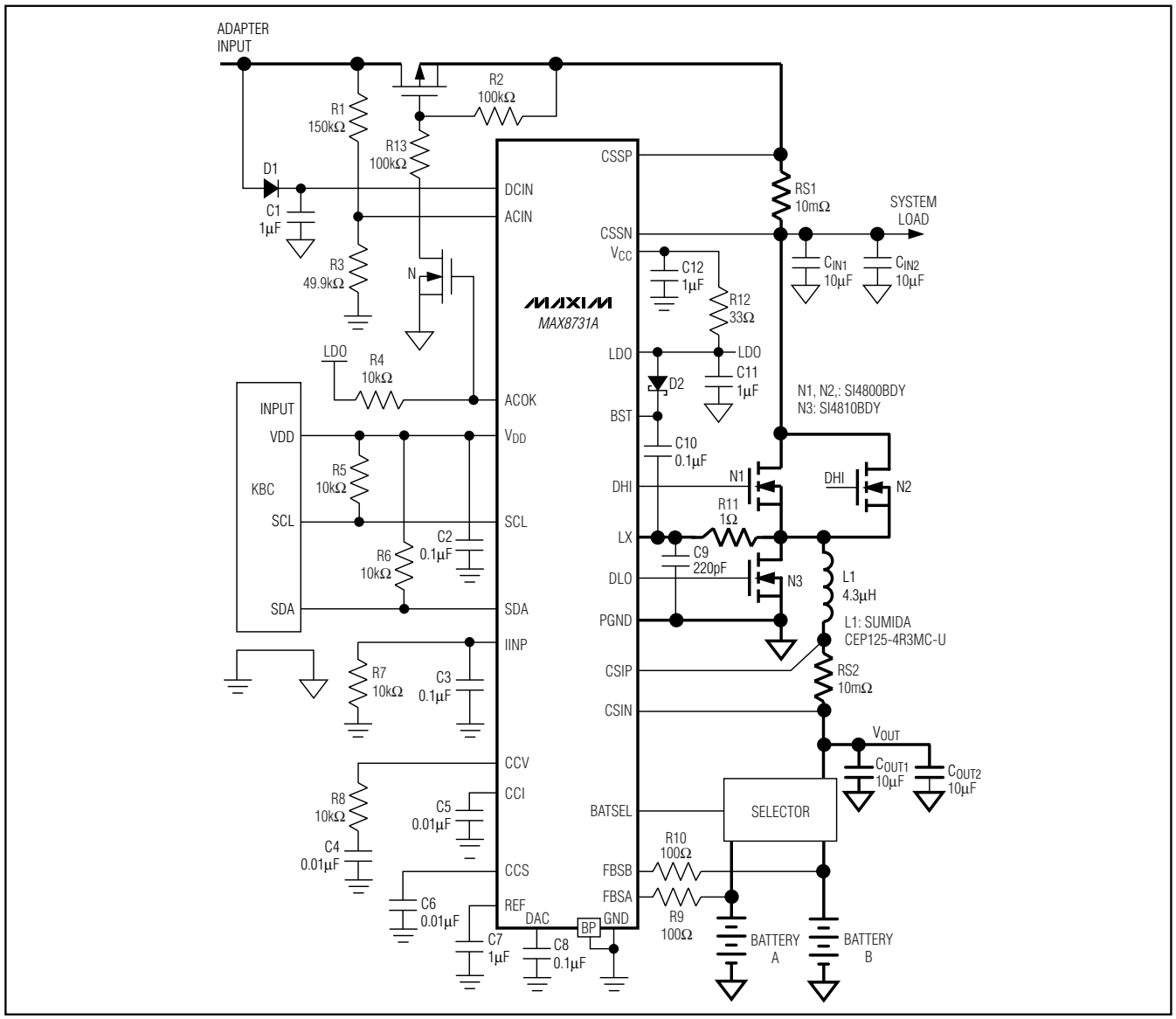


Figure 1. Typical Dual-Battery Application Circuit

Detailed Description

The typical application circuit is shown in Figure 1. The MAX8731A includes all the functions necessary to charge Li+, NiMH, and NiCd smart batteries. A high-efficiency, synchronous-rectified, step-down DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The DC-DC converter drives a high-side n-channel MOSFET and provides synchronous rectification with a low-side n-channel MOSFET. The charge current and input current-sense amplifiers have low input-offset error (±64µV typ), allowing the use of small-valued sense resistors.

The MAX8731A features a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors either FBSA or FBSB to ensure that its voltage never exceeds the voltage set by the ChargeVoltage() command. The CCI battery current-regulation loop monitors the current delivered to the selected battery to ensure that it never exceeds the current limit set by the ChargeCurrent()

command. The charge current-regulation loop is in control as long as the selected battery voltage is below the charge voltage set point. When the selected battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the adapter current exceeds the input current limit set by the InputCurrent() command.

A functional diagram is shown in Figure 2.

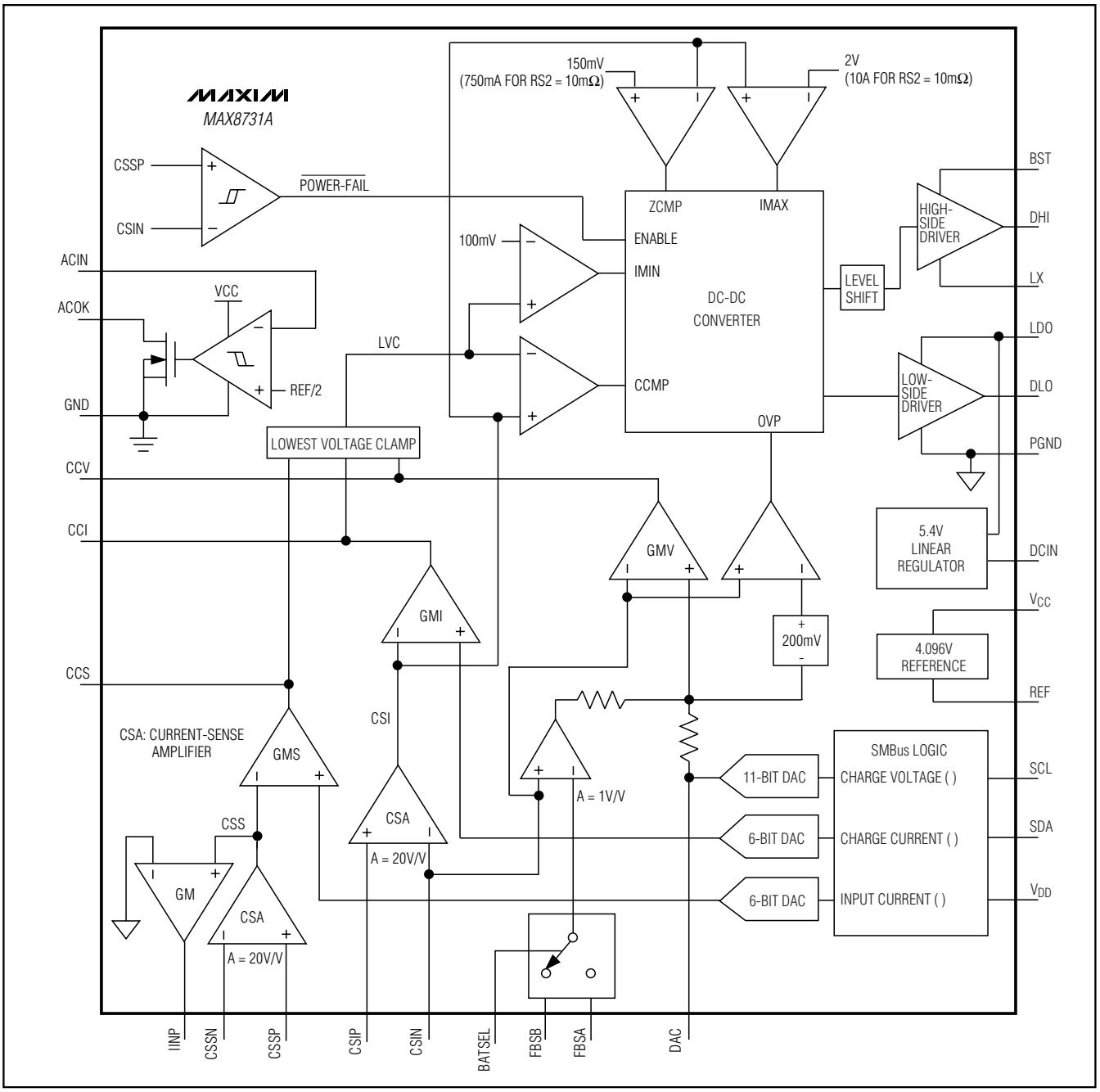


Figure 2. Functional Diagram

SMBus Level 2 Battery Charger with Remote Sense

Setting Charge Voltage

To set the output voltage, use the SMBus to write a 16-bit ChargeVoltage() command using the data format listed in Table 1. The ChargeVoltage() command uses the Write-Word protocol (see Figure 3). The command code for ChargeVoltage() is 0x15 (0b00010101). The MAX8731A provides a 1.024V to 19.200V charge voltage range, with 16mV resolution. Set ChargeVoltage() below 1.024V to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both DHI and DLO remain low until the charger is restarted.

Table 1. ChargeVoltage () (0x15)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally a 8mV weight.
4	Charge voltage, DACV 0	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 16mV of charger voltage compliance.
5	Charge voltage, DACV 1	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 32mV of charger voltage compliance.
6	Charge voltage, DACV 2	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 64mV of charger voltage compliance.
7	Charge voltage, DACV 3	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 128mV of charger voltage compliance.
8	Charge voltage, DACV 4	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 256mV of charger voltage compliance.
9	Charge voltage, DACV 5	0 = Adds 0mV of charger voltage compliance, 1024mV min. 1 = Adds 512mV of charger voltage compliance.
10	Charge voltage, DACV 6	0 = Adds 0mA of charger voltage compliance. 1 = Adds 1024mV of charger voltage compliance.
11	Charge voltage, DACV 7	0 = Adds 0mV of charger voltage compliance. 1 = Adds 2048mV of charger voltage compliance.
12	Charge voltage, DACV 8	0 = Adds 0mV of charger voltage compliance. 1 = Adds 4096mV of charger voltage compliance.
13	Charge voltage, DACV 9	0 = Adds 0mV of charger voltage compliance. 1 = Adds 8192mV of charger voltage compliance.
14	Charge voltage, DACV 10	0 = Adds 0mV of charger voltage compliance. 1 = Adds 16,384mV of charger voltage compliance, 19,200mV max.
15	—	Not used. Normally a 32,768mV weight.

Setting Charge Current

To set the charge current, use the SMBus to write a 16-bit ChargeCurrent() command using the data format listed in Table 2. The ChargeCurrent() command uses the Write-Word protocol (see Figure 3). The command code for ChargeCurrent() is 0x14 (0b00010100). When RS2 =10mΩ, the MAX8731A provides a charge current range of 128mA to 8.064A, with 128mA resolution. Set ChargeCurrent() to 0 to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() commands are sent. Both DHI and DLO remain low until the charger is restarted.

The MAX8731A includes a foldback current limit when the battery voltage is low. If the battery voltage is less than 2.5V, the charge current is temporarily set to 128mA. The ChargeCurrent() register is preserved and becomes active again when the battery voltage is higher than 2.5V. This function effectively provides a foldback current limit, which protects the charger during short circuit and overload.

Setting Input-Current Limit

System current normally fluctuates as portions of the system are powered up or put to sleep. By using the input-current-limit circuit, the output-current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current, from a wall cube or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the MAX8731A decreases the charge current to provide priority to system load current. As the system supply rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit.

The internal amplifier compares the differential voltage between CSSP and CSSN to a scaled voltage set by the InputCurrent() command (see Table 3). The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as follows:

Table 2. ChargeCurrent() (0x14) (10mΩ Sense Resistor, RS2)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mA weight.
1	—	Not used. Normally a 2mA weight.
2	—	Not used. Normally a 4mA weight.
3	—	Not used. Normally an 8mA weight.
4	—	Not used. Normally a 16mA weight.
5	—	Not used. Normally a 32mA weight.
6	—	Not used. Normally a 64mA weight.
7	Charge Current, DACI 0	0 = Adds 0mA of charger current compliance. 1 = Adds 128mA of charger current compliance.
8	Charge Current, DACI 1	0 = Adds 0mA of charger current compliance. 1 = Adds 256mA of charger current compliance.
9	Charge Current, DACI 2	0 = Adds 0mA of charger current compliance. 1 = Adds 512mA of charger current compliance.
10	Charge Current, DACI 3	0 = Adds 0mA of charger current compliance. 1 = Adds 1024mA of charger current compliance.
11	Charge Current, DACI 4	0 = Adds 0mA of charger current compliance. 1 = Adds 2048mA of charger current compliance.
12	Charge Current, DACI 5	0 = Adds 0mA of charger current compliance. 1 = Adds 4096mA of charger current compliance, 8064mA max.
13	—	Not used. Normally a 8192mA weight.
14	—	Not used. Normally a 16,386mA weight.
15	—	Not used. Normally a 32,772mA weight.

SMBus Level 2 Battery Charger with Remote Sense

$$I_{INPUT} = I_{LOAD} + \left[\frac{(I_{CHARGE} \times V_{BATTERY})}{(V_{IN} \times \eta)}\right] + I_{BIAS}$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

To set the input current limit, use the SMBus to write a 16-bit InputCurrent() command using the data format listed in Table 3. The InputCurrent() command uses the Write-Word protocol (see Figure 3). The command code for InputCurrent() is 0x3F (0b00111111). When RS1 = 10mΩ, the MAX8731A provides an input-current-limit range of 256mA to 11.004A, with 256mA resolution. InputCurrent() settings from 1mA to 256mA result in a current limit of 256mA. Upon reset the input current limit is 256mA.

Charger Timeout

The MAX8731A includes a timer to terminate charging if the charger does not receive a ChargeVoltage() or ChargeCurrent() command within 175s. If a timeout occurs, both ChargeVoltage() and ChargeCurrent() commands must be resent to reenable charging.

Remote Sense

The MAX8731A features dual remote sense, which allows the rejection of board resistance and selector resistance when used in either single- or dual-battery systems. To fully utilize remote sensing, connect FBS_ directly to the battery interface through an unshared battery sense trace in series with a 100Ω resistor, and 10nF capacitor (see Figure 1). In single-battery systems, connect BATSEL directly to GND and use only FBSA.

Remote sensing cancels the effect of impedance in series with the battery. This impedance normally causes the battery charger to prematurely enter constant-voltage mode with reducing charge current. The result is that the last 20% of charging takes longer than necessary. When in constant-voltage mode, the remaining charge time is proportional to the total resistance in series with the battery. Remote sensing reduces charge time according to the following equation:

$$t_{CVRS} = t_{CV0} \times \frac{R_{Pack}}{R_{Pack} + R_{Board}}$$

Table 3. InputCurrent() (0x3F) (10mΩ Sense Resistor, RS1)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 2mA weight.
1	—	Not used. Normally a 4mA weight.
2	—	Not used. Normally an 8mA weight.
3	—	Not used. Normally a 16mA weight.
4	—	Not used. Normally a 32mA weight.
5	—	Not used. Normally a 64mA weight.
6	—	Not used. Normally a 128mA weight.
7	Input Current, DACS 0	0 = Adds 0mA of input current compliance. 1 = Adds 256mA of input current compliance.
8	Input Current, DACS 1	0 = Adds 0mA of input current compliance. 1 = Adds 512mA of input current compliance.
9	Input Current, DACS 2	0 = Adds 0mA of input current compliance. 1 = Adds 1024mA of input current compliance.
10	Input Current, DACS 3	0 = Adds 0mA of input current compliance. 1 = Adds 2048mA of input current compliance.
11	Input Current, DACS 4	0 = Adds 0mA of input current compliance. 1 = Adds 4096mA of input current compliance.
12	Input Current, DACS 5	0 = Adds 0mA of input current compliance. 1 = Adds 8192mA of input current compliance, 11,004mA max.
13	—	Not used. Normally a 16,384mA weight.
14	—	Not used. Normally a 32,768mA weight.
15	—	Not used. Normally a 65,536mA weight.

where R_{Pack} is the total resistance in the battery pack, R_{Board} is the board resistance in series with the battery charge path, t_{CV0} is the constant-voltage charge time without remote sense, and t_{CVRS} is the constant-voltage charge time with remote sense.

The MAX8731A includes a safety feature, which limits the charge voltage when FBS_ or the selector is disconnected. The MAX8731A guarantees that CSIN does not regulate more than 250mV above the selected charging voltage. This also limits the extent to which remote sense can cancel charge-path impedance.

Input Current Measurement

Use IINP to monitor the system-input current sensed across CSSP and CSSN. The voltage at IINP is proportional to the input current by the equation:

$$V_{IINP} = I_{INPUT} \times RS1 \times G_{IINP} \times R8$$

where I_{INPUT} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of IINP (3mA/V typ), and R8 is the resistor connected between IINP and ground. Typically, IINP has a 0 to 3.5V output voltage range. Leave IINP open if not used.

LDO Regulator

An integrated low-dropout (LDO) linear regulator provides a 5.4V supply derived from DCIN, and delivers over 30mA of load current. The LDO powers the gate drivers of the n-channel MOSFETs. See the *MOSFET Drivers* section. LDO has a minimum current limit of 35mA. This allows the MAX8731A to work with 87nC of total gate charge (both high-side and low-side MOSFETs). Bypass LDO to PGND with a 1µF or greater ceramic capacitor.

AC Adapter Detection

The MAX8731A includes a hysteretic comparator that detects the presence of an AC power adapter. When ACIN is greater than 2.048V, the open-drain ACOK output becomes high impedance. Connect 10kΩ pullup resistance between LDO and ACOK. Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Select the resistive voltage-divider not to exceed the 6V absolute maximum rating of ACIN.

V_{DD} Supply

The V_{DD} input provides power to the SMBus interface. Connect V_{DD} to LDO, or apply an external supply to V_{DD} to keep the SMBus interface active while the supply to DCIN is removed. When V_{DD} is biased the internal registers are maintained. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.

Operating Conditions

The MAX8731A has the following operating states:

- **Adapter Present:** When DCIN is greater than 7.5V, the adapter is considered to be present. In this condition, both the LDO and REF function properly and battery charging is allowed:

  a) Charging: The total MAX8731A quiescent current when charging is 1mA (max) plus the current required to drive the MOSFETs.

  b) Not Charging: To disable charging, set either ChargeCurrent() or ChargeVoltage() to zero. When the adapter is present and charging is disabled, the total adapter quiescent current is less than 1mA and the total battery quiescent current is less than 5µA.

- **Adapter Absent (Power Fail):** When V_{CSSP} is less than V_{CSIN} + 10mV, the MAX8731A is in the power-fail state, since the DC-DC converter is in dropout. The charger does not attempt to charge in the power-fail state. Typically, this occurs when the adapter is absent. When the adapter is absent, the total MAX8731A quiescent battery current is less than 1µA (max).

- **V_{DD} Undervoltage (POR):** When V_{DD} is less than 2.5V, the V_{DD} supply is in an undervoltage state and the internal registers are in their POR state. The SMBus interface does not respond to commands. When V_{DD} rises above 2.5V, the MAX8731A is in a power-on reset state. Charging does not occur until the ChargeVoltage() and ChargeCurrent() commands are sent. When V_{DD} is greater than 2.5V, SMBus registers are preserved.

The MAX8731A allows charging under the following conditions:

1) DCIN > 7.5V, LDO > 4V, REF > 3.1V
2) $V_{CSSP} > V_{CSIN}$ + 210mV (15mV falling threshold)
3) V_{DD} > 2.5V

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SMBus Interface

The MAX8731A receives control inputs from the SMBus interface. The MAX8731A uses a simplified subset of the commands documented in System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The MAX8731A uses the SMBus Read-Word and Write-Word protocols (Figure 3) to communicate with the smart battery. The MAX8731A performs only as an SMBus slave device with address 0b0001001_ (0x12) and does not initiate communication on the bus. In addition, the MAX8731A has two identification (ID) registers (0xFE): a 16-bit device ID register and a 16-bit manufacturer ID register (0xFF).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors (10kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figures 4 and 5 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX8731A because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The MAX8731A supports the charger commands as described in Table 4.

a) WRITE-WORD FORMAT

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	
	PRESET TO 0b0001001			ChargerMode() = 0x12 ChargeCurrent() = 0x14 ChargeVoltage() = 0x15 AlarmWarning() = 0x16 InputCurrent() = 0x3F		D7 D0		D15 D8		

b) READ-WORD FORMAT

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	
	Preset to 0b0001001			ChargerSpecInfo() = 0x11 ChargerStatus() = 0x13			PRESET TO 0b0001001			D7 D0		D15 D8		

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 3. SMBus Write-Word and Read-Word Protocols

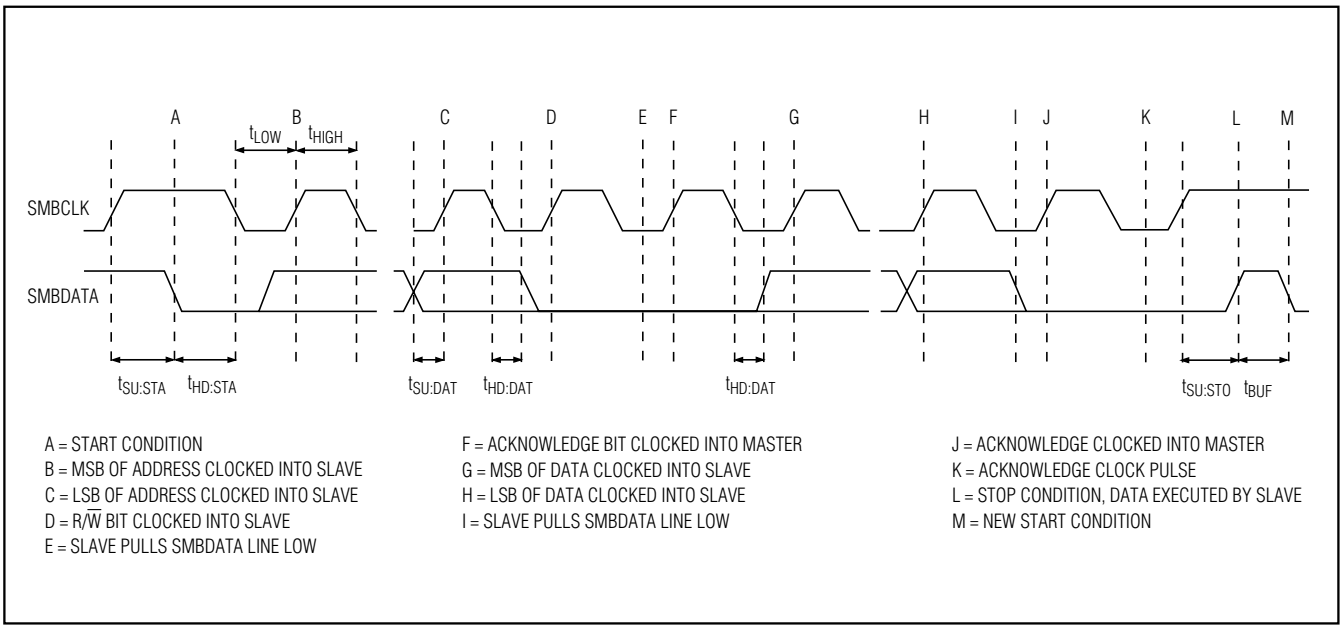


Figure 4. SMBus Write Timing

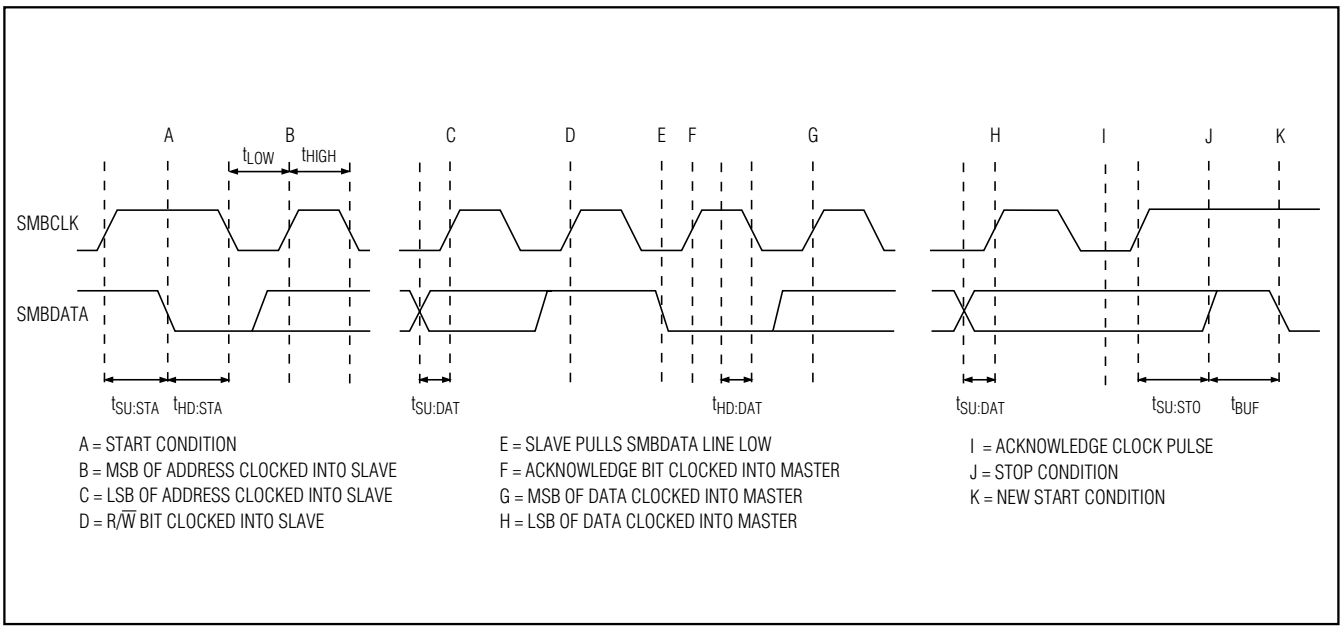


Figure 5. SMBus Read Timing

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Table 4. Battery-Charger Command Summary

COMMAND	COMMAND NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent()	Write Only	6-Bit Charge-Current Setting	0x0000
0x15	ChargeVoltage()	Write Only	11-Bit Charge-Voltage Setting	0x0000
0x3F	InputCurrent()	Write Only	6-Bit Charge-Current Setting	0x0080
0xFE	ManufacturerID()	Read Only	Manufacturer ID	0x004D
0xFF	DeviceID()	Read Only	Device ID	0x0008

Battery-Charger Commands

The MAX8731A supports four battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 4. ManufacturerID() and DeviceID() can be used to identify the MAX8731A. On the MAX8731A, the ManufacturerID() command always returns 0x004D and the DeviceID() command always returns 0x0008.

DC-DC Converter

The MAX8731A employs a synchronous step-down DC-DC converter with an n-channel high-side MOSFET switch and an n-channel low-side synchronous rectifier. The MAX8731A features a pseudo-fixed-frequency, current-mode control scheme with cycle-by-cycle current limit. The controller's constant off-time (t_{OFF}) is calculated based on V_{CSSP}, V_{CSIN}, and a time constant with a minimum value of 300ns. The MAX8731A can also operate in discontinuous-conduction mode for improved light-load efficiency. The operation of the DC-DC controller is determined by the following four comparators as shown in the functional diagrams in Figures 2 and 6:

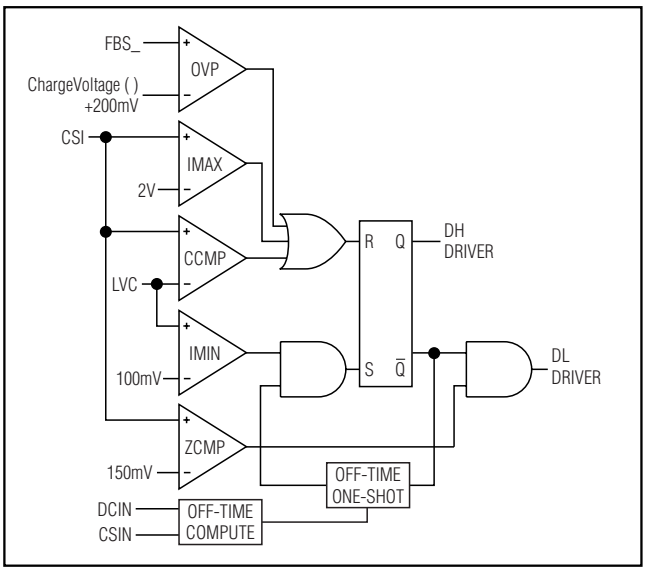


Figure 6. DC-DC Converter Functional Diagram

The **IMIN** comparator triggers a pulse in discontinuous mode when the accumulated error is too high. IMIN compares the control signal (LVC) against 100mV (typ). When LVC is less than 100mV, DHI and DLO are both forced low. Indirectly, IMIN sets the peak inductor current in discontinuous mode.

The **CCMP** comparator is used for current-mode regulation in continuous-conduction mode. CCMP compares LVC against the inductor current. The high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.

The **IMAX** comparator provides a secondary cycle-by-cycle current limit. IMAX compares CSI to 2V (corresponding to 10A when RS2 = 10mΩ). The high-side MOSFET on-time is terminated when the current-sense signal exceeds 10A. A new cycle cannot start until the IMAX comparator's output goes low.

The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 750mA (RS2 = 10mΩ). When the inductor current is lower than the 750mA threshold, the comparator output is high and DLO is turned off.

The **OVP** comparator is used to prevent overvoltage at the output due to battery removal. OVP compares FBS_ against the set voltage (ChargeVoltage()). When FBS_ is 200mV above the set value, the OVP comparator output goes high and the high-side MOSFET on-time is terminated. DHI and DLO remain off until the OVP condition is removed.

CCV, CCI, CCS, and LVC Control Blocks

The MAX8731A controls input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops—CCV, CCI, and CCS—are brought together internally at the lowest voltage-clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the

control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section).

Continuous-Conduction Mode

With sufficient charge current, the MAX8731A's inductor current never crosses zero, which is defined as continuous-conduction mode. The regulator switches at 400kHz (nominal) if $V_{CSIN} < 0.88 \times V_{CSSP}$. The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon V_{CSIN} and V_{CSSP}. The off-time is set by the following equation:

$$t_{OFF} = 2.5\mu s \times \frac{V_{CSSP} - V_{CSIN}}{V_{CSSP}}$$

The on-time can be determined using the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

The switching frequency can then be calculated:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}}$$

These equations describe the controller's pseudo-fixed-frequency performance over the most common operating conditions.

At the end of the fixed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 100mV and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the controller to initiate a new cycle. If the peak inductor current exceeds the IMAX comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

If during the off-time the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. ZCOMP causes the MAX8731A to enter into discontinuous-conduction mode (see the *Discontinuous Conduction* section).

There is a 0.3µs minimum off-time when the (V_{CSSP} - V_{CSIN}) differential becomes too small. If $V_{CSIN} \geq 0.88 \times V_{CSSP}$, the threshold for the 0.3µs minimum off-time is reached. The switching frequency in this mode varies according to the equation:

$$f = \frac{1}{\frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}} + 0.3\mu s}$$

Discontinuous Conduction

The MAX8731A can also operate in discontinuous-conduction mode to ensure that the inductor current is always positive. The MAX8731A enters discontinuous-conduction mode when the output of the LVC control point falls below 100mV. This corresponds to peak inductor current = 500mA:

$$I_{CHG} = \frac{1}{2} \times \frac{100mV}{20 \times RS2} = 250mA$$

charge current for RS2 = 10mΩ.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 100mV. Discontinuous-mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

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Compensation

The charge-voltage and charge-current regulation loops are independent and compensated separately at the CCV, CCI, and CCS.

CCV Loop Compensation

The simplified schematic in Figure 7 is sufficient to describe the operation of the MAX8731A when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with C_{CV} and R_{CV}. The zero is necessary to compensate the pole formed by the output capacitor and the load. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = \Delta V_{BATT} / \Delta I_{CHG}$. The equivalent output impedance of the GMV amplifier, R_{OGMV}, is greater than 10MΩ. The voltage amplifier transconductance, GMV = 0.125µA/mV. The DC-DC converter transconductance is dependent upon the charge-current sense resistor RS2:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

where A_{CSI} = 20V/V, and RS2 = 10mΩ in the typical application circuits, so GM_{OUT} = 5A/V. The loop-transfer function is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \frac{(1+sC_{OUT} \times R_{ESR})(1+sC_{CV} \times R_{CV})}{(1+sC_{CV} \times R_{OGMV})(1+sC_{OUT} \times R_L)}$$

The poles and zeros of the voltage loop-transfer function are listed from lowest frequency to highest frequency in Table 5.

Near crossover C_{CV} is much lower impedance than R_{OGMV}. Since C_{CV} is in parallel with R_{OGMV}, C_{CV} dominates the parallel impedance near crossover. Additionally, R_{CV} is much higher impedance than C_{CV} and dominates the series combination of R_{CV} and C_{CV}, so near crossover:

$$\frac{R_{OGMV} \times (1+sC_{CV} \times R_{CV})}{(1+sC_{CV} \times R_{OGMV})} \cong R_{CV}$$

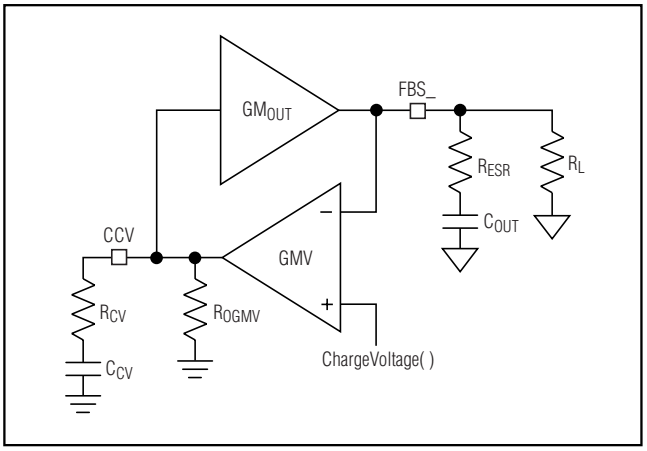


Figure 7. CCV Loop Diagram

Table 5. CCV Loop Poles and Zeros

NAME	EQUATION	DESCRIPTION
CCV Pole	$f_{P_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}}$	Lowest frequency pole created by C_{CV} and GMV's finite output resistance.
CCV Zero	$f_{Z_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$	Voltage-loop compensation zero. If this zero is at the same frequency or lower than the output pole f_{P_OUT}, then the loop-transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least 1 decade below crossover to ensure adequate phase margin.
Output Pole	$f_{P_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output pole formed with the effective load resistance R_L and the output capacitance C_{OUT}. R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
Output Zero	$f_{P_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency; therefore, choose a capacitor with an ESR zero greater than the crossover frequency.

C_{OUT} is also much lower impedance than R_L near crossover so the parallel impedance is mostly capacitive and:

$$\frac{R_L \cdot}{(1+sC_{OUT} \times R_L)} \cong \frac{1}{sC_{OUT}}$$

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop-transfer function can be simplified as follows:

$$LTF = GM_{OUT} \times \frac{R_{CV}}{sC_{OUT}} G_{MV}$$

Setting LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO_CV} = GM_{OUT} \times G_{MV} \times \frac{R_{CV}}{2\pi \times C_{OUT}}$$

For stability, choose a crossover frequency lower than 1/10 the switching frequency. For example, choose a crossover frequency of 50kHz and solve for R_{VC} using the component values listed in Figure 1 to yield R_{CV} = 10kΩ:

$$R_{CV} = \frac{2\pi \times C_{OUT} \times f_{CO_CV}}{GMV \times GM_{OUT}} \cong 10k\Omega$$

GMV = 0.125µA/mV

GM_{OUT} = 5A/V

C_{OUT} = 2 x 10µF

F_{OSC} = 400kHz

R_L = 0.2Ω

F_{CO_CV} = 50kHz

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z_CV} \le f_{P_OUT}$:

$$C_{CV} \ge (R_L / R_{CV})\, C_{OUT}$$

C_{CV} ≥ 400pF (assuming 2 cells and 2A maximum charge current.)

Figure 8 shows the Bode plot of the voltage-loop frequency response using the values calculated above.

CCI Loop Compensation

The simplified schematic in Figure 9 is sufficient to describe the operation of the MAX8731A when the battery current loop (CCI) is in control. Since the output capacitor's impedance has little effect on the response of the current loop, only a simple single pole is required to compensate this loop. A_{CSI} is the internal gain of the current-sense amplifier. RS2 is the charge current-sense resistor (10mΩ). R_{OGMI} is the equivalent output impedance of the GMI amplifier, which is greater than 10MΩ. GMI is the charge-current amplifier transconductance = 1µA/mV. GM_{OUT} is the DC-DC converter transconductance = 5A/V.

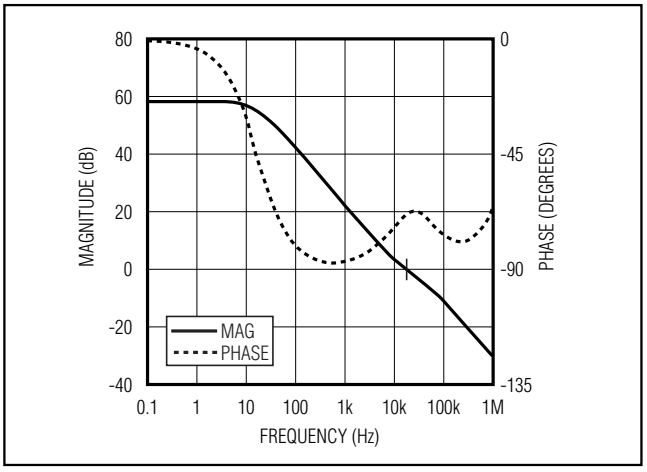


Figure 8. CCV Loop Response

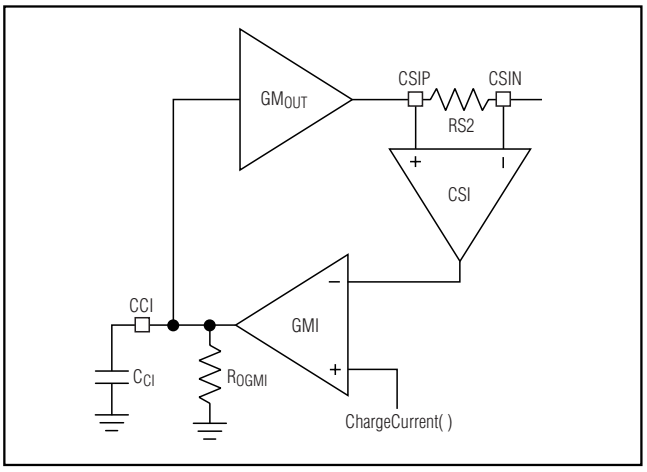


Figure 9. CCI Loop Diagram

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The loop-transfer function is given by:

$$LTF = GM_{OUT} \times A_{CSI} \times RS2 \times GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

This describes a single-pole system. Since:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

the loop-transfer function simplifies to:

$$LTF = GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

The crossover frequency is given by:

$$f_{CO_CI} = \frac{GMI}{2\pi C_{CI}}$$

For stability, choose a crossover frequency lower than 1/10 the switching frequency:

$C_{CI} > 10 \times GMI / (2\pi f_{OSC}) = 4nF$, for a 400kHz switching frequency.

Values for C_{CI} greater than 10 times the minimum value can slow down the current-loop response. Choosing C_{CI} = 10nF yields a crossover frequency of 15.9kHz. Figure 10 shows the Bode plot of the current-loop frequency response using the values calculated above.

CCS Loop Compensation

The simplified schematic in Figure 11 is sufficient to describe the operation of the MAX8731A when the input current-limit loop (CCS) is in control. Since the output capacitor's impedance has little effect on the response of the input current-limit loop, only a single pole is required to compensate this loop. A_{CSS} is the internal gain of the current-sense resistor; RS1 = 10mΩ in the typical application circuits. R_{OGMS} is the equivalent output impedance of the GMS amplifier, which is greater than 10MΩ. GMS is the charge-current amplifier transconductance = 1µA/mV. GM_{IN} is the DC-DC converter's input-referred transconductance = (1/D) x GM_{OUT} = (1 / D) x 5A/V.

The loop-transfer function is given by:

$$LTF = GM_{IN} \times A_{CSS} \times RSI \times GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}}$$

Since:

$$GM_{IN} = \frac{1}{A_{CSS} \times RS2}$$

the loop-transfer function simplifies to:

$$LTF = GMS \frac{R_{OGMS}}{1 + SR_{OGMS} \times C_{CS}}$$

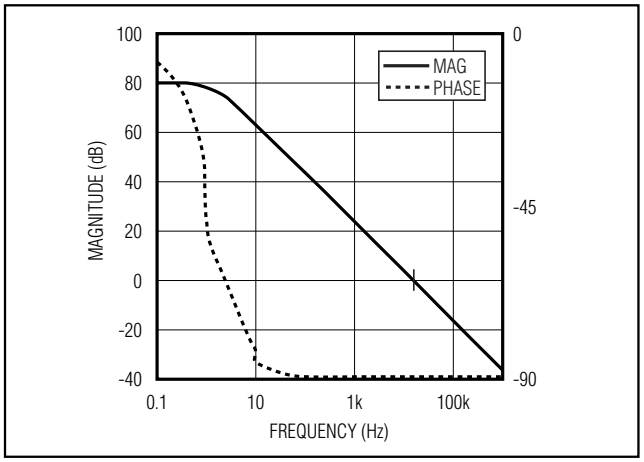


Figure 10. CCI Loop Response

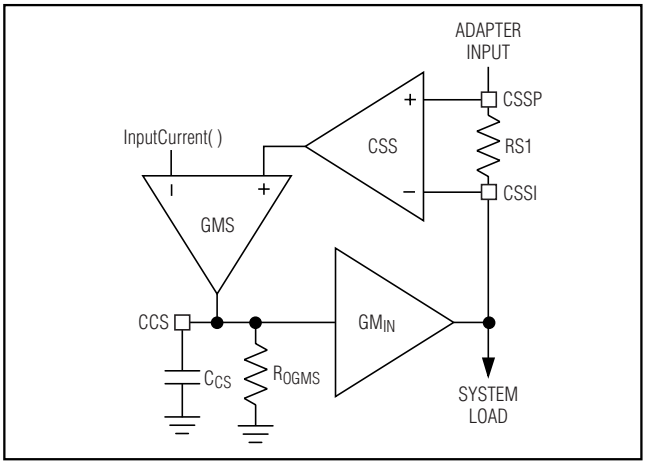


Figure 11. CCS Loop Diagram

The crossover frequency is given by:

$$f_{CO_CS} = \frac{GMS}{2\pi C_{CS}}$$

For stability, choose a crossover frequency lower than 1/10 the switching frequency:

$$C_{CS} = 5 \times GMS / (2\pi f_{OSC})$$

Choosing a crossover frequency of 30kHz and using the component values listed in Figure 1 yields C_{CS} > 5.4nF. Values for CCS greater than 10 times the minimum value may slow down the current-loop response excessively. Figure 12 shows the Bode plot of the input current-limit-loop frequency response using the values calculated above.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-sides switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate to prevent shoot-through. Otherwise, the sense circuitry in the MAX8731A interprets the MOSFET gate as "off" while there is still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares or less (1.25mm to 2.5mm wide if the MOSFET is 25mm from the device). Unlike the DLO output, the DHI output uses a 50ns (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same considerations should be used for routing the DHI signal to the high-side MOSFET.

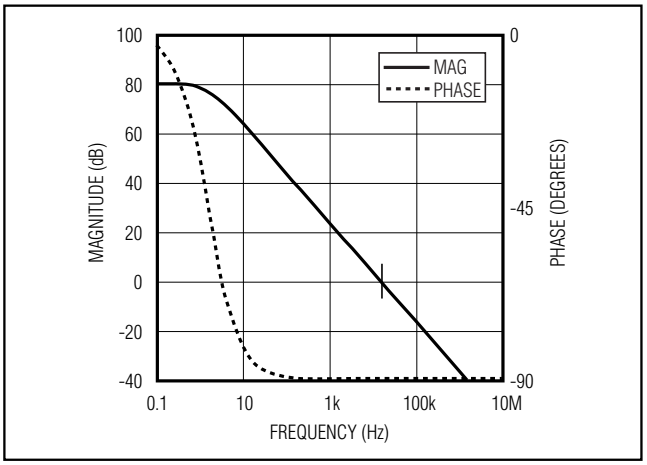


Figure 12. CCS Loop Response

The high-side driver (DHI) swings from LX to 5V above LX (BST) and has a typical impedance of 3Ω sourcing and 1Ω sinking. The low-side driver (DLO) swings from DLOV to ground and has a typical impedance of 1Ω sinking and 3Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on, due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

MOSFET Selection

Choose the n-channel MOSFETs according to the maximum required charge current. The MOSFETs must be able to dissipate the resistive losses plus the switching losses at both $V_{DCIN(MIN)}$ and $V_{DCIN(MAX)}$.

For the high-side MOSFET, the worst-case resistive power losses occur at the maximum battery voltage and minimum supply voltage:

$$PD_{CONDUCTION}(HighSide) = \frac{V_{FBS_}}{V_{CSSP}} \times I_{CHG}{}^2 \times R_{DS(ON)}$$

Generally a low-gate charge high-side MOSFET is preferred to minimize switching losses. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. Calculating the power dissipation in N1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides a rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on N1:

$$PD_{SWITCHING}(High\ Side) = \frac{1}{2} \times t_{Trans} \times V_{DCIN} \times I_{CHG} \times f_{SW}$$

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where t_{TRANS} is the driver's transition time and can be calculated as follows:

$$t_{TRANS} = \left(\frac{1}{I_{Gsrc}} + \frac{1}{I_{Gsnk}}\right) \times \frac{2Q_G}{I_{GATE}}, \text{ and } f_{SW} \approx 400kHz$$

I_{GATE} is the peak gate-drive current.

The following is the power dissipated due to the high-side n-channel MOSFET's output capacitance (C_{RSS}):

$$PD_{COSS}(HighSide) \approx \frac{V_{DCIN}^2 \times C_{RSS} \times f_{SW}}{2}$$

The following high-side MOSFET's loss is due to the reverse-recovery charge of the low-side MOSFET's body diode:

$$PD_{QRR}(HighSide) = Q_{RR2} \times V_{DCIN} \times f_{SW} \times 0.5$$

Ignore PD_{QRR} (HighSide) if a Schottky diode is used parallel to the low-side MOSFET.

The total high-side MOSFET power dissipation is:

$$PD_{TOTAL}(HighSide) \approx PD_{CONDUCTION}(HighSide) + PD_{SWITCHING}(HighSide) + PD_{COSS}(HighSide) + PD_{QRR}(HighSide)$$

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance. For the low-side MOSFET (N2), the worst-case power dissipation always occurs at maximum input voltage:

$$PD_{CONDUCTION}(LowSide) = \left(1 - \frac{V_{FBS_}}{V_{CSSP}}\right) \times I_{CHG}^2 \times R_{DS(ON)}$$

The following additional loss occurs in the low-side MOSFET due to the body diode conduction losses:

$$PD_{BDY}(Low\ Side) = 0.05 \times I_{PEAK} \times 0.4V$$

The total power low-side MOSFET dissipation is:

$$PD_{TOTAL}(LowSide) \approx PD_{CONDUCTION}(LowSide) + PD_{BDY}(LowSide)$$

These calculations provide an estimate and are not a substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on the MOSFET.

Inductor Selection

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L = \frac{V_{BATT} \times t_{OFF}}{0.3 \times I_{CHG}}$$

This sets the ripple current to 1/3 the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values save cost but require higher saturation current capabilities and degrade efficiency.

Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 the ripple current (ΔIL):

$$I_{SAT} = I_{CHG} + (1/2)\ \Delta IL$$

The ripple current is determined by:

$$\Delta IL = V_{BATT} \times t_{OFF} / L$$

where:

t_{OFF} = 2.5µs (V_{DCIN} - V_{BATT}) / V_{DCIN} for V_{BATT} < 0.88 V_{DCIN}

or during dropout:

t_{OFF} = 0.3µs for V_{BATT} > 0.88 V_{DCIN}

Input-Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{CHG}\left(\frac{\sqrt{V_{BATT}(V_{DCIN} - V_{BATT})}}{V_{DCIN}}\right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately +10°C. The maximum ripple current occurs at 50% duty factor or $V_{DCIN} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output-Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure stability of the DC-DC converter (see the *Compensation* section). Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents.

Applications Information

Smart-Battery System Background Information

Smart-battery systems have evolved since the conception of the smart-battery system (SBS) specifications. Originally, such systems consisted of a smart battery and smart-battery charger that were compatible with the SBS specifications and communicated directly with one another using SMBus protocols. Modern systems still employ the original commands and protocols, but often use a keyboard controller or similar digital intelligence to mediate the communication between the battery and the charger (Figure 13). This arrangement permits considerable freedom in the implementation of charging algorithms at the expense of standardization. Algorithms can vary from the simple detection of the battery with a fixed set of instructions for charging the battery to highly complex programs that can accommodate multiple battery configurations and chemistries. Microcontroller programs can perform frequent tests on the battery's state of charge and dynamically change the voltage and current applied to enhance safety. Multiple batteries can also be utilized with a selector that is programmable over the SMBus.

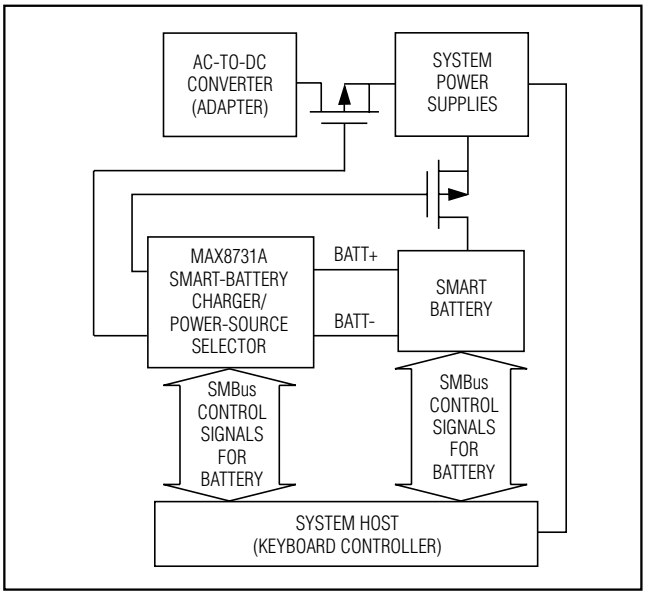


Figure 13. Typical Smart-Battery System

Setting Input-Current Limit

The input-current limit should be set based on the current capability of the AC adapter and the tolerance of the input-current limit. The upper limit of the input current threshold should never exceed the adapter's minimum available output current. For example, if the adapter's output current rating is 5A ±10%, the input current limit should be selected so that its upper limit is less than 5A × 0.9 = 4.5A. Since the input current-limit accuracy of the MAX8731A is ±3%, the typical value of the input-current limit should be set at 4.5A / 1.03 ≈ 4.36A. The lower limit for input current must also be considered. For chargers at the low end of the spec, the input-current limit for this example could be 4.36A × 0.95, or approximately 4.14A.

Layout and Bypassing

Bypass DCIN with a 1µF ceramic to ground (Figure 1). D1 protects the MAX8731A when the DC power source input is reversed. Bypass V_{DD}, DCIN, LDO, VCC, DAC, and REF as shown in Figure 1.

SMBus Level 2 Battery Charger with Remote Sense

Good PCB layout is required to achieve specified noise immunity, efficiency, and stable performance. The PCB layout artist must be given explicit instructions—preferably, a sketch showing the placement of the power-switching components and high-current routing. Refer to the PCB layout in the MAX8731A evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections, and the inner layers for uninterrupted ground planes.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:
   a) Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   b) Minimize ground trace lengths in the high-current paths.
   c) Minimize other trace lengths in the high-current paths.

      Use > 5mm wide traces in the high-current paths.
   d) Connect C1 and C2 to high-side MOSFET (10mm max length). Place the input capacitor between the input current-sense resistor and drain of the high-side MOSFET.
   e) Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm max length)). Keep LX on one side of the PCB to reduce EMI radiation.
   f) Since the return path of DHI is LX, route DHI near LX. Optimally, LX and DHI should overlap. The same principle is applied to DLO and PGND.
   g) Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the paddle. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates approximately 90% of all PCB layout problems.
2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF capacitor).

   Important: The IC must be no further than 10mm from the current-sense resistors. Quiet connections to REF, CCS, DAC, CCV, CCI, ACIN, and VCC should be returned to a separate ground (GND) island. The analog ground is separately worked from power ground in Figure 1. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low-current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.
3) Keep the gate-drive traces (DHI and DLO) as short as possible (L < 20mm), and route them away from the current-sense lines and REF. These traces should also be relatively wide (W > 1.25mm).
4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.
5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

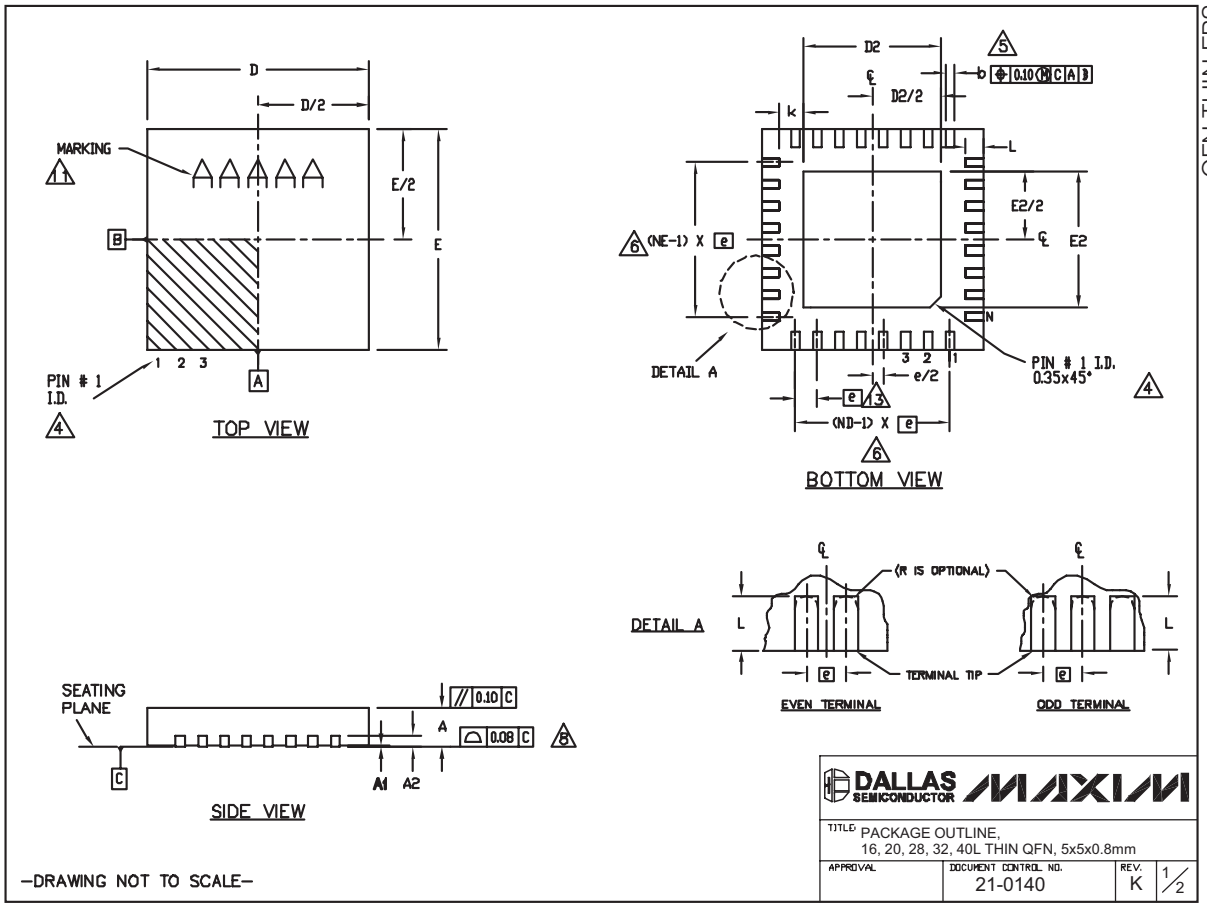
Chip Information

TRANSISTOR COUNT: 10,234

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



SMBus Level 2 Battery Charger with Remote Sense

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

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