19-0793; Rev 5; 5/12

EVALUATION KIT AVAILABLE

TFT-LCD DC-DC Converter with Operational Amplifiers

MAX8795A

General Description

The MAX8795A includes a high-performance step-up regulator, two linear-regulator controllers, and five high-current operational amplifiers for active-matrix, thin-film transistor (TFT), liquid-crystal displays (LCDs). Also included is a logic-controlled, high-voltage switch with adjustable delay.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency (1.2MHz) current-mode regulator with an integrated 20V n-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 85%.

The gate-on and gate-off linear-regulator controllers provide regulated TFT gate-on and gate-off supplies using external charge pumps attached to the switching node. The MAX8795A includes five high-performance operational amplifiers. These amplifiers are designed to drive the LCD backplane (VCOM) and/or the gamma-correction divider string. The device features high output current (±130mA), fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs.

The MAX8795A is available in a lead-free, 32-pin, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels, as well as in a 32-pin LQFP package with 0.8mm pin pitch.

Applications

Notebook Computer Displays

LCD Monitor Panels

Automotive Displays

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8795AETJ+	-40°C to +85°C	32 Thin QFN
MAX8795AGCJ+	-40°C to +105°C	32 LQFP
MAX8795AGCJ/V+	-40°C to +105°C	32 LQFP
MAX8795AGTJ+	-40°C to +105°C	32 TQFN
MAX8795AGTJ/V+	-40°C to +105°C	32 TQFN

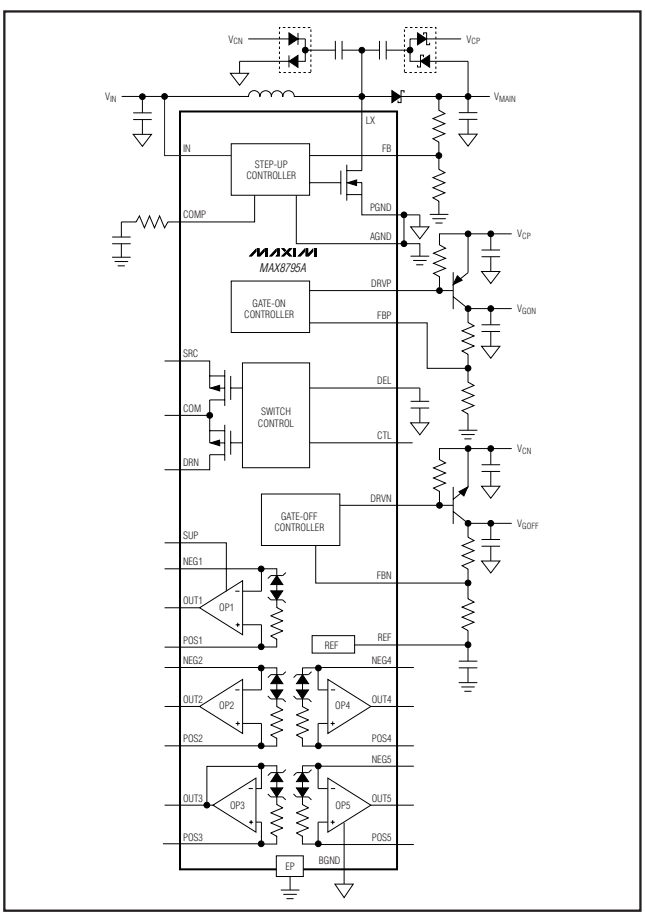
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive-qualified part.

Pin Configurations appear at end of data sheet.

Features

- **2.5V to 5.5V Input Supply Range**
- **1.2MHz Current-Mode Step-Up Regulator**
  - **Fast Transient Response to Pulsed Load**
  - **High-Accuracy Output Voltage (1%)**
  - **Built-In 20V, 3A, 0.16Ω n-Channel MOSFET**
  - **High Efficiency (85%)**
- **Linear-Regulator Controllers for V_{GON} and V_{GOFF}**
- **High-Performance Operational Amplifiers**
  - **±130mA Output Short-Circuit Current**
  - **45V/µs Slew Rate**
  - **20MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs/Outputs**
- **Logic-Controlled, High-Voltage Switch with Adjustable Delay**
- **Timer-Delay Fault Latch for All Regulator Outputs**
- **Thermal-Overload Protection**
- **0.6mA Quiescent Current**

Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

TFT-LCD DC-DC Converter with Operational Amplifiers

ABSOLUTE MAXIMUM RATINGS

IN, CTL to AGND .....-0.3V to +7.5V
COMP, FB, FBP, FBN, DEL, REF to AGND ....-0.3V to (V_{IN} + 0.3V)
PGND, BGND to AGND .....±0.3V
LX to PGND .....-0.3V to +20V
SUP to AGND .....-0.3V to +20V
DRVP to AGND.....-0.3V to +36V
POS_, NEG_, OUT_ to AGND .....-0.3V to (V_{SUP} + 0.3V)
DRVN to AGND .....(V_{IN} - 30V) to (V_{IN} + 0.3V)
SRC to AGND.....-0.3V to +40V
COM, DRN to AGND .....-0.3V to (V_{SRC} + 0.3V)
DRN to COM.....-30V to +30V
POS_ to NEG_ RMS Current .....5mA (Note 1)
OUT_ Maximum Continuous Output Current.....±75mA
LX Switch Maximum Continuous RMS Current.....1.6A
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 34.5mW/°C above +70°C) 2758mW
32-Pin LQFP (derate 48.4mW/°C above +70°C)....1652.9mW
Operating Temperature Range, E Grade .....-40°C to +85°C
Operating Temperature Range, G Grade .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: See Figure 2 for the op amp clamp structure.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range	V_{IN}	(Note 2)		2.5		6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising, typical hysteresis = 50mV		2.05	2.25	2.45	V
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching			0.6	1.0	mA
		V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching			2	3	
Duration-to-Trigger Fault Condition		FB or FBP below threshold or FBN above threshold			200		ms
REF Output Voltage		No external load	T_A = +25°C to +85°C	1.238	1.250	1.262	V
			T_A = 0°C to +85°C	1.232	1.250	1.266	
REF Load Regulation		0 < I_{LOAD} < 50µA				10	mV
REF Sink Current		In regulation		10			µA
REF Undervoltage Lockout Threshold		Rising edge; typical hysteresis = 160mV				1.15	V
Thermal Shutdown		Temperature rising			+160		°C
		Hysteresis			15		
MAIN STEP-UP REGULATOR							
Output Voltage Range	V_{MAIN}			V_{IN}		18	V
Operating Frequency	f_{OSC}			1000	1200	1400	kHz
Oscillator Maximum Duty Cycle				86	90	93	%
FB Regulation Voltage	V_{FB}	No load	T_A = +25°C to +85°C	1.221	1.233	1.245	V
			T_A = 0°C to +85°C	1.212	1.233	1.248	
FB Fault Trip Level		V_{FB} falling		1.10	1.14	1.17	V
FB Load Regulation		0 < I_{MAIN} < full load, transient only			-1		%
FB Line Regulation		V_{IN} = 2.5V to 6V			0.1	±0.4	%/V
FB Input Bias Current		V_{FB} = 1.233V			+100	+200	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Transconductance		ΔI_{COMP} = ±2.5µA	75	160	280	µS
FB Voltage Gain		From FB to COMP		700		V/V
LX On-Resistance	$R_{LX(ON)}$	I_{LX} = 200mA		160	260	mΩ
LX Leakage Current	I_{LX}	V_{LX} = 19V		10	20	µA
LX Current Limit	I_{LIM}	V_{FB} = 1.2V, duty cycle = 75%	2.5	3.0	3.5	A
Current-Sense Transresistance			0.1	0.2	0.3	V/A
Soft-Start Period	t_{SS}			14		ms
Soft-Start Step Size				V_{REF} / 128		V
OPERATIONAL AMPLIFIERS						
SUP Supply Range	V_{SUP}		6.0		18.0	V
SUP Overvoltage Fault Threshold			18.0	19	19.9	V
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS_}$ = V_{SUP} / 2, no load		3.5	5.0	mA
Input Offset Voltage	V_{OS}	($V_{NEG_}$, $V_{POS_}$, $V_{OUT_}$) ≅ V_{SUP} / 2		0	12	mV
Input Bias Current	I_{BIAS}	($V_{NEG_}$, $V_{POS_}$, $V_{OUT_}$) ≅ V_{SUP} / 2	-50	0	+50	nA
Input Common-Mode Voltage Range	V_{CM}		0		V_{SUP}	V
Common-Mode Rejection Ratio	CMRR	0 ≤ ($V_{NEG_}$, $V_{POS_}$) ≤ V_{SUP}	45	80		dB
Open-Loop Gain				125		dB
Output Voltage Swing, High	V_{OH}	$I_{OUT_}$ = 5mA	V_{SUP} - 100	V_{SUP} - 50		mV
Output Voltage Swing, Low	V_{OL}	$I_{OUT_}$ = -5mA		50	100	mV
Short-Circuit Current		To V_{SUP} / 2, source or sink	75	130		mA
Power-Supply Rejection Ratio	PSRR	DC, 6V ≤ V_{SUP} ≤ 18V, ($V_{NEG_}$, $V_{POS_}$) ≅ V_{SUP} / 2	60			dB
Slew Rate				45		V/µs
-3dB Bandwidth		R_L = 10kΩ, C_L = 10pF, buffer configuration		20		MHz
GATE-ON LINEAR-REGULATOR CONTROLLER						
FBP Regulation Voltage	V_{FBP}	I_{DRVN} = 100µA	1.231	1.250	1.269	V
FBP Fault Trip Level		V_{FBP} falling	0.96	1.00	1.04	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.25V	-50		+50	nA
FBP Effective Load-Regulation Error (Transconductance)		V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA		-0.7	-1.5	%
FBP Line (IN) Regulation Error		I_{DRVP} = 100µA, 2.5V < V_{IN} < 6V		±1	±10	mV
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V	1	5		mA
DRVP Off-Leakage Current		V_{FBP} = 1.4V, V_{DRVP} = 34V		0.01	10	µA
Soft-Start Period	t_{SS}			14		ms
Soft-Start Step Size				V_{REF} / 128		V

TFT-LCD DC-DC Converter with Operational Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE-OFF LINEAR-REGULATOR CONTROLLER						
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.984	1	1.015	V
FBN Fault Trip Level		V_{FBN} rising	370	420	470	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0.25V	-50		+50	nA
FBN Effective Load-Regulation Error (Transconductance)		V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		11	25	mV
FBN Line (IN) Regulation Error		I_{DRVN} = 0.1mA, 2.5V < V_{IN} < 6V		±0.7	±5	mV
DRVN Source Current	I_{DRVN}	V_{FBN} = 300mV, V_{DRVN} = -10V	1	5		mA
DRVN Off-Leakage Current		V_{FBN} = 0V, V_{DRVN} = -25V		-0.01	-10	µA
Soft-Start Period	t_{SS}			14		ms
Soft-Start Step Size				(V_{REF} - V_{FBN}) / 128		V
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES						
DEL Capacitor Charge Current		During startup, V_{DEL} = 1V	4	5	6	µA
DEL Turn-On Threshold	$V_{TH(DEL)}$		1.19	1.25	1.31	V
DEL Discharge Switch On-Resistance		During UVLO, V_{IN} = 2.0V		20		Ω
CTL Input Low Voltage		V_{IN} = 2.5V to 5.5V			0.6	V
CTL Input High Voltage		V_{IN} = 2.5V to 5.5V	2			V
CTL Input Leakage Current		CTL = AGND or IN	-1		+1	µA
CTL-to-SRC Propagation Delay				100		ns
SRC Input Voltage Range					36	V
SRC Input Current	I_{SRC}	V_{DEL} = 1.5V, CTL = IN		200	300	µA
		V_{DEL} = 1.5V, CTL = AGND		115	200	
SRC-to-COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN		5	10	Ω
DRN-to-COM Switch On-Resistance	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND		30	60	Ω

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
IN Supply Range	V_{IN}	(Note 2)		2.5	6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising, typical hysteresis = 150mV		2.05	2.45	V
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching			1.0	mA
		V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching			3	
REF Output Voltage		No external load		1.218	1.277	V
REF Undervoltage-Lockout Threshold		Rising edge; typical hysteresis = 160mV			1.15	V
MAIN STEP-UP REGULATOR						
Output Voltage Range	V_{MAIN}			V_{IN}	18	V
Operating Frequency	f_{OSC}			900	1400	kHz
FB Regulation Voltage	V_{FB}	No load		1.198	1.260	V
FB Line Regulation		V_{IN} = 2.5V to 6V			±0.4	%/V
FB Transconductance		ΔI_{COMP} = ±2.5µA		75	280	µS
LX On-Resistance	$R_{LX(ON)}$	I_{LX} = 200mA			260	mΩ
LX Current Limit	I_{LIM}	V_{FB} = 1.2V, duty cycle = 75%		2.5	3.5	A
OPERATIONAL AMPLIFIERS						
SUP Supply Range	V_{SUP}			6	18	V
SUP Overvoltage Fault Threshold				18.0	19.9	V
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS_}$ = V_{SUP} / 2, no load			5	mA
Input Offset Voltage	V_{OS}	($V_{NEG_}$, $V_{POS_}$, $I_{OUT_}$) = ≅ V_{SUP} / 2			12	mV
Input Common-Mode Voltage Range	V_{CM}			0	V_{SUP}	V
Output Voltage Swing, High	V_{OH}	$I_{OUT_}$ = 5mA		V_{SUP} - 100		mV
Output Voltage Swing Low	V_{OL}	$I_{OUT_}$ = -5mA			100	
Short-Circuit Current		To V_{SUP} / 2	Source	75		mA
			Sink	75		
GATE-ON LINEAR-REGULATOR CONTROLLER						
FBP Regulation Voltage	V_{FBP}	I_{DRVP} = 100µA		1.210	1.280	V
FBP Effective Load-Regulation Error (Transconductance)		V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA			-1.5	%
FBP Line (IN) Regulation Error		I_{DRVP} = 100µA, 2.5V < V_{IN} < 6V			10	mV
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V		1		mA

TFT-LCD DC-DC Converter with Operational Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
GATE-OFF LINEAR-REGULATOR CONTROLLER					
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.972	1.022	V
FBN Effective Load-Regulation Error (Transconductance)		V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		25	mV
FBN Line (IN) Regulation Error		I_{DRVN} = 0.1mA, 2.5V < V_{IN} < 6V		±5	mV
DRVN Source Current	I_{DRVN}	V_{FBN} = 300mV, V_{DRVN} = -10V	1		mA
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
DEL Capacitor Charge Current		During startup, V_{DEL} = 1V	4	6	µA
DEL Turn-On Threshold	$V_{TH(DEL)}$		1.19	1.31	V
CTL Input Low Voltage		V_{IN} = 2.5V to 5.5V		0.6	V
CTL Input High Voltage		V_{IN} = 2.5V to 5.5V	2		V
SRC Input Voltage Range				36	V
SRC Input Current	I_{SRC}	V_{DEL} = 1.5V, CTL = IN		300	µA
		V_{DEL} = 1.5V, CTL = AGND		200	
SRC-to-COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN		10	Ω
DRN-to-COM Switch On-Resistance	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND		60	Ω

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +105°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range	V_{IN}	(Note 2)		2.5		6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising, typical hysteresis = 50mV		2.05	2.25	2.45	V
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching			0.6	1.0	mA
		V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching			2	3	
Duration-to-Trigger Fault Condition		V_{FB} or FBP below threshold or FBN above threshold			200		ms
REF Output Voltage		No external load	T_A = +25°C to +105°C	1.238	1.250	1.262	V
			T_A = 0°C to +105°C	1.232	1.250	1.266	
REF Load Regulation		0 < I_{LOAD} < 50µA				10	mV
REF Sink Current		In regulation		10			µA
REF Undervoltage-Lockout Threshold		Rising edge, typical hysteresis = 160mV				1.15	V
Thermal Shutdown		Temperature rising			+160		°C
		Hysteresis			15		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +105°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAIN STEP-UP REGULATOR							
Output Voltage Range	V_{MAIN}			V_{IN}		18	V
Operating Frequency	f_{OSC}			1000	1200	1400	kHz
Oscillator Maximum Duty Cycle				86	90	93	%
FB Regulation Voltage	V_{FB}	No load	T_A = +25°C to +105°C	1.221	1.233	1.245	V
			T_A = 0°C to +105°C	1.212	1.233	1.248	
FB Fault Trip Level		V_{FB} falling		1.10	1.14	1.17	V
FB Load Regulation		0 < I_{MAIN} < full load, transient only			-1		
FB Line Regulation		V_{IN} = 2.5V to 6V			0.1	±0.4	%/V
FB Input Bias Current		V_{FB} = 1.233V			+100	+200	nA
FB Transconductance		ΔI_{COMP} = ±2.5µA		75	160	280	µS
FB Voltage Gain		From FB to COMP			700		V/V
LX On-Resistance	$R_{LX(ON)}$	I_{LX} = 200mA			160	300	mΩ
LX Leakage Current	I_{LX}	V_{LX} = 19V			10	20	µA
LX Current Limit	I_{LIM}	V_{FB} = 1.2V, duty cycle = 75%		2.5	3.0	3.5	A
Current-Sense Transresistance				0.1	0.2	0.3	V/A
Soft-Start Period	t_{SS}				14		ms
Soft-Start Step Size					V_{REF} / 128		V
OPERATIONAL AMPLIFIERS							
SUP Supply Range	V_{SUP}			6.0		18.0	V
SUP Overvoltage Fault Threshold				18.0	19	19.9	
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS_}$ = V_{SUP} / 2, no load			3.5	5.0	mA
Input Offset Voltage	V_{OS}	($V_{NEG_}$, $V_{POS_}$, $V_{OUT_}$) ≅ V_{SUP} / 2			0	12	mV
Input Bias Current	I_{BIAS}	($V_{NEG_}$, $V_{POS_}$, $V_{OUT_}$) ≅ V_{SUP} / 2		-50	0	+50	nA
Input Common-Mode Voltage Range	V_{CM}			0		V_{SUP}	V
Common-Mode Rejection Ratio	CMRR	0 ≤ ($V_{NEG_}$, $V_{POS_}$) ≤ V_{SUP}		45	80		dB
Open-Loop Gain					125		dB
Output Voltage Swing, High	V_{OH}	$I_{OUT_}$ = 5mA		V_{SUP} - 100	V_{SUP} - 50		mV
Output Voltage Swing, Low	V_{OL}	$I_{OUT_}$ = -5mA			50	100	mV
Short-Circuit Current		To V_{SUP} / 2, source or sink		75	130		mA
Power-Supply Rejection Ratio	PSRR	DC, 6V ≤ V_{SUP} ≤ 18V, ($V_{NEG_}$, $V_{POS_}$) ≅ V_{SUP} / 2		60			dB
Slew Rate					45		V/µs
-3dB Bandwidth		R_L = 10kΩ, C_L = 10pF, buffer configuration			20		MHz

TFT-LCD DC-DC Converter with Operational Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = 0°C to +105°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE-ON LINEAR-REGULATOR CONTROLLER						
FBP Regulation Voltage	V_{FBP}	I_{DRVP} = 100µA	1.231	1.250	1.269	V
FBP Fault Trip Level		V_{FBP} falling	0.96	1.00	1.04	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.25V	-50		+50	nA
FBP Effective Load-Regulation Error (Transconductance)		V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA		-0.7	-1.5	%
FBP Line (IN) Regulation Error		I_{DRVP} = 100µA, 2.5V < V_{IN} < 6V		±1	±10	mV
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V	1	5		mA
DRVP Off-Leakage Current		V_{FBP} = 1.4V, V_{DRVP} = 34V		0.01	10	µA
Soft-Start Period	t_{SS}			14		ms
Soft-Start Step Size				V_{REF} / 128		V
GATE-OFF LINEAR-REGULATOR CONTROLLER						
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.984	1	1.015	V
FBN Fault Trip Level		V_{FBN} rising	340	420	510	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0.25V	-50		+50	nA
FBN Effective Load-Regulation Error (Transconductance)		V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		11	25	mV
FBN Line (IN) Regulation Error		I_{DRVN} = 0.1mA, 2.5V < V_{IN} < 6V		±0.7	±5	mV
DRVN Source Current	I_{DRVN}	V_{FBN} = 300mV, V_{DRVN} = -10V	1	5		mA
DRVN Off-Leakage Current		V_{FBN} = 0V, V_{DRVN} = -25V		-0.01	-10	µA
Soft-Start Period	t_{SS}			14		ms
Soft-Start Step Size				(V_{REF} - V_{FBN}) / 128		V
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES						
DEL Capacitor Charge Current		During startup, V_{DEL} = 1V	4	5	6	µA
DEL Turn-On Threshold	$V_{TH(DEL)}$		1.19	1.25	1.31	V
DEL Discharge Switch On-Resistance		During UVLO, V_{IN} = 2.0V		20		Ω
CTL Input Low Voltage		V_{IN} = 2.5V to 5.5V			0.6	V
CTL Input High Voltage		V_{IN} = 2.5V to 5.5V	2			V
CTL Input Leakage Current		CTL = AGND or IN	-1		+1	µA
CTL-to-SRC Propagation Delay				100		ns
SRC Input Voltage Range					36	V
SRC Input Current	I_{SRC}	V_{DEL} = 1.5V, CTL = IN		200	300	µA
		V_{DEL} = 1.5V, CTL = AGND		115	200	
SRC-to-COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN		5	12	Ω
DRN-to-COM Switch On-Resistance	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND		30	70	Ω

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
IN Supply Range	V_{IN}	(Note 2)		2.5	6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising, typical hysteresis = 150mV		2.05	2.45	V
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching			1.0	mA
		V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching			3	
REF Output Voltage		No external load		1.218	1.277	V
REF Undervoltage-Lockout Threshold		Rising edge, typical hysteresis = 160mV			1.15	V
MAIN STEP-UP REGULATOR						
Output Voltage Range	V_{MAIN}			V_{IN}	18	V
Operating Frequency	f_{OSC}			900	1400	kHz
FB Regulation Voltage	V_{FB}	No load		1.198	1.260	V
FB Line Regulation		V_{IN} = 2.5V to 6V			±0.4	%/ V
FB Transconductance		ΔI_{COMP} = ±2.5µA		75	280	µS
LX On-Resistance	$R_{LX(ON)}$	I_{LX} = 200mA			300	mΩ
LX Current Limit	I_{LIM}	V_{FB} = 1.2V, duty cycle = 75%		2.5	3.5	A
OPERATIONAL AMPLIFIERS						
SUP Supply Range	V_{SUP}			6	18	V
SUP Overvoltage Fault Threshold				18.0	19.9	V
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS_}$ = V_{SUP} / 2, no load			5	mA
Input Offset Voltage	V_{OS}	($V_{NEG_}$, $V_{POS_}$, $V_{OUT_}$) ≅ V_{SUP} / 2			12	mV
Input Common-Mode Voltage Range	V_{CM}			0	V_{SUP}	V
Output Voltage Swing, High	V_{OH}	$I_{OUT_}$ = 5mA		V_{SUP} - 100		mV
Output Voltage Swing, Low	V_{OL}	$I_{OUT_}$ = -5mA			100	mV
Short-Circuit Current		To V_{SUP} / 2	Source	75		mA
			Sink	75		

TFT-LCD DC-DC Converter with Operational Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{MAIN} = V_{SUP} = 14V, V_{PGND} = V_{AGND} = V_{BGND} = 0V, I_{REF} = 25µA, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
GATE-ON LINEAR-REGULATOR CONTROLLER					
FBP Regulation Voltage	V_{FBP}	I_{DRVP} = 100µA	1.210	1.280	V
FBP Effective Load-Regulation Error (Transconductance)		V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA		-1.5	%
FBP Line (IN) Regulation Error		I_{DRVP} = 100µA, 2.5V < V_{IN} < 6V		10	mV
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V	1		mA
GATE-OFF LINEAR-REGULATOR CONTROLLER					
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.972	1.022	V
FBN Effective Load-Regulation Error (Transconductance)		V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		25	mV
FBN Line (IN) Regulation Error		I_{DRVN} = 0.1mA, 2.5V < V_{IN} < 6V		±5	mV
DRVN Source Current	I_{DRVN}	V_{FBN} = 300mV, V_{DRVN} = -10V	1		mA
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
DEL Capacitor Charge Current		During startup, V_{DEL} = 1V	4	6	µA
DEL Turn-On Threshold	$V_{TH(DEL)}$		1.19	1.31	V
CTL Input Low Voltage		V_{IN} = 2.5V to 5.5V		0.6	V
CTL Input High Voltage		V_{IN} = 2.5V to 5.5V	2		V
SRC Input Voltage Range				36	V
SRC Input Current	I_{SRC}	V_{DEL} = 1.5V, CTL = IN		300	µA
		V_{DEL} = 1.5V, CTL = AGND		200	
SRC-to-COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN		12	Ω
DRN-to-COM Switch On-Resistance	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND		70	Ω

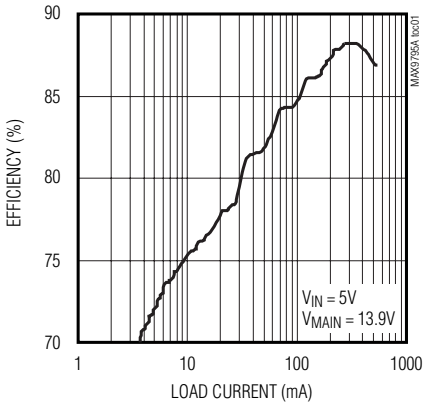
Note 2: For 5.5V < V_{IN} < 6.0V, use MAX8795A for no longer than 1% of IC lifetime. For continuous operation, input voltage should not exceed 5.5V.

Note 3: Specifications to -40°C and +105°C are guaranteed by design, not production tested.

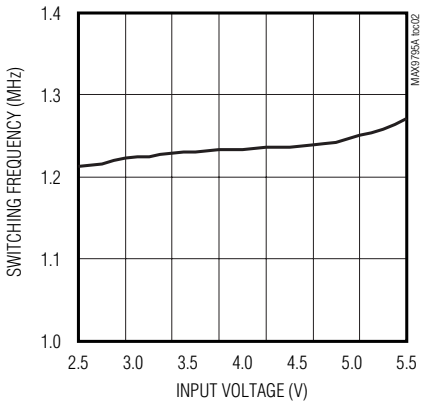
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 14V, V_{GON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

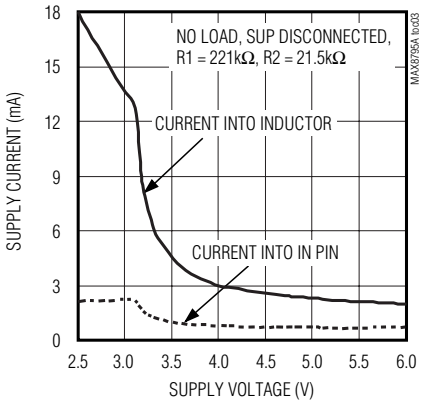
STEP-UP EFFICIENCY vs. LOAD CURRENT



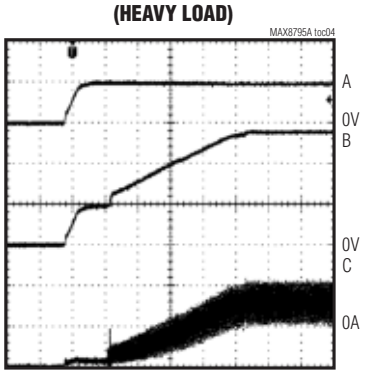
SWITCHING FREQUENCY vs. INPUT VOLTAGE



STEP-UP SUPPLY CURRENT vs. SUPPLY VOLTAGE

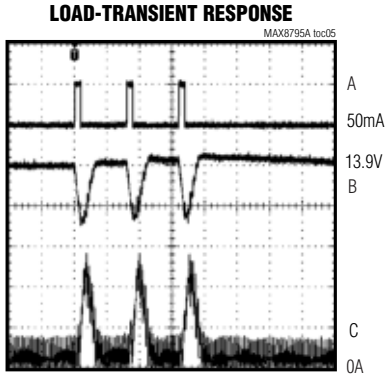


STEP-UP REGULATOR SOFT-START (HEAVY LOAD)



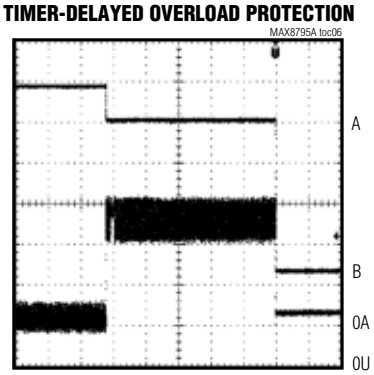
A: V_{IN}, 5V/div
B: V_{MAIN}, 5V/div
C: INDUCTOR CURRENT, 1A/div

STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE



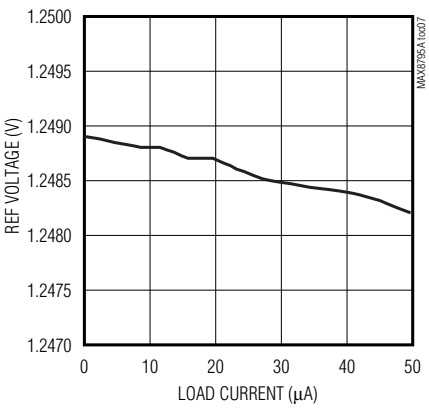
A: LOAD CURRENT, 1A/div
B: V_{MAIN}, 200mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div

TIMER-DELAYED OVERLOAD PROTECTION

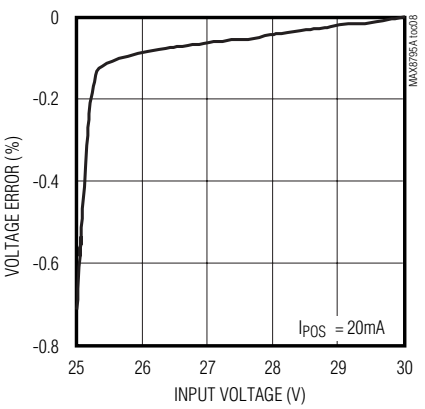


A: V_{MAIN}, 2V/div
B: INDUCTOR CURRENT, 1A/div

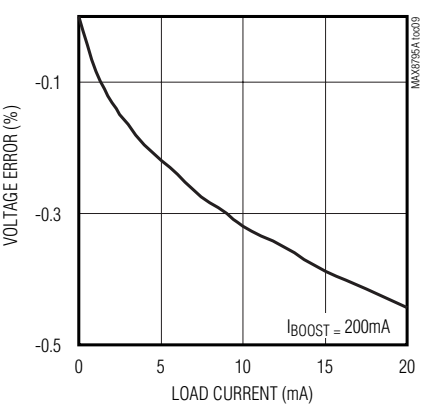
REF VOLTAGE LOAD REGULATION



GATE-ON REGULATOR LINE REGULATION



GATE-ON REGULATOR LOAD REGULATION

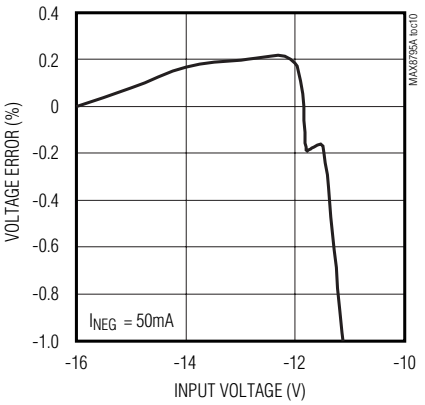


TFT-LCD DC-DC Converter with Operational Amplifiers

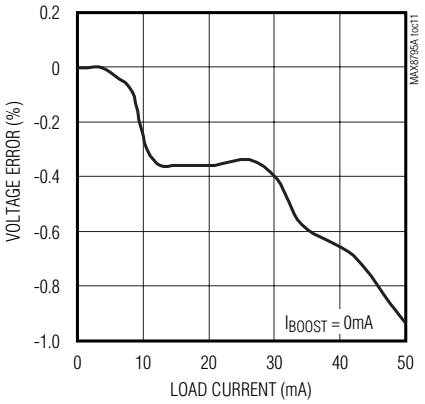
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 14V, V_{GON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

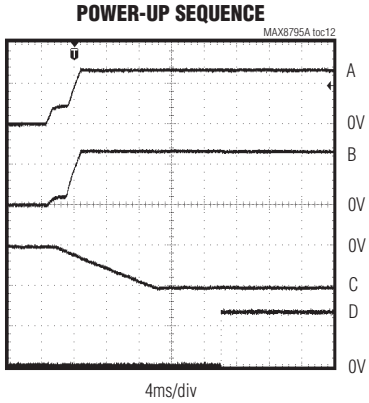
GATE-OFF REGULATOR LINE REGULATION



GATE-OFF REGULATOR LOAD REGULATION

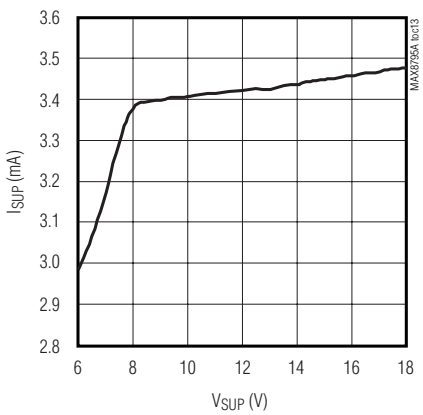


POWER-UP SEQUENCE

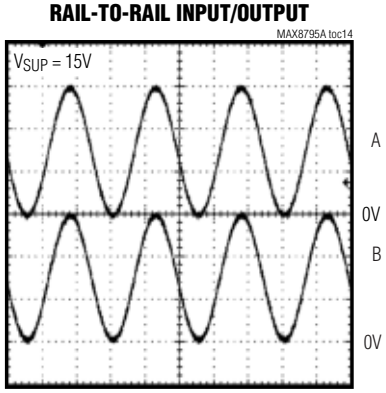


A: V_{MAIN}, 10V/div
B: V_{POS}, 20V/div
C: V_{NEG}, 10V/div
D: V_{COM}, 20V/div

SUP SUPPLY CURRENT vs. SUP VOLTAGE



OPERATIONAL-AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT

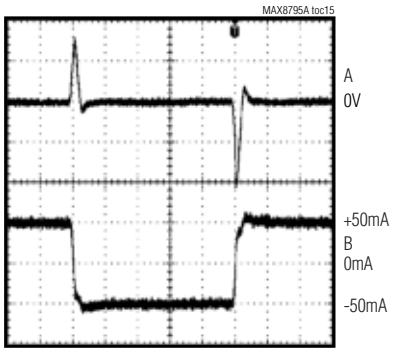


A: INPUT SIGNAL, 5V/div
B: OUTPUT SIGNAL, 5V/div

Typical Operating Characteristics (continued)

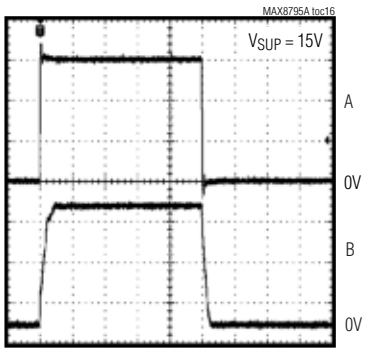
(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 14V, V_{GON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

OPERATIONAL-AMPLIFIER LOAD-TRANSIENT RESPONSE



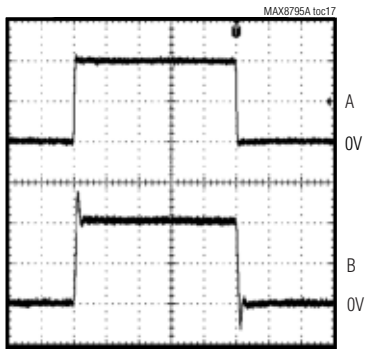
A: OUTPUT VOLTAGE, 1V/div, AC-COUPLED
B: OUTPUT CURRENT, 50mA/div

OPERATIONAL-AMPLIFIER LARGE-SIGNAL RESPONSE



A: INPUT SIGNAL, 5V/div
B: OUTPUT SIGNAL, 5V/div

OPERATIONAL-AMPLIFIER SMALL-SIGNAL RESPONSE



A: INPUT SIGNAL, 100mV/div
B: OUTPUT SIGNAL, 100mV/div

Pin Description

PIN	NAME	FUNCTION
1	SRC	Switch Input. Source of the internal high-voltage p-channel MOSFET. Bypass SRC to PGND with a minimum 0.1µF capacitor close to the pins.
2	REF	Reference Bypass Terminal. Bypass REF to AGND with a minimum of 0.22µF close to the pins.
3	AGND	Analog Ground for Step-Up Regulator and Linear Regulators. Connect to power ground (PGND) underneath the IC.
4	PGND	Power Ground. PGND is the source of the main step-up n-channel power MOSFET. Connect PGND to the output-capacitor ground terminals through a short, wide PCB trace. Connect to analog ground (AGND) underneath the IC.
5	OUT1	Operational-Amplifier 1 Output
6	NEG1	Operational-Amplifier 1 Inverting Input
7	POS1	Operational-Amplifier 1 Noninverting Input
8	OUT2	Operational-Amplifier 2 Output
9	NEG2	Operational-Amplifier 2 Inverting Input
10	POS2	Operational-Amplifier 2 Noninverting Input
11	BGND	Analog Ground for Operational Amplifiers. Connect to power ground (PGND) underneath the IC.
12	POS3	Operational-Amplifier 3 Noninverting Input
13	OUT3	Operational-Amplifier 3 Output
14	SUP	Operational-Amplifier Power Input. Positive supply rail for the operational amplifiers. Typically connected to V_{MAIN}. Bypass SUP to BGND with a 0.1µF capacitor.
15	POS4	Operational-Amplifier 4 Noninverting Input
16	NEG4	Operational-Amplifier 4 Inverting Input

TFT-LCD DC-DC Converter with Operational Amplifiers

Pin Description (continued)

PIN	NAME	FUNCTION
17	OUT4	Operational-Amplifier 4 Output
18	POS5	Operational-Amplifier 5 Noninverting Input
19	NEG5	Operational-Amplifier 5 Inverting Input
20	OUT5	Operational-Amplifier 5 Output
21	LX	n-Channel Power MOSFET Drain and Switching Node. Connect the inductor and Schottky diode to LX and minimize the trace area for lowest EMI.
22	IN	Supply Voltage Input. IN can range from 2.5V to 6V.
23	FB	Step-Up Regulator Feedback Input. Regulates to 1.233V (nominal). Connect a resistive voltage-divider from the output (V_{MAIN}) to FB to analog ground (AGND). Place the divider within 5mm of FB.
24	COMP	Step-Up Regulator Error-Amplifier Compensation Point. Connect a series RC from COMP to AGND. See the *Loop Compensation* section for component selection guidelines.
25	FBP	Gate-On Linear-Regulator Feedback Input. FBP regulates to 1.25V (nominal). Connect FBP to the center of a resistive voltage-divider between the regulator output and AGND to set the gate-on linear-regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
26	DRVP	Gate-On Linear-Regulator Base Drive. Open drain of an internal n-channel MOSFET. Connect DRVP to the base of an external pnp pass transistor. See the *Pass-Transistor Selection* section.
27	FBN	Gate-Off Linear-Regulator Feedback Input. FBN regulates to 250mV (nominal). Connect FBN to the center of a resistive voltage-divider between the regulator output and REF to set the gate-off linear-regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
28	DRVN	Gate-Off Linear-Regulator Base Drive. Open drain of an internal p-channel MOSFET. Connect DRVN to the base of an external npn pass transistor. See the *Pass-Transistor Selection* section.
29	DEL	High-Voltage Switch Delay Input. Connect a capacitor from DEL to AGND to set the high-voltage switch startup delay.
30	CTL	High-Voltage Switch Control Input. When CTL is high, the high-voltage switch between COM and SRC is on and the high-voltage switch between COM and DRN is off. When CTL is low, the high-voltage switch between COM and SRC is off and the high-voltage switch between COM and DRN is on. CTL is inhibited by the undervoltage lockout or when the voltage on DEL is less than 1.25V.
31	DRN	Switch Input. Drain of the internal high-voltage back-to-back p-channel MOSFETs connected to COM.
32	COM	Internal High-Voltage MOSFET Switch Common Terminal. Do not allow the voltage on COM to exceed V_{SRC}.
—	EP	Exposed Paddle. Must be connected to AGND. Do not use as the only ground connection.

Typical Operating Circuit

The MAX8795A typical operating circuit (Figure 1) is a complete power-supply system for TFT LCDs. The circuit generates a +14V source-driver supply and +25V and -10V gate-driver supplies. The input voltage range for the IC is from +2.5V to +5.5V. The listed load currents in Figure 1 are available from a +4.5V to +5.5V supply. Table 1 lists some recommended components, and Table 2 lists the contact information of component suppliers.

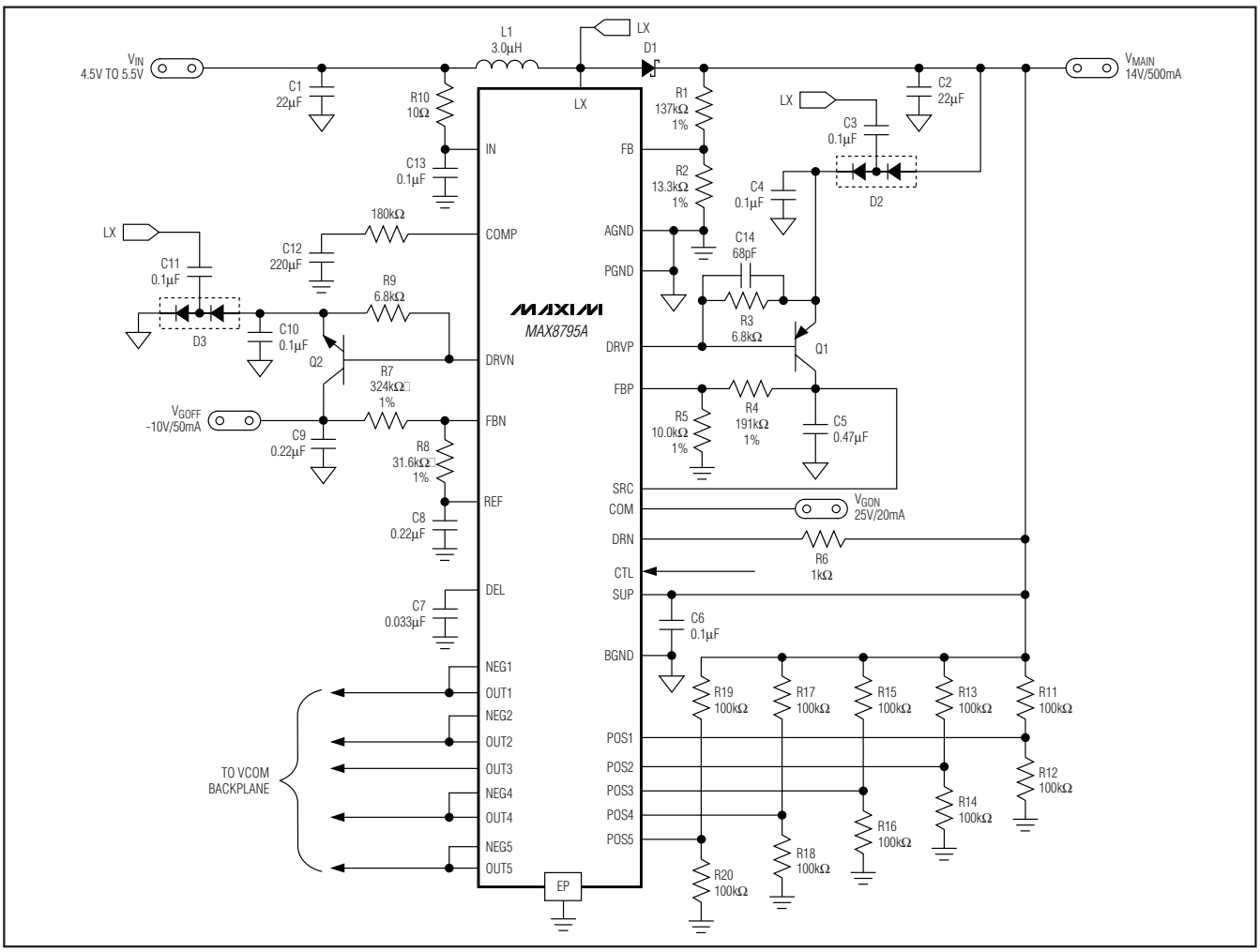


Figure 1. Typical Operating Circuit

Table 1. Component List

DESIGNATION	DESCRIPTION
C1	22µF, 6.3V X5R ceramic capacitor (1210) TDK C3225X5R0J227M
C2	22µF, 16V X5R ceramic capacitor (1812) TDK C4532X5X1C226M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02
D2, D3	200mA, 100V, dual ultra-fast diodes (SOT23) Fairchild MMBD4148SE

DESIGNATION	DESCRIPTION
L1	3.0µH, 3A inductor Sumida CDRH6D28-3R0
Q1	200mA, 40V pnp bipolar transistor (SOT23) Fairchild MMBT3906
Q2	200mA, 40V npn bipolar transistor (SOT23) Fairchild MMBT3904

TFT-LCD DC-DC Converter with Operational Amplifiers

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

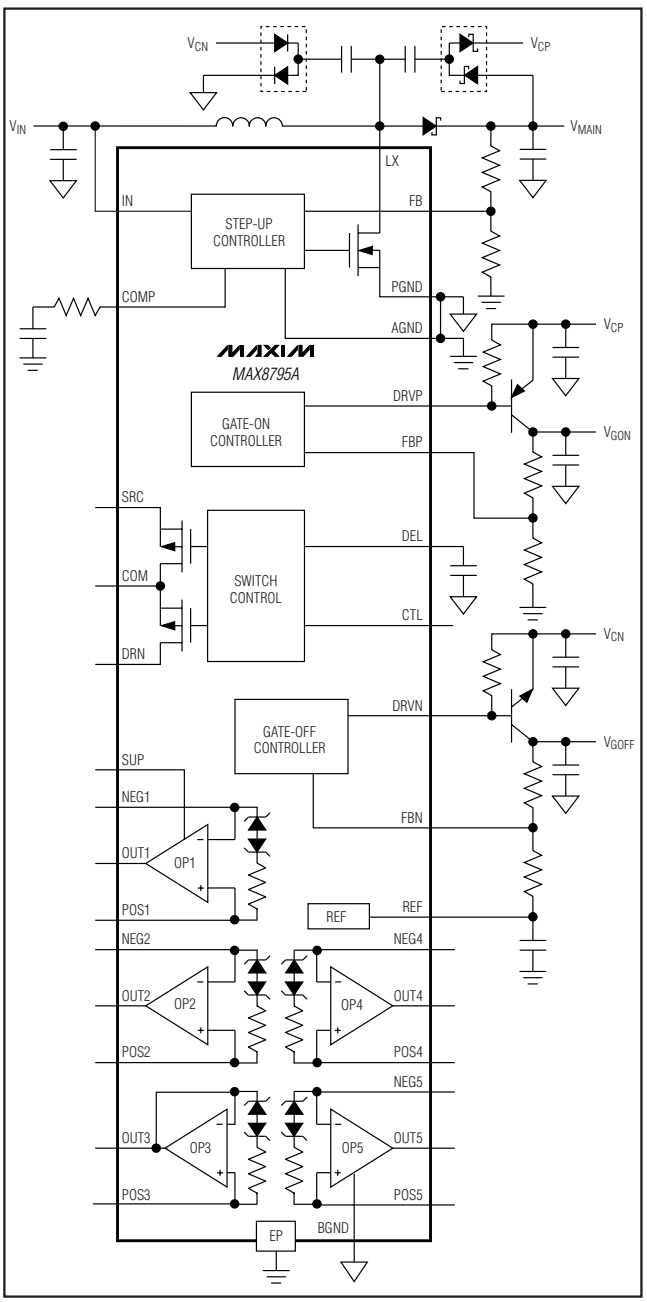


Figure 2. MAX8795A Functional Diagram

Detailed Description

The MAX8795A contains a high-performance step-up switching regulator, two low-cost linear-regulator controllers, multiple high-current operational amplifiers, and startup timing and level-shifting functionality useful for active-matrix TFT LCDs. Figure 2 shows the MAX8795A functional diagram.

Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.2MHz switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 3 shows the functional diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.233V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceeds the COMP

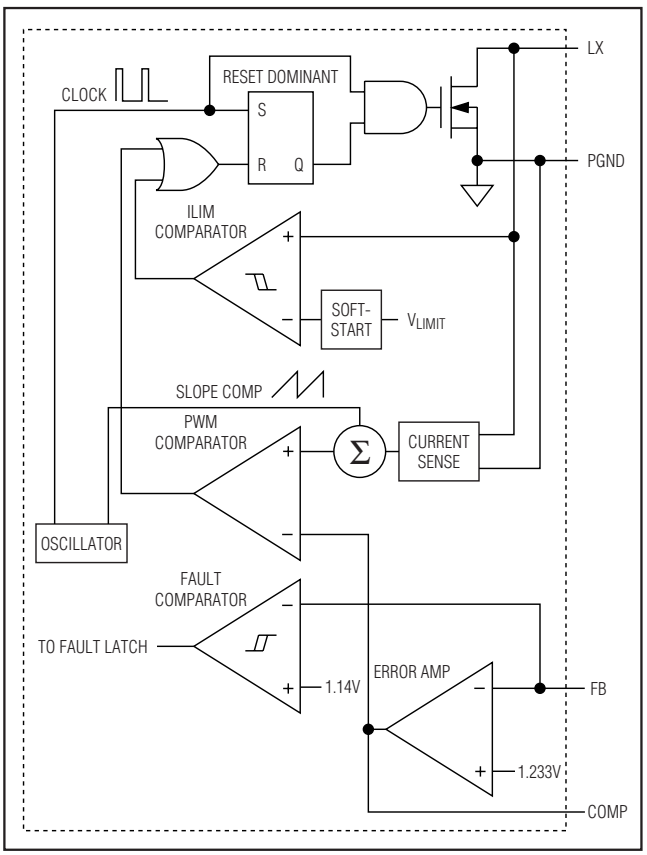


Figure 3. Step-Up Regulator Functional Diagram

voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Gate-On Linear-Regulator Controller, REG P

The gate-on linear-regulator controller (REG P) is an analog gain block with an open-drain n-channel output. It drives an external pnp pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 1). Its guaranteed base-drive sink current is at least 1mA. The regulator including Q1 in Figure 1 uses a 0.47µF ceramic output capacitor and is designed to deliver 20mA at 25V. Other output voltages and currents are possible with the proper pass transistor and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirements* sections.

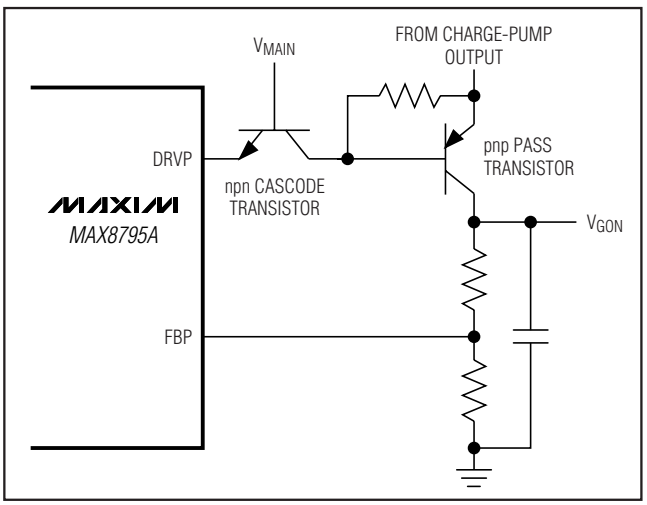


Figure 4. Using Cascoded npn for Charge-Pump Output Voltages > 36V

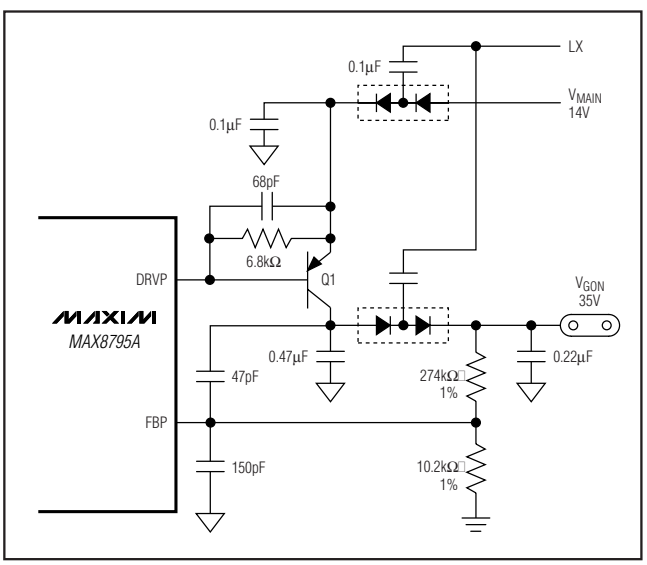


Figure 5. The linear regulator controls the intermediate charge-pump stage.

REG P is typically used to provide the TFT-LCD gate drivers' gate-on voltage. Use a charge pump with as many stages as necessary to obtain a voltage exceeding the required gate-on voltage (see the *Selecting the Number of Charge-Pump Stages* section). Note the voltage rating of DRVP is 36V. If the charge-pump output voltage can exceed 36V, an external cascode npn transistor should be added as shown in Figure 4. Alternately, the linear regulator can control an intermediate charge-pump stage while regulating the final charge-pump output (Figure 5).

TFT-LCD DC-DC Converter with Operational Amplifiers

REG P is enabled after the REF voltage exceeds 1.0V. Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC in 128 steps.

Gate-Off Linear-Regulator Controller, REG N

The gate-off linear-regulator controller (REG N) is an analog gain block with an open-drain p-channel output. It drives an external npn pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 1). Its guaranteed base-drive source current is at least 1mA. The regulator including Q2 in Figure 1 uses a 0.47µF ceramic output capacitor and is designed to deliver 50mA at -10V. Other output voltages and currents are possible with the proper pass transistor and output capacitor (see the *Pass-Transistor Selection* and *Stability Requirements* sections).

REG N is typically used to provide the TFT-LCD gate drivers' gate-off voltage. A negative voltage can be produced using a charge-pump circuit as shown in Figure 1. REG N is enabled after the voltage on REF exceeds 1.0V. Each time it is enabled, the control goes through a soft-start routine that ramps down its internal reference DAC from V_{REF} to 250mV in 128 steps.

Operational Amplifiers

The MAX8795A has five operational amplifiers. The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. They feature ±130mA output short-circuit current, 45V/µs slew rate, and 20MHz/3dB bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Short-Circuit Current Limit and Input Clamp

The operational amplifiers limit short-circuit current to approximately ±130mA if the output is directly shorted to SUP or to BGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled.

The operational amplifiers have 4V input clamp structures in series with a 500Ω resistance and a diode (Figure 2).

Driving Pure Capacitive Load

The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT_ and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.25V rising, 2.20V falling, typ) to ensure the input voltage is high enough for reliable operation. The 50mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, turns off the linear-regulator outputs, and disables the switch control block; the operational-amplifier outputs are high impedance.

Reference Voltage (REF)

The reference output is nominally 1.25V and can source at least 50µA (see the *Typical Operating Characteristics*). Bypass REF with a 0.22µF ceramic capacitor connected between REF and AGND.

Power-Up Sequence and Soft-Start

Once the voltage on IN exceeds approximately 2.25V, the reference turns on. With a 0.22µF REF bypass capacitor, the reference reaches its regulation voltage of 1.25V in approximately 1ms. When the reference voltage exceeds 1.0V, the IC enables the main step-up regulator, the gate-on linear-regulator controller, and the gate-off linear-regulator controller simultaneously.

The IC employs soft-start for each regulator to minimize inrush current and voltage overshoot and to ensure a well-defined startup behavior. Each output uses a 7-bit soft-start DAC. For the step-up and the gate-on linear regulator, the DAC output is stepped in 128 steps from zero up to the reference voltage. For the gate-off linear regulator, the DAC output steps from the reference down to 250mV in 128 steps from zero up to the reference voltage. For the gate-off linear regulator's voltage ramp soft-start, the DAC output steps from the reference down to 250mV in 128 steps. The soft-start duration is 14ms (typ) for all three regulators, and DEL remains pulled down to AGND during the soft start period.

Once the main step-up regulator, the gate-on linear-regulator controller, and the gate-off linear-regulator controller reach regulation, a 5µA current source starts charging

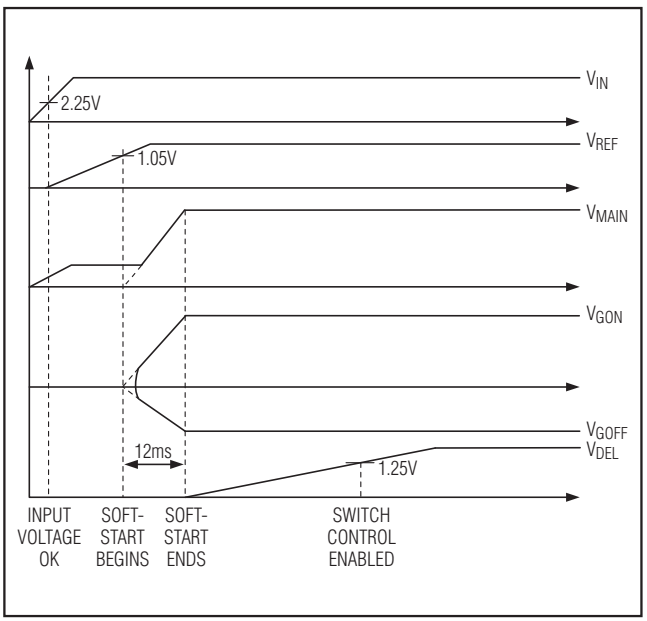


Figure 6. Power-Up Sequence

C_{DEL}. Once the C_{DEL} capacitor voltage exceeds 1.25V (typ), the switch-control block is and op amps are enabled as shown in Figure 6. After the switch-control block is enabled, COM can be connected to SRC or DRN through the internal p-channel switches, depending upon the state of CTL. Before startup and when IN is less than V_{UVLO}, DEL is internally connected to AGND to discharge C_{DEL}. Select C_{DEL} to set the initial start-up delay and the switch-control block startup delay times using the following equation:

$$C_{DEL} = DELAY_TIME \times \frac{16\mu A}{1.25V}$$

Switch-Control Block

The switch-control input (CTL) is not activated until all four of the following conditions are satisfied: the input voltage exceeds V_{UVLO}, the soft-start routine of all the regulators is complete, there is no fault condition detected, and V_{DEL} exceeds its turn-on threshold. Once activated and if CTL is high, the 5Ω internal p-channel switch (Q1) between COM and SRC turns on and the

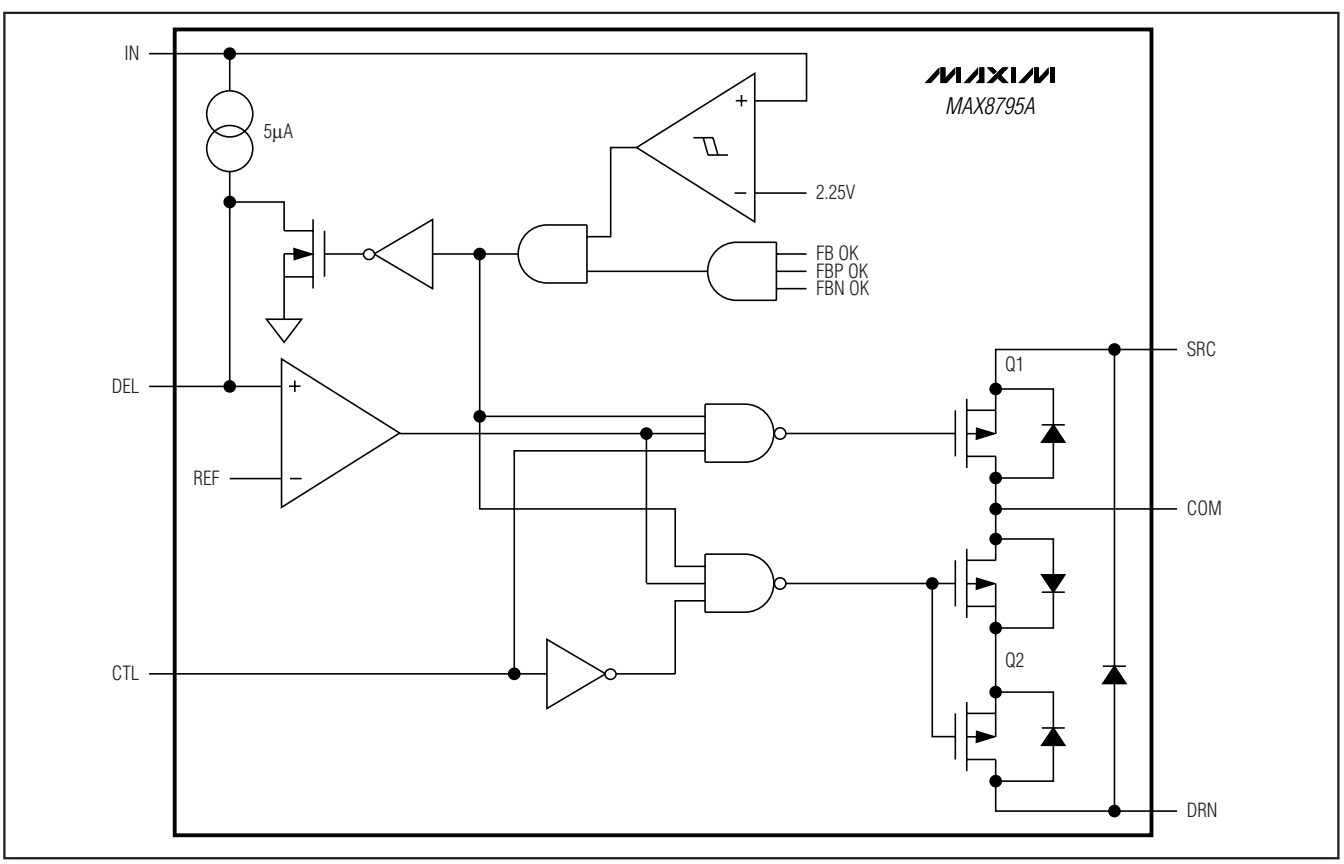


Figure 7. Switch-Control Block

TFT-LCD DC-DC Converter with Operational Amplifiers

30Ω p-channel switch (Q2) between DRN and COM turns off. If CTL is low, Q1 turns off and Q2 turns on.

Fault Protection

During steady-state operation, if the output of the main regulator or any of the linear-regulator outputs does not exceed its respective fault-detection threshold, the MAX8795A activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (200ms typ), the MAX8795A sets the fault latch to shut down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX8795A. When the junction temperature exceeds +160°C, a thermal sensor immediately activates the fault protection, which shuts down all outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output voltage ripple. Size and cost are also important factors to consider.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and conduction losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase size and can increase conduction losses in the inductor. Low inductance values decrease the size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.6. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics* section, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{IN(MIN)}$) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from the appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8795A's LX current limit (I_{LIM}) should exceed I_{PEAK}, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 500mA with a 14V output and

a typical input voltage of 5V. Choosing an LIR of 0.5 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{5V}{14V}\right)^2 \left(\frac{14V - 5V}{0.5A \times 1.2MHz}\right)\left(\frac{0.85}{0.5}\right) \approx 3.3\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.5A \times 14V}{4.5V \times 0.8} \approx 1.94A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (14V - 4.5V)}{3.3\mu H \times 14V \times 1.2MHz} \approx 0.77A$$

$$I_{PEAK} = 1.94A + \frac{0.77A}{2} \approx 2.33A$$

Output-Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{RIPPLE} is the RIPPLE inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 22µF ceramic capacitor is used in the typical applications circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical applications circuit. Ensure a low-noise supply at IN by using adequate C_{IN}. Alternately, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R10 and C13 in Figure 1).

Rectifier Diode

The MAX8795A's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.233V. Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{253 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement. Figures 8 and 9 show the positive and negative charge-pump output voltages for a given V_{MAIN} for one-, two-, and three-stage charge pumps.

TFT-LCD DC-DC Converter with Operational Amplifiers

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

where n_{POS} is the number of positive charge-pump stages, V_{GON} is the gate-on linear-regulator REG P output, V_{MAIN} is the main step-up regulator output, V_D is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

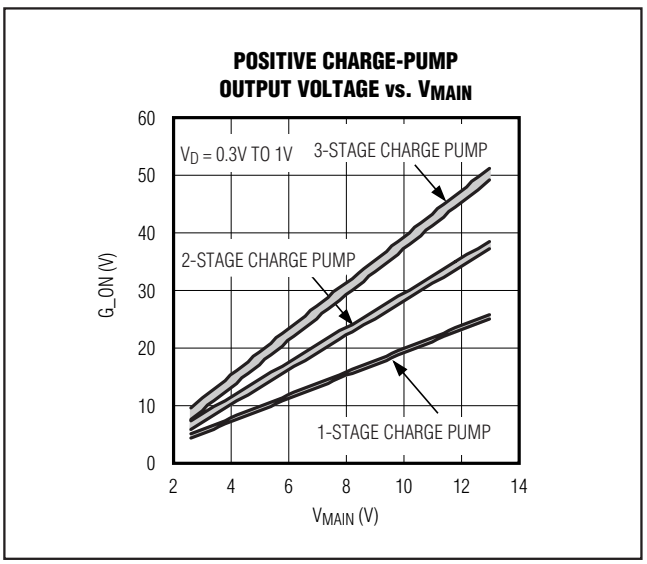


Figure 8. Positive Charge-Pump Output Voltage vs. V_{MAIN}

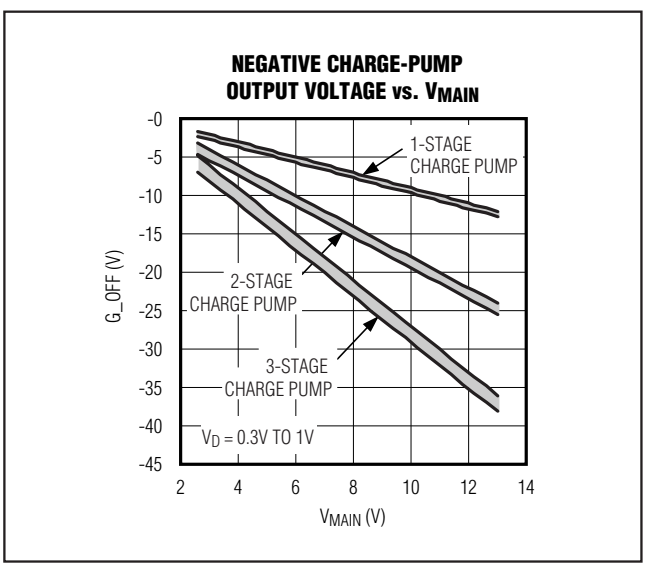


Figure 9. Negative Charge-Pump Output Voltage vs. V_{MAIN}

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{MAIN} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages, V_{GOFF} is the gate-off linear-regulator REG N output, V_{MAIN} is the main step-up regulator output, V_D is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{MAIN} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{IN} or another available supply. If the first charge-pump stage is powered from V_{IN}, the above equations become:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

Flying Capacitors

Increasing the flying-capacitor (C_X) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{MAIN}$$

where n is the stage number in which the flying capacitor appears, and V_{MAIN} is the output voltage of the main step-up regulator.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT_CP} \geq \frac{I_{LOAD_CP}}{2f_{OSC}\ V_{RIPPLE_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use low-cost silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

Linear-Regulator Controllers

Output-Voltage Selection

Adjust the gate-on linear-regulator (REG P) output voltage by connecting a resistive voltage-divider from the REG P output to AGND with the center tap connected to FBP (Figure 1). Select the lower resistor of the divider R5 in the range of 10kΩ to 30kΩ. Calculate the upper resistor R4 with the following equation:

$$R4 = R5 \times \left(\frac{V_{GON}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typ).

Adjust the gate-off linear-regulator REG N output voltage by connecting a resistive voltage-divider from V_{GOFF} to REF with the center tap connected to FBN (Figure 1). Select R8 in the 20kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{FBN} = 250mV, V_{REF} = 1.25V. Note that REF can only source up to 50µA; using a resistor less than 20kΩ for R8 results in higher bias current than REF can supply.

Pass-Transistor Selection

The pass transistor must meet specifications for current gain (h_{FE}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{BE}}{R_{BE}} \right) \times h_{FE(MIN)}$$

where I_{DRV} is the minimum guaranteed base-drive current, V_{BE} is the transistor's base-to-emitter forward voltage drop, and R_{BE} is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended unless the high gain is needed to meet the load-current requirements.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum load current ($I_{LOAD(MAX)_LR}$) multiplied by the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)_LR} \times (V_{IN(MAX)_LR} - V_{OUT_LR})$$

where $V_{IN(MAX)_LR}$ is the maximum input voltage of the linear regulator, and V_{OUT_LR} is the output voltage of the linear regulator.

Stability Requirements

The MAX8795A linear-regulator controllers use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability. The following applies to both linear-regulator controllers in the MAX8795A.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V_LR} \cong \left(\frac{10}{V_T} \right) \times \left[1 + \left(\frac{I_{BIAS} \times h_{FE}}{I_{LOAD_LR}} \right) \right] \times V_{REF}$$

where V_T is 26mV at room temperature, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). For the MAX8795A, the bias currents for both the gate-on

and gate-off linear-regulator controllers are 0.1mA. Therefore, the base-to-emitter resistor for both linear regulators should be chosen to set 0.1mA bias current:

$$R_{BE} = \frac{V_{BE}}{0.1mA} = \frac{0.7V}{0.1mA} \approx 6.8k\Omega$$

The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following equations to verify the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE_LR} = \frac{I_{LOAD(MAX)_LR}}{2\pi \times C_{OUT_LR} \times V_{OUT_LR}}$$

The unity-gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V_LR} \times f_{POLE_LR}$$

2) The pole created by the internal amplifier delay is approximately 1MHz:

$$f_{POLE_AMP} = 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE_IN} = \frac{1}{2\pi \times C_{IN} \times (R_{BE} \,||\, R_{IN})}$$

where:

$$C_{IN} = \frac{g_m}{2\pi f_T},\ R_{IN} = \frac{h_{FE}}{g_m}$$

g_m is the transconductance of the pass transistor, and f_T is the transition frequency. Both parameters can be found in the transistor's data sheet. Because RBE is much greater than RIN, the above equation can be simplified:

$$f_{POLE_IN} = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

Substituting for CIN and RIN yields:

$$f_{POLE_IN} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FB_ and AGND (including stray capacitance):

$$f_{POLE_FB} = \frac{1}{2\pi \times C_{FB} \times (R_{UPPER} \,||\, R_{LOWER})}$$

where CFB is the capacitance between FB_ and AGND, R_{UPPER} is the upper resistor of the linear regulator's feedback divider, and R_{LOWER} is the lower resistor of the divider.

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{POLE_ESR} = \frac{1}{2\pi \times C_{OUT_LR} \times R_{ESR}}$$

where RESR is the equivalent series resistance of COUT_LR.

To ensure stability, choose C_{OUT_LR} large enough so the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several megahertz, and using ceramic capacitors ensures the ESR zero occurs at several megahertz as well. Placing the crossover below 500kHz is sufficient to avoid the amplifier-delay pole and generally works well, unless unusual component choices or extra capacitances move one of the other poles or the zero below 1MHz.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX8795A, with its exposed backside paddle soldered to 1in^2 of PCB copper and a large internal ground plane layer, can dissipate approximately 2.76W into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator has 90% efficiency, approximately 3% to 5% of the power is lost in the internal MOSFET, approximately 3% to 4% in the inductor, and approximately 1% in the output diode. The remaining 1% to 3% is distributed among the input and output capacitors and the PCB traces. If the input power is about 5W, the power lost in the internal MOSFET is approximately 150mW to 250mW.

Operational Amplifier

The power dissipated in the operational amplifiers depends on their output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{OUT_(SOURCE)} \times (V_{SUP} - V_{OUT_})$$

$$PD_{SINK} = I_{OUT_(SINK)} \times V_{OUT_}$$

where $I_{OUT_(SOURCE)}$ is the output current sourced by the operational amplifier, and $I_{OUT_(SINK)}$ is the output current that the operational amplifier sinks.

In a typical case where the supply voltage is 13V and the output voltage is 6V with an output source current of 30mA, the power dissipated is 180mW.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, the output diode, and the output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power-ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier divider ground connections, the COMP and DEL capacitor ground connections, and the device's exposed backside paddle. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside paddle. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors within 5mm of their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Take care to avoid running any feedback trace near LX or the switching nodes in the charge pumps, or provide a ground shield.
- Place the IN pin and REF pin bypass capacitors as close as possible to the device. The ground connection of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces to shield if necessary.

Refer to the MAX8795A evaluation kit for an example of proper PCB layout.

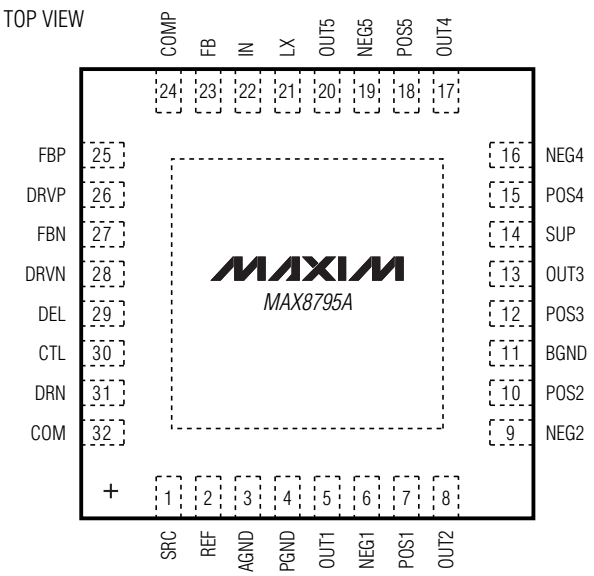
Chip Information

TRANSISTOR COUNT: 6595

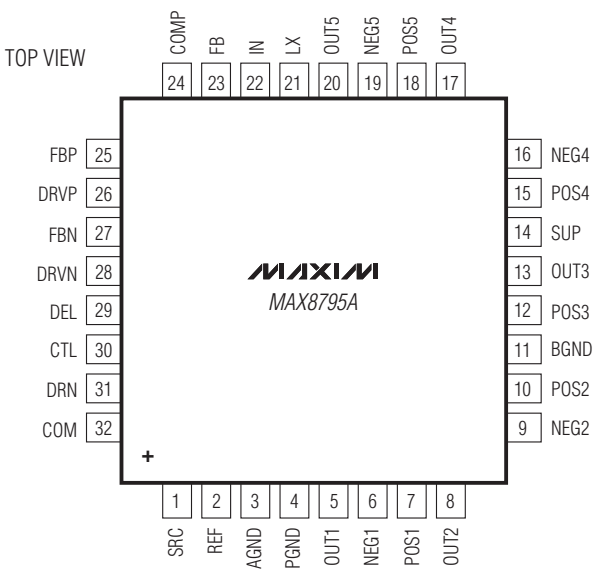
PROCESS: BiCMOS

TFT-LCD DC-DC Converter with Operational Amplifiers

Pin Configurations



THIN QFN
5mm x 5mm

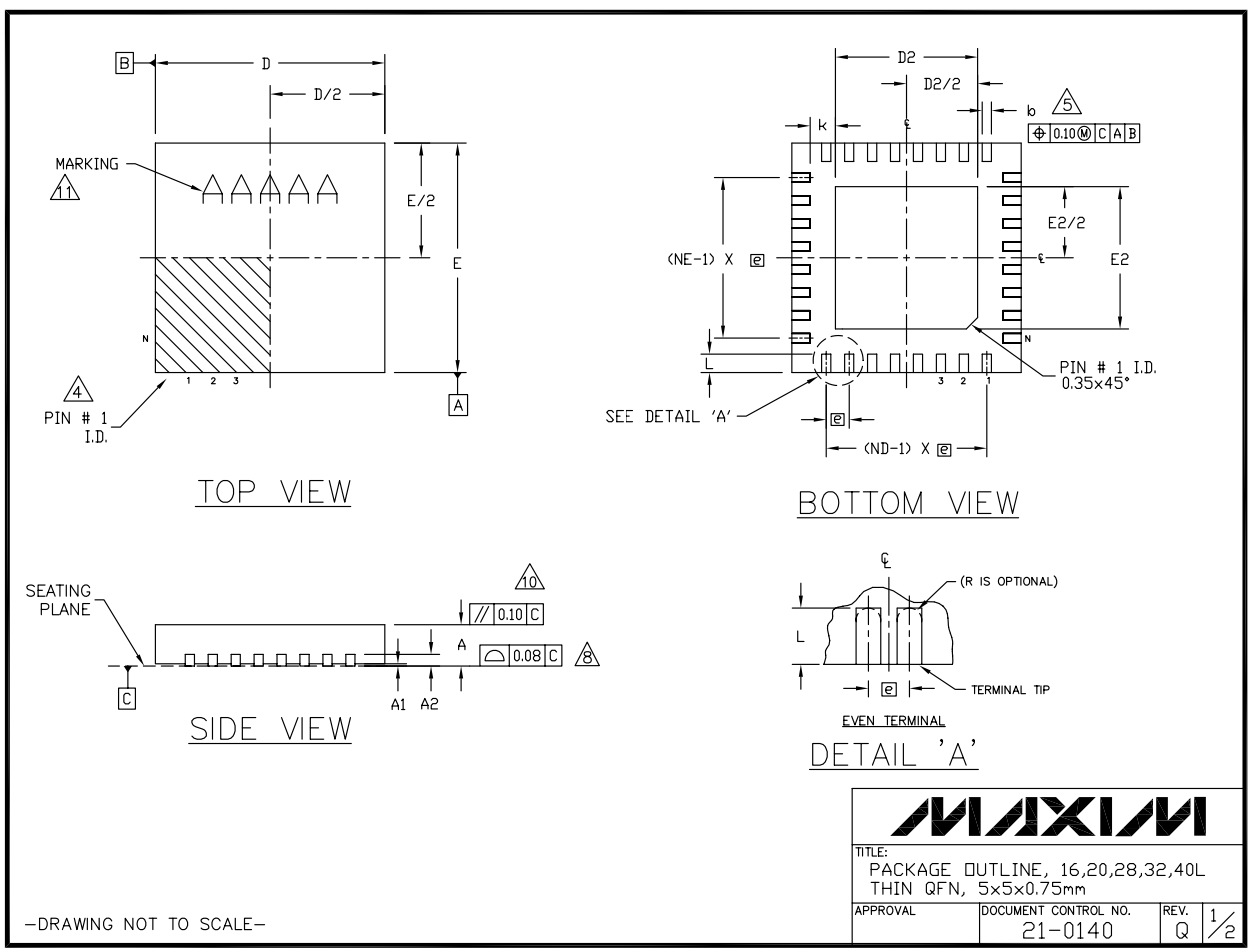


LQFP
7mm x 7mm

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+3	21-0140	90-0025
32 LQFP	C32+2	21-0054	90-0111



TFT-LCD DC-DC Converter with Operational Amplifiers

Package Information (continued)

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COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055M-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855M-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855MK-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

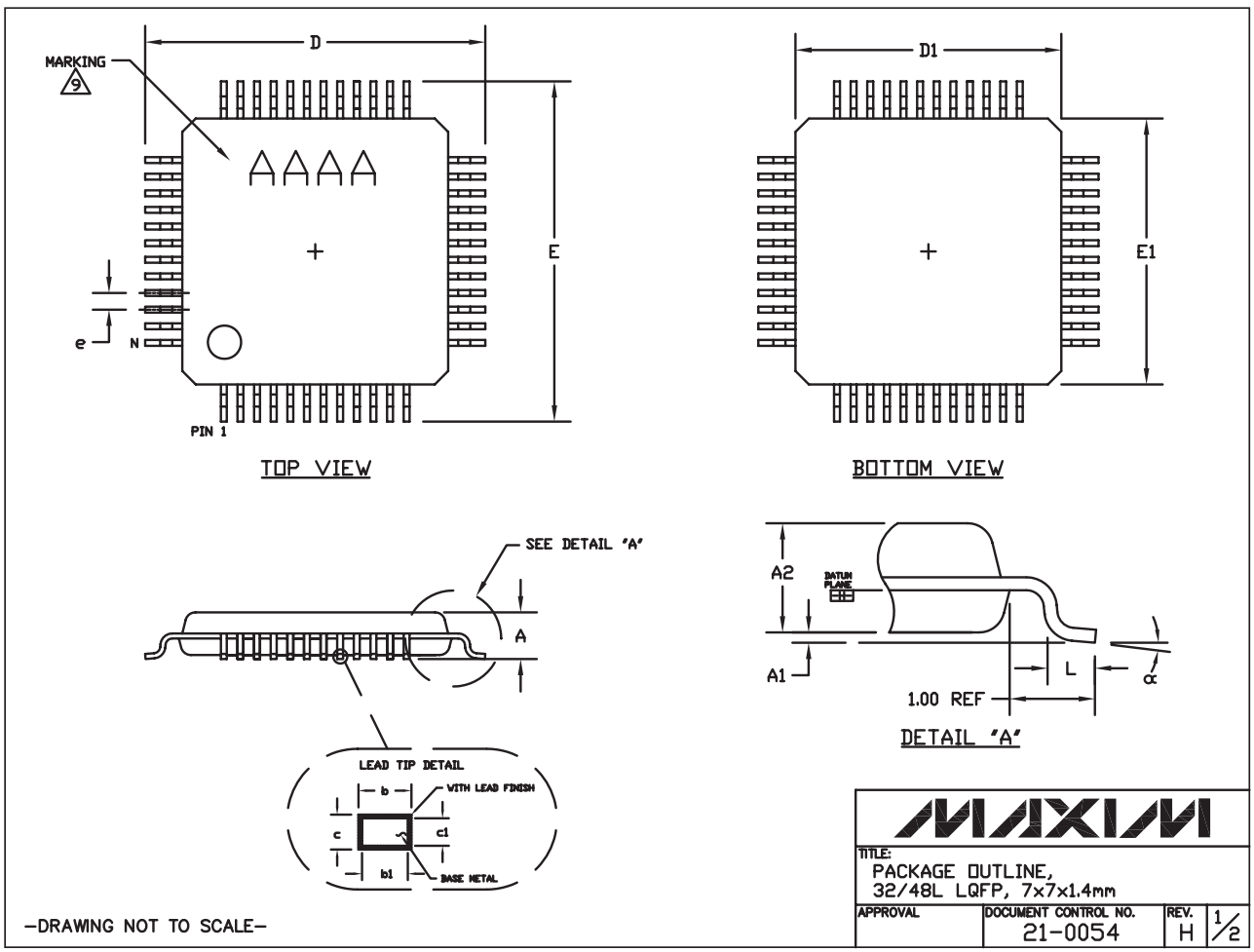
MAXIM

TITLE:
PACKAGE OUTLINE, 16,20,28,32,40L
THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	Q	2/2

Package Information (continued)

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TFT-LCD DC-DC Converter with Operational Amplifiers

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°
PKG. CODES	C32-1, C32-2, C48-1, C48-2, C48-3, C48-5, C48-6			

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 32/48L LQFP, 7x7x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0054	H	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/07	Initial release	0
1	6/07	Added LQFP package and G temperature grade versions	1, 2, 6–30
2	12/10	Added TQFN version	1–10, 27–30
3	3/11	Added automotive-qualified part	1
4	6/11	Corrected automotive /V temperature range	1
5	5/12	Added automotive-qualified part	1

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