19-4238; Rev 2; 11/08

EVALUATION KIT AVAILABLE

Low-Power Video Switches for Dual SCART Connectors

General Description

The MAX9655/MAX9656 dual SCART switches route video signals between a set-top box decoder chip and two external SCART connectors. Under the control of the TV_SEL logic input, the MAX9655 selects whether the CVBS and RGB signals from the encoder or the VCR SCART are routed to the TV SCART. The CVBS signal from the encoder is always routed to the VCR SCART.

The MAX9656 is similar to the MAX9655 except that under the control of the VCR_SEL logic input, the MAX9656 selects whether the CVBS signal from the encoder or the TV SCART is routed to the VCR SCART. The MAX9656 also features a low-power shutdown mode, in which quiescent current falls to 35µA.

The incoming video signals must be AC-coupled to the inputs, which have sync-tip clamps to set the internal DC level. After the input stages, multiplexers select which video signals are routed to the reconstruction filters and output amplifiers. The reconstruction filters are optimized for standard-definition signals and typically have ±1dB passband flatness out to 9.5MHz and 47dB attenuation at 27MHz.

The amplifiers have 2V/V gain, and the outputs can be DC-coupled to a 75Ω load, which is the equivalent of two video loads, or AC-coupled to a 150Ω load.

Applications

SCART Set-Top Boxes

Features

- ♦ **Dual SCART Support for Video Signals**
- ♦ **Supports CVBS Input from TV SCART (MAX9656)**
- ♦ **Reconstruction Filters with 9.5MHz Passband and 47dB Attenuation at 27MHz**
- ♦ **Fixed Gain of 2V/V**
- ♦ **Input Sync-Tip Clamps**
- ♦ **2.7V to 3.6V Single-Supply Operation**

Ordering Information

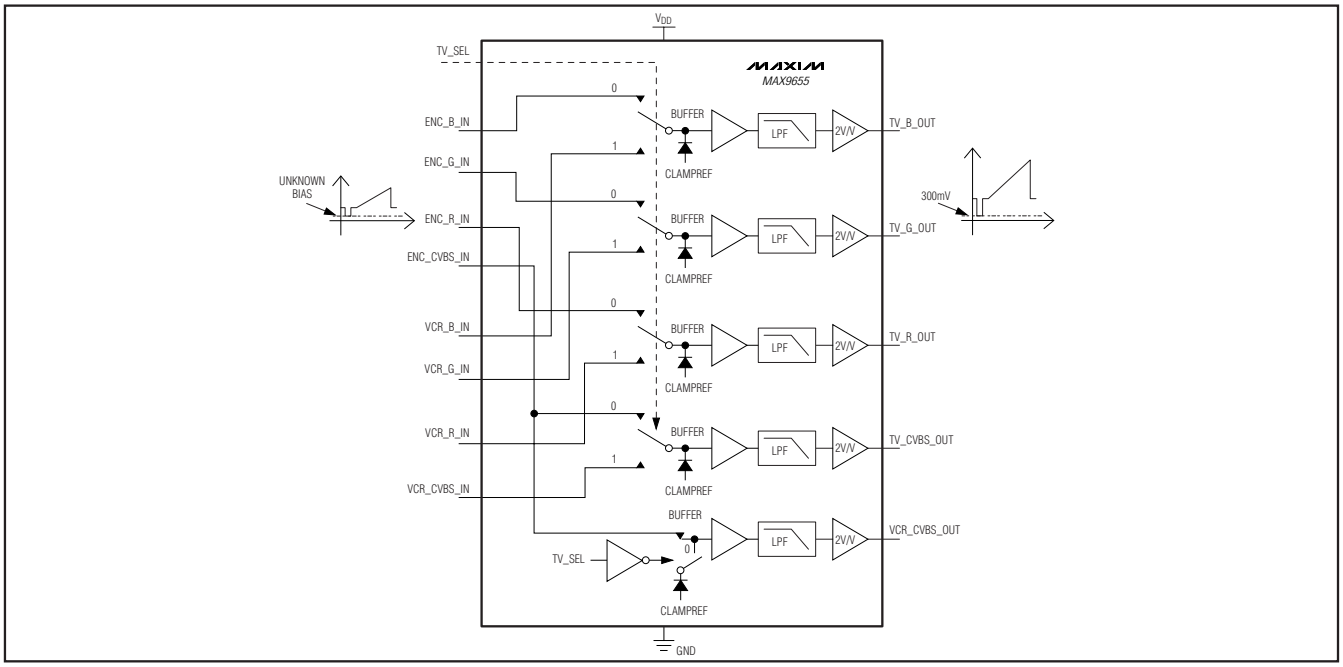
PART	PIN-PACKAGE	TV SCART CVBS RETURN SUPPORT
MAX9655AEE+	16 QSOP	No
MAX9656AEP+	20 QSOP	Yes

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead-free/RoHS-compliant package.

Pin Configurations and Typical Application Circuits appear at end of data sheet.

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Power Video Switches for Dual SCART Connectors

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{DD} to GND .....-0.3V to +4V
All Video and Logic Input Pins.....(GND - 0.3V) to +4V
Duration of Output Short Circuit to V_{DD} or GND .....Continuous
Continuous Input Current
All Video and Logic Input Pins .....±20mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
20-Pin QSOP (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{GND} = 0, $V_{\overline{SHDN}}$ = V_{DD}, VCR_SEL = V_{DD}, TV_SEL = V_{DD}, R_L = 150Ω to GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by power-supply rejection test		2.7	3.3	3.6	V
Quiescent Supply Current	I_{DD}	No load			21	45	mA
Shutdown Supply Current	I_{SHDN}	$V_{\overline{SHDN}}$ = TV_SEL = VCR_SEL = GND (MAX9656 only)			35	70	µA
Input Voltage		Unselected input			V_{DD}/3		V
Input Resistance		Unselected input			222		kΩ
Sync-Tip Clamp Level	V_{CLP}			0.23	0.3	0.39	V
Input Voltage Range		Guaranteed by output-voltage swing	2.7V ≤ V_{DD} ≤ 3.6V			1.05	V_{P-P}
			3.0V ≤ V_{DD} ≤ 3.6V			1.2	
Sync Crush		Sync-tip clamp; percentage reduction in sync pulse (0.3V_{P-P}); guaranteed by input clamping current measurement				2	%
Input Clamping Current					1	2	µA
Maximum Input Source Resistance					300		Ω
DC Voltage Gain	A_V	R_L = 150Ω to GND (Note 2)	V_{DD} = 2.7V, 0V ≤ V_{IN} ≤ 1.05V	1.96	2	2.04	V/V
			V_{DD} = 3.0V, 0V ≤ V_{IN} ≤ 1.2V	1.96	2	2.04	
DC Gain Mismatch		Guaranteed by output-voltage swing		-2		+2	%
Output Level		Measured at output, $C_{IN_}$ = 0.1µF to GND		0.218	0.3	0.39	V
Output-Voltage Swing		Measured at output, V_{DD} = 2.7V, V_{IN} = V_{CLP} to (V_{CLP} +1.05V), R_L = 150Ω to -0.2V			2.1		V_{P-P}
		Measured at output, V_{DD} = 2.7V, V_{IN} = V_{CLP} to (V_{CLP} +1.05V), R_L = 150Ω to V_{DD}/2			2.1		
		Measured at output, V_{DD} = 3.0V, V_{IN} = V_{CLP} to (V_{CLP} +1.2V), R_L = 150Ω to -0.2V			2.4		
		Measured at output, V_{DD} = 3.0V, V_{IN} = V_{CLP} to (V_{CLP} +1.2V), R_L = 150Ω to V_{DD}/2			2.4		
		Measured at output, V_{DD} = 3.135V, V_{IN} = V_{CLP} to (V_{CLP} +1.05V), R_L = 75Ω to -0.2V			2.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{GND} = 0, $V_{\overline{SHDN}}$ = V_{DD}, VCR_SEL = V_{DD}, TV_SEL = V_{DD}, R_L = 150Ω to GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

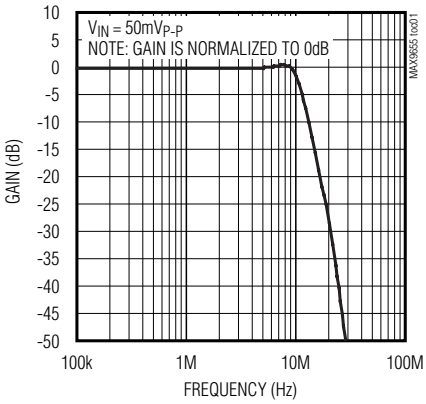
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current		Short to GND (sourcing)			140		mA
		Short to V_{DD} (sinking)			70		
Output Resistance	R_{OUT}	V_{OUT} = 1.5V, -10mA ≤ I_{LOAD} ≤ +10mA			0.2		Ω
Power-Supply Rejection Ratio		2.7V ≤ V_{DD} ≤ 3.6V		48	64		dB
		f = 1MHz, 100mV_{P-P}			20		
Standard-Definition Reconstruction Filter		V_{OUT} = 2V_{P-P}, reference frequency is 100kHz, ±1dB passband flatness			9.5		MHz
		V_{OUT} = 2V_{P-P}, reference frequency is 100kHz	f = 5.5MHz		0.1		dB
			f = 9.5MHz		-1		
			f = 10MHz		-3		
			f = 27MHz		-47		
Differential Gain	DG	5-step modulated staircase of 129mV step size and 286mV peak-to-peak subcarrier amplitude, f = 4.43MHz			0.4		%
Differential Phase	DP	5-step modulated staircase of 129mV step size and 286mV peak-to-peak subcarrier amplitude, f = 4.43MHz			0.45		deg
Group-Delay Distortion		100kHz ≤ f ≤ 5MHz, outputs are 2V_{P-P}			9		ns
Peak Signal to RMS Noise		100kHz ≤ f ≤ 5MHz			71		dB
2T Pulse Response		2T = 200ns			0.2		K%
2T Bar Response		2T = 200ns; bar time is 18µs; the beginning 2.5% and the ending 2.5% of the bar time are ignored			0.2		K%
2T Pulse-to-Bar K Rating		2T = 200ns; bar time is 18µs; the beginning 2.5% and the ending 2.5% of the bar time are ignored			0.3		K%
Nonlinearity		5-step staircase			0.1		%
Output Impedance		f = 5.5MHz			8.07		Ω
All-Hostile Crosstalk		f = 15kHz			-82		dB
		f = 4.43MHz			-78		
Output-to-Input Crosstalk		f = 30MHz			-68		dB
LOGIC SIGNALS (MAX9655: TV_SEL, MAX9656: TV_SEL, VCR_SEL, $\overline{SHDN}$)							
Logic-Low Threshold	V_{IL}	T_A = +25°C				0.3 x V_{DD}	V
Logic-High Threshold	V_{IH}	T_A = +25°C		0.7 x V_{DD}			V
Logic Input Current	I_{IN}	T_A = +25°C				10	µA

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Voltage gain (A_V) is a two-point measurement in which the output-voltage swing is divided by the input-voltage swing.

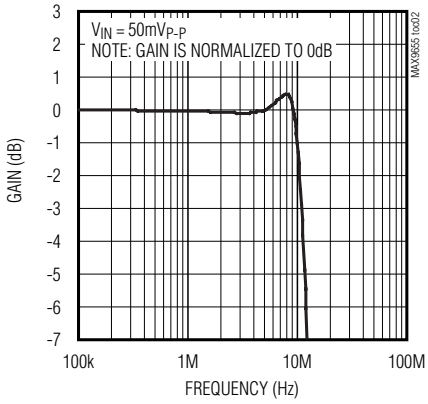
Typical Operating Characteristics

(V_{DD} = 3.3V, V_{GND} = 0, $V_{\overline{SHDN}}$ = V_{DD}, R_L = 150Ω to GND, T_A = +25°C.)

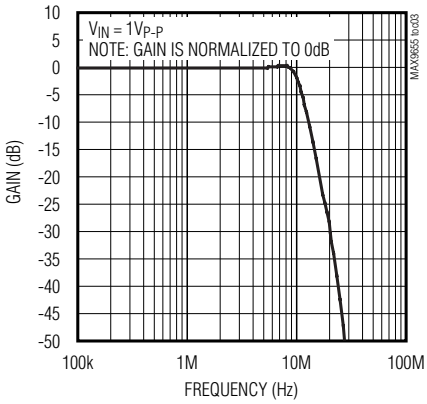
SMALL-SIGNAL GAIN vs. FREQUENCY



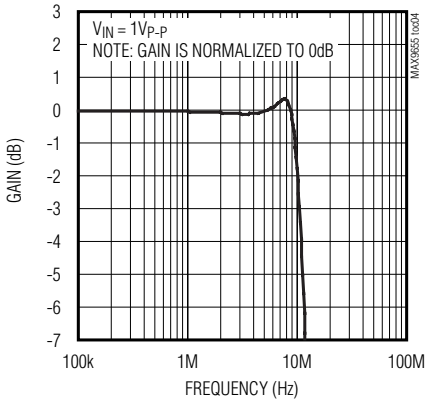
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



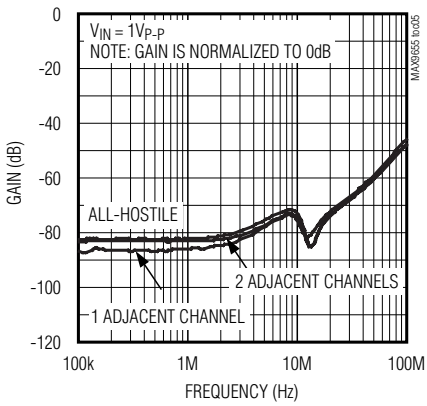
LARGE-SIGNAL GAIN vs. FREQUENCY



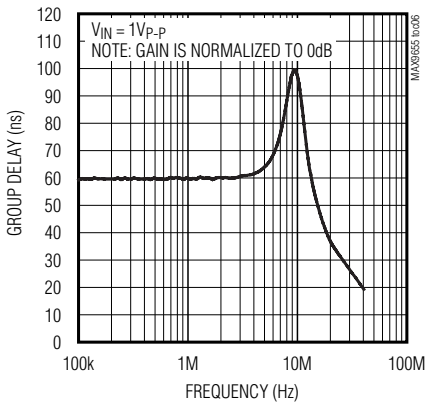
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



VIDEO CROSSTALK vs. FREQUENCY



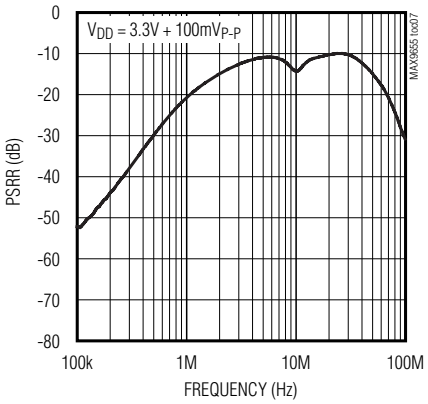
VIDEO GROUP DELAY DISTORTION vs. FREQUENCY



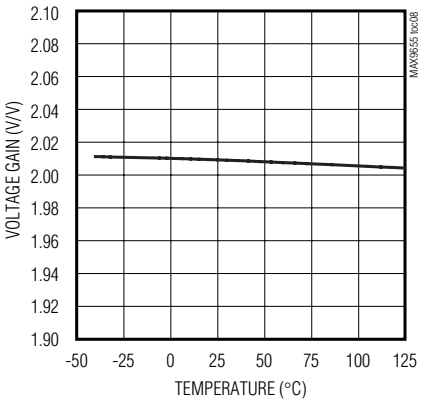
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{GND} = 0, $V_{\overline{SHDN}}$ = V_{DD}, R_L = 150Ω to GND, T_A = +25°C.)

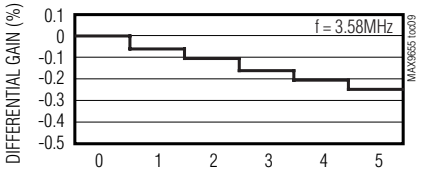
VIDEO PSRR vs. FREQUENCY



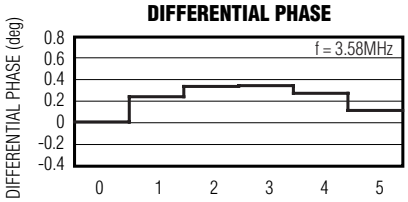
VOLTAGE GAIN vs. TEMPERATURE



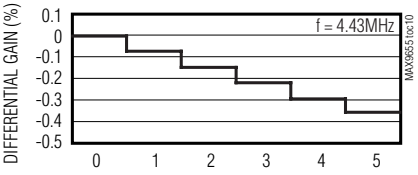
DIFFERENTIAL GAIN



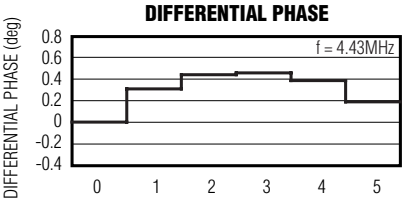
DIFFERENTIAL PHASE



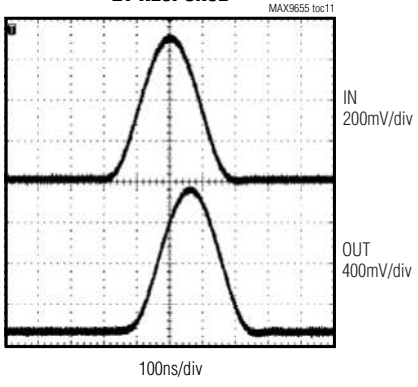
DIFFERENTIAL GAIN



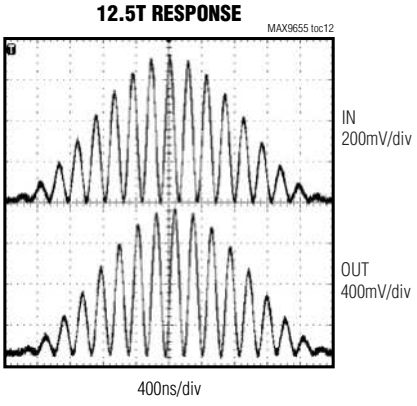
DIFFERENTIAL PHASE



2T RESPONSE



12.5T RESPONSE

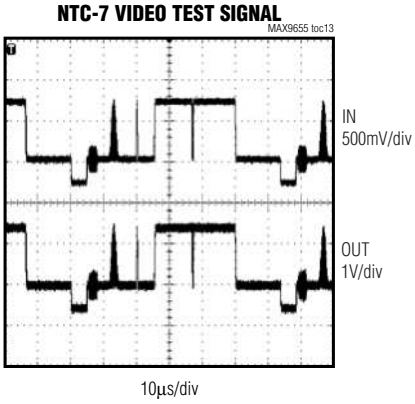


Low-Power Video Switches for Dual SCART Connectors

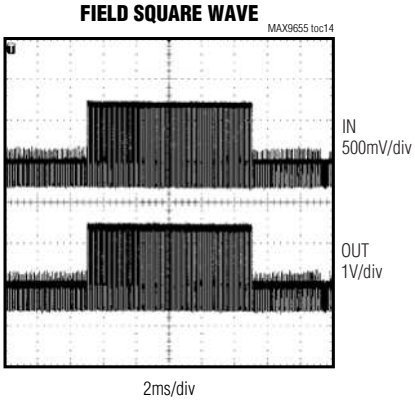
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{GND} = 0, $V_{\overline{SHDN}}$ = V_{DD}, R_L = 150Ω to GND, T_A = +25°C.)

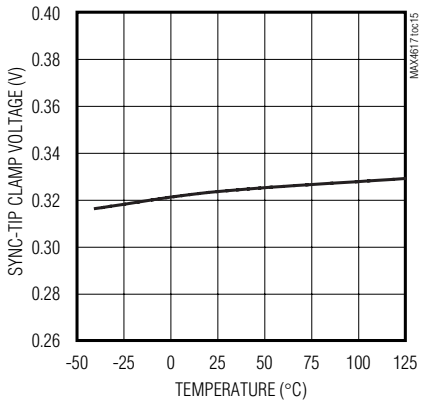
NTC-7 VIDEO TEST SIGNAL



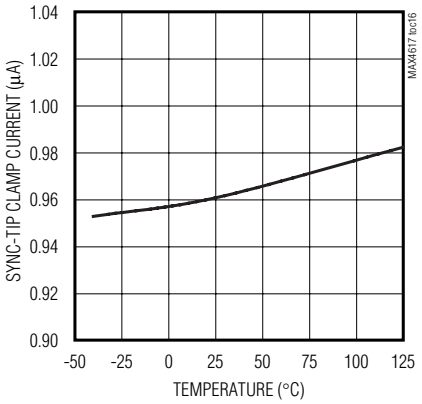
FIELD SQUARE WAVE



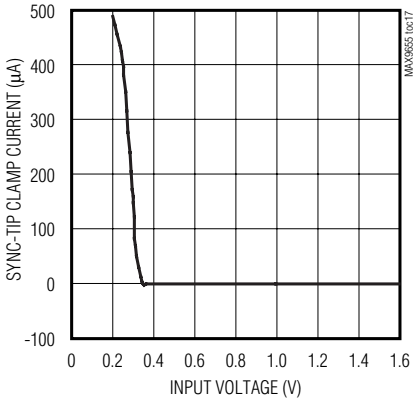
VIDEO SYNC-TIP CLAMP VOLTAGE vs. TEMPERATURE



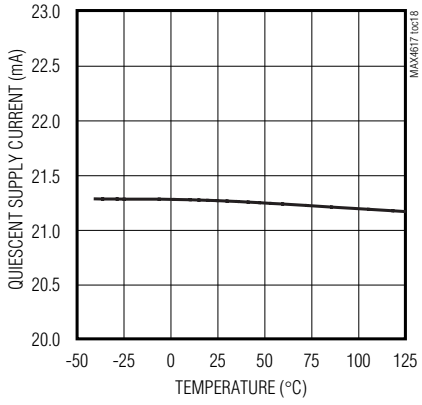
VIDEO SYNC-TIP CLAMP CURRENT vs. TEMPERATURE



SYNC-TIP CLAMP CURRENT vs. INPUT VOLTAGE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX9655	MAX9656		
1	2	ENC_B_IN	Encoder Blue Video Input. AC-couple the signal through a 0.1µF capacitor.
2	3	ENC_G_IN	Encoder Green Video Input. AC-couple the signal through a 0.1µF capacitor.
3	4	ENC_R_IN	Encoder Red Video Input. AC-couple the signal through a 0.1µF capacitor.
4	5	ENC_CVBS_IN	Encoder Composite Video Input. AC-couple the signal through a 0.1µF capacitor.
5	6	VCR_B_IN	VCR SCART Blue Video Input. AC-couple the signal through a 0.1µF capacitor.
6	7	VCR_G_IN	VCR SCART Green Video Input. AC-couple the signal through a 0.1µF capacitor.
7	8	VCR_R_IN	VCR SCART Red Video Input. AC-couple the signal through a 0.1µF capacitor.
8	9	VCR_CVBS_IN	VCR SCART Composite Video Input. AC-couple the signal through a 0.1µF capacitor.
9	11	GND	Ground
10	13	VCR_CVBS_OUT	VCR SCART Composite Video Output. The sync tip is biased at 0.3V.
11	14	TV_CVBS_OUT	TV SCART Composite Video Output. The sync tip is biased at 0.3V.
12	15	TV_R_OUT	TV SCART Red Video Output. The sync tip is biased at 0.3V.
13	16	TV_G_OUT	TV SCART Green Video Output. The sync tip is biased at 0.3V.
14	17	TV_B_OUT	TV SCART Blue Video Output. The sync tip is biased at 0.3V.
15	18	TV_SEL	TV SCART Output Selection. Connect to GND to route the encoder video signals to the TV SCART outputs. Connect to V_{DD} to route the VCR SCART video signals to the TV SCART outputs.
16	19	V_{DD}	Positive Power Supply. Bypass with 0.1µF ceramic capacitors to GND.
—	1	TV_CVBS_IN	Television SCART Composite Video Input. AC-couple the signal through a 0.1µF capacitor.
—	10	N.C.	No Connection. Not internally connected.
—	12	$\overline{SHDN}$	Active-Low Shutdown Logic Input. Connect to GND to place device in shutdown. Connect to V_{DD} for normal operation.
—	20	VCR_SEL	VCR SCART Output Selection. Connect to GND to route ENC_CVBS_IN to the VCR SCART CVBS output. Connect to V_{DD} to route TV_CVBS_IN to the VCR SCART CVBS output.

Detailed Description

A MAX9655 or a MAX9656 can comprise the video portion of a low-cost, dual SCART solution in set-top boxes with a subset of the full SCART functions. The MAX9655/MAX9656 select whether the CVBS, red, green, and blue video signals from the encoder or the VCR SCART are routed to the TV SCART. The MAX9655/MAX9656 support the output of one CVBS signal to the VCR SCART. In the MAX9655, the CVBS signal from the encoder is routed to the VCR SCART.

In the MAX9656, the CVBS signal routed to the VCR SCART can come from the encoder or TV SCART. In the typical usage case, the VCR (or DVD recorder) records a television program from the set-top box. In such a case, the encoder would be the source of the CVBS signal. Support for the TV SCART CVBS return path is useful when a person wants to record on his VCR (or more likely DVD recorder) a television program received through the television's antenna. The television program is transmitted from the television to the set-top box and then to the VCR.

Both the MAX9655 and MAX9656 have integrated reconstruction filters so that when the encoder video signals are routed to the TV SCART or the VCR SCART, the steps and spikes left by the video digital-to-analog converter (DAC) are smoothed away. Although the incoming video signals from the VCR SCART are assumed to be filtered already, the reconstruction filter has wide enough bandwidth so that the video signals from the VCR SCART are not degraded.

Low-Power Video Switches for Dual SCART Connectors

The incoming video signals can have any DC bias because the input sync-tip clamps restore the DC level. The output amplifiers have a gain of 2V/V. The MAX9655/MAX9656 operate from a single 3.3V supply and consume low quiescent power and low average power. In addition, the MAX9656 also has shutdown mode.

Operating Modes

TV_SEL controls whether the encoder or VCR video signals are sent to the TV SCART. See Table 1.

On the MAX9656, VCR_SEL controls whether the CVBS signal from the TV SCART or the encoder is sent to the VCR SCART. $\overline{SHDN}$ controls whether the device is on or off. See Tables 2 and 3. In shutdown, the outputs of the MAX9656 are high impedance.

Input

Every video signal must be AC-coupled to the MAX9655/MAX9656 through 0.1µF capacitors. The MAX9655/MAX9656 have sync-tip clamps and bias circuits to restore the DC level of the video signal after the input coupling capacitor. When a video input is selected, the input has a sync-tip clamp, which accepts video signals that have sync pulses or that reach their minimum level during sync. Composite video with blanking and sync (CVBS) is an example of a video signal with sync pulses. The red, green, and blue signals in an RGBS signal set are examples of signals that return to their blank level during sync. The sync-tip voltage is internally set to 300mV.

When a video input is not selected, the inputs to the MAX9655 and the MAX9656 do not distort the video signal in case the video source is driving video signals to another video circuit such as a video multiplexer. The inputs are biased at $V_{DD}/3$, which is sufficiently above ground so that the ESD diodes never forward bias as the video signal changes. The input resistance is 220kΩ, which presents negligible loading on the video current DAC. The sole exception to this condition is ENC_CVBS_IN (MAX9655), in which the input circuit is always a sync-tip clamp. Table 4 summarizes which input circuit is active on the inputs of the MAX9655 depending on TV_SEL. Table 5 summarizes which input circuit is active on the inputs of the MAX9656 depending on TV_SEL and VCR_SEL.

Table 1. TV_SEL Logic (Applicable to Both the MAX9655 and the MAX9656)

LOGIC STATE	MODE
Low	Encoder video signals are routed to the TV SCART.
High	VCR SCART video signals are routed to the TV SCART.

Table 2. VCR_SEL Logic (Only Applicable to the MAX9656)

LOGIC STATE	MODE
Low	CVBS signal from encoder is routed to the VCR SCART.
High	CVBS signal from the TV SCART is routed to the VCR SCART.

Table 3. $\overline{SHDN}$ Logic (Only Applicable to the MAX9656)

LOGIC STATE	MODE
Low	Off
High	On

Table 4. MAX9655 Input Circuit of Input as Determined by State of TV_SEL

INPUT	INPUT CIRCUIT (TV_SEL = LOW)	INPUT CIRCUIT (TV_SEL = HIGH)
ENC_B_IN	Sync-tip clamp	Bias
ENC_G_IN	Sync-tip clamp	Bias
ENC_R_IN	Sync-tip clamp	Bias
ENC_CVBS_IN	Sync-tip clamp	Sync-tip clamp
VCR_B_IN	Bias	Sync-tip clamp
VCR_G_IN	Bias	Sync-tip clamp
VCR_R_IN	Bias	Sync-tip clamp
VCR_CVBS_IN	Bias	Sync-tip clamp

Table 5. MAX9656 Input Circuit of Input as Determined by State of TV_SEL

INPUT	INPUT CIRCUIT (TV_SEL = LOW)		INPUT CIRCUIT (TV_SEL = HIGH)	
ENC_B_IN	Sync-tip clamp		Bias	
ENC_G_IN	Sync-tip clamp		Bias	
ENC_R_IN	Sync-tip clamp		Bias	
ENC_CVBS_IN	Sync-tip clamp (VCR_SEL = 0)	Sync-tip clamp (VCR_SEL = 1)	Sync-tip clamp (VCR_SEL = 0)	Bias (VCR_SEL = 1)
TV_CVBS_IN	Bias (VCR_SEL = 0)	Sync-tip clamp (VCR_SEL = 1)	Bias (VCR_SEL = 0)	Sync-tip clamp (VCR_SEL = 1)
VCR_B_IN	Bias		Sync-tip clamp	
VCR_G_IN	Bias		Sync-tip clamp	
VCR_R_IN	Bias		Sync-tip clamp	
VCR_CVBS_IN	Bias		Sync-tip clamp	

Note: *VCR_SEL = X (don't care), except where noted.*

When the MAX9656 is in shutdown, its inputs are biased at the same voltage and present the same input resistance as unselected inputs.

Video Filter

The MAX9655/MAX9656 video filter features ±1dB passband out to 9.5MHz and 47dB attenuation at 27MHz, making the filter suitable for standard-definition video signals from all sources (e.g., broadcast and DVD). Broadcast video signals are channel limited: NTSC signals have 4.2MHz bandwidth, and PAL signals have 5MHz bandwidth. Video signals from a DVD player, however, are not channel limited; so the bandwidth of DVD video signals can approach the Nyquist limit of 6.75MHz. Recommendation: ITU-R BT.601-5 specifies 13.5MHz as the sampling rate for standard-definition video. Therefore, the maximum bandwidth of the signal is 6.75MHz. To ease the filtering requirements, most modern video systems oversample by two times, clocking the video current DAC at 27MHz.

Outputs

The video output amplifiers can both source and sink load current, allowing output loads to be DC- or AC-coupled. The amplifier output stage needs approximately 300mV of headroom from either supply rail. The devices have an internal level-shift circuit that positions the sync tip at approximately 300mV at the output.

If the supply voltage is greater than 3.135V (5% below a 3.3V supply), each amplifier can drive two DC-coupled video loads to ground. If the supply is less than 3.135V, each amplifier can drive only one DC-coupled or AC-coupled video load.

Applications Information

Audio Switch for Dual SCART Connectors

In addition to video signals, SCART connectors also support left and right audio signals that are full duplex. Figure 1 shows a matching audio switch for the MAX9655. Notice that it can be made from low-cost, discrete components. It is assumed that the set-top box chip generates the left and right audio signals directly, or the set-top box chip sends an I^2S stream to a stereo audio DAC that generates the left and right audio signals. In both cases, the audio signals are filtered and amplified by a dual audio op amp before they are presented to the audio switch.

Figure 2 shows a matching audio switch for the MAX9656. Similar to how the MAX9656 handles video signals, the audio signals from the set-top box chip or the audio signals from the TV SCART are routed to the VCR SCART.

AC-Coupling the Outputs

The outputs can be AC-coupled since the output stage can source and sink current as shown in Figure 3. Coupling capacitors should be 220µF or greater to keep the highpass filter, formed by the 150Ω equivalent resistance of the video transmission line, to a corner frequency of 4.8Hz or below. The frame rate of PAL systems is 25Hz. The corner frequency should be well below the frame rate.

Low-Power Video Switches for Dual SCART Connectors

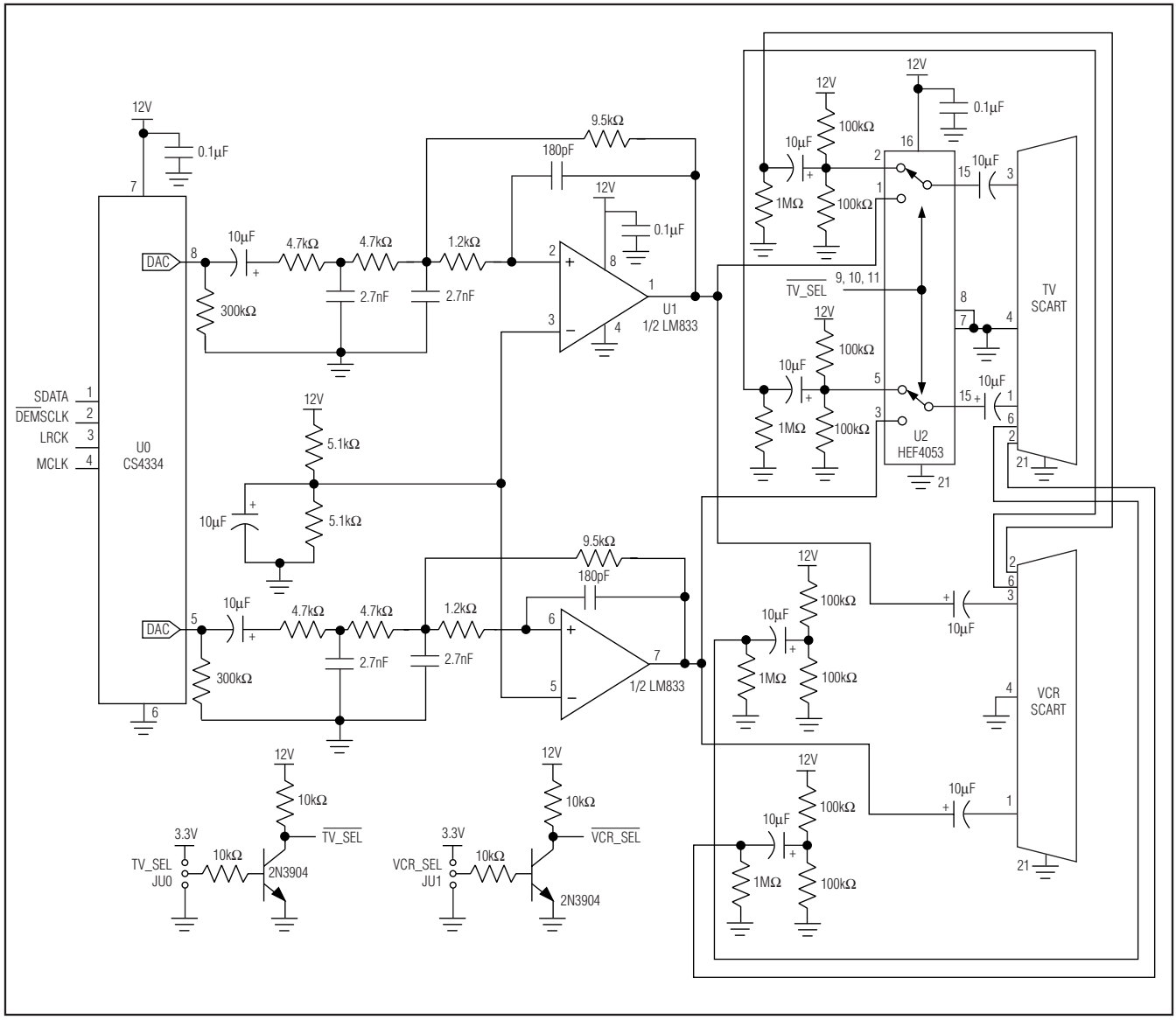


Figure 1. Audio Switch for the MAX9655

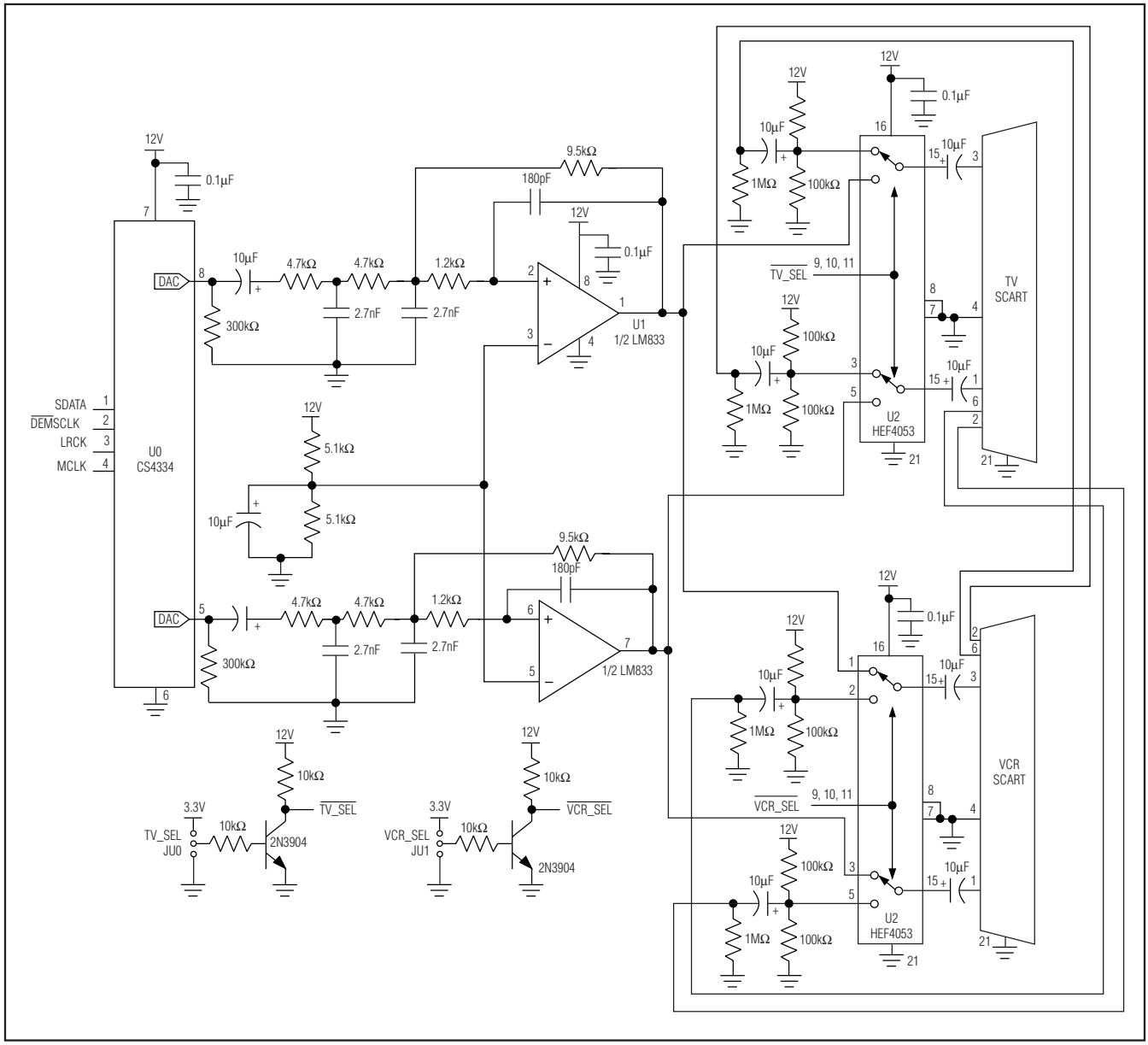


Figure 2. Audio Switch for the MAX9656

Low-Power Video Switches for Dual SCART Connectors

Table 6. Quiescent and Average Power Consumption for MAX9655/MAX9656

MEASUREMENTS	POWER CONSUMPTION (mW)	CONDITIONS
Quiescent Power Consumption	69	No load.
Average Power Consumption	175 (MAX9655)	150Ω to ground on each output. 50% flat field signal on each input.
	200 (MAX9656)	

Power Consumption

The quiescent power consumption and average power consumption of the MAX9655/MAX9656 are very low because of the 3.3V operation and low-power circuit design. Quiescent power consumption is defined when the MAX9655/MAX9656 are operating without loads and without any video signals.

Average power consumption represents the normal power consumption when the devices drive real video signals into real video loads. It is measured when the MAX9655/MAX9656 drive a 150Ω load to ground with a 50% flat field, which serves as a proxy for a real video signal.

Table 6 shows the quiescent and average power consumption of the MAX9655/MAX9656.

Power-Supply Bypassing and Ground

The MAX9655/MAX9656 operate from a single-supply voltage down to 2.7V, allowing for low-power operation. Bypass V_{DD} to GND with a 0.1µF capacitor. Place all external components as close as possible to the device.

Chip Information

PROCESS: BiCMOS

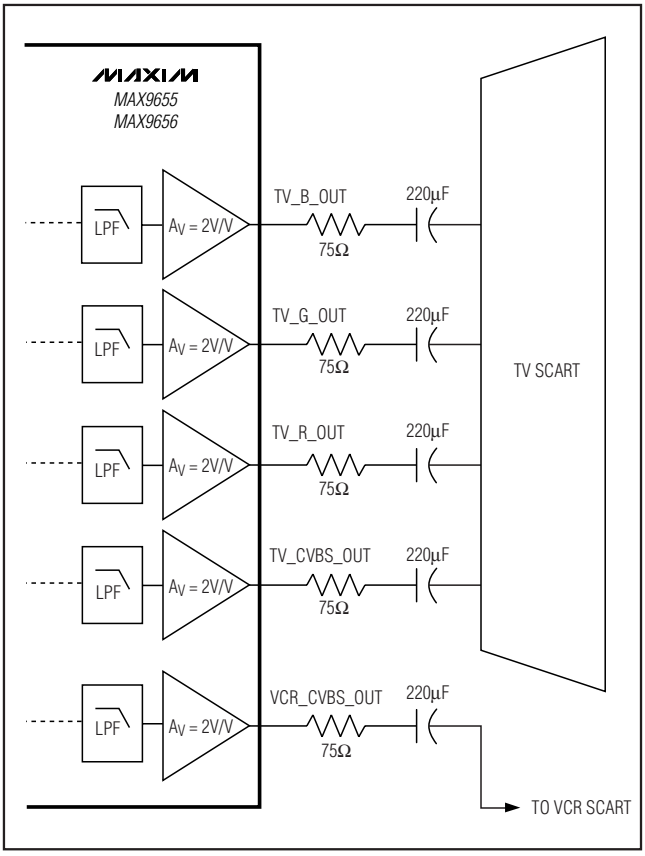
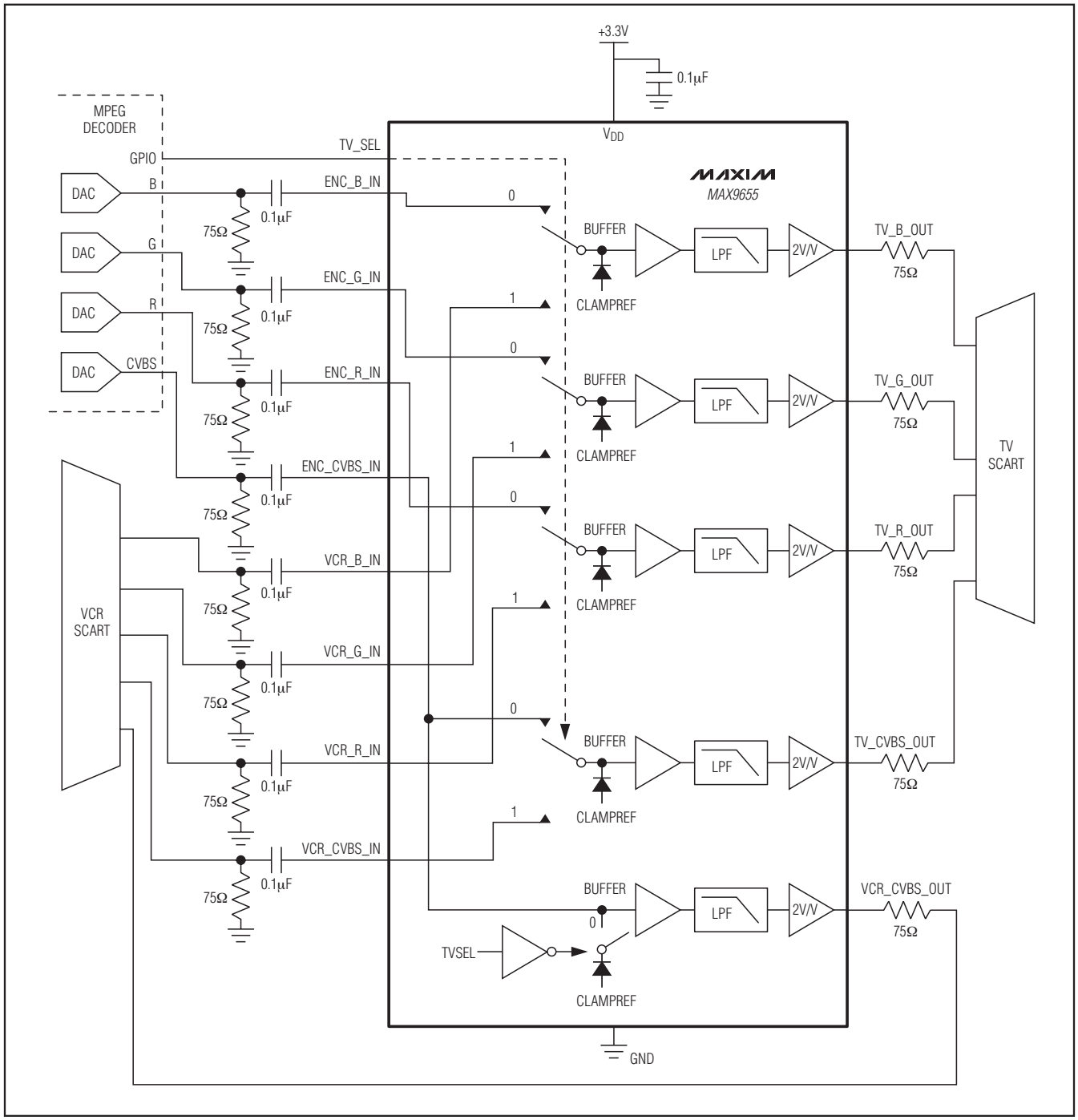


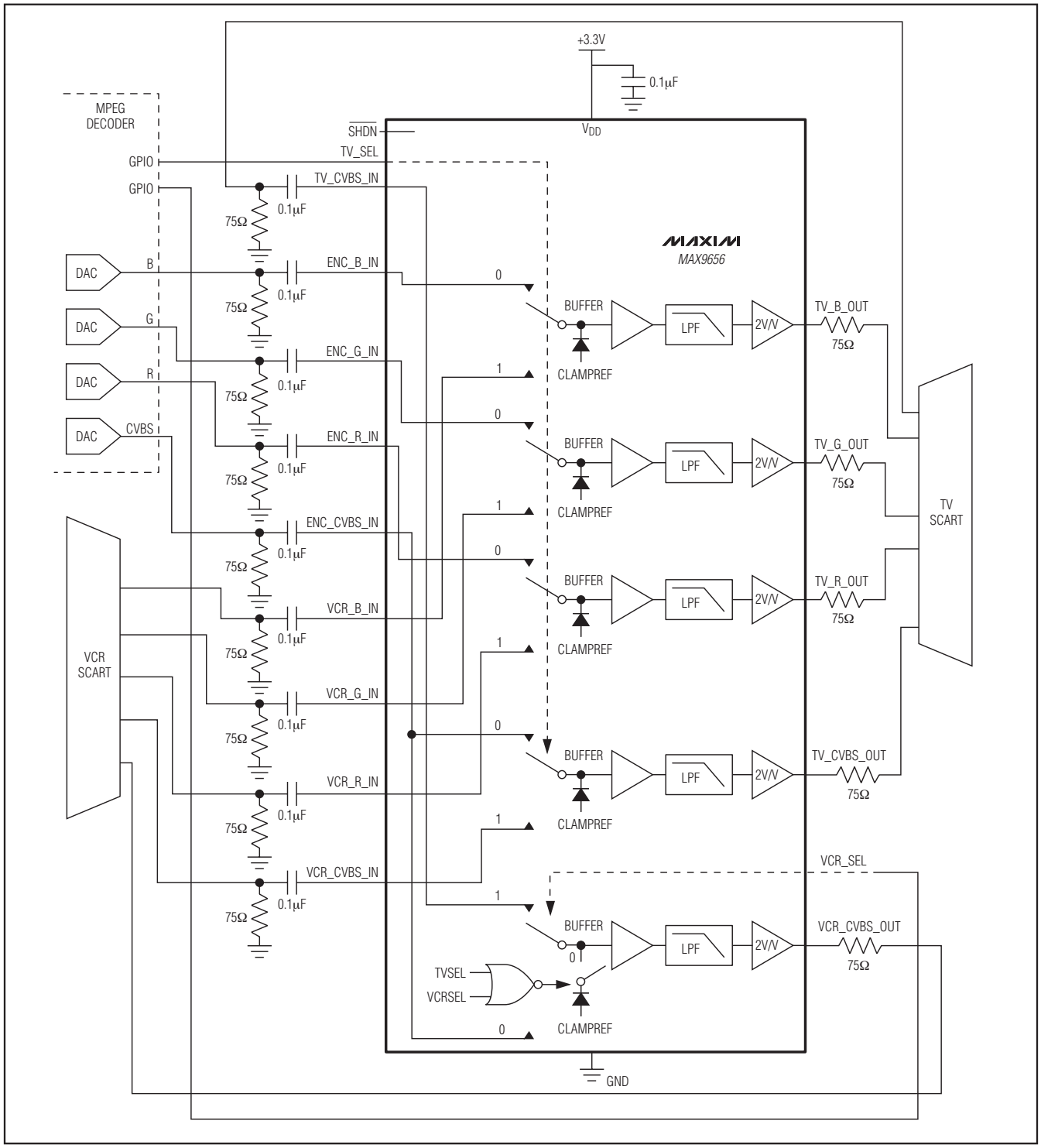
Figure 3. AC-Coupled Outputs

Typical Application Circuits

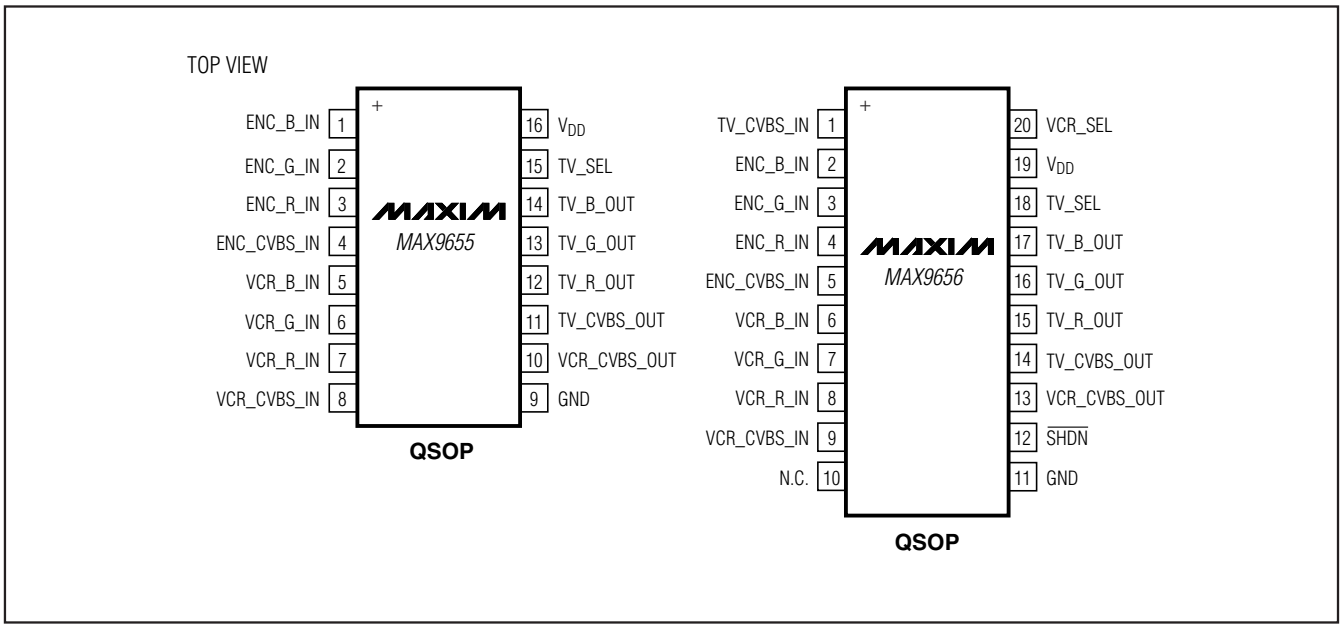


Low-Power Video Switches for Dual SCART Connectors

Typical Application Circuits (continued)



Pin Configurations

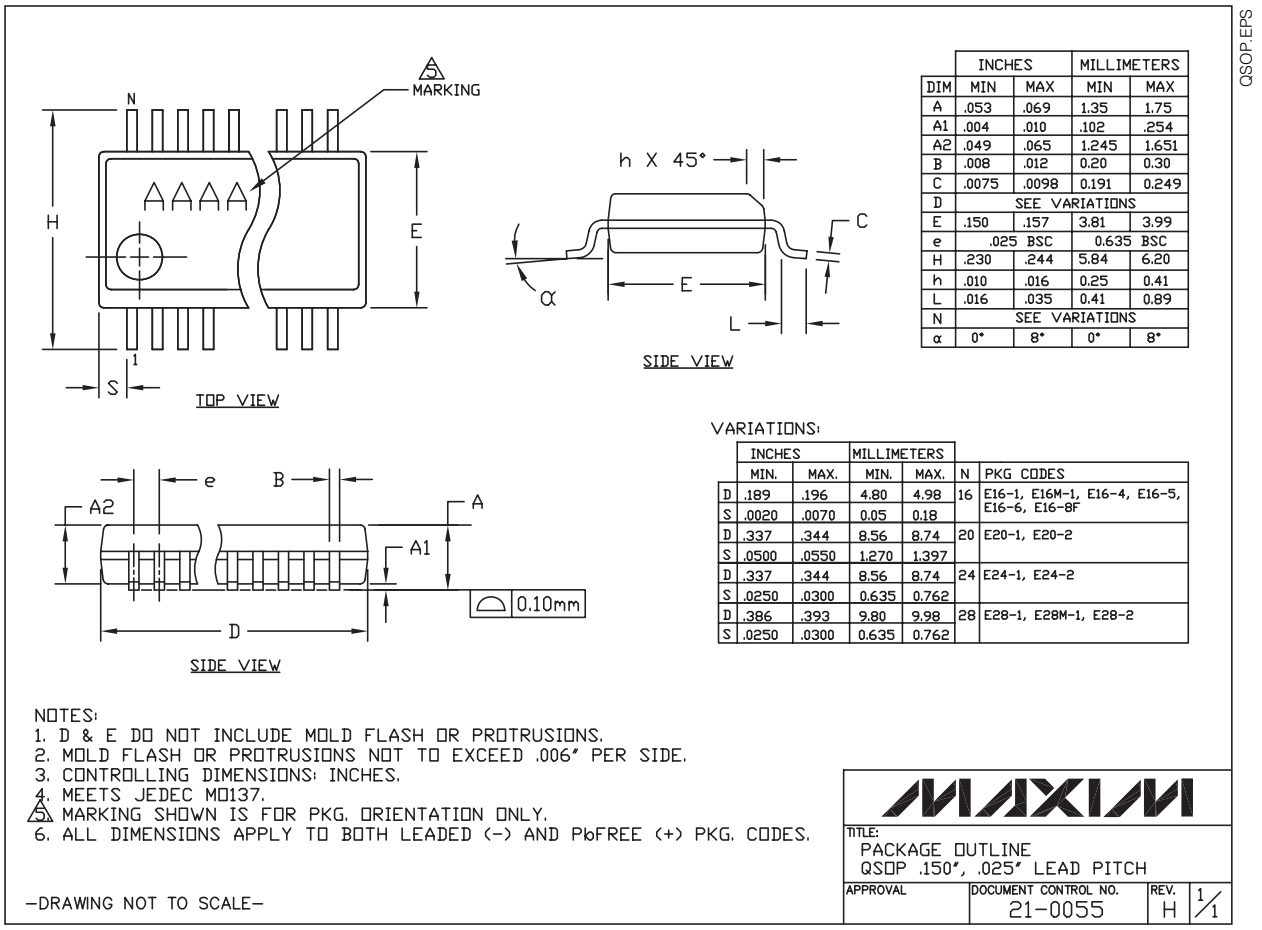


Low-Power Video Switches for Dual SCART Connectors

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	E16-4	21-0055
20 QSOP	E20-1	21-0055



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-6, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE:
PACKAGE OUTLINE
QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	H	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/08	Initial release	—
1	10/08	Removed future product reference from MAX9656, updated Shutdown Supply Current parameter, updated Table 6	1, 2, 12
2	11/08	Updated Shutdown Supply Current maximum value in EC table	2

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