Click here for production status of specific part numbers.

MAX9736

Mono/Stereo High-Power Class D Amplifier

General Description

The MAX9736A/B/D Class D amplifiers provide high-performance, thermally efficient amplifier solutions. The MAX9736A delivers 2 x 15W into 8Ω loads, or 1 x 30W into a 4Ω load. The MAX9736B/D deliver 2 x 6W into 8Ω loads or 1 x 12W into a 4Ω load.

These devices operate from 8V to 28V and provide a high PSRR, eliminating the need for a regulated power supply. The MAX9736 offers up to 88% efficiency at 12V supply.

Pin-selectable modulation schemes select between filterless modulation and classic PWM modulation. Filterless modulation allows the MAX9736 to pass CE EMI limits with 1m cables using only a low-cost ferrite bead and capacitor on each output. Classic PWM modulation is optimized for best audio performance when using a full LC filter.

A pin-selectable stereo/mono mode allows stereo operation into 8Ω loads or mono operation into 4Ω loads. In mono mode, the right input op amp becomes available as a spare device, allowing flexibility in system design.

Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown or mute.

Input op amps allow the user to create summing amplifiers, lowpass or highpass filters, and select an optimal gain.

The MAX9736A/B/D are available in 32-pin TQFN packages and specified over the -40°C to +85°C temperature range.

Features

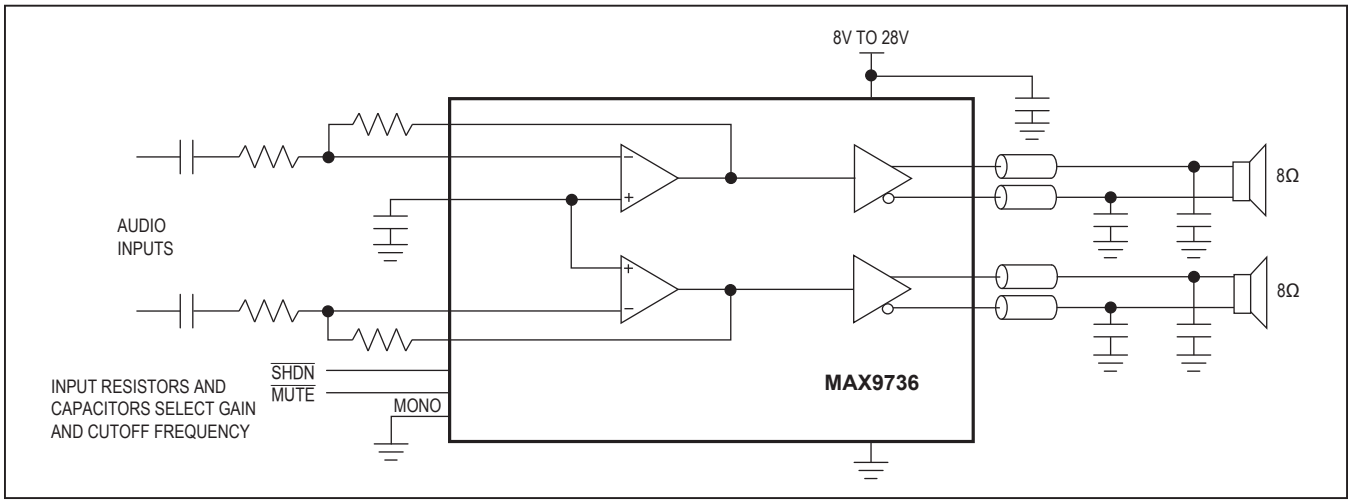
- Independently Controlled Dual Paths
- Wide 8V to 28V Supply Voltage Range
- Spread-Spectrum Modulation Enables Low EMI Solution
- Passes CE EMI Limits with Low-Cost Ferrite Bead/Capacitor Filter
- Low BOM Cost
- High 67dB PSRR at 1kHz Reduces Supply Cost
- 88% Efficiency Eliminates Heatsink
- Thermal and Output Current Protection
- < 1µA Shutdown Mode
- Mute Function
- Space-Saving, 32-Pin TQFN Packages, 7mm x 7mm x 0.8mm (MAX9736A/B), 5mm x 5mm x 0.8mm (MAX9736D)

Applications

- LCD/PDP/CRT Monitors
- LCD/PDP/CRT TVs
- MP3 Docking Stations
- Notebook PCs
- PC Speakers
- All-in-One PCs

Ordering Information *appears at end of data sheet.*

Simplified Diagram



19-3108; Rev 4; 11/19

Absolute Maximum Ratings

PVDD to PGND.....-0.3V to +30V
AGND to PGND.....-0.3V to +0.3V
INL, INR, FBL, FBR, COM to AGND.....-0.3V to (V_{REG} + 0.3V)
MUTE, SHDN, MONO, MOD, REGEN to AGND.....-0.3V to +6V
REG to AGND.....-0.3V to (VS + 0.3V)
VS to AGND (Note 1).....-0.3V to +6V
OUTL+, OUTL-, OUTR+,
OUTR-, to PGND.....-0.3V to (PVDD + 0.3V)
C1N to PGND.....-0.3V to (PVDD + 0.3V)
C1P to PGND.....(PVDD - 0.3V) to (V_{BOOT} + 0.3V)
BOOT to PGND.....(V_{C1P} - 0.3V) to PVDD + 12V
OUTL+, OUTL-, OUTR+, OUTR-,
Short Circuit to PGND or PVDD.....Continuous
Thermal Limits (Notes 2, 3)

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN 5mm x 5mm Multiple Layer PCB
(derate 34.5mW/°C above +70°C).....2.76W
θ_{JA}.....29°C/W
θ_{JC}.....2°C/W
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN 7mm x 7mm Multiple Layer PCB
(derate 37mW/°C above +70°C).....2.96W
θ_{JA}.....27°C/W
θ_{JC}.....1°C/W
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C

Note 1: VS cannot exceed PVDD + 0.3V. See the *Power-Supply Sequencing* section.
Note 2: Thermal performance of this device is highly dependant on PCB layout. See the *Applications Information* section for more details.
Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN-EP (7mm x 7mm)

Package Code	T3277-3
Outline Number	**21-0144**

32 TQFN-EP (5mm x 5mm)

Package Code	T3255-4
Outline Number	**21-0140**

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PVDD} = 20V, V_{VS} = 5V, V_{AGND} = V_{PGND} = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN_}$ = 20kΩ and $R_{FB_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
AMPLIFIER DC CHARACTERISTICS								
Speaker Supply Voltage Range	PVDD	Inferred from PSRR test			8		28	V
Preamplifier Supply Voltage Range	VS	(Notes 1 and 7)			4.5		5.5	V
Undervoltage Lockout	UVLO					7		V
Quiescent Supply Current	I_{PVDD}	R_L = ∞, V_{REGEN} = 5V, V_{VS} = open	T_A = +25°C			30	45	mA
			T_A = T_{MIN} to T_{MAX}				50	
	I_{VS}	R_L = ∞, V_{REGEN} = 0V, V_{VS} = 5V	T_A = +25°C			14	20	mA
			T_A = T_{MIN} to T_{MAX}				22	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V	I_{PVDD}			1	10	µA
			I_{VS}				10	
REG Voltage	V_{REG}					4.2		V
Preregulator Voltage	VS	Internal regulated 5V, V_{REGEN} = 5V				4.8		V
COM Voltage	V_{COM}				1.9	2.05	2.2	V
INPUT AMPLIFIER CHARACTERISTICS								
Capacitive Drive	C_L					30		pF
Output Swing (Note 6)		Sinking ±1mA				±2		V
Open-Loop Gain	A_{VO}	$V_{FB_}$ = V_{COM} ±500mV, $R_{FB_}$ = 20kΩ to IN_				88		dB
Input Offset Voltage	V_{OS}					±1		mV
Input Amplifier Slew Rate						2.5		V/µs
Input Amplifier Unity-Gain Bandwidth						3.5		MHz
AMPLIFIER CHARACTERISTICS								
Output Amplifier Gain (Note 8)	A_V	MAX9736A, MAX9736D			16.5	17	17.5	dB
		MAX9736B			13.1	13.6	14.1	
Output Current Limit					3.3	4.6		A
Output Offset	V_{OS}	OUT_+ to OUT_-, T_A = +25°C				±2	±10	mV
Power-Supply Rejection Ratio	PSRR	PVDD = 8V to 28V, T_A = +25°C			65	80		dB
		f = 1kHz, 100mV_{P-P} ripple				67		
MAX9736A Output Power (THD+N = 1%)	$P_{OUT_1\%}$	V_{PVDD} = 12V	Stereo	R_L = 8Ω		8		W
				R_L = 4Ω		13		
			Mono	R_L = 4Ω		15.5		
		V_{PVDD} = 18V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		
		V_{PVDD} = 24V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		

Electrical Characteristics (continued)

(V_{PVDD} = 20V, V_{VS} = 5V, V_{AGND} = V_{PGND} = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN_}$ = 20kΩ and $R_{FB_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
MAX9736B Output Power (THD+N = 1%)	$P_{OUT_1\%}$	V_{PVDD} = 12V	Stereo	R_L = 8Ω		6		W
				R_L = 4Ω		11		
			Mono	R_L = 4Ω		12		
		V_{PVDD} = 18V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
		V_{PVDD} = 24V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
MAX9736A Output Power (THD+N = 10%)	$P_{OUT_10\%}$	V_{PVDD} = 12V	Stereo	R_L = 8Ω		10		W
				R_L = 4Ω		16		
			Mono	R_L = 4Ω		19.5		
		V_{PVDD} = 18V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
		V_{PVDD} = 24V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
MAX9736B Output Power (THD+N = 10%)	$P_{OUT_10\%}$	V_{PVDD} = 12V	Stereo	R_L = 8Ω		7.5		W
				R_L = 4Ω		14		
			Mono	R_L = 4Ω		15		
		V_{PVDD} = 18V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		
		V_{PVDD} = 24V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		
MAX9736D Output Power (Thermally Limited)		V_{PVDD} = 12V	Stereo	R_L = 8Ω		8.5		W
			Mono	R_L = 4Ω		17		
		V_{PVDD} = 18V	Stereo	R_L = 8Ω		5.5		
			Mono	R_L = 4Ω		11		
		V_{PVDD} = 24V	Stereo	R_L = 8Ω		3.5		
			Mono	R_L = 4Ω		7		
Total Harmonic Distortion Plus Noise	THD+N	MAX9736A, P_{OUT} = 4W, f = 1kHz, PWM modulation mode, R_L = 8Ω				0.04		%
		MAX9736B/D, P_{OUT} = 2W, f = 1kHz, PWM modulation mode, R_L = 8Ω				0.04		
Signal-to-Noise Ratio	SNR	A-weighted	MAX9736A/D, P_{OUT} = 8W, R_L = 8Ω			96.5		dB
			MAX9736B, P_{OUT} = 6W, R_L = 8Ω			97		
Noise	V_N	A-weighted (Note 9)	MAX9736A/D			120		$µV_{RMS}$
			MAX9736B			100		

Electrical Characteristics (continued)

(V_{PVDD} = 20V, V_{VS} = 5V, V_{AGND} = V_{PGND} = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN_}$ = 20kΩ and $R_{FB_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk		L to R, R to L, P_{OUT} = 1W, f = 1kHz, R_L = 8Ω			100		dB
Efficiency	η	P_{OUT} = 8W, MAX9736A, PVDD = 12V, R_L = 8Ω			88		%
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 9 and 10)	Into mute		36		dBV
			Out of mute		36		
Switching Frequency				270	300	330	kHz
Spread-Spectrum Bandwidth					±4		kHz
Thermal Shutdown Level					160		°C
Thermal Shutdown Hysteresis					30		°C
Turn-On Time	t_{ON}				110		ms
DIGITAL INTERFACE							
Input Voltage High	V_{INH}			2			V
Input Voltage Low	V_{INL}					0.8	V
Input Voltage Hysteresis					50		mV
Input Leakage Current						±10	µA

Note 4: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 5: Stereo mode (MONO = GND) specified with 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Mono mode (MONO = 5V) specified with a 4Ω resistive load in series with a 33µH inductive load connected across BTL outputs.

Note 6: Output swing is specified with respect to V_{COM}.

Note 7: For typical applications, an external 5V supply is not required. Therefore, set REGEN = 5V. If thermal performance is a concern, set REGEN = 0V and provide an external regulated 5V supply.

Note 8: Output amplifier gain is defined as:

$$20 \times \log\left(\frac{|(V_{OUT_+}) - (V_{OUT_-})|}{|V_{FB_}|}\right)$$

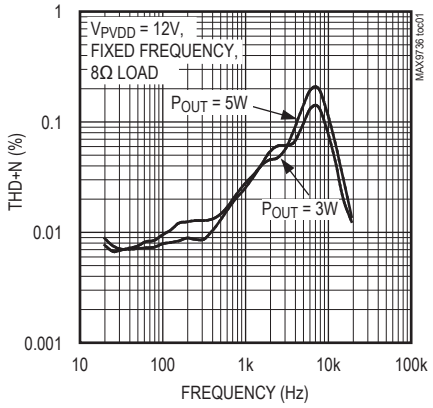
Note 9: Amplifier inputs AC-coupled to GND.

Note 10: Specified at room temperature with an 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Mode transitions controlled by $\overline{SHDN}$ control pin.

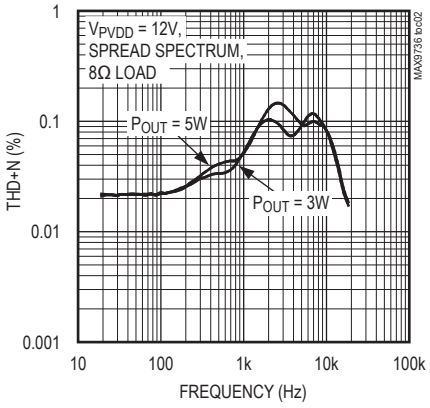
Typical Operating Characteristics

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

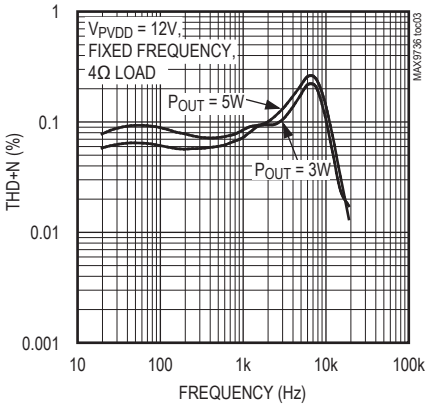
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



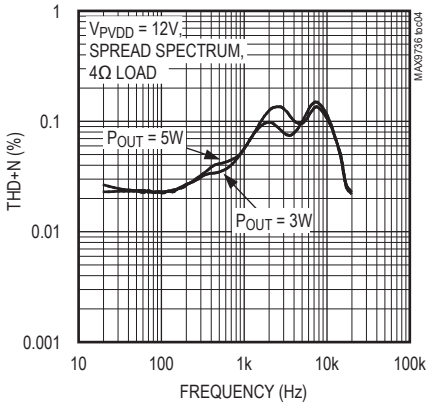
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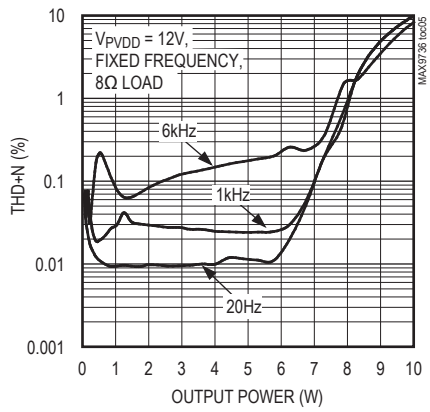
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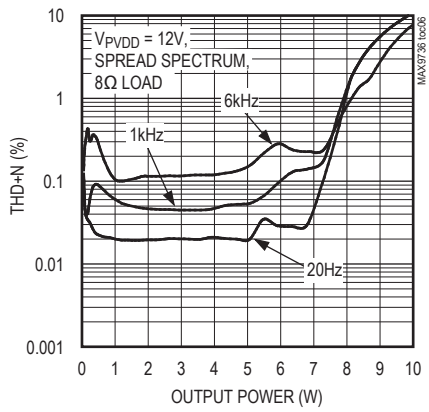
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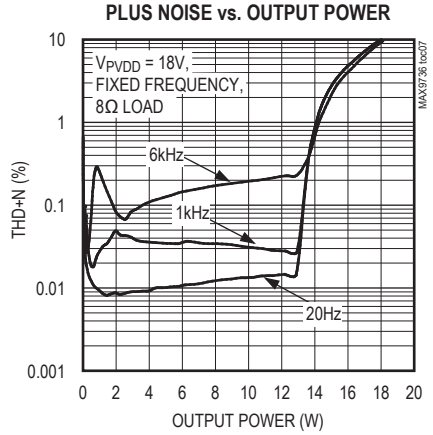
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



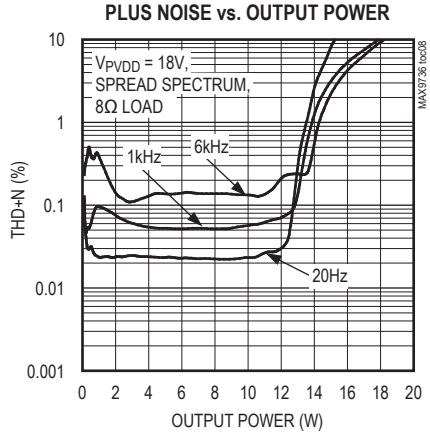
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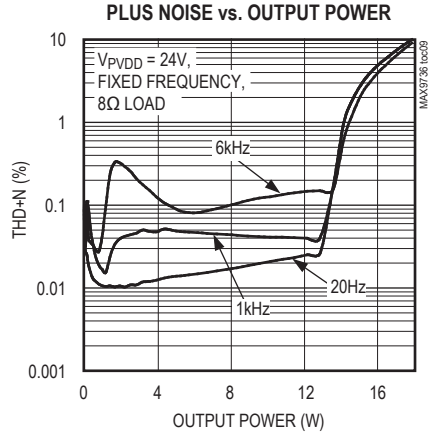
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TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



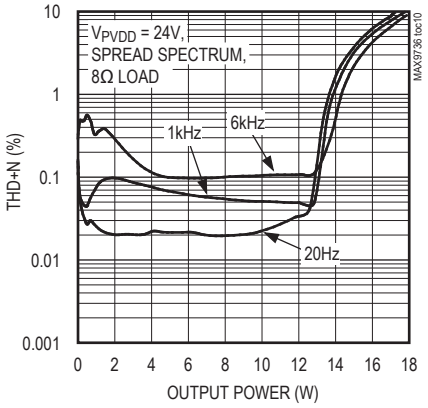
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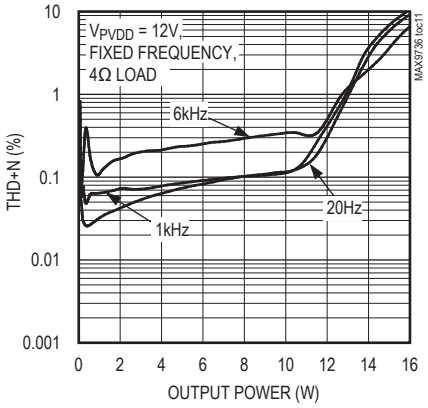
Typical Operating Characteristics (continued)

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

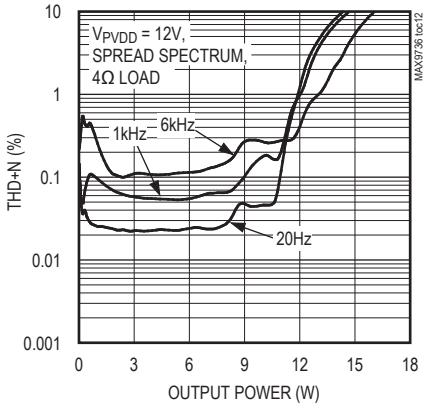
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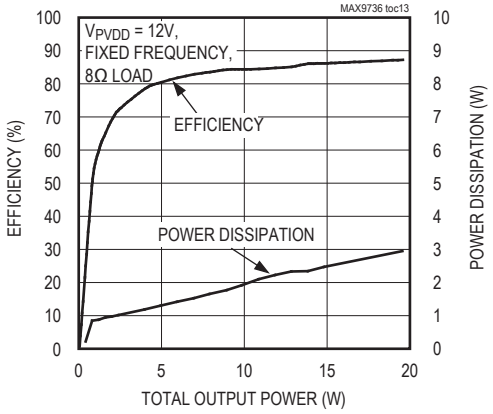
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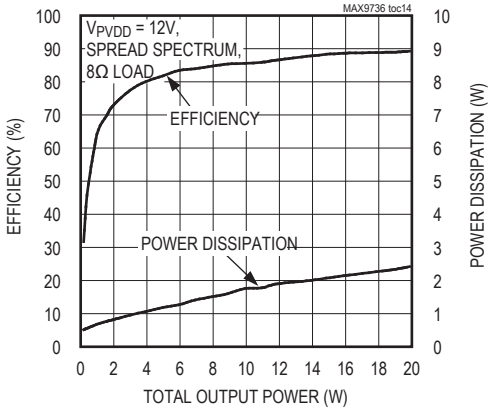
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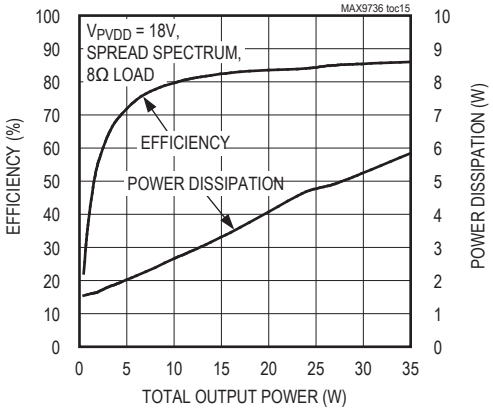
EFFICIENCY vs. TOTAL OUTPUT POWER



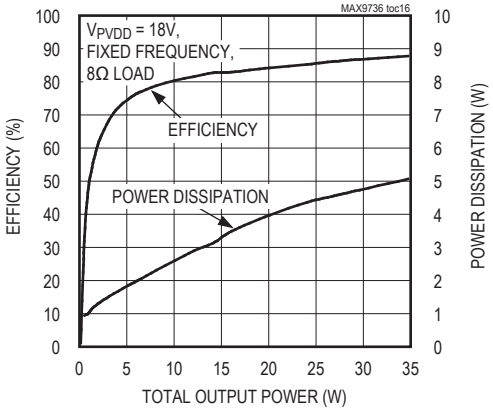
EFFICIENCY vs. TOTAL OUTPUT POWER



EFFICIENCY vs. TOTAL OUTPUT POWER



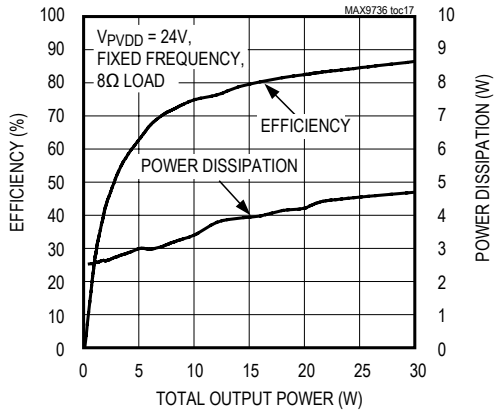
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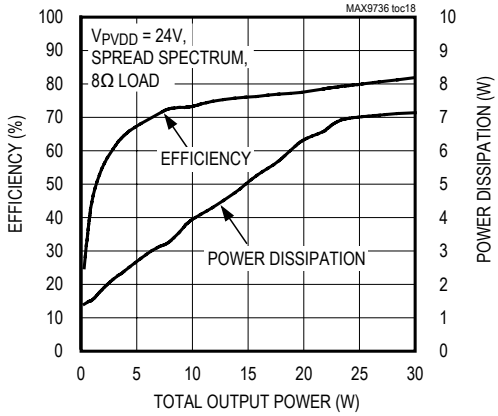
Typical Operating Characteristics (continued)

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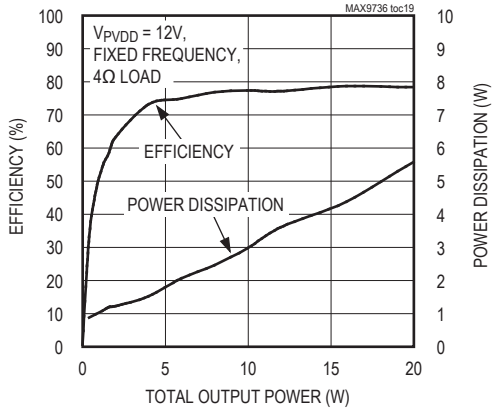
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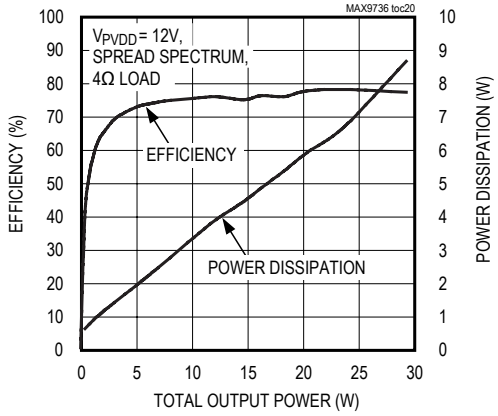
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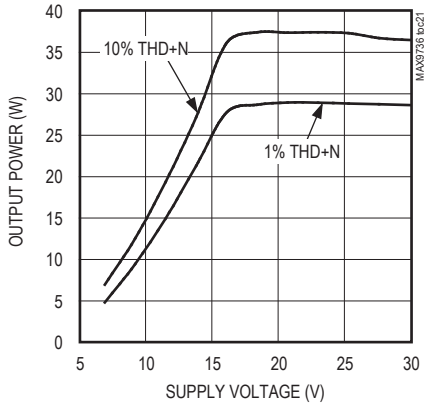
EFFICIENCY vs. TOTAL OUTPUT POWER



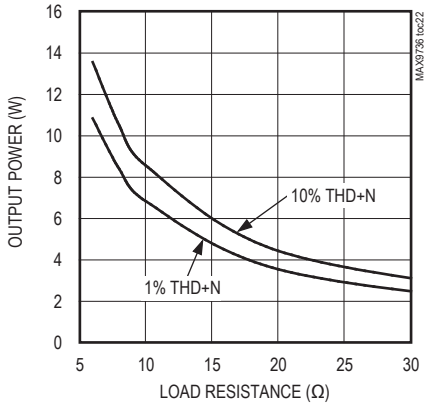
EFFICIENCY vs. TOTAL OUTPUT POWER



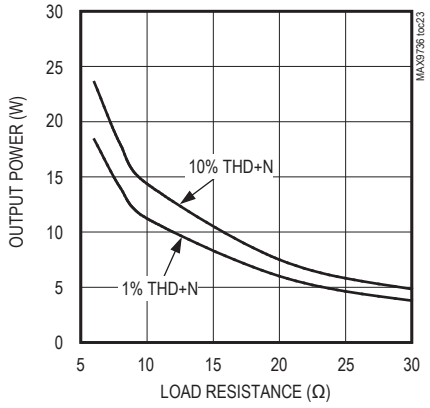
TOTAL OUTPUT POWER vs. V_{DD}
LOAD = 8Ω, f = 1kHz



TOTAL OUTPUT POWER vs. LOAD RESISTANCE
V_{DD} = 12V, f = 1kHz, SPREAD SPECTRUM



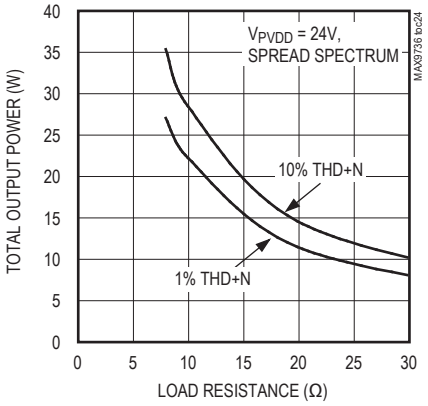
TOTAL OUTPUT POWER vs. LOAD RESISTANCE
V_{DD} = 18V, f = 1kHz, SPREAD SPECTRUM



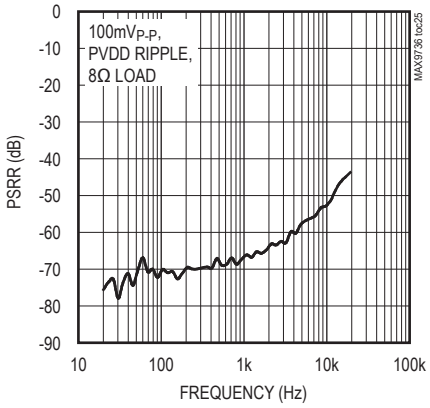
Typical Operating Characteristics (continued)

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

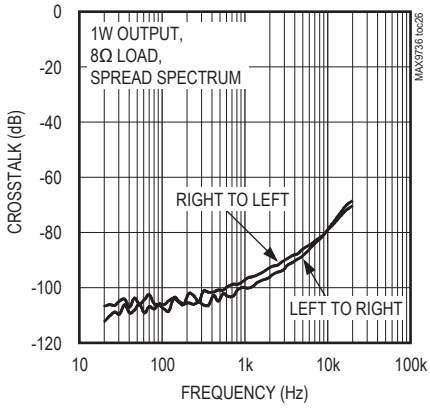
TOTAL OUTPUT POWER vs. LOAD RESISTANCE



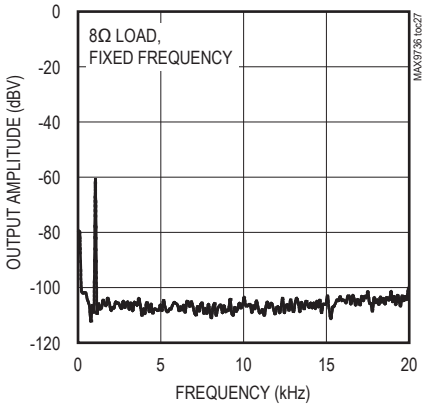
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



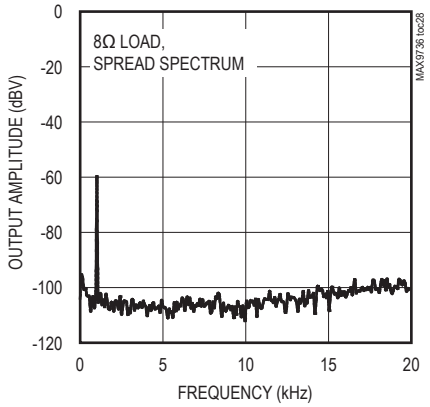
CROSSTALK vs. FREQUENCY



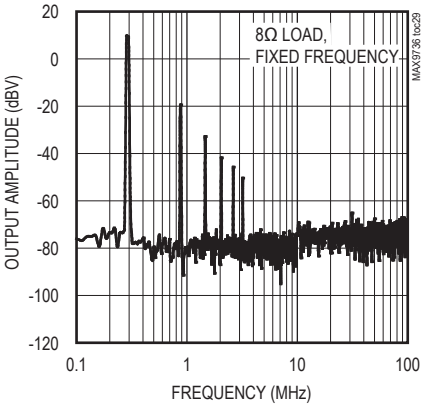
INBAND OUTPUT SPECTRUM



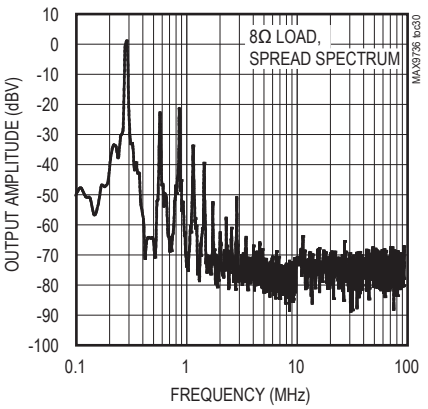
INBAND OUTPUT SPECTRUM



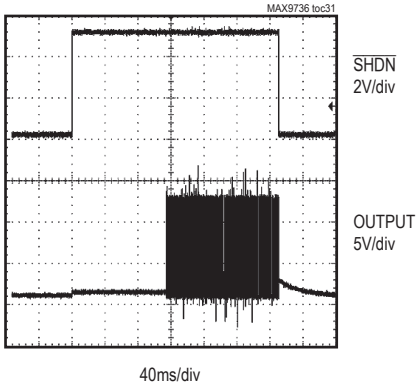
WIDEBAND OUTPUT SPECTRUM



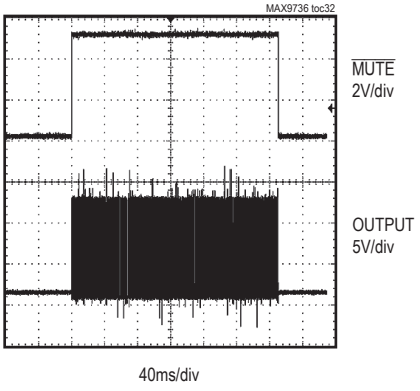
WIDEBAND OUTPUT SPECTRUM



$\overline{SHDN}$ ON-/OFF-RESPONSE



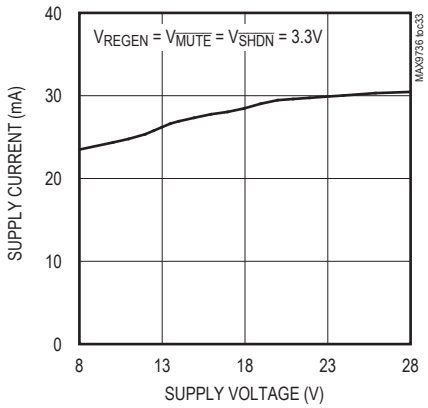
$\overline{MUTE}$ ON-/OFF-RESPONSE



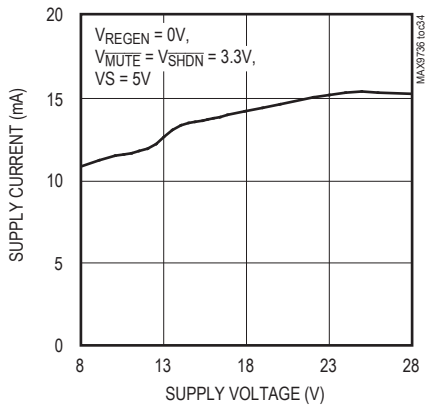
Typical Operating Characteristics (continued)

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

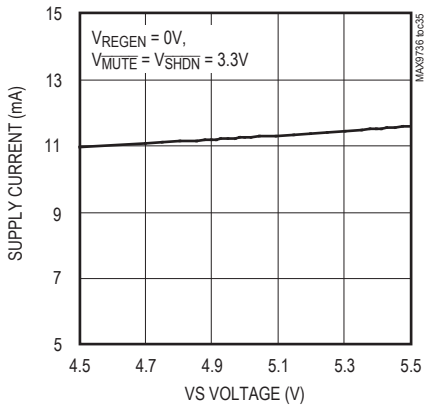
SUPPLY CURRENT vs. PVDD SUPPLY VOLTAGE



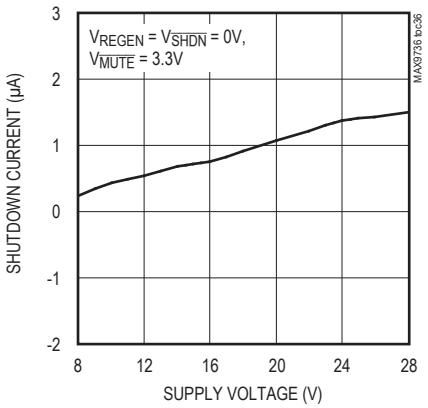
SUPPLY CURRENT vs. PVDD SUPPLY VOLTAGE



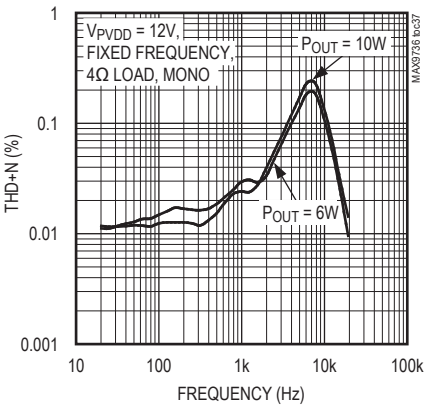
SUPPLY CURRENT vs. VS SUPPLY VOLTAGE



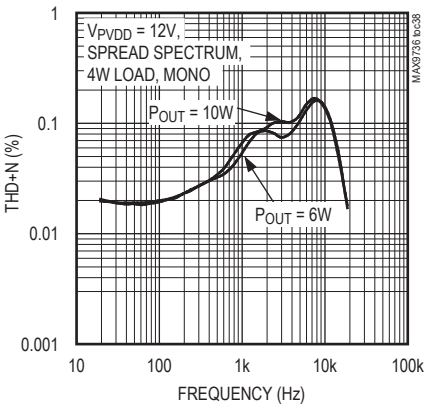
SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



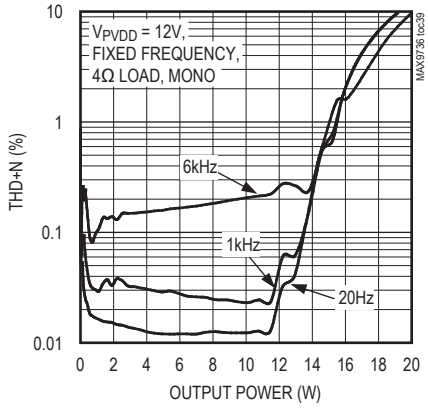
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



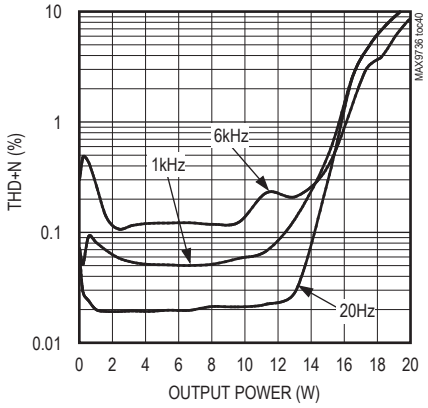
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



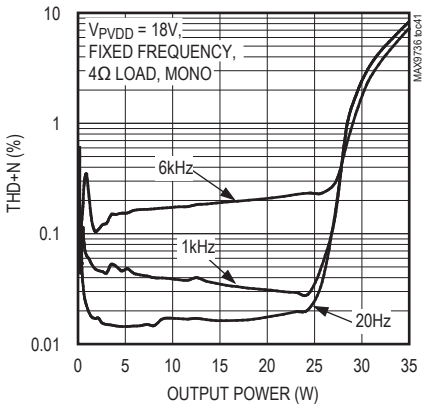
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (V_{DD} = 12V, SPREAD SPECTRUM, 4Ω LOAD, MONO)



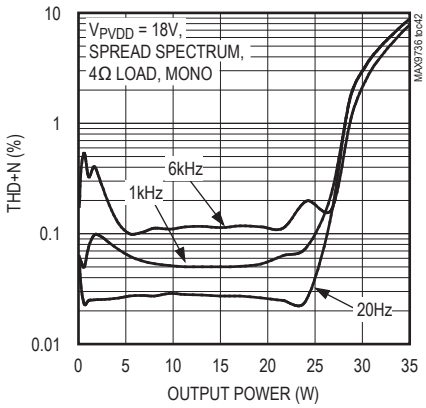
Typical Operating Characteristics (continued)

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

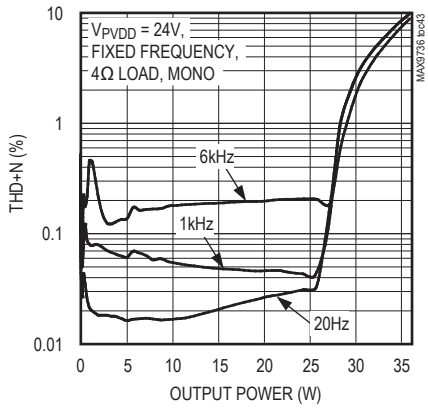
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



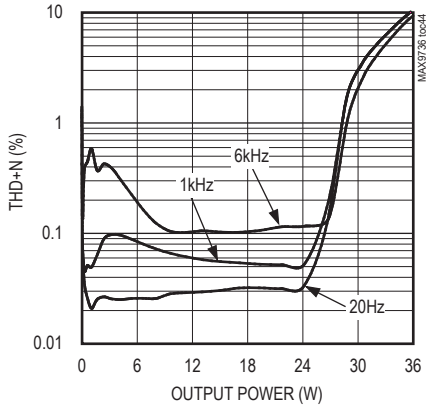
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



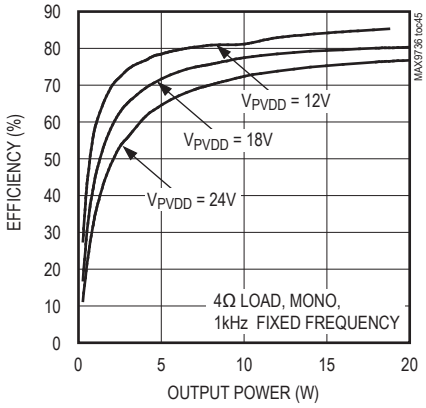
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



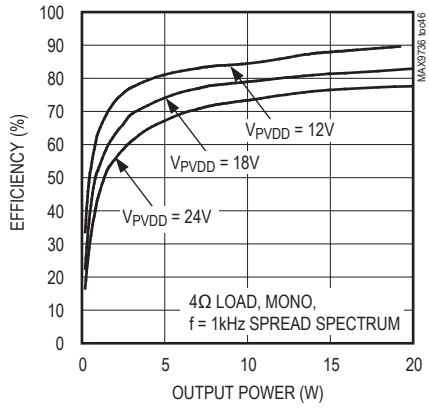
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (V_{DD} = 24V, SPREAD SPECTRUM, 4Ω LOAD, MONO)



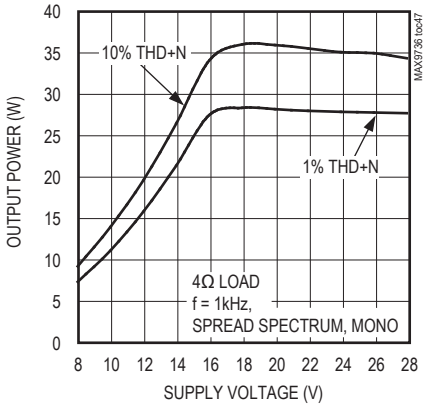
EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



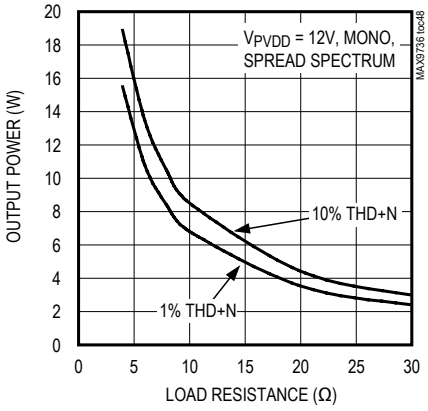
OUTPUT POWER vs. V_{DD} (LOAD = 4Ω, f = 1kHz, SPREAD SPECTRUM, MONO)



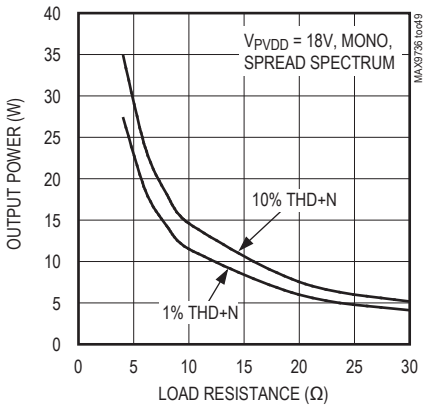
Typical Operating Characteristics (continued)

(MAX9736A, V_{PVDD} = 12V, MOD = high, spread-spectrum modulation mode, V_{GND} = V_{PGND} = 0V, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, unless otherwise noted.)

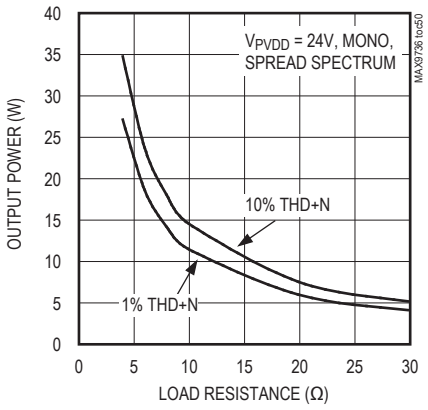
OUTPUT POWER vs. LOAD RESISTANCE



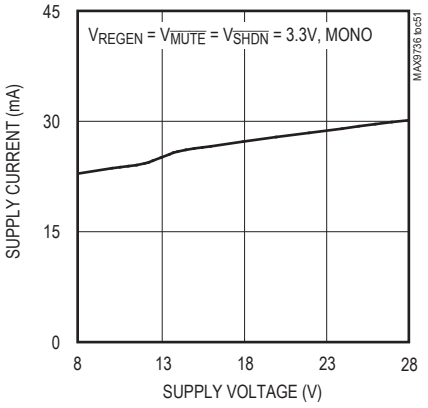
OUTPUT POWER vs. LOAD RESISTANCE



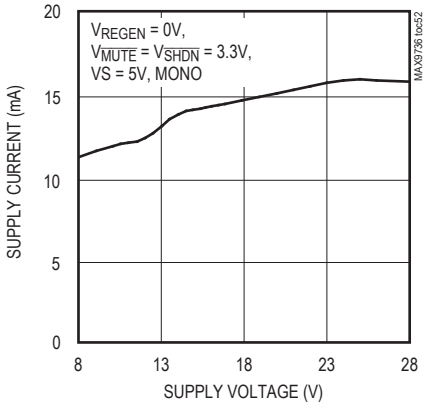
OUTPUT POWER vs. LOAD RESISTANCE



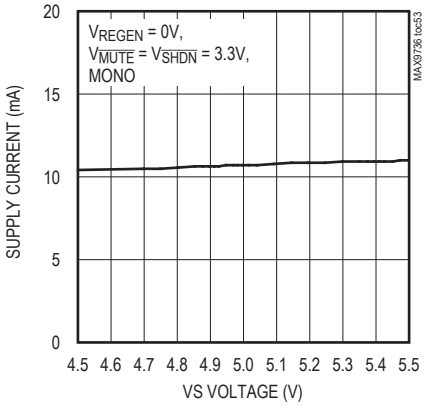
SUPPLY CURRENT vs. PVDD SUPPLY VOLTAGE



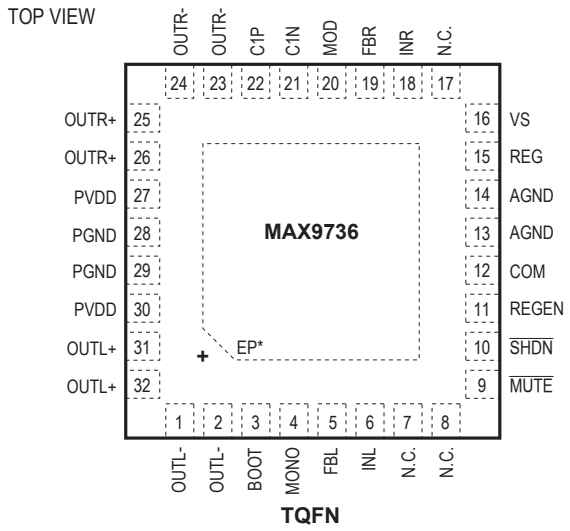
SUPPLY CURRENT vs. PVDD SUPPLY VOLTAGE



SUPPLY CURRENT vs. VS VOLTAGE



Pin Configuration



EP* = EXPOSED PAD, CONNECT TO PGND.

Pin Description

PIN	NAME	FUNCTION
1, 2	OUTL-	Left-Channel Negative Speaker Output
3	BOOT	Charge-Pump Output. Connect a 1µF charge-pump holding capacitor from BOOT to PVDD.
4	MONO	Mono Select. Set MONO high for mono mode, low for stereo mode.
5	FBL	Left-Channel Feedback. Connect feedback resistor between FBL and INL to set amplifier gain.
6	INL	Stereo Left-Channel Inverting Input. In mono mode, INL is the inverting audio input for the mono amplifier.
7, 8, 17	N.C.	No Connection. Not internally connected. OK to connect to PGND.
9	$\overline{\text{MUTE}}$	Mute Input. Drive $\overline{\text{MUTE}}$ low to place the device in mute mode.
10	$\overline{\text{SHDN}}$	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown mode.
11	REGEN	Internal Regulator Enable Input. Connect REGEN to $\overline{\text{SHDN}}$ to enable the internal regulator. Drive REGEN low to disable the internal regulator, and supply the device with an external 5V supply on VS. See the *Power-Supply Sequencing* section.
12	COM	Internal 2V Bias. Bypass COM to AGND with a 1µF capacitor.
13, 14	AGND	Analog Ground
15	REG	Internal Regulator Output. Bypass REG to AGND with a 1µF capacitor.
16	VS	5V Regulator Supply. Bypass VS to AGND with a 1µF capacitor. If REGEN is low, the internal regulator is disabled, and an external 5V supply must be connected to VS. See the *Power-Supply Sequencing* section.

Pin Description (continued)

PIN	NAME	FUNCTION
18	INR	Stereo Right-Channel Inverting Audio Input. In mono mode, INR is the inverting audio input for the uncommitted preamplifier (see the *Mono Configuration* section for more details).
19	FBR	Right-Channel Feedback. Connect feedback resistor between FBR and INR to set amplifier gain.
20	MOD	Output Modulation Select. Sets the output modulation scheme: V_{MOD} = Low, classic PWM/fixed-frequency mode V_{MOD} = High, filterless modulation/spread-spectrum mode
21	C1N	Charge-Pump Flying-Capacitor Negative Terminal
22	C1P	Charge-Pump Flying-Capacitor Positive Terminal
23, 24	OUTR-	Right-Channel Negative Speaker Output
25, 26	OUTR+	Right-Channel Positive Speaker Output
27, 30	PVDD	Power Supply. Bypass each PVDD pin to ground with 0.1µF capacitors. Also, use a single 220µF capacitor between PVDD and PGND.
28, 29	PGND	Power Ground
31, 32	OUTL+	Left-Channel Positive Speaker Output
—	EP	Exposed Pad. Must be externally connected to PGND.

Detailed Description

The MAX9736A/B/D filterless, stereo Class D audio power amplifiers offer Class AB performance and Class D efficiency with minimal board space. The MAX9736A outputs 2x15W in stereo mode and 30W in mono mode. The MAX9736B/D output 2x6W in stereo mode and 12W in mono mode. These devices operate from an 8V to 28V supply range.

The MAX9736 features a filterless, spread-spectrum switching mode (MOD = high) or a classic PWM fixed-frequency switching mode (MOD = low).

The MAX9736 features externally set gain and a low-power shutdown mode that reduces supply current to less than 1µA. Comprehensive click-and-pop circuitry minimizes noise into and out of shutdown or mute.

Operating Modes

Filterless Modulation/PWM Modulation

The MAX9736 features two output modulation schemes, filterless modulation (MOD = high) or classic PWM (MOD = low). Maxim's unique, filterless modulation scheme eliminates the LC filter required by traditional Class D amplifiers, reducing component count, conserving board space, and reducing system cost. Configure for classic PWM output when using a full LC filter.

Click-and-pop protection does not apply when the output is switching between modulation schemes. To maintain click-and-pop protection when switching between output schemes the device must enter shutdown mode and be configured to the new output scheme before the startup sequence is finished.

Spread-Spectrum Mode

The MAX9736 features a unique spread-spectrum mode that flattens the wideband spectral components, improving EMI radiated by the speaker and cables. The switching frequency of the Class D amplifier varies randomly by ±6kHz around the 300kHz center frequency. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this white noise does not corrupt the noise floor in the audio bandwidth. The spread-spectrum mode is enabled only with filterless modulation.

Efficiency

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as switches and consume negligible power. Power loss associated with the Class D output stage is due to the I^2R loss of the MOSFET on-resistance, various switching losses, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78% at peak output power. Under typical music reproduction levels, the efficiency falls below 30%, whereas the MAX9736 exhibits > 80% efficiency under the same conditions (Figure 1).

Shutdown

The MAX9736 features a shutdown mode that reduces power consumption and extends battery life in portable applications. The shutdown mode reduces supply current to 1µA (typ). Drive $\overline{SHDN}$ high for normal operation. Drive $\overline{SHDN}$ low to place the device in low-power shutdown mode. In shutdown mode, the outputs are high impedance; and the common-mode voltage at the output decays to zero. In shutdown mode, connect REGEN low to minimize current consumption.

Mute Function

The MAX9736 features a clickless-and-popless mute mode. When the device is muted, the signal is attenuated at the speaker and the outputs stop switching. To mute the MAX9736, drive $\overline{MUTE}$ low. Hold $\overline{MUTE}$ low during system power-up and power-down to ensure that clicks and pops caused by circuits before the MAX9736 are suppressed.

Click-and-Pop Suppression

The MAX9736 features comprehensive click-and-pop suppression that minimizes audible transients on startup and shutdown. While in shutdown, the H-bridge is in a high-impedance state.

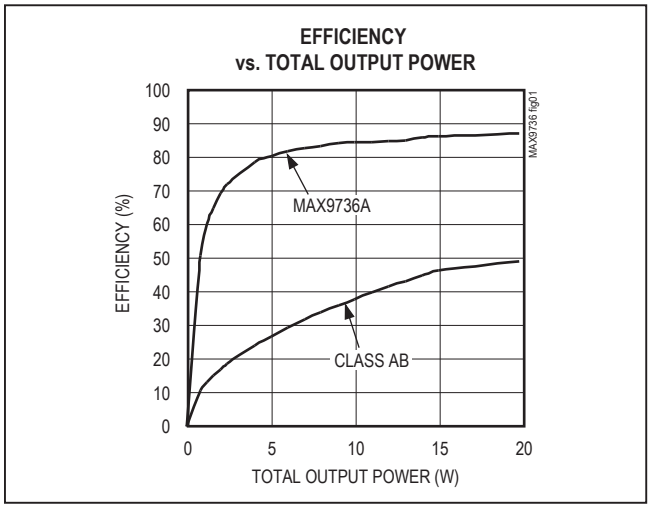


Figure 1. MAX9736A Efficiency vs. Class AB Efficiency

Mono Configuration

The MAX9736 features a mono mode that allows the right and left channels to operate in parallel, achieving up to 30W (MAX9736A) of output power. Apply a logic-high to MONO to enable mono mode. In mono mode, an audio signal applied to the left channel (INL) is routed to the H-bridges of both channels. Also in mono mode, the right-channel preamplifier becomes an uncommitted operational amplifier, allowing for flexibility in system design. Connect OUTL+ to OUTR+ and OUTL- to OUTR- using heavy PCB traces as close as possible to the device. Driving MONO low (stereo mode) while the outputs are wired together in mono mode can trigger the short-circuit or thermal-overload protection or both.

Current Limit

When the output current reaches the current limit, 4.6A (typ), the MAX9736 disables the outputs and initiates a 450µs startup sequence. The shutdown and startup sequence is repeated until the output fault is removed. Properly designed applications do not enter current-limit mode unless the output is short circuited or connected incorrectly.

Thermal Shutdown

When the die temperature reaches the thermal shutdown threshold, +160°C (typ), the MAX9736 outputs are disabled. When the die temperature decreases by 30°C, normal operation resumes. Some causes of thermal shutdown are excessively low load impedance, poor thermal contact between the MAX9736's exposed pad and the PCB, elevated ambient temperature, or poor PCB layout and assembly.

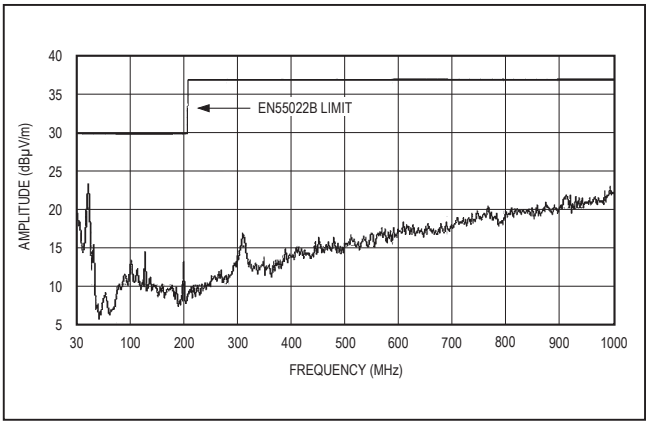


Figure 2. EMI Performance

Applications Information

Filterless Class D Operation

The MAX9736 meets EN55022B EMC radiation limits with an inexpensive ferrite bead and capacitor filter when the speaker leads are less than or equal to 1m. Select a ferrite bead with 100Ω to 600Ω impedance and rated for at least 2A. The capacitor value varies based on the ferrite bead chosen and the speaker lead length. See Figure 3 for the correct connections of these components.

When evaluating the MAX9736 with a ferrite bead filter and resistive load, include a series inductor (68µH for 8Ω load and 33µH for 4Ω load) to model the actual loudspeaker's behavior. Omitting the series inductor reduces the efficiency, the THD+N performance, and the output power of the MAX9736. When evaluating with a load speaker, no series inductor is required.

Inductor-Based Output Filters

Some applications use the MAX9736 with a full inductor-/capacitor-based (LC) output filter. Select the PWM output mode for best audio performance. See Figure 4 for the correct connections of these components.

The load impedance of the speaker determines the filter component selection (see Table 1).

Inductors L1 and L2, and capacitor C1 form the primary output filter. Capacitors C2 and C3 provide common-mode filtering to reduce radiated emissions. Capacitors C4 and C5, plus resistors R1 and R2, form a Zobel at the output. A Zobel corrects the output loading to compensate for the rising impedance of the loudspeaker. Without a Zobel the filter exhibits a peak response near the cutoff frequency.

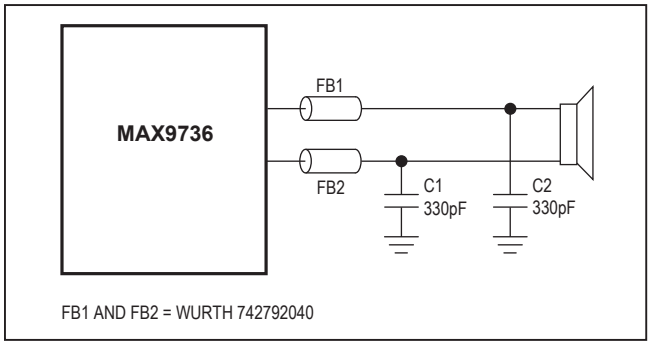


Figure 3. Ferrite Bead Filter

Component Selection

Gain-Setting Resistors

External feedback resistors set the gain of the MAX9736. The output stage provides a fixed internal gain in addition to the externally set input stage gain. For the MAX9736A/D, the fixed output-stage gain is set at 17dB (7V/V). For the MAX9736B, the fixed output-stage gain is set at 13.6dB (4.8V/V). Set overall gain by using resistors R_F and R_{IN} (Figure 5) as follows:

$$MAX9736A: A_V = -7.1\left(\frac{R_F}{R_{IN}}\right) V/V$$

$$MAX9736B: A_V = -4.8\left(\frac{R_F}{R_{IN}}\right) V/V$$

where A_V is the desired voltage gain. Choose R_F between 10kΩ and 50kΩ.

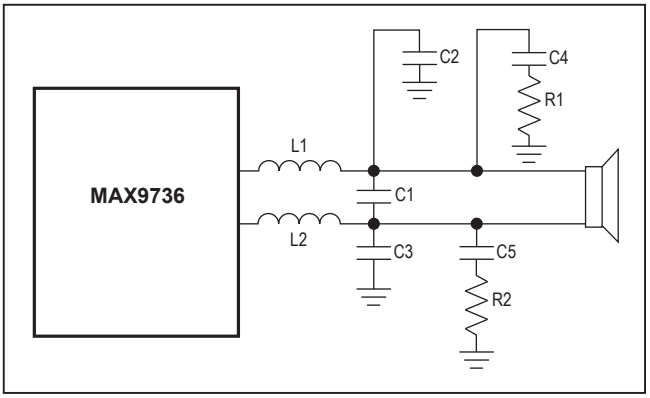


Figure 4. Output Filter for PWM Mode

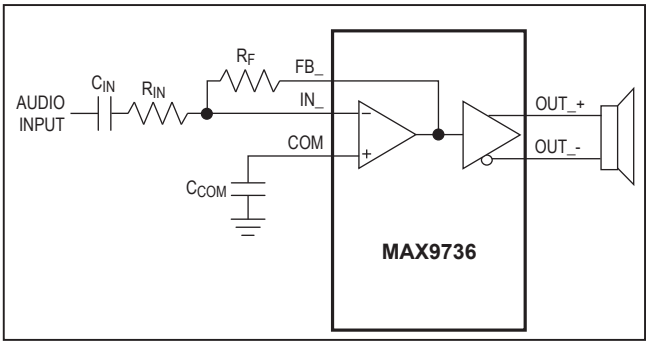


Figure 5. Setting Gain

Table 1. Suggested Values for LC Filter

R_L (Ω)	L1, L2 (µH)	C1 (µF)	C2, C3 (µF)	C4, C5 (µF)	R1, R2 (Ω)
4	10	0.47	0.10	0.22	10
8	15	0.15	0.15	0.15	15
16	33	0.10	0.10	0.10	33

The FB terminal is an op amp output and the IN terminal is the op amp inverting input, allowing the MAX9736 to be configured as a summing amplifier, a filter, or an equalizer.

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input resistor, R_{IN}, of the MAX9736 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Use capacitors whose dielectrics have low voltage coefficients. Capacitors with high-voltage coefficients cause increased distortion close to f_{-3dB}.

COM Capacitor

COM is the output of the internally generated DC bias voltage. Bypass COM with a 1µF capacitor to AGND.

Power Supplies

The MAX9736 features separate supplies for signal and power portions of the device, allowing for the optimum combination of headroom, power dissipation, and noise immunity. The speaker amplifiers are powered from PVDD and can range from 8V to 28V. The remainder of the MAX9736 is powered by VS.

Power-Supply Sequencing

During power-up and power-down, VS must not exceed PVDD. VS greater than PVDD will damage the device.

Internal Regulator

The MAX9736 features an internal 5V regulator, VS, powered from PVDD. Connect REGEN to $\overline{SHDN}$ so that the internal 5V regulator is enabled/disabled when the MAX9736 is enabled/disabled. If an external 5V supply is available, drive REGEN low and connect external 5V supply to VS to minimize the power dissipation of the MAX9736.

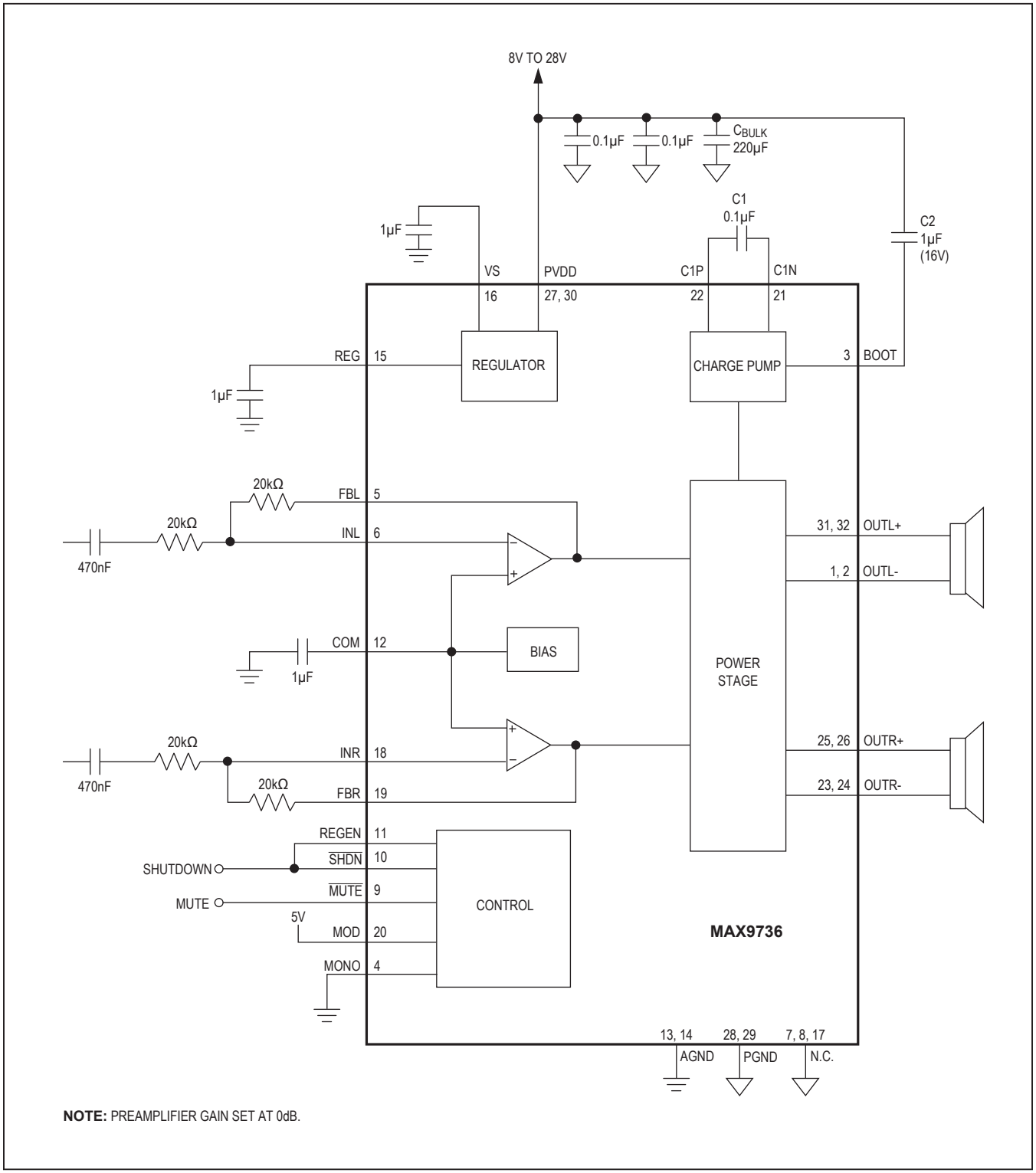
Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use wide traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents switching noise from coupling into the audio signal. Connect PGND and AGND together at a single point on the PCB. Route all traces that carry switching transients away from AGND and the traces/components in the audio signal path.

Bypass each PVDD pin with a 0.1µF capacitor to PGND. Place the bypass capacitors as close as possible to the MAX9736. Place a 220µF capacitor between PVDD and PGND. Bypass VS with a 1µF capacitor to AGND.

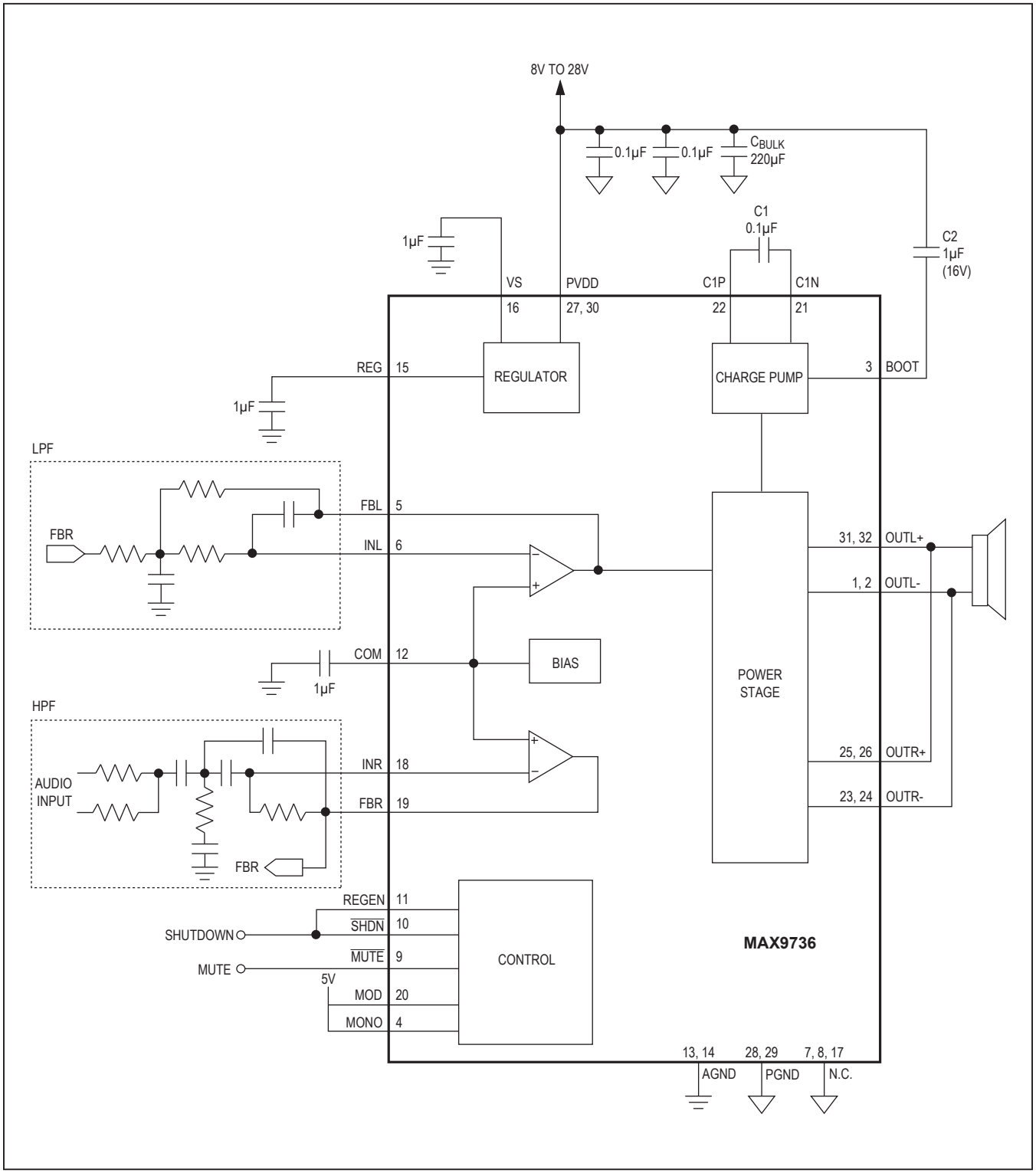
Use wide, low-resistance output traces. Current drawn from the outputs increases as load impedance decreases. High-output trace resistance decreases the power delivered to the load. The MAX9736 TQFN package features an exposed thermal paddle on its underside. This paddle lowers the package's thermal resistance by providing a heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND by using a large pad and multiple vias to the PGND plane.

Typical Application Circuit for Stereo Output Configuration



NOTE: PREAMPLIFIER GAIN SET AT 0dB.

Typical Application Circuit for Single (Mono) Output Configuration



Ordering Information

PART	STEREO/MONO OUTPUT POWER	PIN-PACKAGE
MAX9736AETJ+	2 x 15W/ 1 x 30W	32 TQFN-EP* 7mm x 7mm
MAX9736AETJ/V+	2 x 15W/ 1 x 30W	32 TQFN-EP* 7mm x 7mm
MAX9736BETJ+	2 x 6W/ 1 x 12W	32 TQFN-EP* 7mm x 7mm
MAX9736BETJ/V+	2 x 6W/ 1 x 12W	32 TQFN-EP* 7mm x 7mm
MAX9736DETJ+	2 x 6W/ 1 x 12W	32 TQFN-EP* 5mm x 5mm

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

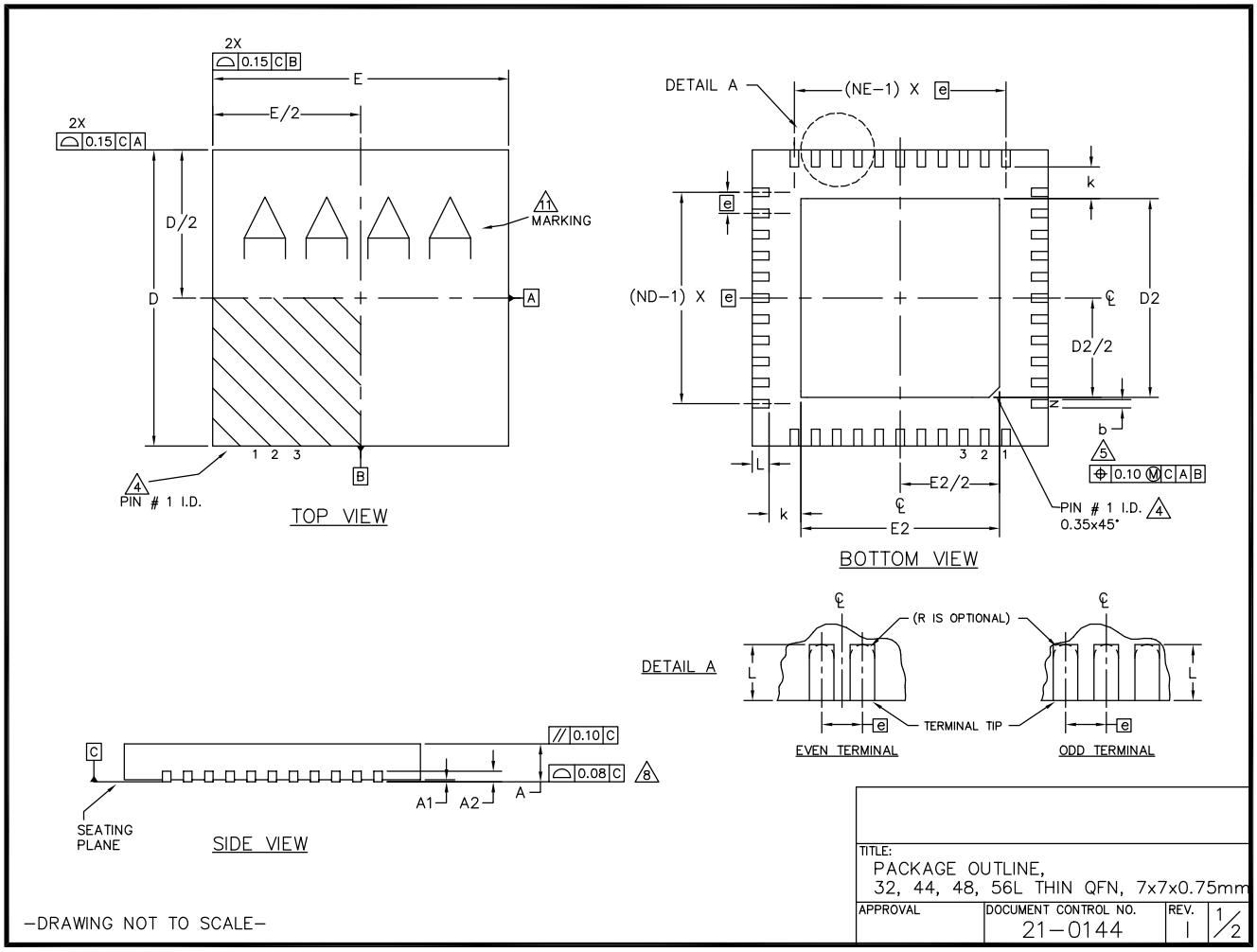
/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877N-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677MN-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-3/-4/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

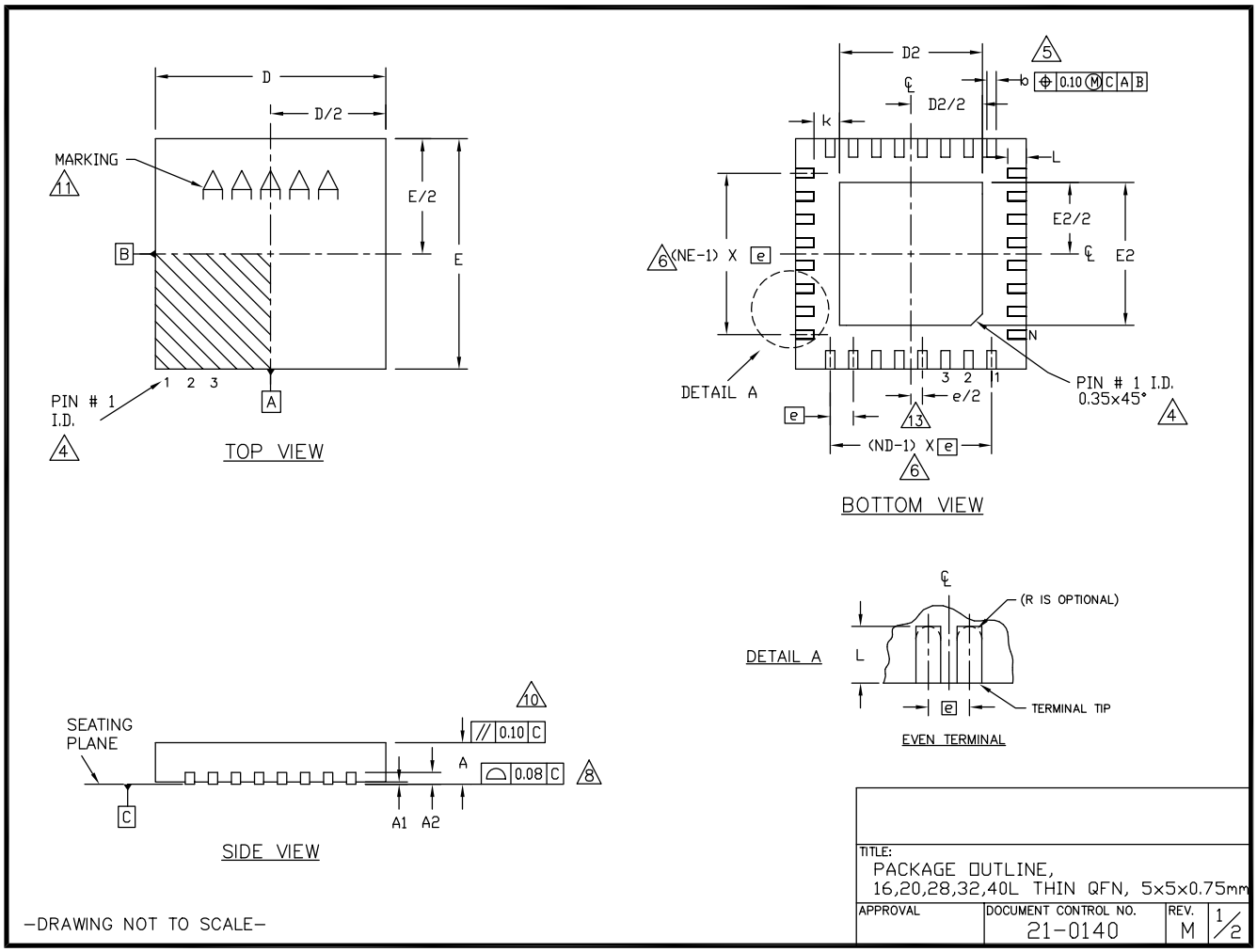
-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 32, 44, 48, 56L THIN QFN, 7x7x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	I	2/2

Package Information (continued)

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COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T165N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

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7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

TITLE:
PACKAGE OUTLINE,
16,20,28,32,40L THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	M	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/08	Initial release	—
1	12/08	Corrected various errors	1–15, 17–21
2	8/09	Added MAX9736D and automotive parts numbers and updated the *Absolute Maximum Ratings* section	1, 2, 3, 4,13, 15, 19, 20, 21
3	9/09	Corrected error in *Absolute Maximum Ratings*, *Pin Description*, *Typical Application Circuit for Stereo Output Configuration*, and *Typical Application Circuit for Single (Mono) Output Configuration*	2, 12, 17, 18
4	11/19	Updated *Ordering Information* table	20

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